MC100SX1230

Advance Information
CMI Coder/Decoder

The MC100SX1230 device consists of a Binary to CMI Coder and CMI to Binary Decoder with integrated loop back capability. The device is designed for CMI (Code Mark Inversion) interfaces in transmission applications supporting either 139.26 Mbit/s E4 or 155.52 Mbit/s STM1 line rates.

In normal operation, the coder and decoder operate independently. Both the coder and decoder operate from a 2X line rate clock. The device incorporates test circuitry to support loop back bypass so either the coder input can be routed to the decoder output or the decoder input can be routed to the coder output. The part is fabricated using ON Semiconductor's proven MOSAIC III™ advanced bipolar process.

The device provides a V_{BB} output for accepting single-ended inputs. The V_{BB} pin should only be used as a bias for the MC100SX1230 as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to ground via a 0.01μF capacitor.

- Binary-to-CMI Coder and CMI-to-Binary Decoder
- Internal Loop Back Test Capability
- Supports SDH or PDH Applications
- Low Power
- Fully Differential 100K Compatible I/O
- V_{BB} Reference Available
- 75kΩ Input Pulldown Resistors
- +5V PECL or −5V ECL Operation
- 28-Pin Surface Mount PLCC Package
- Asynchronous Reset

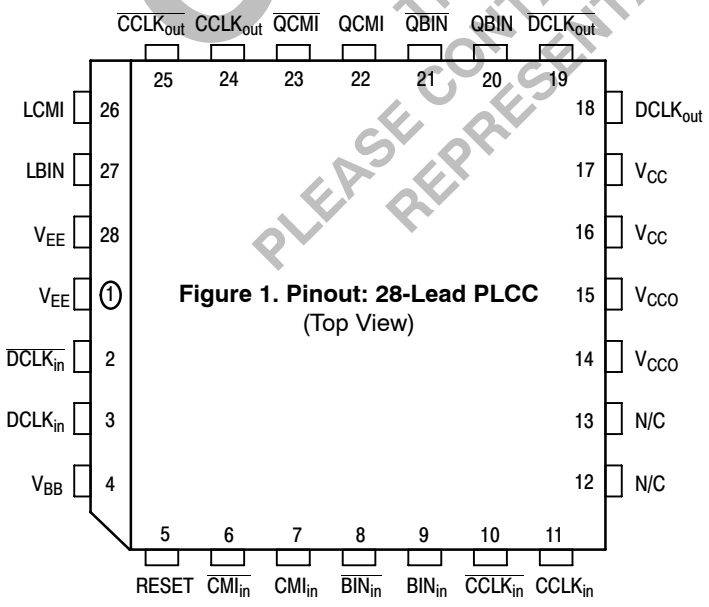

Figure 1. Pinout: 28-Lead PLCC
(Top View)

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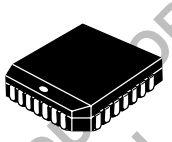
CMI CODER/DECODER

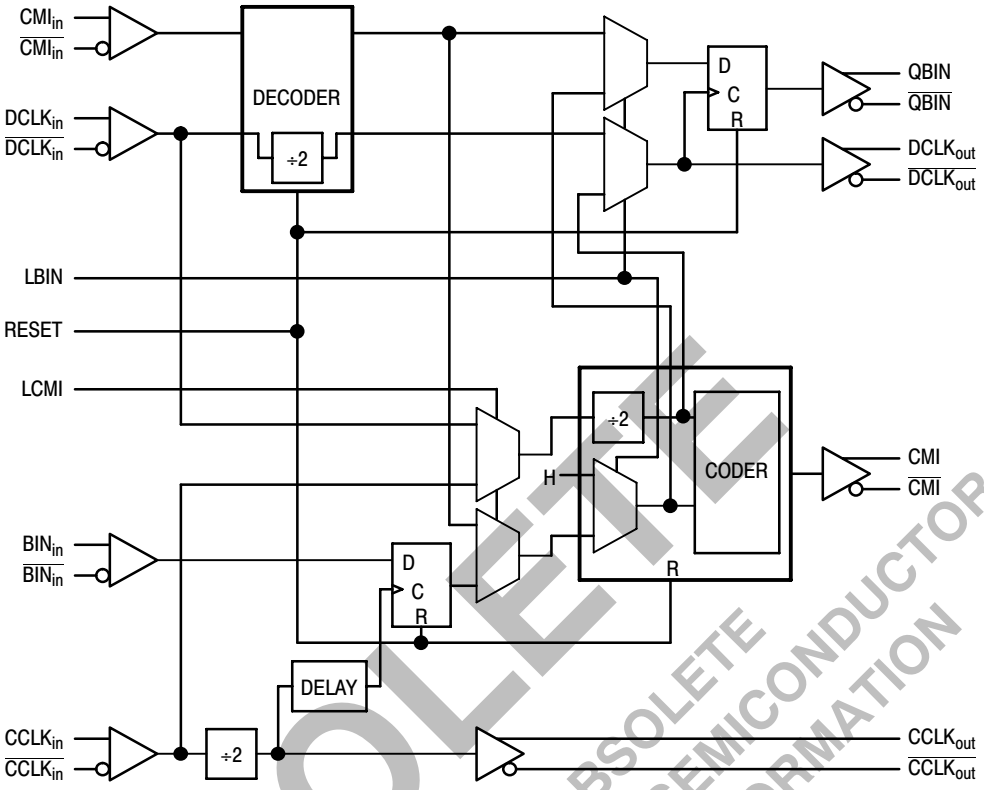


FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02

PIN NAMES

Pins	Function
CMI_{in}, $\overline{CMI_{in}}$	CMI Input to Decoder
$DCLK_{in}$, $\overline{DCLK_{in}}$	Decoder Clock Input
QBIN, $\overline{QBIN}$	Binary Output From Decoder
$DCLK_{out}$, $\overline{DCLK_{out}}$	Decoder Clock Output
BIN_{in}, $\overline{BIN_{in}}$	Binary Input to Coder
$CCLK_{in}$, $\overline{CCLK_{in}}$	Coder Clock Input
QCMI, $\overline{QCMI}$	CMI Output from Coder
$CCLK_{out}$, $\overline{CCLK_{out}}$	Coder Clock Output
RESET	Asynchronous Reset
LBIN	Control Input for Binary Loop Back
LCMI	Control Input for CMI Loop Back

BLOCK DIAGRAM



FUNCTION TABLE

RESET	LBIN	LCMI	Function
H	X	X	Reset, All Output Pairs Set to Logic Low State
L	L	L	Independent Coder and Decoder Operation
L	L	H	CMI Input Routed to Coder Output
L	H	L	Binary Input and Clock Routed to Decoder Outputs Alarm Indication Signal Output from Coder
L	H	H	Illegal, Undefined Operation

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	−8 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0V)	0 to −6	Vdc
I_{OUT}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	0 to +85	°C
V_{EE}	Operating Range[2]	−5.7 to 4.2	V

1 Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

2 Parametric values specified at: −4.2 to 5.46V

DC CHARACTERISTICS (V_{CC} = V_{CCO} = GND; V_{EE} = −4.2 to 5.46V)

		0°C			25°C			85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	−1025	−955	−880	−1025	−955	−880	−1025	−955	−880	mV	V_{in} = $V_{IH(max)}$ or $V_{IL(min)}$
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	−1810	−1705	−1620	−1810	−1705	−1620	mV	V_{in} = $V_{IH(max)}$ or $V_{IL(min)}$
V_{OHA}	Output HIGH Voltage	−1035			−1035			−1035			mV	V_{in} = $V_{IH(max)}$ or $V_{IL(min)}$
V_{OLA}	Output LOW Voltage			−1610			−1610			−1610	mV	V_{in} = $V_{IH(max)}$ or $V_{IL(min)}$
V_{IH}	Input HIGH Voltage	−1165		−880	−1165		−880	−1165		−880	mV	
V_{IL}	Input LOW Voltage	−1810		−1475	−1810		−1475	−1810		−1475	mV	
V_{BB}	Reference Voltage	−1380		−1260	−1380		−1260	−1380		−1260	V	
I_{IH}	Input HIGH Current			200			200			200	μA	
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA	
I_{EE}	Supply Current	61		122	61		122	70		141	mA	

1. 100SX circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is mounted in a test socket or mounted on a printed circuit board and transverse air greater than 500lfm is maintained.
2. All outputs are loaded with 50Ω to V_{CC} − 2V.

AC CHARACTERISTICS (V_{CC} = V_{CCO} = GND; V_{EE} = −4.2 to 5.46V)

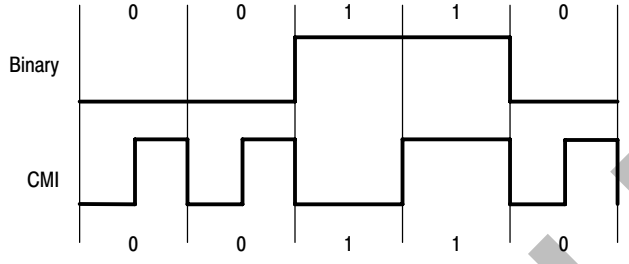
		0 to 85°C					
Symbol	Characteristic	Min	Typ	Max	Unit	Condition	Notes
F_{max}		700			MHz		
t_{pd}	Propagation Delay $CCLK_{in}$ to $CCLK_{out}$	650		1550	ps		
	$CCLK_{in}$ to QCMI	1000		1750		LCMI=LBIN='L'	Add 3 $CCLK_{in}$-Cycles to Delay
	$DCLK_{in}$ to $DCLK_{out}$	550		1700		LCMI=LBIN='L'	
	$DCLK_{in}$ to QBIN	1000		1800		LCMI=LBIN='L'	Add 4 $DCLK_{in}$-Cycles to Delay
	$CCLK_{in}$ to $DCLK_{out}$					LCMI='L', LBIN='H'	
	$CCLK_{in}$ to QBIN	1100		2700		LCMI='L', LBIN='L'	Add 3 $CCLK_{in}$-Cycles to Delay
	$DCLK_{in}$ to QCMI	800		1700		LCMI='H', LBIN='L'	Add 5 $DCLK_{in}$-Cycles to Delay
t_s	Setup Time BIN_{in} to $CCLK_{in}$	−375			ps		
	CMI_{in} to $DCLK_{in}$	140					
t_h	Hold Time $CCLK_{in}$ to BIN_{in}			1000	ps		
	$DCLK_{in}$ to CMI_{in}			120			
V_{PP}	Minimum Input Swing	250			mV		
V_{CMR}	Common Mode Range	−0.4		Note	V		
t_r, t_f	Rise/Fall Times	150		700	ps	20% − 80%	

1. 100SX circuits are designed to meet the AC specifications shown in the table after thermal equilibrium has been established. The circuit is mounted in a test socket or mounted on a printed circuit board and transverse air greater than 500lfm is maintained.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

Applications Information

CMI Code

The CMI code is a 1B2B code. Each information bit is coded into two transmission bits. A binary 0 is coded to 01, and a binary 1 is coded alternately to a 00 or a 11, thus there is at least one transition during every bit period. A typical data pattern is illustrated in the figure below. Because of the coding, the data stream is not only DC balanced, but it contains a rich clock component which aids the clock recovery process at the receiver. A 2X clock is used by the MC100SX1230 to ensure that the mid-bit transition of the data 0 is ideally centered at the CMI encoded output.



1.. CMI Code

Typical Application

In a traditional telecommunications application, the MC100SX1230 is resident on the line card interface which contains circuitry to implement the line transmitter and receiver functions. On the decoder side, a cable equalization filter followed by a clock recovery/decision circuit are required to compensate for the cable attenuation and distortion, extract the 2X clock signal and re-time the CMI data. On the coder side, a PLL is required to synthesize the 2X coder clock and a conditioning circuit is needed at the output of the coder to generate the appropriate signal to drive the cable.

Device Operation

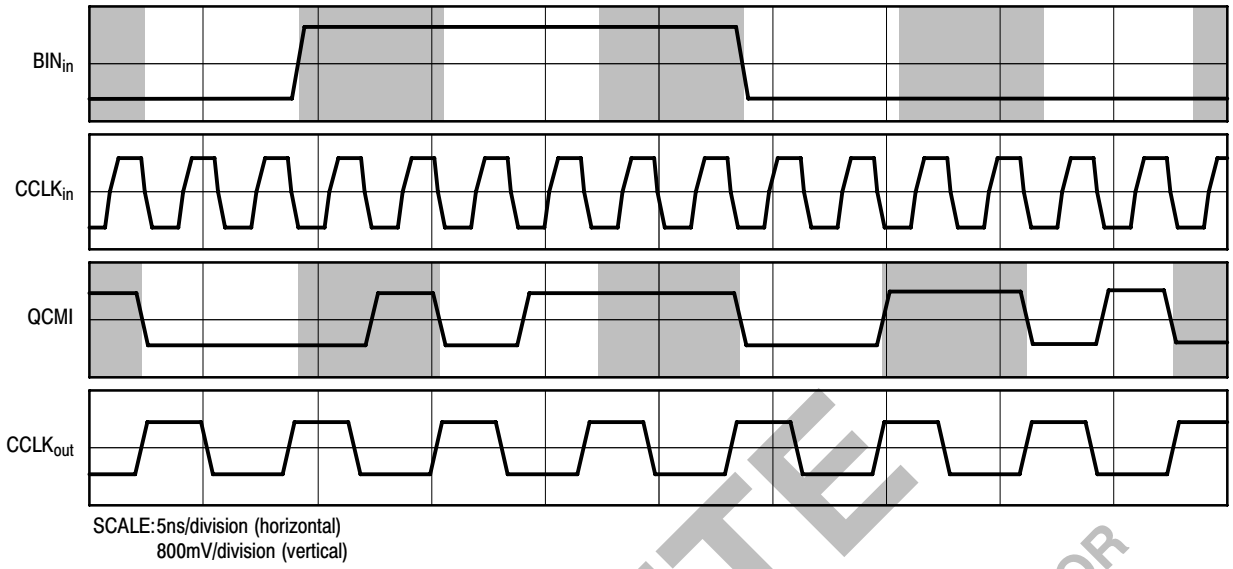
The circuit contains a complete CMI coder and decoder as well as the support circuitry necessary to perform loop back of either the Binary input or the CMI input. The operation is controlled by the LCMI and LBIN inputs. In addition, the device generates an AIS (Alarm Indication Signal) from the coder output when the binary loop back state is active (LBIN='H'). The AIS signal indicates to the receiver at the other end of the cable that 'real' data is not being sent. The device contains a Reset input which should normally be reset as part of the powering up sequence.

The coder accepts a differential data input (BIN_{in}) as well as a differential clock ($CCLK_{in}$). The clock signal must be twice the frequency of the input data signal, i.e. a 155 MBit/s binary signal requires a 310 MHz clock, for proper operation. Typical input and output waveforms are shown in 2.. The incoming clock signal is divided by 2 and supplied at the coder clock output (CLK_{out}). The BINin signal is buffered before being driven into the input register which clocks in the binary data. This results in a negative setup time for the coder. The coded data is output from the coder 3 $CCLK_{in}$ clock cycles plus normal propagation delay after the binary data has been supplied.

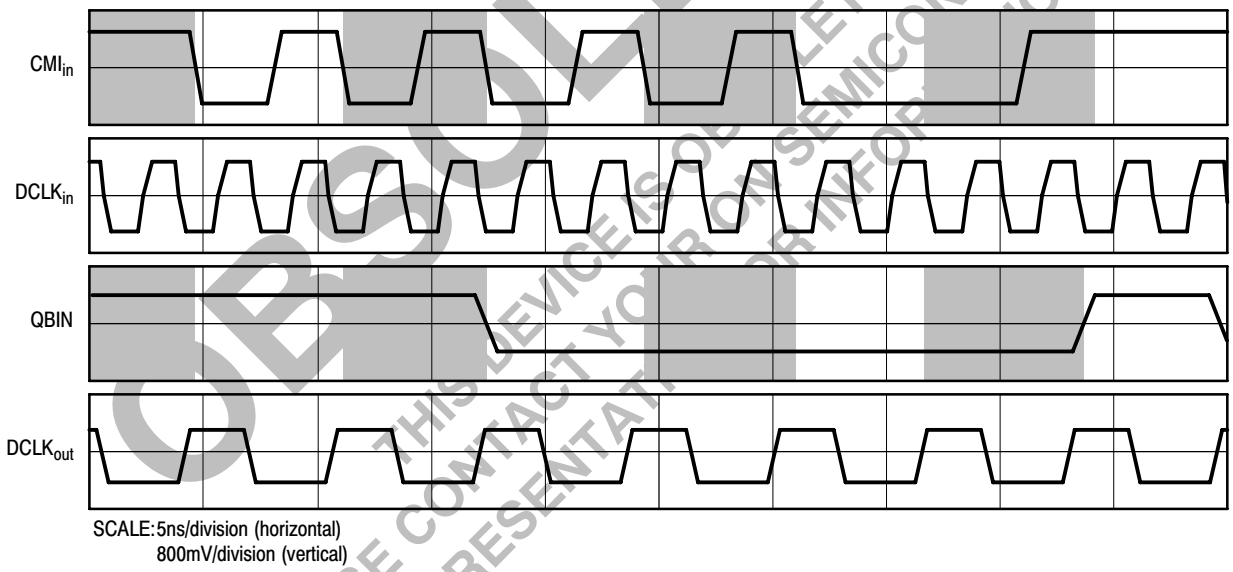
The decoder accepts a differential data input (CMI_{in}) as well as a differential clock ($DCLK_{in}$). The clock signal is supplied from the external clock extraction circuit and runs at the coded rate of either 280 MHz or 310 MHz depending on weather the application is for a PDH system or an SDH system. The decoder has a latency of 4 clock cycles so the decoded data is output 4 cycles plus the normal propagation delay after the input data is captured. 3. illustrates the decoder operation.

Under certain conditions, the user may require that the binary data to be coded be routed back to the output of the decoder to verify proper system operation. This is accomplished through the use of the LBIN input control pin. When this signal is asserted (LBIN = 'H'), the BINin signal as well as a divided by 2 version of the CCLKin input is routed to the QBIN and $DCLK_{out}$ outputs respectively. The BINin to QBIN output has a latency of 3 $CCLK_{in}$ cycles plus internal propagation delays. In addition, the AIS signal is generated and output from the QCMI output. To the receiver the AIS signal is decoded as a constant logic 'H' signal. This operation is seen in 4..

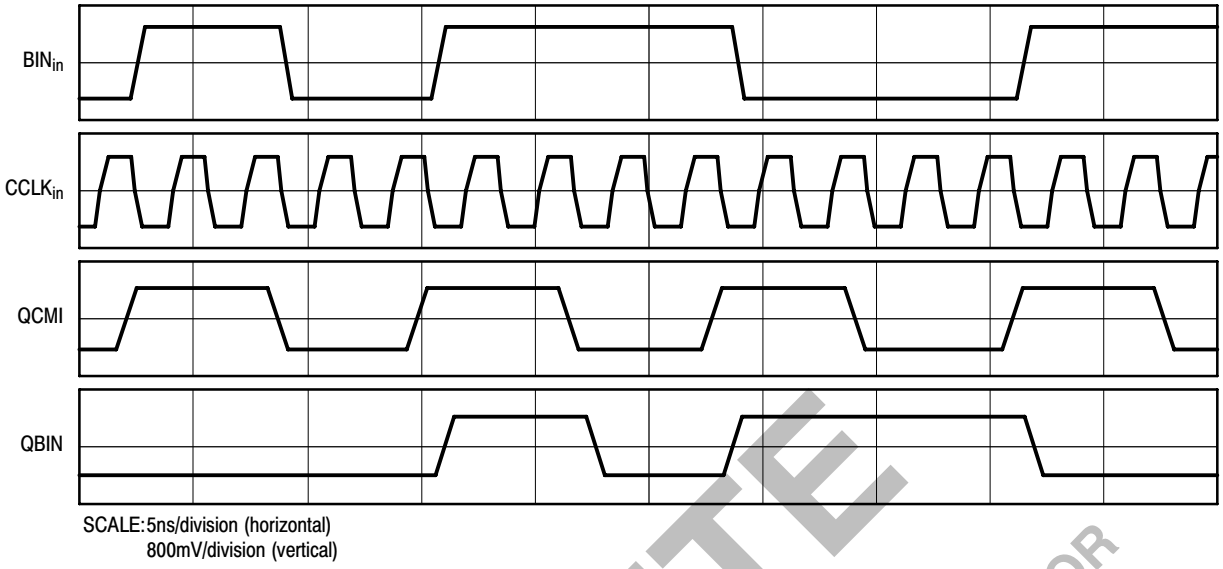
To complement the binary loop back feature, a CMI loop back function is also supported. This is accomplished by asserting the LCMI input control pin (LCMI ='H'). Under this condition, the CMI coded input is decoded, then routed through the coder block to the QCMI output. The CMIin to QCMI output has a latency of 5 $DCLK_{in}$ cycles plus internal propagation delays. 5. shows the CMI loop back operation.



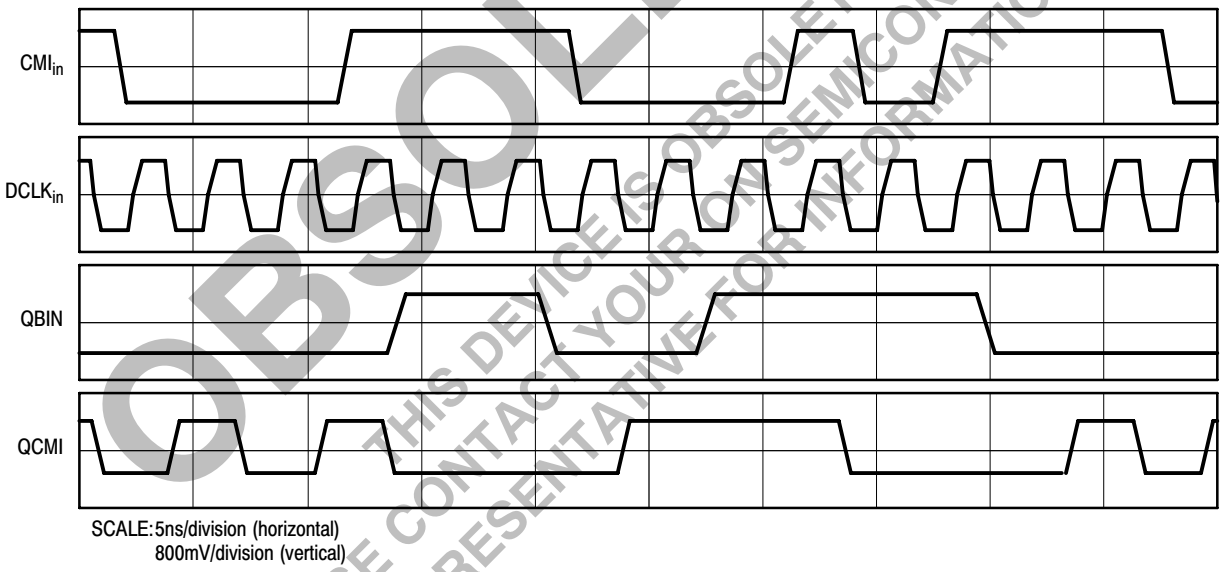
2.. Coder Operation for 155Mbit/s Output Data



3.. Decoder Operation for 155Mbit Output Data



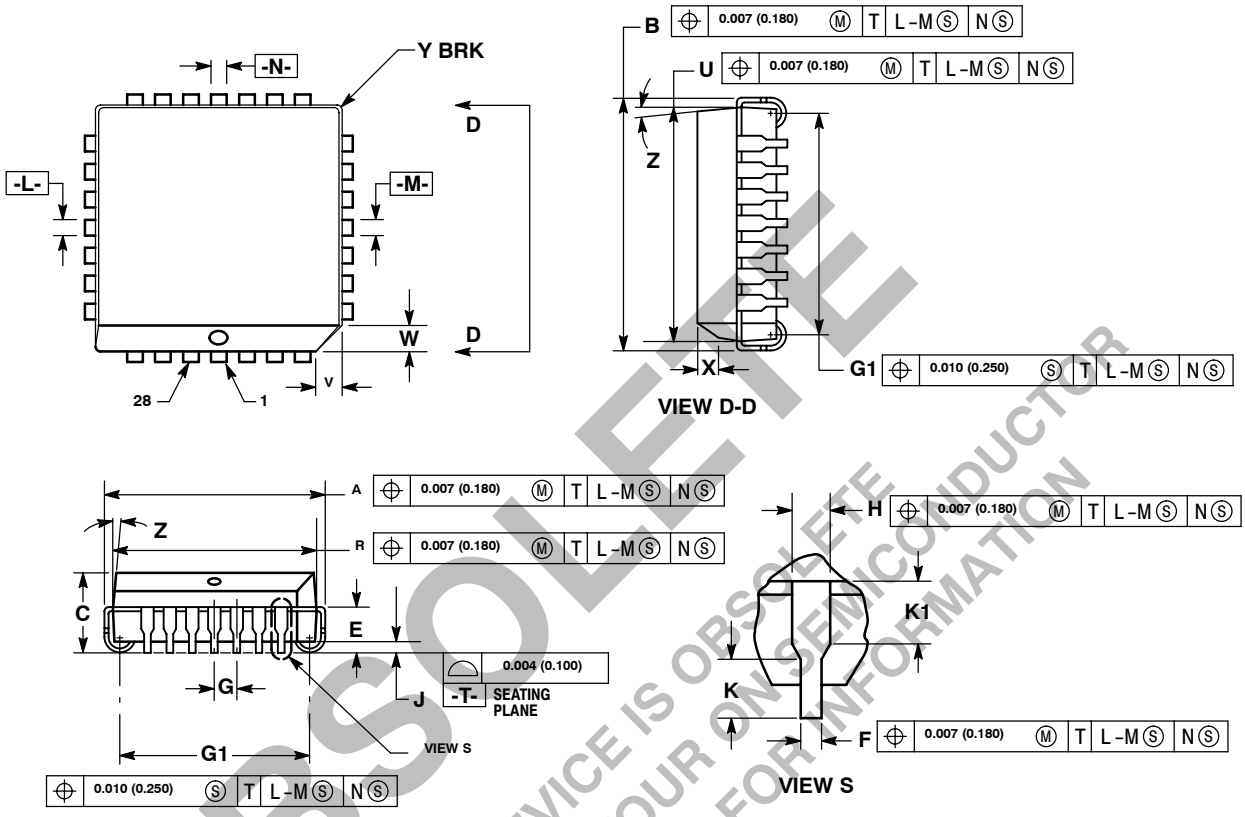
4.. LBIN Active, Alarm Indication Signal Generated on QCMI Output



5.. LCMI Active

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE D



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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