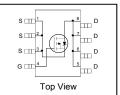


#### **Features**

- Advanced Process Technology
- Low On-Resistance
- · Logic Level Gate Drive
- P Channel MOSFET
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- · Fast Switching
- Fully Avalanche Rated
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



V <sub>DSS</sub>	-30V
R <sub>DS(on)</sub> max.	0.02Ω
I <sub>D</sub>	-10A



G	D	S
Gate	Drain	Source

Base part number   Backage Tune		Standard Pack		Orderable Bort Number	
Base part number	Package Type	Form Quai		Orderable Part Number	
AUIRF7416Q	SO-8	Tape and Reel	4000	AUIRF7416QTR	

## **Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ -10V	-10	
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ -10V	-7.1	A
I <sub>DM</sub>	Pulsed Drain Current ①	-45	
P <sub>D</sub> @T <sub>A</sub> = 25°C	Maximum Power Dissipation	2.5	W
	Linear Derating Factor	0.02	mW°/C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	370	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		C

## Thermal Resistance

THOTHIAI IXOOIOtalloo				
Symbol	Parameter	Тур.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ®		50	°C/W

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<sup>\*</sup>Qualification standards can be found at www.infineon.com



## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30			V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		-0.024		V/°C	Reference to 25°C, I <sub>D</sub> = -1mA
П	Static Drain to Source On Desigtance			0.020		$V_{GS} = -10V, I_D = -5.6A \oplus$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance			0.035	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2.8A ④
$V_{\rm GS(th)}$	Gate Threshold Voltage	-1.0		-2.04	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
gfs	Forward Trans conductance	5.6			S	$V_{DS} = -10V, I_{D} = -2.8A$
	Drain to Source Leakage Current			-1.0		$V_{DS} = -24V, V_{GS} = 0V$
IDSS	Drain-to-Source Leakage Current			-25	μA	$V_{DS} = -24V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
	Gate-to-Source Forward Leakage			-100	- Λ	$V_{GS} = -20V$
I <sub>GSS</sub>	Gate-to-Source Reverse Leakage			100	nA	V <sub>GS</sub> = 20V

## Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

$Q_g$	Total Gate Charge	 61	92		$I_D = -5.6A$
$Q_gs$	Gate-to-Source Charge	 8.0	12	nC	$V_{DS} = -24V$
$Q_{gd}$	Gate-to-Drain Charge	 22	32		V <sub>GS</sub> = -10V, See Fig.6 & 9 ④
$t_{d(on)}$	Turn-On Delay Time	 18			V <sub>DD</sub> = -15V
t <sub>r</sub>	Rise Time	 49		20	$I_{D} = -5.6A$
$t_{d(off)}$	Turn-Off Delay Time	 59		ns	$R_G = 6.2\Omega$
t <sub>f</sub>	Fall Time	 60			$R_D = 2.7\Omega$ , See Fig.10 $\oplus$
C <sub>iss</sub>	Input Capacitance	 1700			$V_{GS} = 0V$
Coss	Output Capacitance	 890		рF	$V_{DS} = -25V$
$C_{rss}$	Reverse Transfer Capacitance	 410			f = 1.0MHz, See Fig.5

## **Diode Characteristics**

	Parameter	Min.	Тур.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)			-3.1		MOSFET symbol showing the
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①			-45		integral reverse p-n junction diode.
$V_{SD}$	Diode Forward Voltage			-1.0	V	$T_J = 25^{\circ}C, I_S = -5.6A, V_{GS} = 0V $ ④
t <sub>rr</sub>	Reverse Recovery Time		56	85	ns	$T_J = 25^{\circ}C$ , $I_F = -5.6A$ ,
Q <sub>rr</sub>	Reverse Recovery Charge		99	150	nC	di/dt = 100A/µs ④

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting  $T_J$  = 25°C, L = 25mH,  $R_G$  = 25 $\Omega$ ,  $I_{AS}$  = -5.6A. (See Fig. 12)
- $\label{eq:local_loss} \mbox{ } \mbox$
- 4 Pulse width  $\leq 300 \mu s$ ; duty cycle  $\leq 2\%$ .



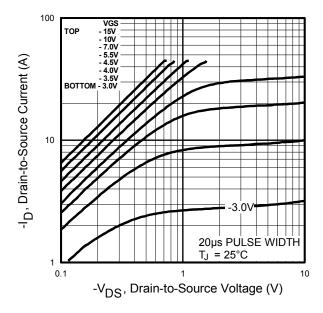


Fig. 1 Typical Output Characteristics

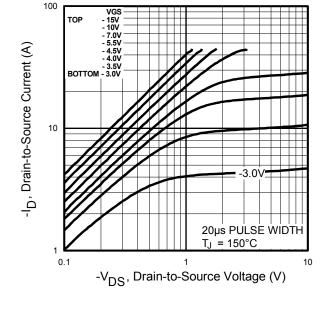


Fig. 2 Typical Output Characteristics

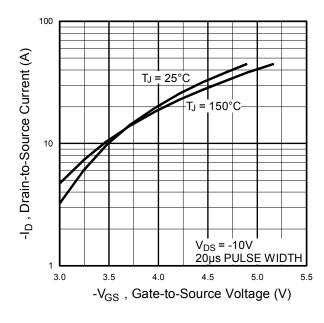
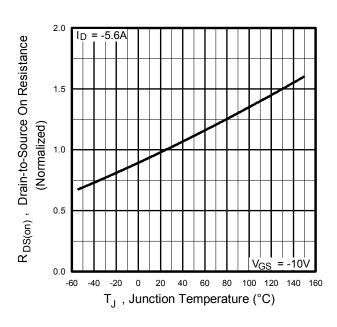
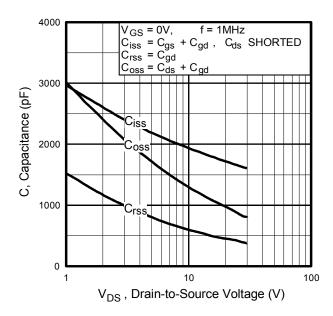


Fig. 3 Typical Transfer Characteristics

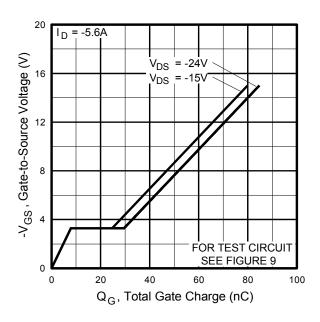


**Fig. 4** Normalized On-Resistance Vs. Temperature





**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

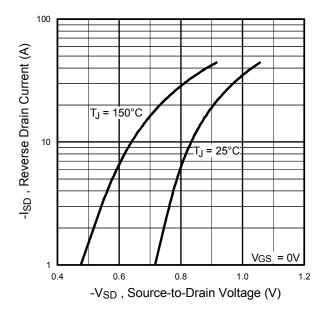


Fig. 7 Typical Source-Drain Diode Forward Voltage

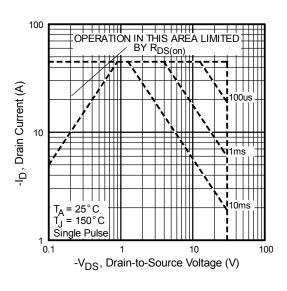


Fig 8. Maximum Safe Operating Area



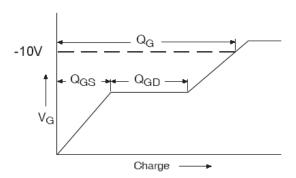


Fig 9a. Gate Charge Waveform

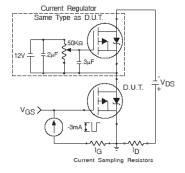


Fig 9b. Gate Charge Test Circuit

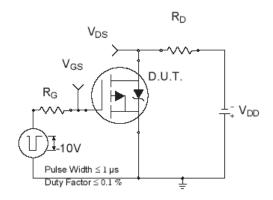


Fig 10a. Switching Time Test Circuit

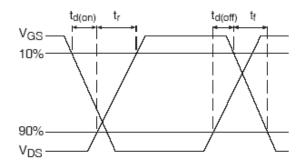


Fig 10b. Switching Time Waveforms

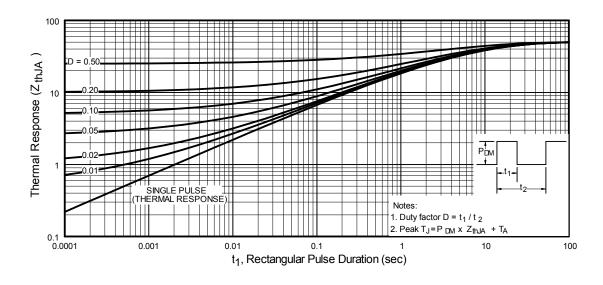


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



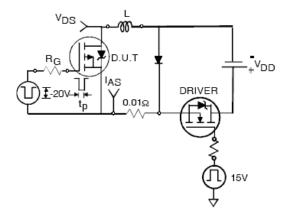


Fig 12a. Unclamped Inductive Test Circuit

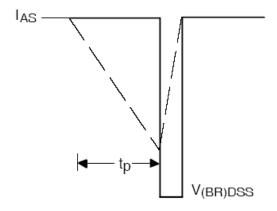
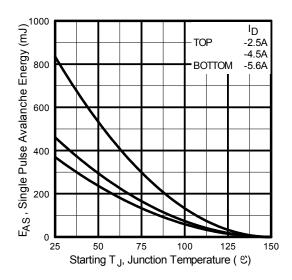


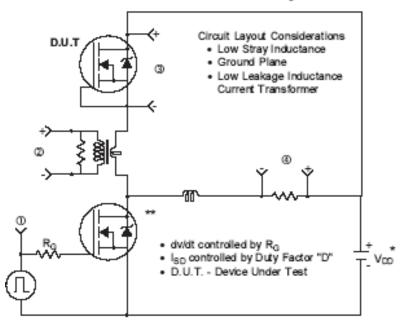
Fig 12b. Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



# Peak Diode Recovery dv/dt Test Circuit



- \* Reverse Polarity for P-Channel
- \*\* Use P-Channel Driver for P-Channel Measurements

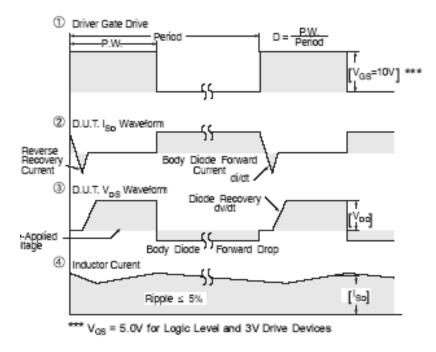
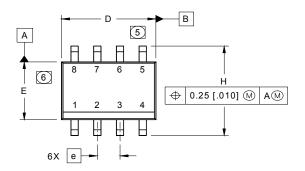


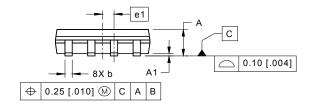
Fig 13. Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs

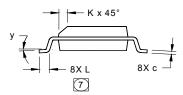


# **SO-8 Package Outline** (Dimensions are shown in millimeters (inches)



DIM INCHI		HES	MILLIM	ETERS
DIIVI	MIN	MAX	MIN	MAX
Α	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
С	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
Е	.1497	.1574	3.80	4.00
е	.050 B	ASIC	1.27 BASIC	
e 1	.025 B	ASIC	0.635 BASIC	
Н	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
у	0°	8°	0°	8°



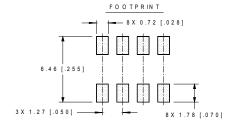


- 1. D IM EN S ION IN G & TOLERAN C IN G PER A S M E Y 1 4 .5 M 1994. 2. C ON TROLLIN G D IM EN S ION: MILLIM ETER

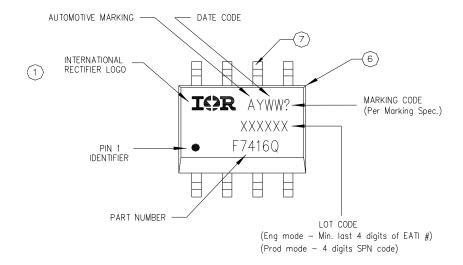
- 2. CONTINCULING DIMENSION. MILLIMETERS (IN CHES).

  4. OUTLINE CONFORMS TO JEDEC OUTLINE M S-012AA.

  3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
- 6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
- 7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

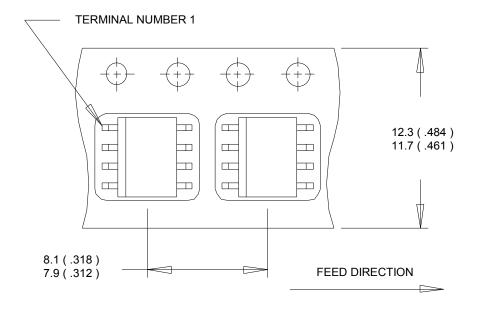


## **SO-8 Part Marking Information**



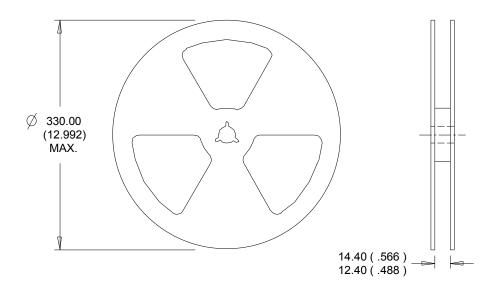


## SO-8 Tape and Reel (Dimensions are shown in millimeters (inches)



#### NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



## NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.



#### **Qualification Information**

		Automotive (per AEC-Q101)				
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.				
Moisture	Sensitivity Level	SO-8	MSL1			
N.4 I-	Manakina Mandal	Class M4 (+/- 425V) <sup>†</sup>				
	Machine Model	AEC-Q101-002				
FOR	Livers on Dody Model	Class H1B (+/- 1000V) <sup>†</sup>				
ESD	Human Body Model	AEC-Q101-001				
	Channed Davisa Madal	Class C5 (+/- 1125V) <sup>†</sup>				
	Charged Device Model	AEC-Q101-005				
RoHS Compliant		Yes				

† Highest passing voltage.

### **Revision History**

Date	Comments					
	Added "Logic Level Gate Drive" bullet in the features section on page 1					
3/27/2014	Updated part marking on page 6.					
	Updated data sheet with new IR corporate template					
9/30/2015	Updated datasheet with corporate template					
9/30/2015	Corrected ordering table on page 1.					

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