

54F/74F573 Octal D-Type Latch with TRI-STATE® Outputs

General Description

The 'F573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable $\overline{(OE)}$ inputs.

This device is functionally identical to the 'F373 but has different pinouts.

- Features
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
 Functionally identical to 'F373
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

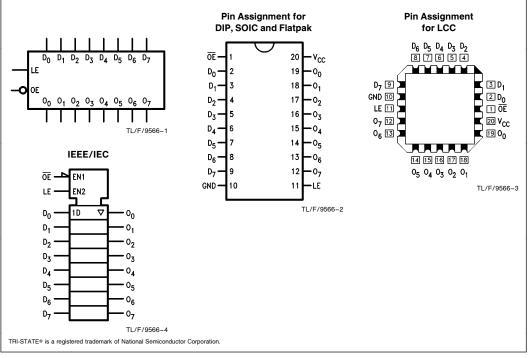
Commercial	Military	Package Number	Package Description
74F573PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F573DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F573SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F573SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F573FM (Note 2)	W20A	20-Lead Cerpak
	54F573LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13'' reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

Connection Diagrams



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			54F/74F
Pin Names	Description	U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
D ₀ -D ₇	Data Inputs	1.0/1.0	20 µA/−0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 µA/−0.6 mA
ŌĒ	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 µA/−0.6 mA
O ₀ -O ₇	TRI-STATE Latch Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)

Functional Description

The 'F573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfer with entering new data into the latches.

Function Table

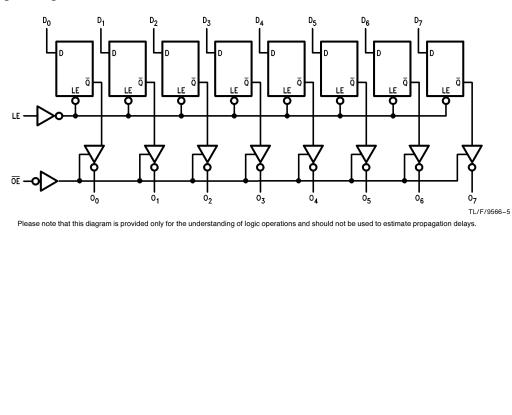
	Inputs		Outputs
ŌĒ	LE	D	0
L	Н	Н	н
L	Н	L	L
L	L	х	O ₀
Н	Х	Х	Z

H = HIGH Voltage Level

L = LOW Voltage Level

 $\begin{array}{l} X = \text{Immaterial} \\ O_0 = \text{Value stored from previous clock cycle} \end{array} \\ \end{array}$

Logic Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C	
Ambient Temperature under Bias	-55°C to +125°C	
Junction Temperature under Bias	-55°C to +175°C	
Plastic	-55°C to +150°C	
V _{CC} Pin Potential to		
Ground Pin	-0.5V to +7.0V	
Input Voltage (Note 2)	-0.5V to $+7.0V$	
Input Current (Note 2)	-30 mA to $+5.0$ mA	
Voltage Applied to Output		
in HIGH State (with $V_{CC} = 0V$)		
Standard Output	- 0.5V to V _{CC}	
TRI-STATE Output	-0.5V to $+5.5V$	
Current Applied to Output		
in LOW State (Max)	twice the rated I _{OL} (mA)	
ESD Last Passing Voltage (Min)	4000V	

Recommended Operating Conditions

Free Air Ambient Temperature

 Military
 -55°C to + 125°C

 Commercial
 0°C to + 70°C

 Supply Voltage
 Military

 Military
 + 4.5V to + 5.5V

 Commercial
 + 4.5V to + 5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied. Note 2: Either voltage limit or current limit is sufficient to protect inputs.

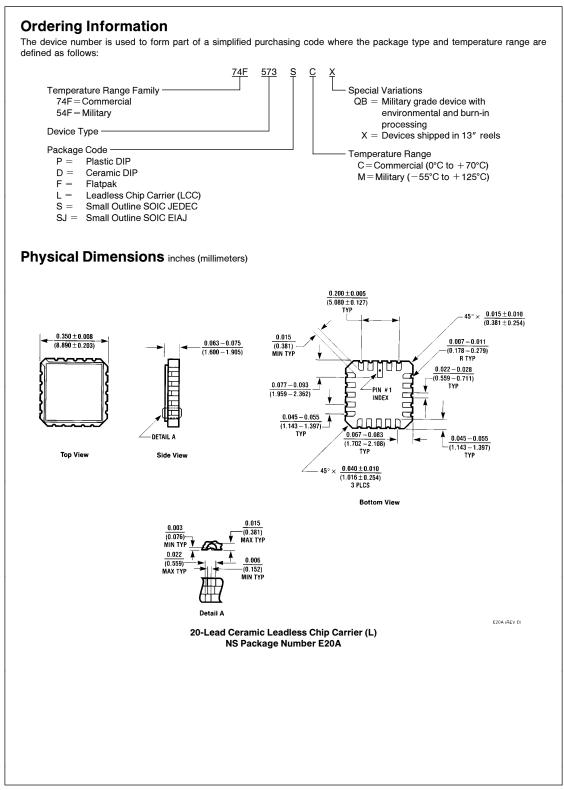
DC Electrical Characteristics

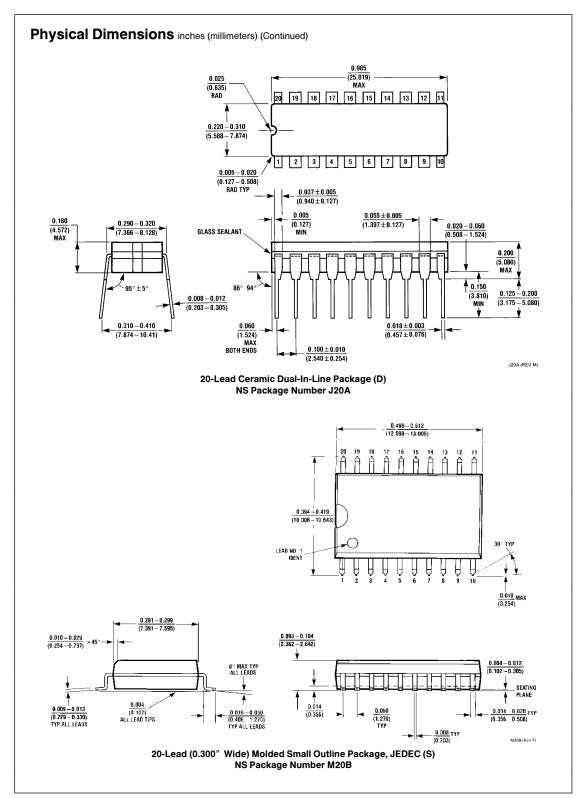
Symbol	Parame	ter		54F/74	=	Units	Vcc	Conditions
oymbol	i arame		Min	Тур	Max		•00	Conditions
VIH	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signa
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signa
V _{CD}	Input Clamp Diode Vo	oltage			-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7			V	Min	
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}			0.5 0.5	v	Min	$I_{OL} = 20 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
I _{IH}	Input HIGH Current	54F 74F			20.0 5.0	μΑ	Max	$V_{IN} = 2.7V$
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μΑ	Max	$V_{IN} = 7.0V$
ICEX	Output HIGH Leakage Current	54F 74F			250 50	μΑ	Max	$V_{OUT} = V_{CC}$
V _{ID}	Input Leakage Test	74F	4.75			v	0.0	$I_{ID} = 1.9 \ \mu A$ All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F			3.75	μΑ	0.0	V _{IOD} = 150 mV All Other Pins Grounded
Ι _{ΙL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I _{OZH}	Output Leakage Curre	ent			50	μA	Max	$V_{OUT} = 2.7V$
I _{OZL}	Output Leakage Curre	ent			-50	μA	Max	$V_{OUT} = 0.5V$
I _{OS}	Output Short-Circuit (Current	-60		-150	mA	Max	$V_{OUT} = 0V$
I _{ZZ}	Bus Drainage Test				500	μΑ	0.0V	$V_{OUT} = 5.25V$
I _{CCL}	Power Supply Curren	t		35	55	mA	Max	$V_{O} = LOW$
I _{CCZ}	Power Supply Curren	t		35	55	mA	Max	V _O = HIGH Z

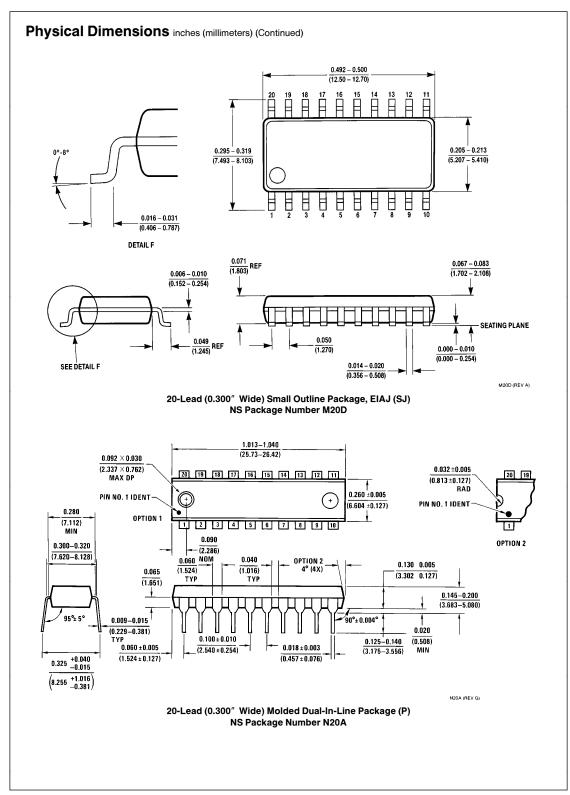
			74F		5	4F	7	4F	
Symbol	Parameter	v	T _A = +25°(/ _{CC} = +5.0 C _L = 50 pF	v		_C = Mil 50 pF	T _A , V _{CC} C _L =	= Com 50 pF	Units
		Min	Тур	Мах	Min	Max	Min	Мах	
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n	3.0 2.0	5.3 3.7	7.0 6.0	3.0 2.0	9.0 7.0	3.0 2.0	8.0 6.5	ns
t _{PLH} t _{PHL}	Propagation Delay LE to O _n	5.0 3.0	9.0 5.2	11.0 7.0	5.0 3.0	13.5 7.5	5.0 3.0	12.0 7.0	ns
t _{PZH} t _{PZL}	Output Enable Time	2.0 2.0	5.0 5.6	8.0 8.5	2.0 2.0	10.0 10.0	2.0 2.0	9.0 9.5	- ns
t _{PHZ} t _{PLZ}	Output Disable Time	1.5 1.5	4.5 3.8	5.5 5.5	1.5 1.5	7.0 5.5	1.5 1.5	6.5 5.5	115

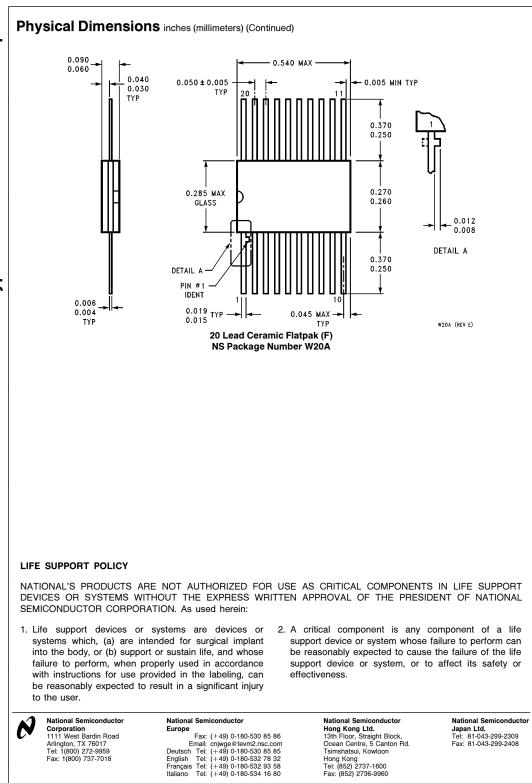
AC Operating Requirements

		7	4F	54	F	74		
Symbol	Parameter	T _A = V _{CC} =	+ 25°C + 5.0V	T _A , V _{CC}	; = Mil	T _A , V _{CC}	e = Com	Units
		Min	Max	Min	Max	Min	Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to LE	2.0 2.0		2.0 2.0		2.0 2.0		
t _h (H)	Hold Time, HIGH or LOW	3.0		3.0		3.0		– ns
t _h (L) t _w (H)	D _n to LE LE Pulse Width, HIGH	3.5 4.0		4.0		3.5 4.0		ns









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<u>Products > Military/ Aerospace > Logic > FAST > 54F573</u>



54F573 Octal D Latch with TRI-STATE Outputs

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Datasheet

Title	Size (in Kbytes)	Date	View Online	X Download	Receive via Email
54F573 Octal D-Type Latch with TRI-STATE(RM) Outputs	166 Kbytes	9-Dec-97	View Online	Download	Receive via Email

Please use <u>Adobe Acrobat</u> to view PDF file(s). If you have trouble printing, see <u>Printing Problems</u>.

Package Availability, Models, Samples & Pricing

Part Number	Pack	age	Status	Mod	els	Samples &	Budgetar	ry Pricing	Std Pack	Package
	Туре	# pins	Status	SPICE	IBIS	Electronic Orders	Quantity	\$US each		Marking
5962-9173801M2A	LCC	20	Full production	N/A	N/A		50+	\$8.0000	tube of 50	[logo]¢Z¢S¢4¢A 54F573 LMQB/Q¢M\$E 5962- 9173801M2A
5962-9173801MRA	Cerdip	20	Full production	N/A	N/A		50+	\$5.4000	tube of 20	[logo]¢Z¢S¢4¢A\$E 54F573DMQB /Q¢M 5962-9173801MRA
JM38510/34604B2	LCC	20	Full production	N/A	N/A		50+	\$15.1000	tube of 50	[logo] JM38510 /34604B2A 27014 QS ¢Z¢S¢4¢A\$E
JM38510/34604BR	Cerdip	20	Full production	N/A	N/A		50+	\$11.0000		[logo] ¢Z¢S¢4¢A\$E JM38510/34604BRA 27014 QS
JM38510/34604BS	Cerpack	20	Full production	N/A	N/A		50+	\$16.0000	tube of 19	[logo]¢Z¢S¢4¢A\$E JM38510/ 34604BSA 27014 QS

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