Data Sheet

SCA720-D01 SINGLE AXIS ACCELEROMETER WITH ANALOG INTERFACE

The SCA720 accelerometer consists of a silicon bulk micro machined sensing element chip and a signal conditioning ASIC. The chips are mounted on a pre-molded package and wire bonded to appropriate contacts. The sensing element and ASIC are protected with silicone gel and lid. The sensor has 12 SMD legs (Gull-wing type).

Features

- Single +5 V supply
- Current consumption 2.5 mA typical
- Ratiometric output in relation to supply voltage (Vdd = 4.75 V...5.25 V)
- Enhanced failure detection features
  - Digitally activated, true self-test by proof mass deflection using electrostatic force
  - Memory parity check during power up, and self-test cycle.
  - Built in connection failure detection
- Digitally activated, true self-test by proof mass deflection using electrostatic force
- Wide load drive capability (max. 20 nF)
- True DC response
- Full traceability information in 2D-matrix on the lid
- Qualified according to AEC-Q100 standard

Applications

SCA720 product family is targeted to automotive applications with high stability and reliability requirements. Automotive target applications are:

- Electrically Controlled Suspension
- Engine Anti-Vibration

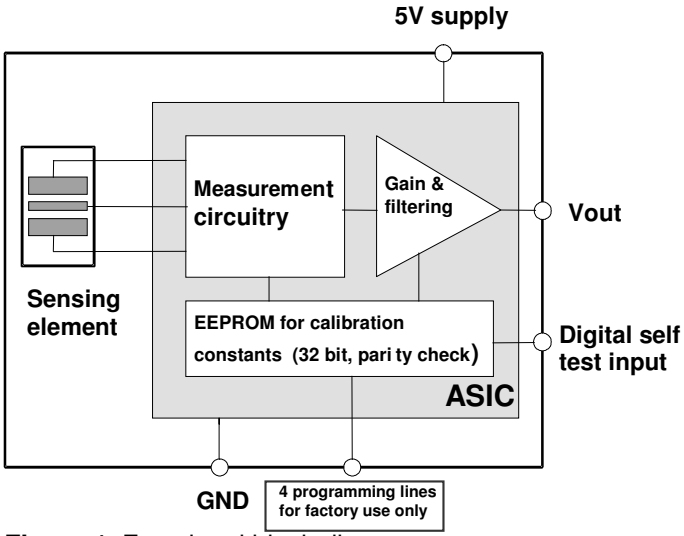

Figure 1. Functional block diagram.

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1. Electrical Specifications

1.1. Absolute Maximum Ratings

Parameter	Value	Units
Acceleration (powered or non-powered)	20 000 [1]	g
Supply voltage	–0.3 to +7.0	V
Voltage at input / output pins	–0.3 to V_{DD} + 0.3	V
ESD HBM (Human Body Model)	±2	kV
ESD CDM (Charged Device Model)	±500 middle pins ±750 corner pins	V
Temperature range (storage)	–50 to +125	℃
Temperature range (operating)	–40 to +125	℃

[1] Equals to drop from 1 meter on a concrete surface.

1.2. Performance Characteristics

V_{DD} = 5.00 V and ambient temperature unless otherwise specified.

KPC[A)]	Parameter	Condition	Min.	Typ	Max.	Units
	Measuring range	Nominal	-1.11		+3.11	g
	Supply voltage Vdd		4.75	5.0	5.25	V
<CC>	Current consumption	Vdd = 5 V; No load		2.5	4.0	mA
	Operating temperature		–40		+125	℃
	Resistive output load	Vout to Vdd or Vss	20			kΩ
	Capacitive load	Vout to Vdd or Vss			20	nF
	Min. output voltage; Vdd = 5 V	20k from Vout to Vdd	0		0.25	V
	Max. output voltage; Vdd = 5 V	20k from Vout to Vss	4.75		5.00	V
	Linear output voltage range	Limiter function enabled	0.5		4.5	V
<CC>	Offset (Output at +1 g)	@ room temperature		Vdd/2		V
<CC>	Sensitivity	@ room temperature		0.1875 × Vdd (≈ 0.9375)		V/g
<SC>	Offset Error (Output at +1 g)	–40 ℃...125 ℃	-137	0	+137	mg
<SC>	Sensitivity error	–40 ℃...125 ℃	–3	0	+3	%
	Typical non-linearity	Within the measuring range	–60		+60	mg
	Amplitude response –3 dB [B)]		68	115	170	Hz
	Ratiometric error	Vdd = 4.75 V...5.25 V	–2		+2	%
<SC>	Cross-axis sensitivity	@ room temperature			3.9	%
	Output noise	From DC...4 kHz			5	mV_{rms}
	Start-up delay	Reset and parity check			10	ms
	Self test pull down resistor (Internal)		44	62	80	kΩ

A) CC= Critical Characteristics. Must be 100% monitored during production
SC= Significant Characteristic. The process capability (Cpk) must be better than 1.33, which allows sample based testing. If process is not capable the part will be 100% tested

B) Output has true DC response

1.3. Offset and sensitivity calibration

Vout offset is calibrated in 0g position:

$$Offset = V_{out}(+1g)\,[\mathrm{V}]$$

Nominal offset is Vdd/2:

$$Offset_{nom} = \frac{V_{dd}}{2}\,[\mathrm{V}]$$

Sensitivity is calibrated as:

$$Sensitivity = \frac{V_{out}(+1g) - V_{out}(-1g)}{2g}\ [\mathrm{V/g}]$$

Nominal sensitivity is:

$$Sensitivity_{nom} = 0.9375\ [\mathrm{V/g}]$$

1.4. Error calculations

Total error is the allowed maximum error, which include partial error sources. Total error over lifetime is specified as a sum of offset and sensitivity errors:

$$Total\_Error = Offset\_Error + Sensitivity\_Error\,[\mathrm{mg}]$$

Offset error is specified as:

$$Offset\_Error = \frac{Vout(+1g) - \frac{V_{dd}}{2}}{Sensitivity}\ [\mathrm{mg}]$$

Sensitivity error percent is specified as:

$$Sensitivity\_Error\% = \frac{[Vout(+1g) - Vout(-1g)]/2g - Sensitivity_{nom}}{Sensitivity_{nom}} \times 100\%$$

Sensitivity error is specified as:

$$Sensitivity\_Error = \frac{[Vout - Vout(+1g)] \times Sensitivity\_Error\%}{Sensitivity}\ [\mathrm{mg}]$$

1.5. Supply voltage

Usage of external 100 nF power supply bypass capacitor is recommended.

ASIC start-up should be tolerant to noise between Vdd and GND. Recommended power-up ramp is presented below.

Parameter	Min	Max
T_1	T_0 + 0.1 µs	
T_2		T_0 + 100 µs
V_1	–0.3 V	0.5 V
V_2	4.5 V	5.5 V

Supply voltage ramp at startup.

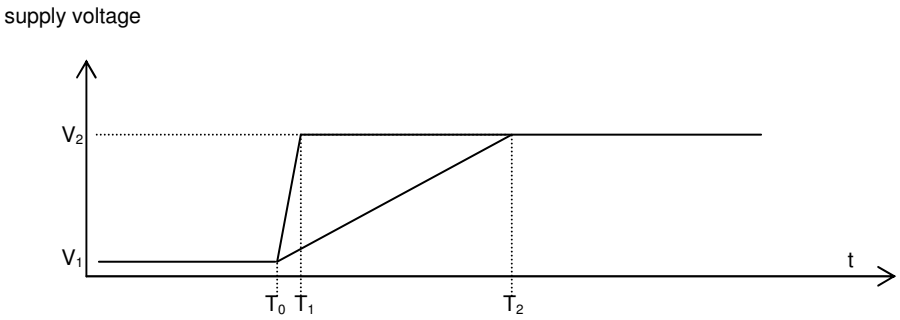


Figure 2. V_{DD} Start-up sequence.

1.6. Electrical Connection

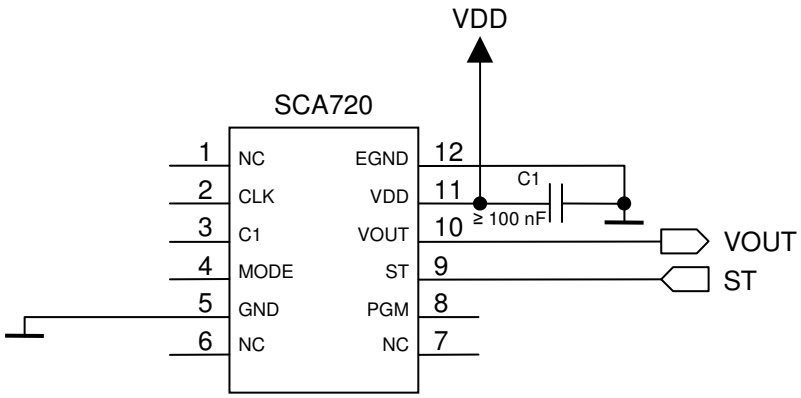
The following is minimum requirement for electrical interface to the SCA720. If over-voltage or reverse polarity protection is needed, please contact Murata Electronics Oy for application information.

Usage of external minimum 100 nF power supply bypass capacitor is recommended. Maximum rise time of V_{DD} is 100 us.

If self-test (Pin 9) is not used it should be left floating.

Pins 1, 2, 3, 4, 6, 7 and 8 are left floating.

If the self test is used



If the self test is not used

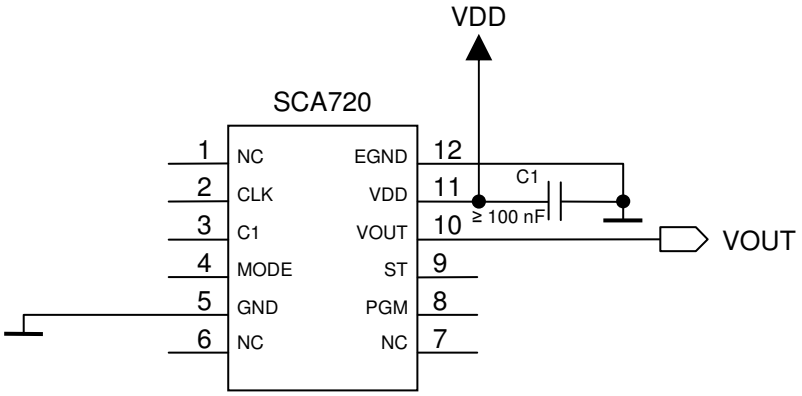
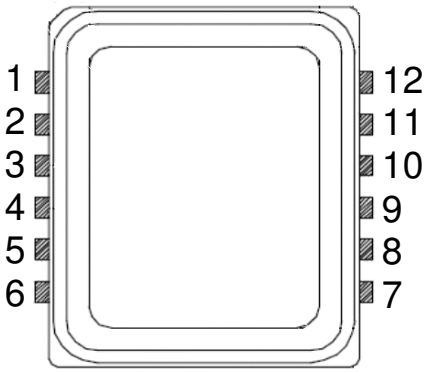


Figure 3. Electrical connection of SCA720 component.



No.	Name	Function	Connect
1	Reserved	Not used	Not connected
2	CLK	Data shift clock (factory only)	Not connected
3	C1	(Factory only)	Not connected
4	MODE	Mode control input (factory only)	Not connected
5	GND	Negative supply voltage (V_{SS})	Ground
6	Reserved	Not used	Not connected
7	Reserved	Not used	Not connected
8	PGM	Programming voltage (factory only)	Not connected
9	ST	Self test control	Float when not used
10	VOUT	Sensor output voltage	Next stage input
11	VDD	Positive supply voltage (V_{DD})	V_{DD} (+5 V)
12	EGND	EMC ground (lid grounding)	Ground

1.7. Limiter function

The table below defines the limiter function.

Parameter	Condition	Min	Max	Unit
Limiter cutoff voltage	Low voltage limit High voltage limit	0.05 × Vdd 0.90 × Vdd	0.10 × Vdd 0.95 × Vdd	V V
Min output voltage	Limiter enabled, VDD = 5 V	0.25		V
Max output voltage	Limiter enabled, VDD = 5 V		4.75	V
Linear range	Limiter enabled, VDD = 5 V	0.5	4.5	V

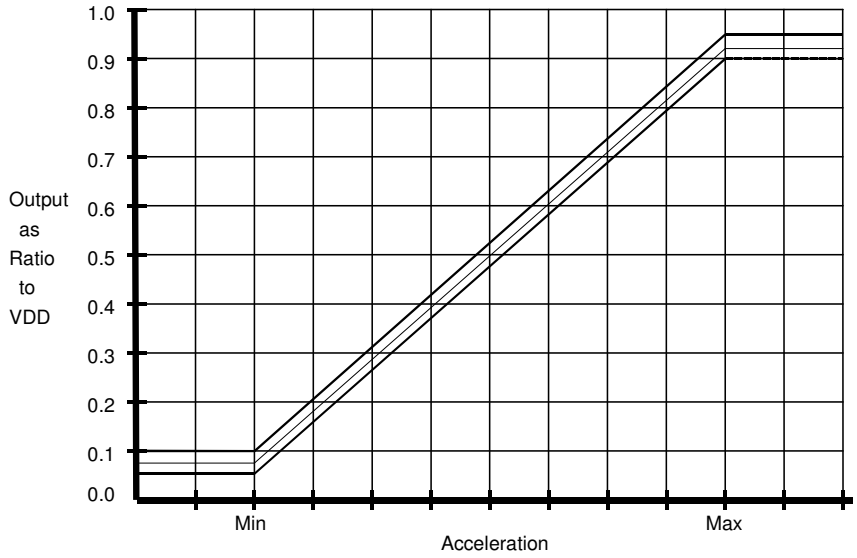
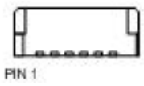


Figure 4. Limiter function.

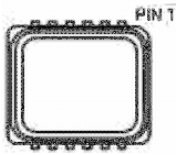
Limiter function limits the output voltage between specified upper and lower limit. In normal operation (V_{DD} = 5.0 V), when limiter is enabled, the output voltage is valid between 0.5 V…4.5 V. Limiting activates between 0.25 V…0.5 V and 4.5 V…4.75 V. Only failures drive output voltage beyond cutoff voltages.

2. Functional Description

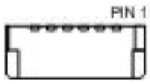
2.1. Measuring directions



+1 g position
$V_{out,nom}$ = 2.5 V



0 g position
$V_{out.nom}$ = 1.5625 V



–1 g position
$V_{out.nom}$ = 0.625 V

2.2. Voltage to acceleration conversion

Analog output can be transferred to acceleration using the following equation for conversion:

$$Acceleration = \frac{V_{out} - V_{out}(0g)}{Sensitivity} \text{ [g]}$$

where: $V_{out}(0g)$ = nominal output of the device at 0g position with 5 V supply voltage (ratiometric output), Sensitivity is the sensitivity of the device and V_{out} is the output of the sensor.

2.3. Ratiometric Output

Ratiometric output means that the zero offset point and sensitivity of the sensor are proportional to the supply voltage. If the SCA720 supply voltage is fluctuating the SCA720 output will also vary. When the same reference voltage for both the SCA720 sensor and the measuring part (A/D-converter) is used, the error caused by reference voltage variation is automatically compensated for.

2.4. Selftest and failure detection modes

To ensure reliable measurement results the SCA720 has continuous interconnection failure and calibration memory validity detection. A detected failure forces the output signal close to power supply ground or VDD level, outside the normal output range.

The calibration memory validity is verified by continuously running parity check for the control register memory content. In the case where a parity error is detected, the control register is automatically re-loaded from the EEPROM. If a new parity error is detected after re-loading data analog output voltage is forced to go close to ground level (<0.25 V).

The SCA720 also includes a separate self test mode. The true self test simulates acceleration, or deceleration, using an electrostatic force. The electrostatic force simulates acceleration that is high enough to deflect the proof mass to the extreme positive position, and this causes the output signal to go to the maximum value. The self test function is activated by a separate on-off command on the self test input.

The self-test generates an electrostatic force, deflecting the sensing element's proof mass, thus checking the complete signal path. The true self test performs following checks:

- Sensing element movement check
- ASIC signal path check
- PCB signal path check
- Micro controller A/D and signal path check

The created deflection can be seen in analogue output. Self test can be activated applying logic"1" (positive supply voltage level) to ST pin (pin 9) of SCA720. The self test Input high voltage level is 4 – Vdd+0.3 V and input low voltage level is 0.3 – 1 V.

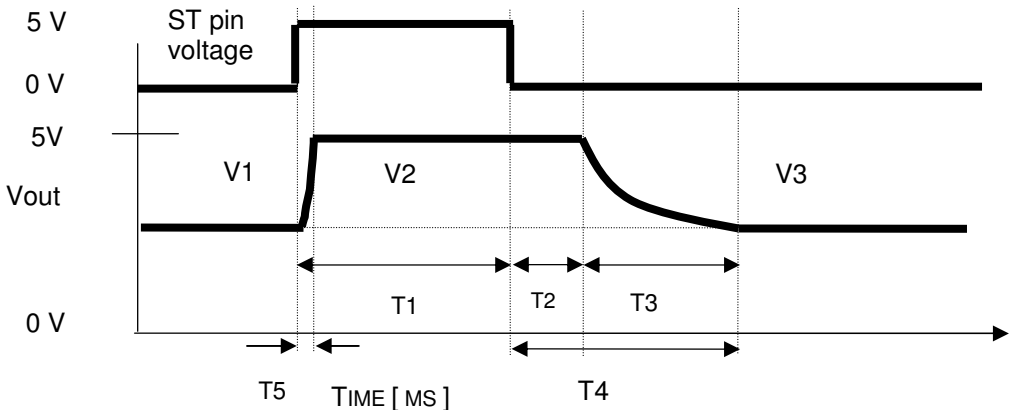


Figure 7. Self test wave forms.

V1 = initial output voltage before the self test function is activated.
V2 = output voltage during the self test function.
V3 = output voltage after the self test function has been de-activated and after stabilization time Please note that the error band specified for V3 is to guarantee that the output is within 5% of the initial value after the specified stabilization time. After a longer time (max. 1 second) V1=V3.
T1 = Pulse length for Self test activation
T2 = Saturation delay
T3 = Recovery time
T4 = Stabilization time =T2+T3
T5 = Rise time during self test.

T1 [ms]	T2 [ms]	T3 [ms]	T4 [ms]	T5 [ms]	V2:	V3:
10-100	Typ. 20	Typ. 50	Typ. 70	Typ. 10	Min 0.95*VDD (4.75V @Vdd=5V)	0.95*V1-1.05*V1

Self test characteristics.

3. Application information

The SCA720 should be powered from a well regulated 5 V DC power supply. Coupling of digital noise to the power supply line should be minimized. 100nF filtering capacitor between VDD pin 11 and GND plane must be used. If regulator is placed far from component for example other PCB it is recommend adding more capacitance between VDD and GND to ensure current drive capability of the system. For example 470 pF and 1uF capacitor can be used.

The SCA720 has a ratiometric output. To get the best performance use the same reference voltage for both the SCA720 and Analog/Digital converter.

Locate the 100nF power supply filtering capacitor close to VDD pin 11. Use as short a trace length as possible. Connect the other end of capacitor directly to the ground plane. Connect the GND pin 5 to underlying ground plane. Use as wide ground and power supply planes as possible. Avoid narrow power supply or GND connection strips on PCB.

3.1. Housing dimensions and recommended PCB layout

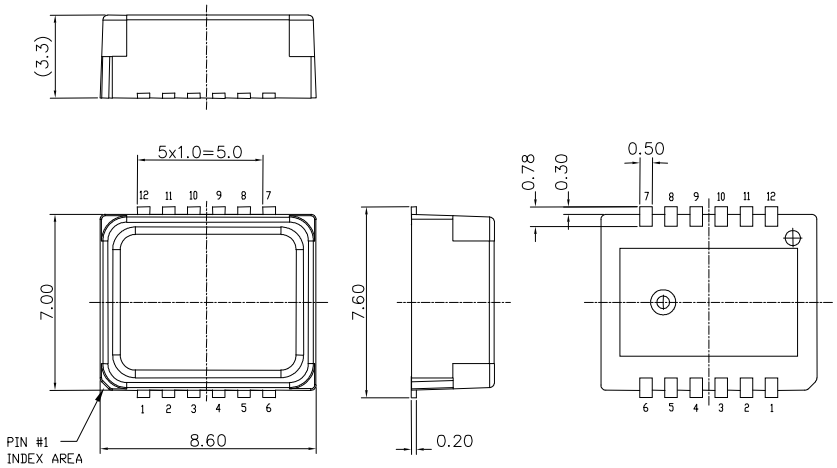


Figure 8. Housing dimensions and recommended PCB layout [mm].

Notes:

- It is important that the part is parallel to the PCB plane and that there is no angular alignment error from intended measuring direction during assembly process.
- 1° mounting alignment error will increase the cross-axis sensitivity by 1.7%
- 1° mounting alignment error will change the output by 17 mg
- Wave soldering is not recommended
- Ultrasonic cleaning is not allowed
- A supply voltage by-pass capacitor (> 100 nF) is recommended

3.2. Reflow soldering

The SCA720 is suitable for Sn-Pb eutectic and Pb- free soldering process and mounting with normal SMD pick-and-place equipment. Recommended body temperature profile during reflow soldering:

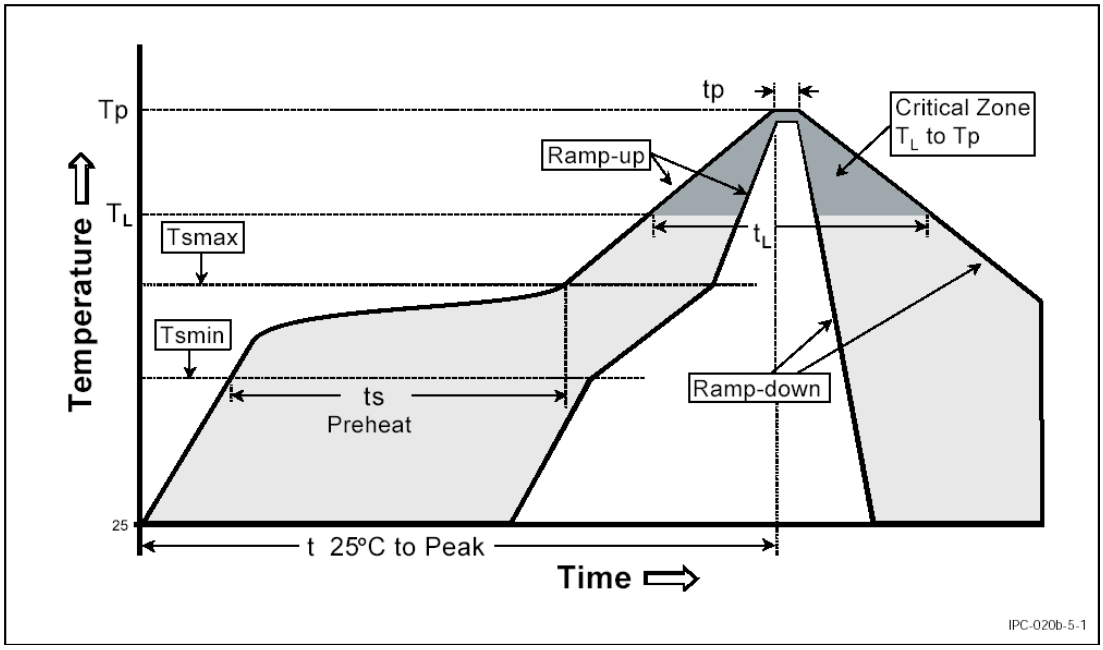


Figure 10. Recommended body temperature profile during reflow soldering. Ref. IPC/JEDEC J-STD-020D.

Profile feature	Sn-Pb Eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T_L to T_P)	3 °C/second max.	3 °C/second max.
Preheat - Temperature min (T_{smin}) - Temperature max (T_{smax}) - Time (min to max) (ts)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Tsmax to T_L - Ramp up rate		3°C/second max
Time maintained above: - Temperature (T_L) - Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak temperature (T_P)	240 +0/–5 °C	250 +0/–5 °C
Time within 5 °C of actual Peak Temperature (T_P)	10-30 seconds	20-40 seconds
Ramp-down rate	6 °C/second max	6 °C/second max
Time 25 °C to Peak temperature	6 minutes max	8 minutes max

The Moisture Sensitivity Level of the part is 3 according to the IPC/JEDEC J-STD-020D. The part should be delivered in a dry pack. The manufacturing floor time (out of bag) in the customer's end is 168 hours.

Notes:

- Preheating time and temperatures according to guidance from solder paste manufacturer.
- It is important that the part is parallel to the PCB plane and that there is no angular alignment error from intended measuring direction during assembly process.
- Wave soldering is not recommended.
- **Ultrasonic cleaning is not allowed**. The sensing element may be damaged by an ultrasonic cleaning process

The Moisture Sensitivity Level of the part is 3 according to the IPC/JEDEC J-STD-020B. The part should be delivered in a dry pack. The manufacturing floor time (out of bag) in the customer's end is 168 hours. Maximum soldering temperature is 250 ℃/40 sec.

Rework after the initial soldering process is not recommended. Rework can cause heat build-up to the leg and this heat build-up will cause the housing material to get soft thus allowing the leg to move. The movement can cause bond wire disconnection inside the part.