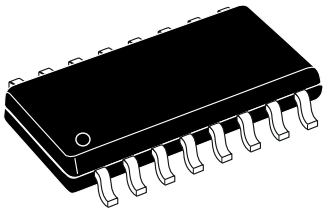
STDRIVEG600

Datasheet

High voltage half-bridge gate driver for GaN transistors



SO-16

Features

- dV/dt immunity ±200 V/ns
- Driver current capability:
  - 1.3/2.4 A source/sink typ @ 25 °C, 6 V
  - 5.5/6 A source/sink typ @ 25 °C, 15 V
- Separated turn on and turn off gate driver pins
- 45 ns propagation delay with tight matching
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Interlocking function
- UVLO on low-side and high-side sections
- Dedicated pin for shut down functionality
- Over temperature protection

Applications

- High-voltage PFC, DC-DC and DC-AC converters
- Switch-mode power supplies
- UPS systems
- Solar power
- Motor driver for home appliances, factory automation and industrial drives.

Product status link
STDRIVEG600

Product label
SUSTAINABLE TECHNOLOGY

Description

The STDRIVEG600 is a single chip half-bridge gate driver for Enhancement mode GaN FETs or N-channel power MOSFET.

The high-side section is designed to stand a voltage up to 600 V and is suitable for designs with bus voltage up to 500 V.

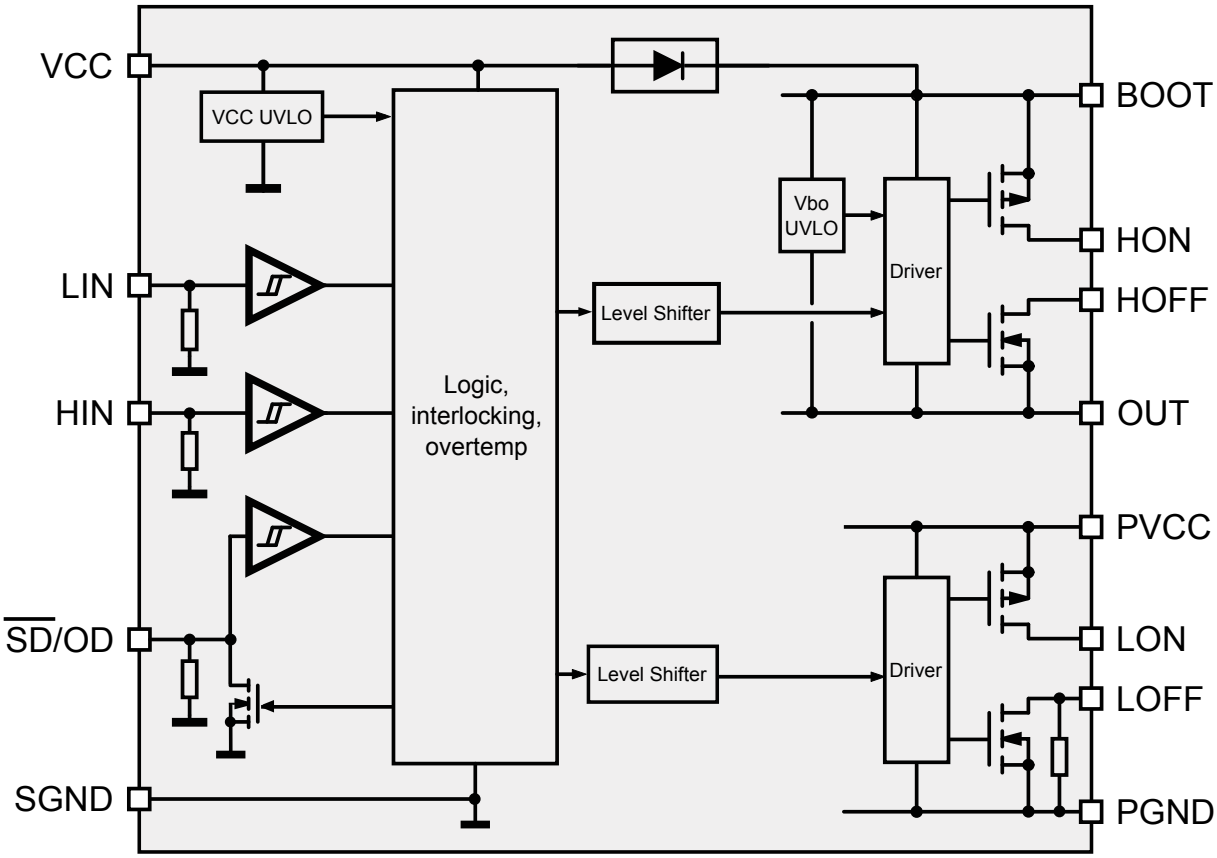
The device is designed for driving high-speed GaN and Si FETs thanks to high current capability, short propagation delay and operation with supply voltage down to 5 V.

The STDRIVEG600 features UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions, and the interlocking function avoids cross-conduction conditions.

The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing with microcontroller and DSP.

1 Block diagram

Figure 1. **STDRIVEG600 block diagram**



2 Pin description and connection diagram

Figure 2. **Pin connection SO-16 (top view)**

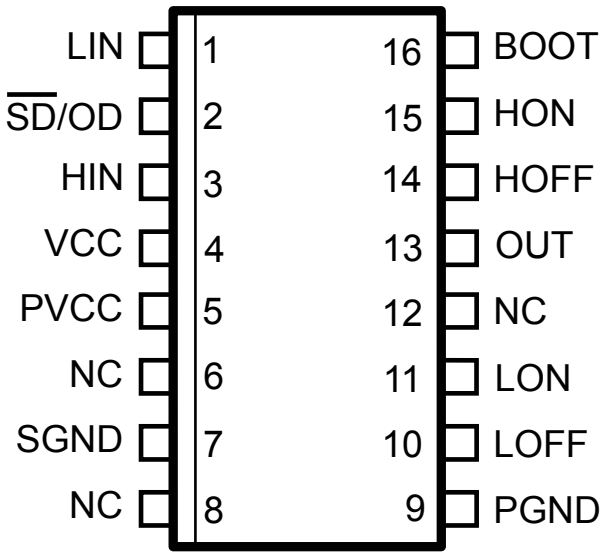


Table 1. **Pin description**

Pin #	Pin Name	Type	Function
1	LIN	I	Low-side driver logic input (active high)
2	$\overline{SD}$/OD	I	Shut down logic input (active low); open-drain output signals overtemperature protection
3	HIN	I	High-side driver logic input (active high)
4	VCC	P	Logic supply voltage
5	PVCC	P	Low-side driver supply voltage
7	SGND	P	Signal ground
9	PGND	P	Low-side driver ground
10	LOFF	O	Low-side driver sink output
11	LON	O	Low-side driver source output
13	OUT	P	High-side (floating) common voltage
14	HOFF	O	High-side driver sink output
15	HON	O	High-side driver source output
16	BOOT	P	Bootstrap supply voltage
6, 8, 12	NC	-	Not connected

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value[1]		Unit
		Min.	Max.	
VCC	Logic supply voltage	-0.3	21	V
V_{PG} [2]	Low-side driver supply voltage	-0.3	21	V
VCC-PGND	Logic supply vs. Low-side driver ground	-0.3	21	V
PVCC	Low-side driver supply vs. logic ground	-0.3	21	V
PGND	Low-side driver ground vs. logic ground	-21	21	V
V_{BO} [3]	High-side supply voltage	-0.3	21	V
BOOT	Bootstrap voltage	-0.3	620	V
V_{HS}	High-side gate output voltage (HON, HOFF)	OUT - 0.3	BOOT + 0.3	V
V_{LS}	Low-side gate output voltage (LON, LOFF)	PGND - 0.3	PVCC + 0.3	V
V_i	Logic input pins voltage (LIN, HIN, $\overline{SD}$/OD)	-0.3	21	V
dV_{OUT}/dt	Output slew rate [4]	-	200	V/ns
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C
ESD	Human body model	1750[5]		V

1. *Each voltage referred to SGND unless otherwise specified*
2. *V_{PG} = PVCC - PGND*
3. *V_{BO} = BOOT - OUT*
4. *See Figure 15*
5. *High voltage pins 13 to 16 vs. SGND have HBM 1250 V ratings conforming to ANSI/ESDA/JEDEC JS-001-2014*

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ (JA)}$	Thermal resistance junction to ambient [1]	80	°C/W
$R_{th(JCtop)}$	Thermal resistance junction to case top [2]	34	°C/W

1. *JEDEC JESD51-3 1s board, still air.*
2. *JEDEC JESD51-12 cold plate*

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test conditions	Value (1)		Unit
				Min.	Max.	
VCC	4 vs. 7	Logic Supply voltage	-	4.75	20	V
V_{PG} (2)	5 vs. 9	Low-side driver supply voltage	-	4.75	20	V
VCC-PGND	4 vs. 9	Logic supply vs. LS driver ground	-	0	20	V
VCC-PVCC	4 vs. 5	Logic supply vs. LS driver supply	-	-3	3	V
PVCC	5 vs. 7	Low-side supply pin	-	3	20	V
PGND	9 vs. 7	Low-side driver ground	-	-5	5	V
V_{BO} (3)	16 vs. 13	Floating supply voltage	-	4.4	20	V
OUT	13 vs. 7	DC output voltage	-	-15 (4)	520	V
BOOT	16 vs. 7	Bootstrap voltage	-	0 (5)(6)	530	V
V_i	1,2,3	Logic input voltage	-	0	20	V
f_{sw}	-	Switching frequency(7)	-	-	1	MHz
T_J	-	Junction temperature	-	-40	125	°C

1. *Each voltage referred to SGND unless otherwise specified*
2. *V_{PG} = PVCC - PGND*
3. *V_{BO} = BOOT - OUT*
4. *VCC = 5 V, V_{BO} = 20 V*
5. *BOOT must be ≥ 5 V to propagate high-side commands. Refer to Section 5.4.2*
6. *Actual limit could be limited by bootstrap diode dissipation*
7. *Actual limit depends on power dissipation constraints.*

4 Electrical characteristics

4.1 Electrical characteristics

(VCC = PVCC = 6 V, PGND = SGND, V_{BO} = 6 V; LON = LOFF, HON = HOFF; T_J = +25 °C, unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic section supply							
VCC_{thON}	4	VCC UV turn ON threshold	-	4.2	4.5	4.75	V
VCC_{thOFF}		VCC UV turn OFF threshold	-	3.9	4.2	4.5	V
VCC_{hys}		VCC UV hysteresis	-	0.2	0.3	0.45	V
I_{QVCCU}		VCC Undervoltage quiescent supply current	VCC = PVCC = 3.8 V	-	320	410	µA
I_{QVCC}		VCC quiescent supply current	$\overline{SD}$/OD = LIN = 5 V; HIN = 0 V; OUT = 6 V	-	680	900	µA
I_{SVCC}		VCC switching supply current	$\overline{SD}$/OD = 5 V; f_{SW} = 500 kHz; LIN = not HIN; OUT = 6 V	-	800	-	µA
Low-side driver section supply (1)							
I_{QPVCC}	5	PVCC quiescent current	$\overline{SD}$/OD = LIN = 5 V; HIN = 0 V	-	75	120	µA
I_{SPVCC}		PVCC switching supply current	f_{SW} = 500kHz; No load (2)	-	390	-	µA
High-side floating section supply(3)							
V_{BOthON}	16 - 13	V_{BO} UV turn ON threshold	-	3.6	4.0	4.4	V
$V_{BOthOFF}$		V_{BO} UV turn OFF threshold	-	3.4	3.7	4.0	V
V_{BOhys}		V_{BO} UV hysteresis	-	0.1	0.3	0.5	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	VCC = PVCC = V_{BO} = 3.4 V	-	140	200	µA
I_{QBO}		V_{BO} quiescent current	$\overline{SD}$/OD = HIN = 5 V; LIN = 0 V; OUT = 6 V	-	160	210	µA
I_{SBO}	-	BOOT switching supply current	f_{SW} = 500 kHz; No load; OUT = 20 V (2)	-	1100	-	µA
I_{LK}	13, 14 15, 16	High voltage leakage current	HON = HOFF = OUT = BOOT = 600 V; LIN = 0 V	-	-	11	µA
Bootstrap structure							

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{Dboot}	4 - 16	Bootstrap diode on resistance	LIN = $\overline{SD}$/OD = 5 V; HIN = 0 V; OUT = BOOT = 5.5 V	100	140	170	Ω
Output driving buffers							
I_{SO}	15, 11	High/low-side source short circuit current	V_{PG} = V_{BO} = 15 V (2)	4	5.5	7.5	A
			V_{PG} = V_{BO} = 6 V	1	1.3	1.9	
			V_{PG} = V_{BO} = 6 V; T_J = -40 to +125°C (2)	0.75	-	2.5	
I_{SI}	14, 10	High/low-side sink short circuit current	V_{PG} = V_{BO} = 15 V (2)	4.5	6	8	A
			V_{PG} = V_{BO} = 6 V	1.9	2.4	3	
			V_{PG} = V_{BO} = 6 V; T_J = -40 to +125°C (2)	1.4	-	3.7	
R_{DSonON}	15, 11	High/low-side source R_{DSon}	I = 10 mA; V_{PG} = V_{BO} = 15 V	0.9	1.25	1.7	Ω
			I = 10 mA; V_{PG} = V_{BO} = 6 V	1.3	2	2.4	
			I = 10 mA; V_{PG} = V_{BO} = 6 V; T_J = -40 to +125°C (2)	1	-	3.4	
$R_{DSonOFF}$	14, 10	High/low-side sink R_{DSon}	I = 10 mA; V_{PG} = V_{BO} = 15 V	0.65	0.9	1.25	Ω
			I = 10 mA, V_{PG} = V_{BO} = 6 V	0.85	1.2	1.55	
			I = 10 mA; V_{PG} = V_{BO} = 6 V; T_J = -40 to +125°C (2)	0.7	-	2.2	
R_{BLEED}	10, 9	LS gate bleeder resistor	-	75	100	125	kΩ
Logic inputs							
V_{ih}	1, 2, 3	High level logic threshold voltage	T_J = 25 °C	2	2.17	2.5	V
			T_J = -40 to +125°C (2)	-	-	2.7	
V_{il}		Low level logic threshold voltage	T_J = 25 °C	1.1	1.31	1.45	V
			T_J = -40 to +125°C (2)	0.8	-	-	
V_{hyst}		Logic input threshold hysteresis	-	0.7	0.86	1.2	V
I_{INh}	1, 3	LIN, HIN logic “1” input bias current	LIN = HIN = 5 V	23	33	55	µA
I_{INl}		LIN, HIN logic “0” input bias current	LIN = HIN = 0 V	-	-	1	µA
R_{PD_IN}		LIN, HIN pull-down resistor	-	90	150	220	kΩ
I_{SDh}	2	$\overline{SD}$/OD logic “1” input bias current	$\overline{SD}$/OD = 5 V	11	15	20	µA
I_{SDl}		$\overline{SD}$/OD logic “0” input bias current	$\overline{SD}$/OD = 0 V	-	-	1	µA
R_{PD_SD}		$\overline{SD}$/OD pull-down resistor	-	250	330	450	kΩ

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{TSD}	2	Thermal shutdown unlatch threshold	T_J = 25 °C (4)	0.5	0.75	1.0	V
R_{ON_OD}		$\overline{SD}$/OD on resistance	T_J = 25 °C; $\overline{SD}$/OD = 400 mV (4)	8	10	18	Ω
I_{OL_OD}		$\overline{SD}$/OD low level sink current	T_J = 25 °C; $\overline{SD}$/OD = 400 mV (4)	22	40	50	mA
Over temperature protection							
T_{TSD}	-	Shutdown temperature	(2)	150	175	200	°C
T_{HYS}	-	Temperature hysteresis	(2)	17	20	23	°C
Dynamic characteristics (5)							
t_{on}	1, 3 vs. 10=11 and 14=15	High/low-side driver turn-on propagation delay	OUT = 0 V; LIN, HIN: 0 to 3.3 V; Pulse width > 120 ns; No load	30	45	60	ns
t_{off}		High/low-side driver turn-off propagation delay		30	45	60	ns
t_r	10=11 14=15	Rise time	C_L = 1 nF	-	7	-	ns
t_f		Fall time		-	5	-	ns
MT	1, 3 vs. 10=11 and 14=15	Delay matching high/low-side turn-on/off(6)	OUT = 0 V; LIN, HIN: 0 to 3.3 V; Pulse width > 120 ns; No load	-	0	10	ns
t_{SDon}	2 vs. 10=11 and 14=15	High/low-side driver turn-on propagation delay	OUT = 0 V; SD/OD: 0 to 3.3 V; Pulse width > 120 ns; No load	30	45	60	ns
t_{SDoff}		High/low-side driver turn-off propagation delay		30	45	60	ns

1. *V_{PG} = PVCC - PGND*
2. *Values by characterization data, not tested in production*
3. *V_{BO} = BOOT - OUT*
4. *Wafer level test before packaging*
5. *See Figure 14*
6. *MT = max (|t_{on}(LON/LOFF) - t_{off}(LON/LOFF)|, |t_{on}(HON/HOFF) - t_{off}(HON/HOFF)|, |t_{off}(LON/LOFF) - t_{on}(HON/HOFF)|, |t_{off}(HON/HOFF) - t_{on}(LON/LOFF)|)*

5 Functional description

5.1 Logic inputs

The STDRIVEG600 is a half-bridge gate driver with three logic inputs to control the external high-side and low-side power transistors.

The device is controlled through following logic inputs:

- $\overline{SD}$/OD: Shut-down input, active low;
- LIN: low-side driver inputs, active high;
- HIN: high-side driver inputs, active high.

Table 6. Truth table *(applicable when the device is not in UVLO)*

Inputs			Outputs	
$\overline{SD}$/OD	LIN	HIN	LON = LOFF	HON = HOFF
L	X(1)	X(1)	L	L
H	L	L	L	L
H	L	H	L	H
H	H	L	H	L
H	H	H	L(2)	L(2)

1. *X: Don't care.*
2. *Interlocking function*

The logic inputs have internal pull-down resistors. The purpose of these resistors is to set a proper logic level in case, for example, there is an interruption in the logic lines or the controller outputs are in tri-state conditions.

If logic inputs are left floating, the gate driver outputs are set to low level to turn-off the external power transistors.

The recommended input pulse width to obtain undistorted output pulses (with MT as in Table 5) is 120 ns. Shorter pulses could be extended up to 120 ns or blanked, if shorter than 30 ns (typ).If all inputs are high, the interlocking function turns low both outputs.

5.2 Supply rails, UVLO protections

The device is supplied by three rails (VCC, PVCC and BOOT).

The VCC pin supplies current to the logic circuit, level-shifters in the low-side section and the integrated bootstrap diode.

The PVCC pin supplies low-side output buffer. During outputs commutations the average current used to provide gate charge to the high-side and low-side power switch flow through this pin.

The PVCC pin can be connected either to the same supply voltage of the VCC pin or to a separated voltage source. In case the same voltage source is used, it is suggested to connect VCC and PVCC pins by means of a small decoupling resistance. The use of dedicated bypass ceramic capacitors located as close as possible to each supply pin is highly recommended.

BOOT supplies high-side output buffer through a bootstrap capacitor connected to the OUT pin.

The VCC and BOOT supplies are monitored by undervoltage lockout protection (UVLO) to prevent power switch conduction in dissipative condition due to low V_{GS}.

5.2.1 VCC UVLO protection

Undervoltage protection is available on VCC to GND supply pins, with dedicated circuitry. A hysteresis sets the respective turn-off threshold.

When VCC voltage falls below the VCC_{thOFF} threshold, all the outputs are switched low, both LON/LOFF and HON/HOFF.

When VCC voltage reaches the VCC_{thON} threshold, the device returns to normal operation and sets:

- LON/LOFF output according to actual input pin status;
- HON/HOFF output according to actual input pin status if BOOT-OUT (V_{BO}) is not in UVLO.

Figure 4 shows device behavior while V_{BO} is not in UVLO.

Figure 3. VCC UVLO and LON, LOFF

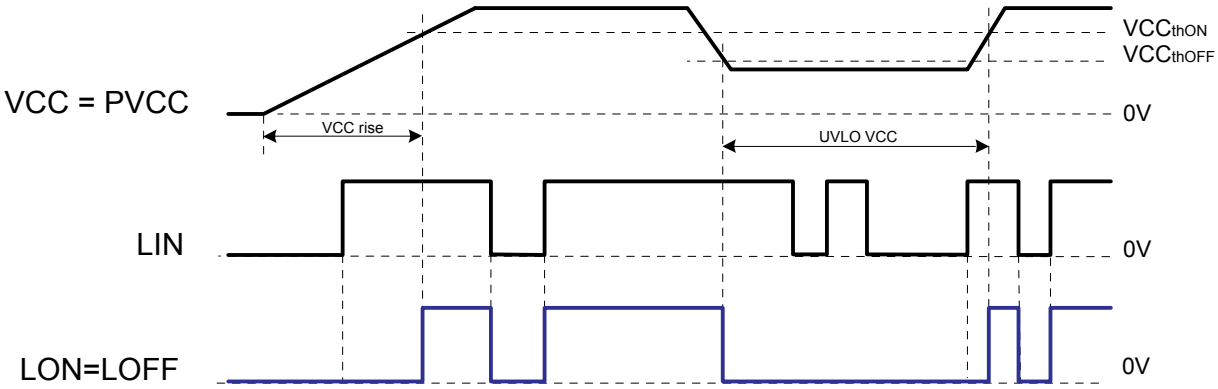
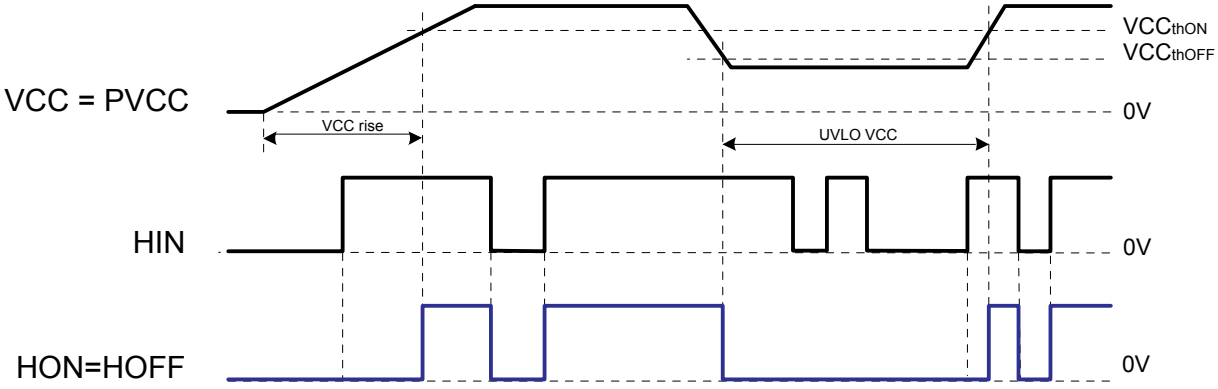


Figure 4. VCC UVLO and HON, HOFF

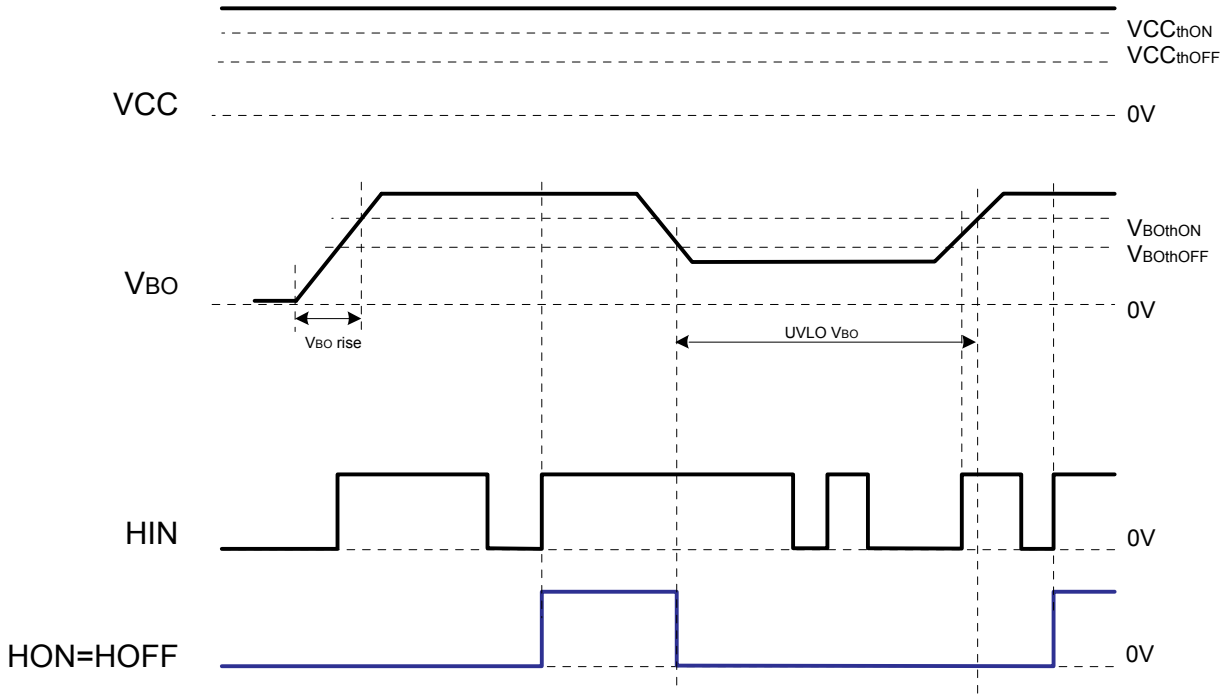


5.2.2 V_{BO} UVLO protection

Undervoltage protection is available on the bootstrap section between BOOT to OUT supply pins (V_{BO}). A hysteresis sets the turn-off threshold.

When V_{BO} voltage goes below $V_{BOthOFF}$ threshold, the HON/HOFF output is switched low. When V_{BO} voltage reaches the V_{BOthON} threshold, the device returns to normal operation and the output remains low until the next HIN input pin transition or VCC UVLO exit.

Figure 5. V_{BO} UVLO



5.3 Thermal shutdown

The STDRIVEG600 has a thermal shutdown protection feature.

When junction temperature reaches the T_{TSD} temperature threshold, the device turns low both driver outputs to leave the half-bridge in 3-state and signaling the state forcing $\overline{SD}$/OD pin low.

The $\overline{SD}$/OD pin is released when junction temperature is below 'T_{TSD}-T_{HYS}' and $\overline{SD}$/OD is below V_{TSD}.

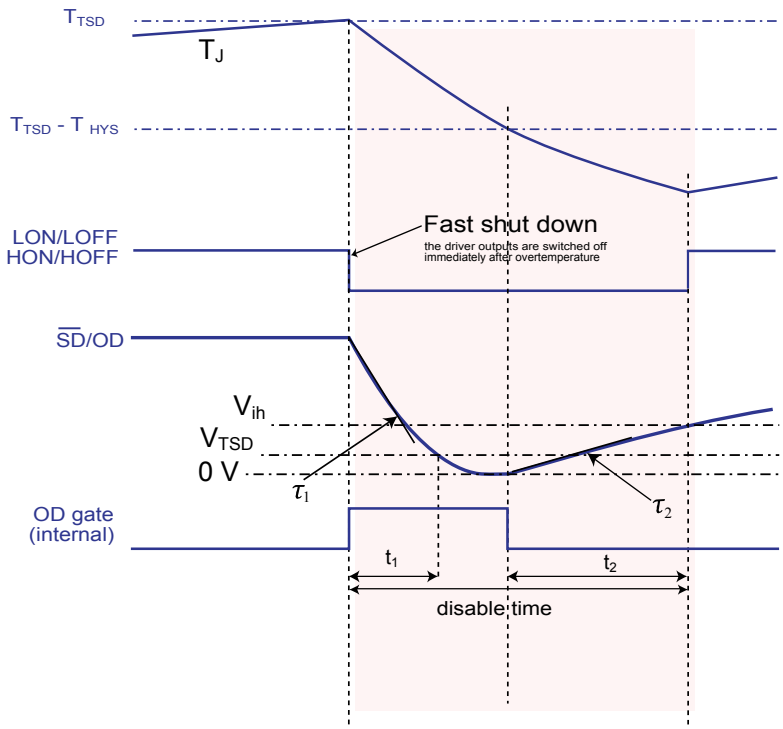
The STDRIVEG600 driver outputs are driven again according to inputs when $\overline{SD}$/OD rise above V_{ih}.

The thermal smart shutdown system gives the possibility to further increase the disable time after the overtemperature event adding the C_{OD} capacitor.

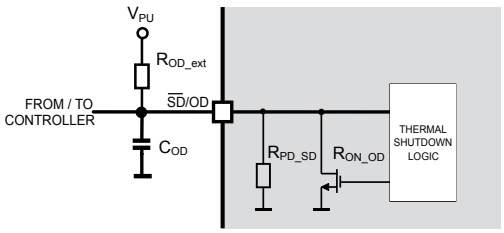
Adding C_{OD} enables to increase the disable time up to very large values without delaying the protection intervention time.

The RC time constant tuned by C_{OD} and R_{OD_ext} determine the additional disable time t_2.

Figure 6. **Thermal Shutdown timing waveform**



THERMAL SHUTDOWN CIRCUIT



5.4 OUT below ground ruggedness and operation

The STDRIVEG600 is a half-bridge gate driver with a high current capability to target high frequency and high current applications.

Any half-bridge inverter inherently includes some inductive parasites in the power loop that generates positive and negative output voltage spikes during power switch commutations, due to dI/dt.

These spikes could be detrimental for inverter EMI, efficiency, power switch operation and application design margin, so spikes shall be minimized to achieve best performance and inverter ruggedness.

Overall spike level is generally minimized first by carefully designing PCB and secondly by tuning switching speed.

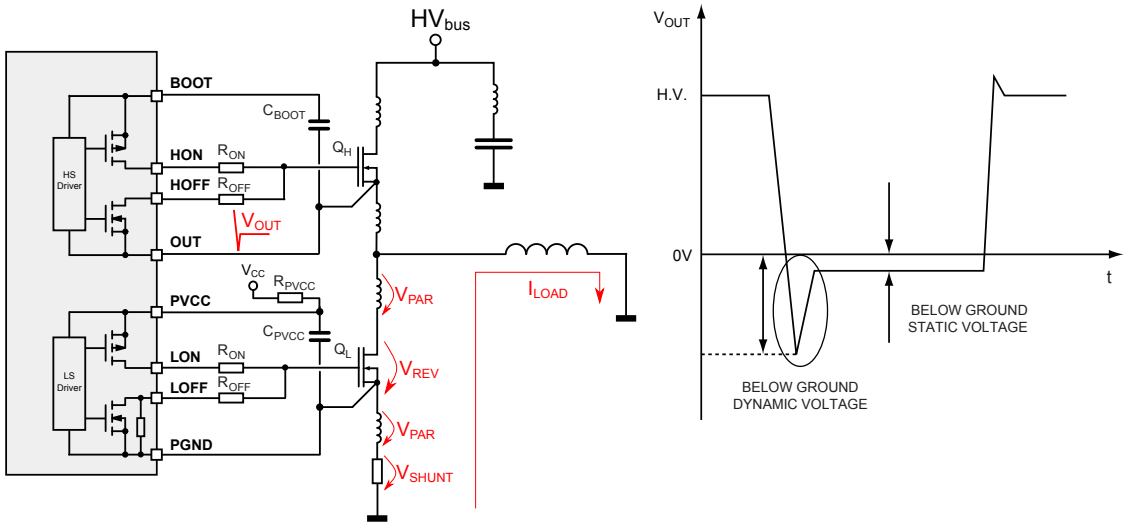
However, low switching speed generally decrease inverter efficiency: a tradeoff between EMI and efficiency is necessary, and some spikes could still be present.

A very common phenomenon observed and analyzed in the application is the OUT below-ground level which is composed by two contributes:

- Dynamic OUT below-GND, primarily due to parasitic inductance, secondary by power switch timing characteristics, with spiky shape.

- Static below-ground, due to low-side reverse conduction characteristics V_{REV} and shunt voltage drop V_{SHUNT}.

Figure 7. Dynamic and static OUT below ground



5.4.1 Dynamic OUT below-GND spike

The dynamic OUT below-ground spike is caused by parasitic inductance due to dI/dt on low-side power switch while current start recirculating after high side Q_H hard turn-off.

Since the dI/dt increases with the value of operating current, the below-GND spike amplitude is generally higher in overload or short-circuit conditions.

Other effects may contribute to the below-GND amplitude, such as for example the low-side MOSFET forward recovery or gate ringing in case of GaN FETs with not optimal gate loop.

The duration of the dynamic below-GND is very short, and for GaN devices usually limited to less than 10 ns.

The waveform Figure 8 shows the STDRIVEG600 observed ruggedness in respect to OUT below-ground dynamic voltage spike obtained with the test setup in Figure 9.

To purposely increase and test very deep OUT below-GND spike, an inductance has been intentionally placed in series to the low-side drain. The STDRIVEG600 operated even with -200 V and deeper spikes.

This deep spike is however unrealistic in properly designed applications and the waveform is reported as ruggedness example. It is always recommended to keep below ground spike small to minimize EMI and maximize application ruggedness.

Figure 8. Dynamic below-ground OUT voltage waveform with -210V peak

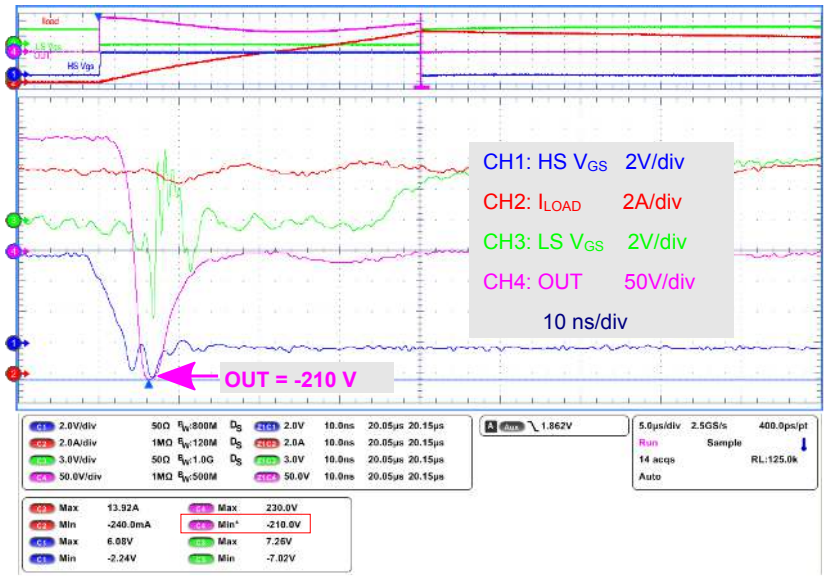
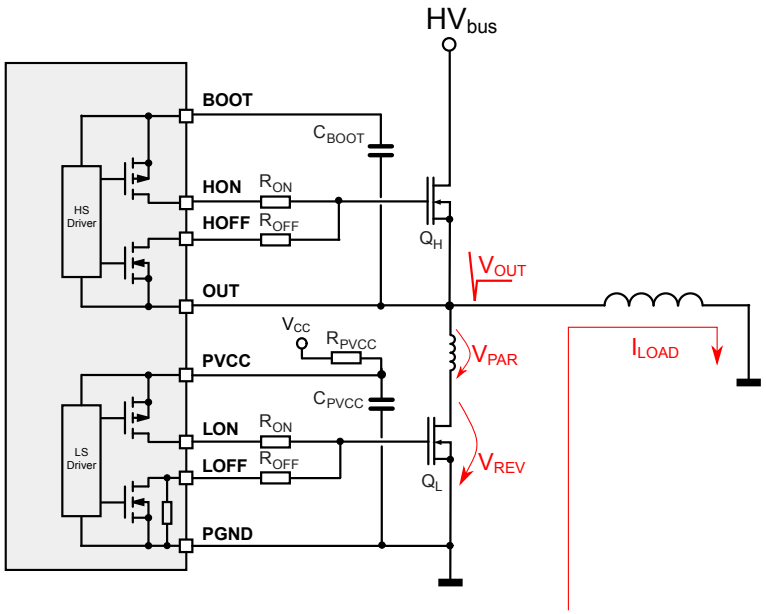


Figure 9. Dynamic below ground OUT voltage test setup



5.4.2 Static OUT below-GND and hard switching topologies

During the below-ground static voltage due to load current recirculation on low side switch Q_L, OUT negative voltage level is determined by low-side power switch reverse conduction drop V_{REV} and the shunt resistor voltage drop V_{SHUNT} (refer to Figure 7).

The voltage on BOOT pin follows OUT voltage with V_{BO} (BOOT-OUT, High-Side driver supply voltage) offset voltage:

Equation 1

$$BOOT = OUT + V_{BO} \quad (1)$$

For example, if OUT= -1 V, with a V_{BO} = 6 V (which is a typical gate voltage for many GaN device), BOOT is 5 V.

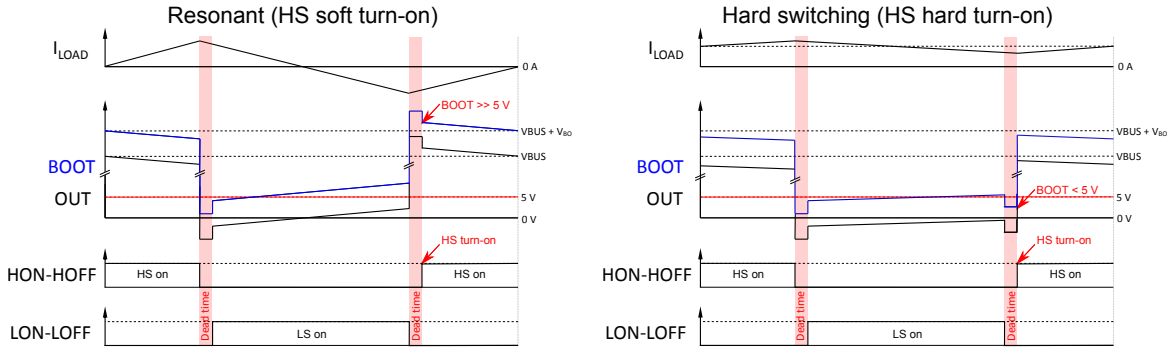
To achieve the driver propagation performance, BOOT shall be ≥ 5 V (refer to Table 4. Recommended operating conditions).

GaN devices have several benefits compared to the Si MOSFET, one of them is the absence of body diode reverse recovery. On the other hand, GaN have worse reverse conduction characteristics.

During current recirculation on low-side while the GaN is off, OUT voltage is typically lower compared to Si MOSFET counterparts and BOOT could be lower than 5 V during a high-side hard turn-on. In such a case, high-side turn-on propagation delay could be higher, or, at the highest current levels, turn-on command missed.

The following Figure 10 schematically shows typical voltages present on a GaN based half-bridge without additional recirculation diodes in parallel to GaN devices.

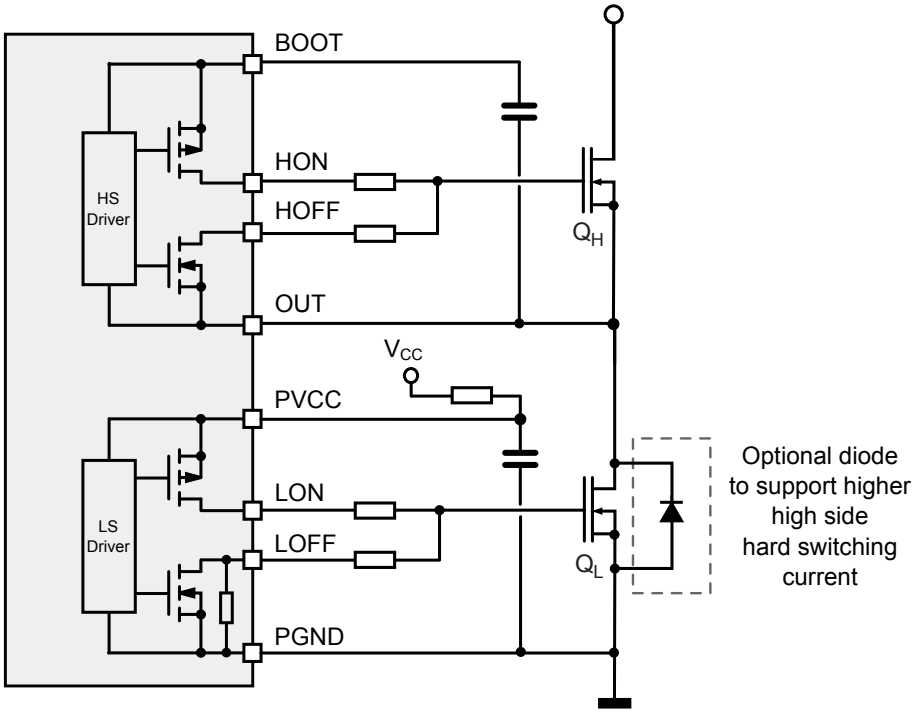
Figure 10. Resonant vs. Hard switching on GaN based half-bridge



In resonant topologies, high-side turn-on command is typically performed “soft” while OUT is already at BUS voltage, so BOOT >> 5 V within recommended conditions.

In hard switching topologies, if high-side turn-on command is performed “hard”, depending on load current, BOOT could be lower than 5 V in GaN based half-bridges. Adding a diode in parallel to low-side GaN can limit drop voltage enabling the use of the driver in those topologies also at high current as shown in Figure 11.

Figure 11. Hard switching topologies with optional diode to increase hard switching current



5.5 PGND and Kelvin source connection

The STDRIVEG600 natively supports source Kelvin connection on both high-side and low-side.

Source Kelvin connection is very beneficial for optimal gate driving, especially for GaN devices.

The dedicated PGND pin of the STDRIVEG600 enables to operate in presence of source bouncing due to the Kelvin connection.

The presence of the dedicated PGND and PVCC pins also enables the use of shunt resistors for load current sensing. This feature simplifies application schematic in GaN shunt-based applications without requiring input isolator or critical input filtering solutions, as suggested by some counterpart devices without dedicated PGND pin.

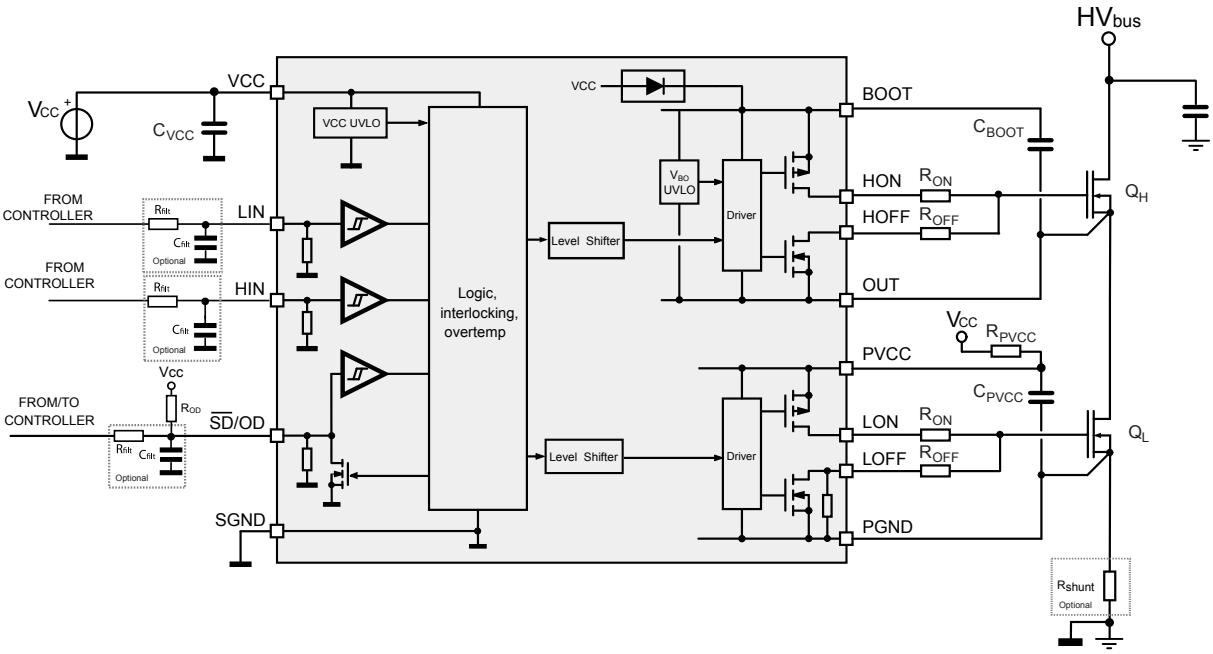
The driver PVCC can be supplied with a simple RC filter like the one shown in Figure 12.

An example of layout using Source Kelvin connection is shown in Figure 13.

6 Typical application diagram and layout guidelines

6.1 Typical application diagram

Figure 12. **Typical application diagram**



6.2 Layout guidelines and considerations

In order to optimize the PCB layout, the following considerations should be taken into account:

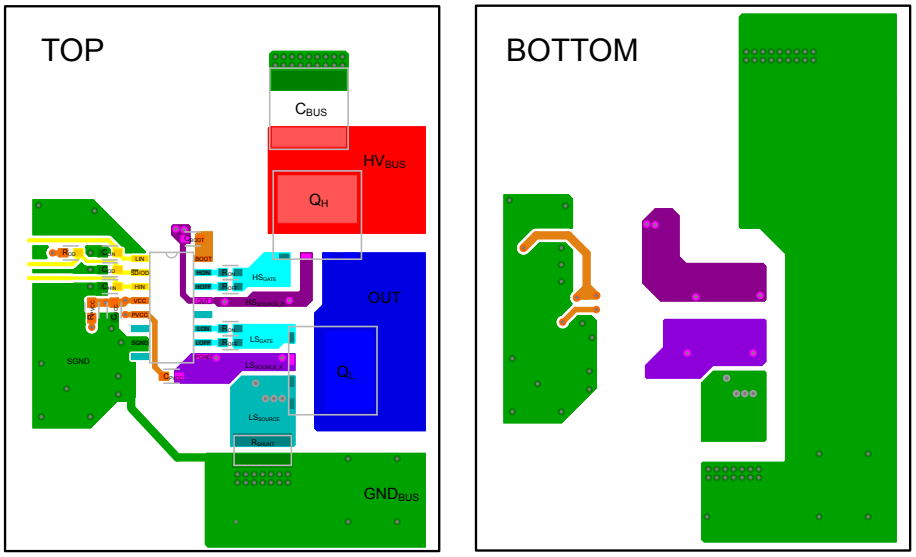
- The power transistors must be placed as close as possible to the gate driver, so to minimize the gate loop area and inductance that might bring about noise, ringing and, in the worst cases, induced turn-on. Gate loop inductance is crucial especially in GaN applications, where the V_{GSth} is typically lower than other technologies. To further minimize gate loop inductance, it is recommended to use an inner plane layer to route the gate current return path (high-side source to the OUT pin and low-side source to the PGND pin) flowing just underneath gate resistors. Adequate vias to connect to the plane shall be placed near driver and power switch source pins.
- If the power transistor provides Kelvin source pin, it shall be used for gate driving while using the standard source pin(s) only for load current. The standard source pin(s) and the Kelvin source pin shall not be shorted together on PCB.
- If the power transistor does not provide Kelvin source pin, the net connecting the driver (PGND and OUT pin) to the power switch source pin shall use a dedicated trace/plane. The trace/plane shall start just on power switch source pin to minimize path sharing between gate current and load current.
- SMT ceramic capacitors (low-ESR and low-ESL) must be placed close to each supply rail pins. A typical 100 nF capacitor must be placed between VDD and SGND, between PVCC and PGND and between BOOT and OUT, as close as possible to device pins, to filter high-frequency noise and spikes. Small case size capacitor of 0603 or even lower size are recommended. In case of high gate charge power transistor, in order to provide local storage for pulsed current gate current, a second capacitor should also be placed close to the supply pins.
- As a good practice it is suggested to foresee filtering capacitors close to logic inputs of the device (HIN, LIN, $\overline{SD}$/OD), in particular for fast switching or noisy applications.

6.3 Layout example

Figure 13 shows an example of STDRIVEG600 half-bridge PCB in a 2-layer layout, corresponding to Figure 12 schematic. The main signals are highlighted by different colors. It is recommended to follow this example for proper positioning and connection of filtering capacitors, gate resistor and minimizing gate loop inductance.

Additional examples are provided with the evaluation boards for Powerflat 5x6 GaN in a 4-layer PCB or with DPAK with 2-layer PCB.

Figure 13. Two-layer layout example



7 Testing and characterization information

Figure 14. **Timing definition**

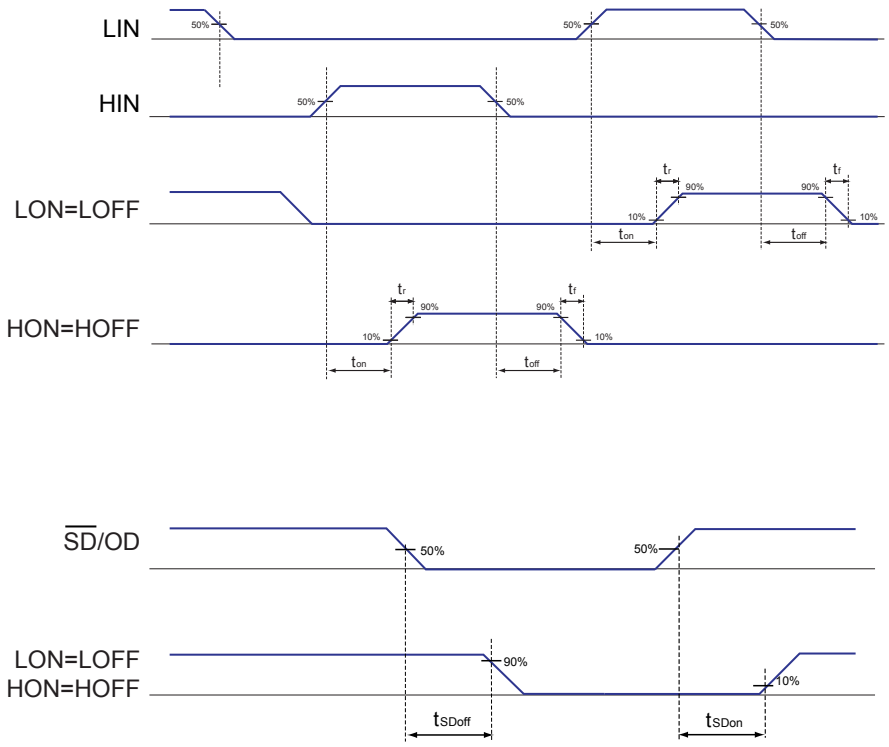
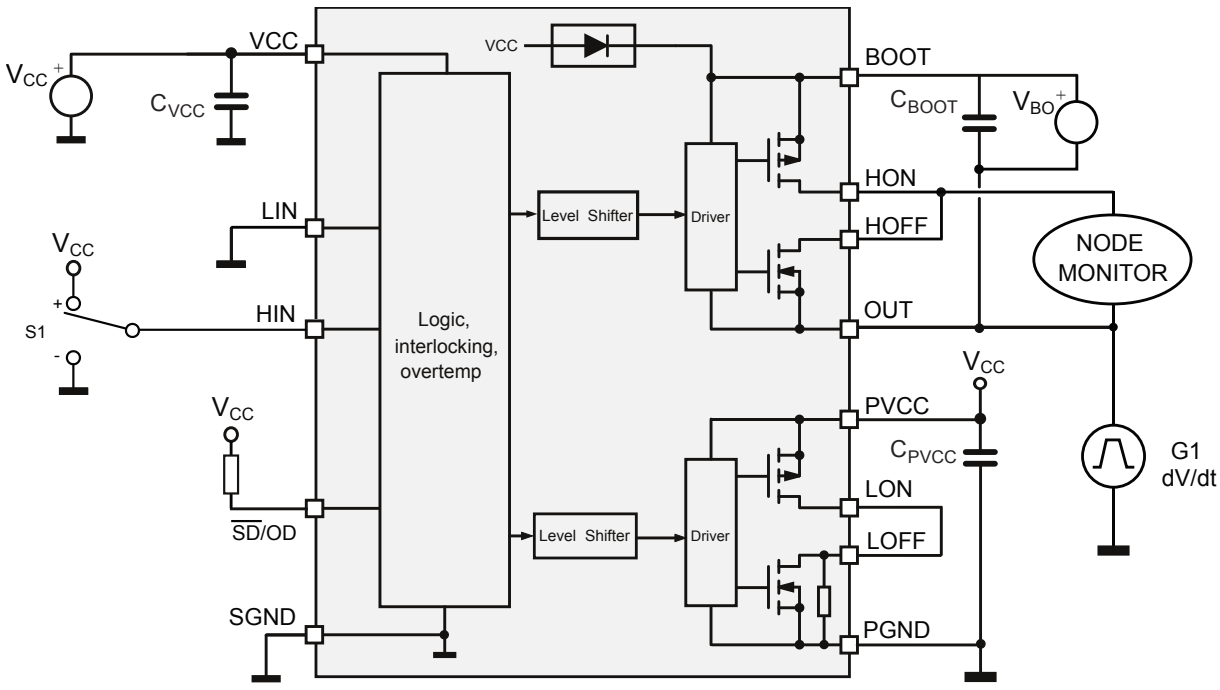


Figure 15. **CMTI characterization test setup**



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 SO-16 package information

Figure 16. **SO-16 mechanical data**

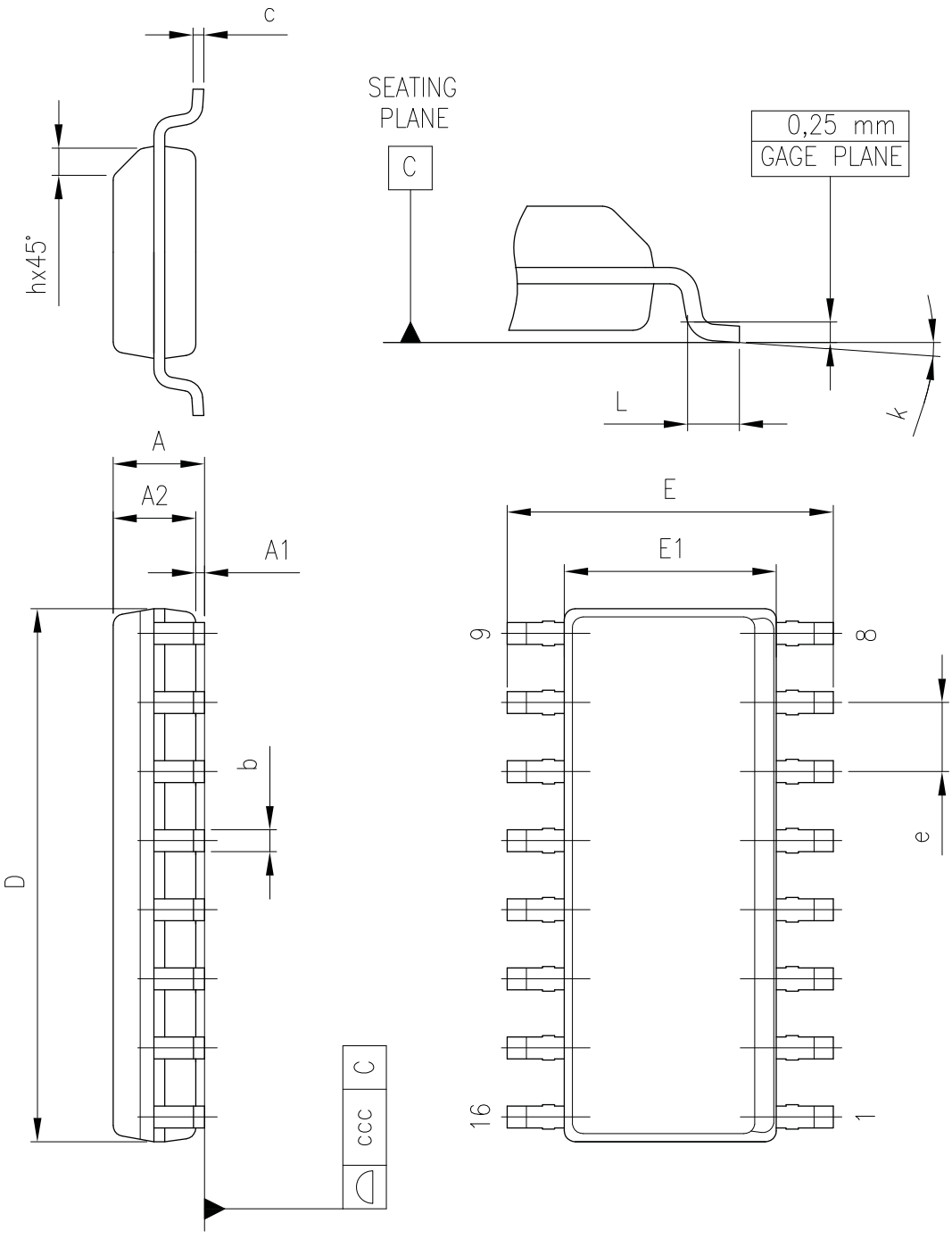
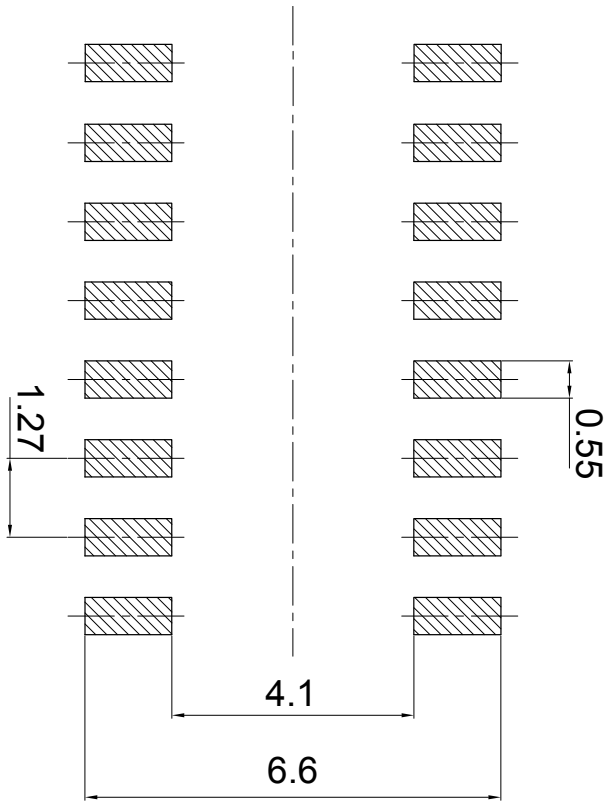


Table 7. **SO-16 package dimensions**

Dim.	mm		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	-	1.27	-
h	0.25	-	0.50
L	0.40	-	1.27
k	0°	-	8°
ccc	-	-	0.10

Figure 17. **SO-16 suggested land pattern**



9 Ordering information

Table 8. **Order codes**

Order Code	Package	Marking	Packaging
STDRIVEG600	SO-16	STDRIVEG600	Tube
STDRIVEG600TR	SO-16	STDRIVEG600	Tape and reel

Revision history

Table 9. **Document revision history**

Date	Version	Changes
21-Jun-2021	1	Initial release.

Contents

List of figures

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