

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C6 650V

650V CoolMOS™ C6 Power Transistor
IPS65R950C6

Data Sheet

Rev. 2.0
Final

Industrial & Multimarket

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ C6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features

- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

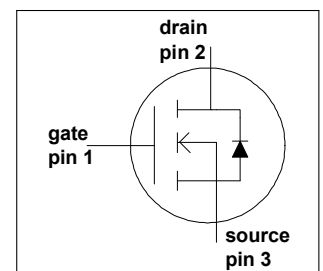


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j \max}$	700	V
$R_{DS(on), \max}$	0.95	Ω
Q_g, typ	15.3	nC
I_D, pulse	12	A
$E_{oss} @ 400V$	1.5	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPS65R950C6	PG-TO 251	65C6950	see Appendix A

Table of Contents

Description	2
Table of Contents	3
Maximum ratings	4
Thermal characteristics	5
Electrical characteristics	6
Electrical characteristics diagrams	8
Test Circuits	12
Package Outlines	13
Appendix A	14
Revision History	15
Disclaimer	15

2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			4.5	A	$T_C = 25^\circ\text{C}$
				2.8		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			12	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			50	mJ	$I_D = 1.0\text{A}$, $V_{DD} = 50\text{V}$ (see table 18)
Avalanche energy, repetitive	E_{AR}			0.15	mJ	$I_D = 1.0\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			1.0	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 480\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{Hz}$)
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Continuous diode forward current	I_S			3.9	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			12	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$ (see table 16)
Maximum diode commutation speed	di_t/dt			500	A/ μs	
Power dissipation	P_{tot}			37	W	$T_C = 25^\circ$

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics IPAK SL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			3.4	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			62	°C/W	leaded
			35			
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0\text{V}$, $I_D = 1\text{mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS} = V_{GS}$, $I_D = 0.2\text{mA}$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 25^\circ\text{C}$
			10			$V_{DS} = 650\text{V}$, $V_{GS} = 0\text{V}$, $T_j = 150^\circ\text{C}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20\text{V}$, $V_{DS} = 0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$		0.855	0.95	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$, $T_j = 25^\circ\text{C}$
			2.223			$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$, $T_j = 150^\circ\text{C}$
Gate resistance	R_G		5.5		Ω	$f = 1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		328		pF	$V_{GS} = 0\text{V}$, $V_{DS} = 100\text{V}$, $f = 1\text{MHz}$
Output capacitance	C_{oss}		23		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		14		pF	$V_{GS} = 0\text{V}$, $V_{DS} = 0 \dots 480\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		58.5		pF	$I_D = \text{constant}$, $V_{GS} = 0\text{V}$, $V_{DS} = 0 \dots 480\text{V}$
Turn-on delay time	$t_{d(on)}$		6.6		ns	$V_{DD} = 400\text{V}$, $V_{GS} = 13\text{V}$, $I_D = 2.2\text{A}$, $R_G = 10.2\Omega$ (see table 17)
Rise time	t_r		5.2		ns	
Turn-off delay time	$t_{d(off)}$		41		ns	
Fall time	t_f		13.6		ns	

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		1.8		nC	$V_{DD} = 480\text{V}$, $I_D = 2.2\text{A}$, $V_{GS} = 0 \text{ to } 10\text{V}$
Gate to drain charge	Q_{gd}		8		nC	
Gate charge total	Q_g		15.3		nC	
Gate plateau voltage	$V_{plateau}$		5.1		V	

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 2.2A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		226		ns	$V_R = 400V, I_F = 2.2A,$ $di_F/dt = 100A/\mu s$ (see table 16)
Reverse recovery charge	Q_{rr}		1.3		μC	
Peak reverse recovery current	I_{rrm}		9.9		A	

5 Electrical characteristics diagrams

Table 8

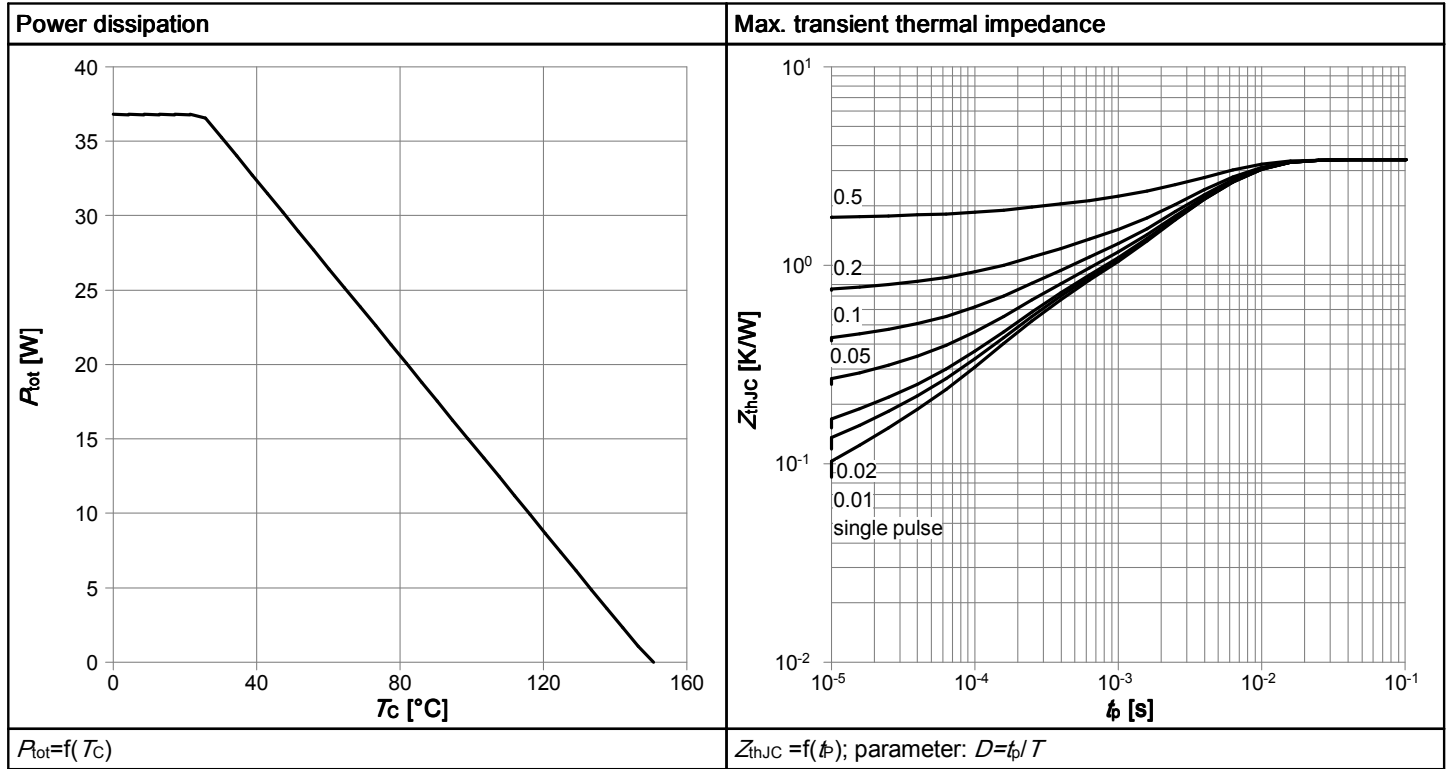


Table 9

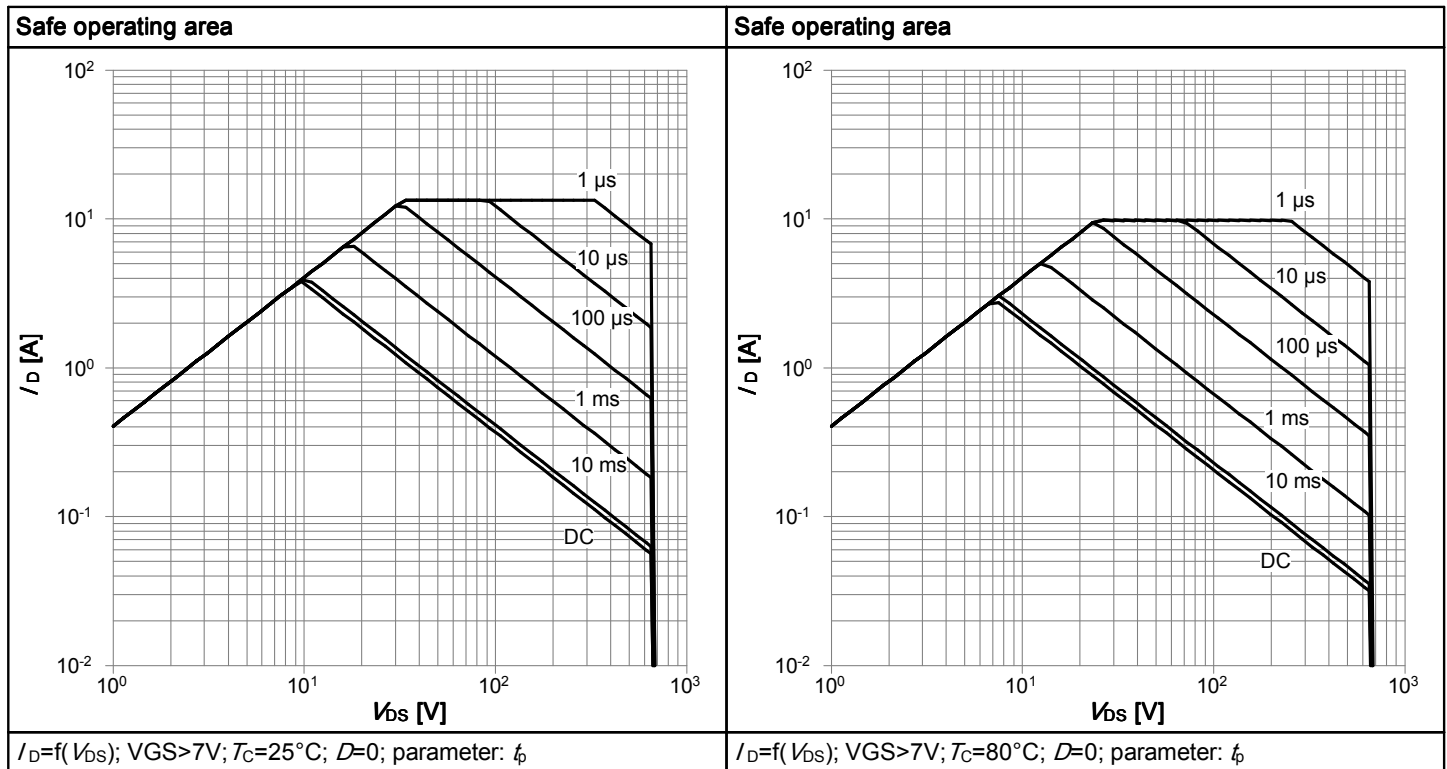


Table 10

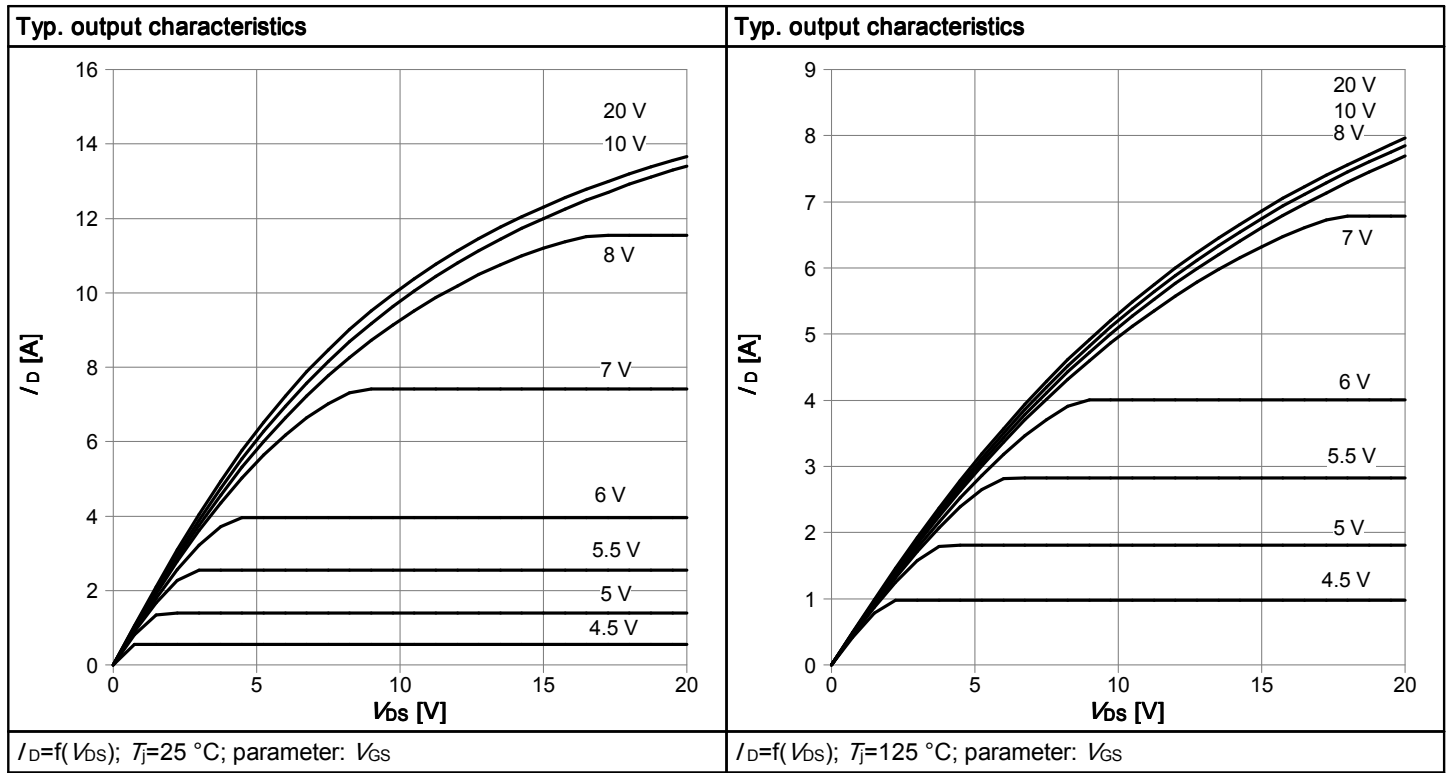


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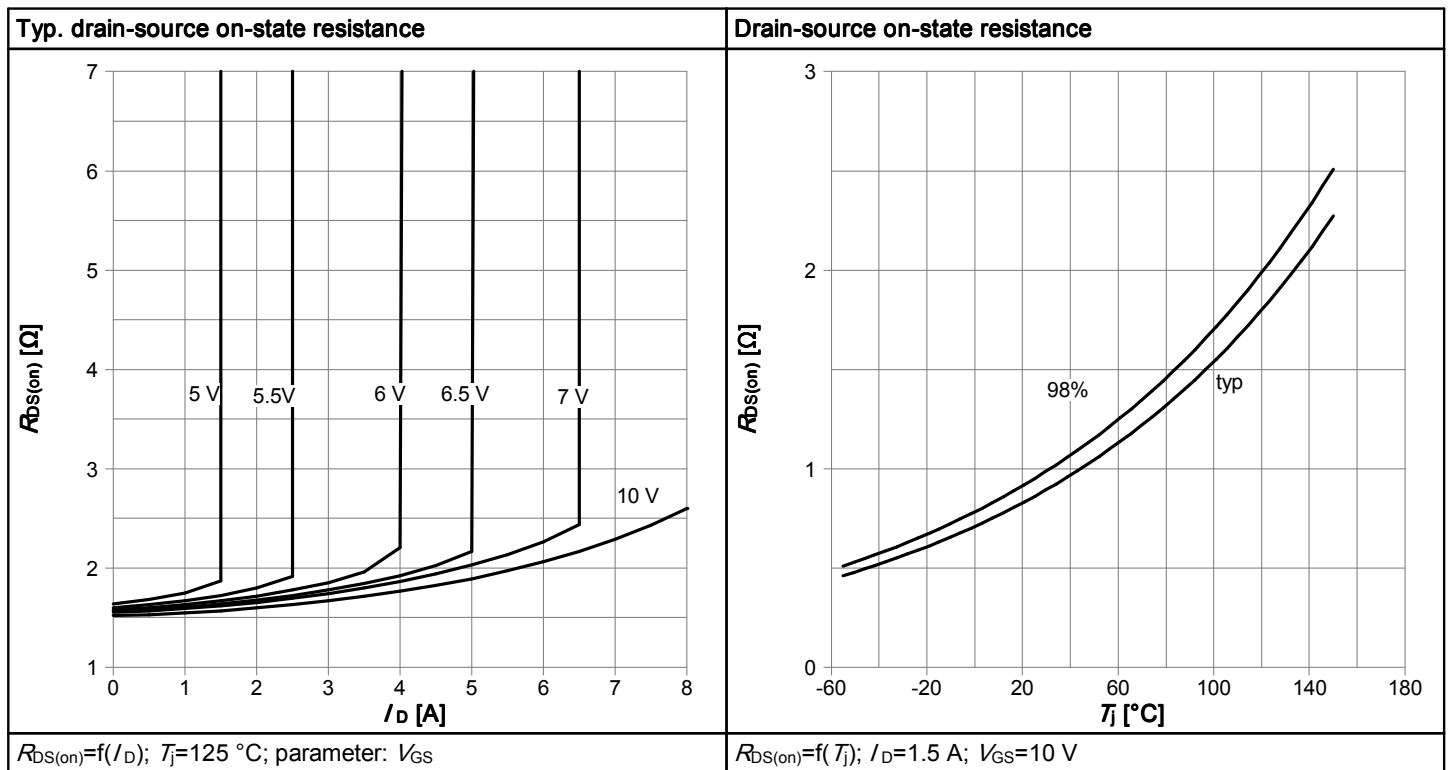


Table 12

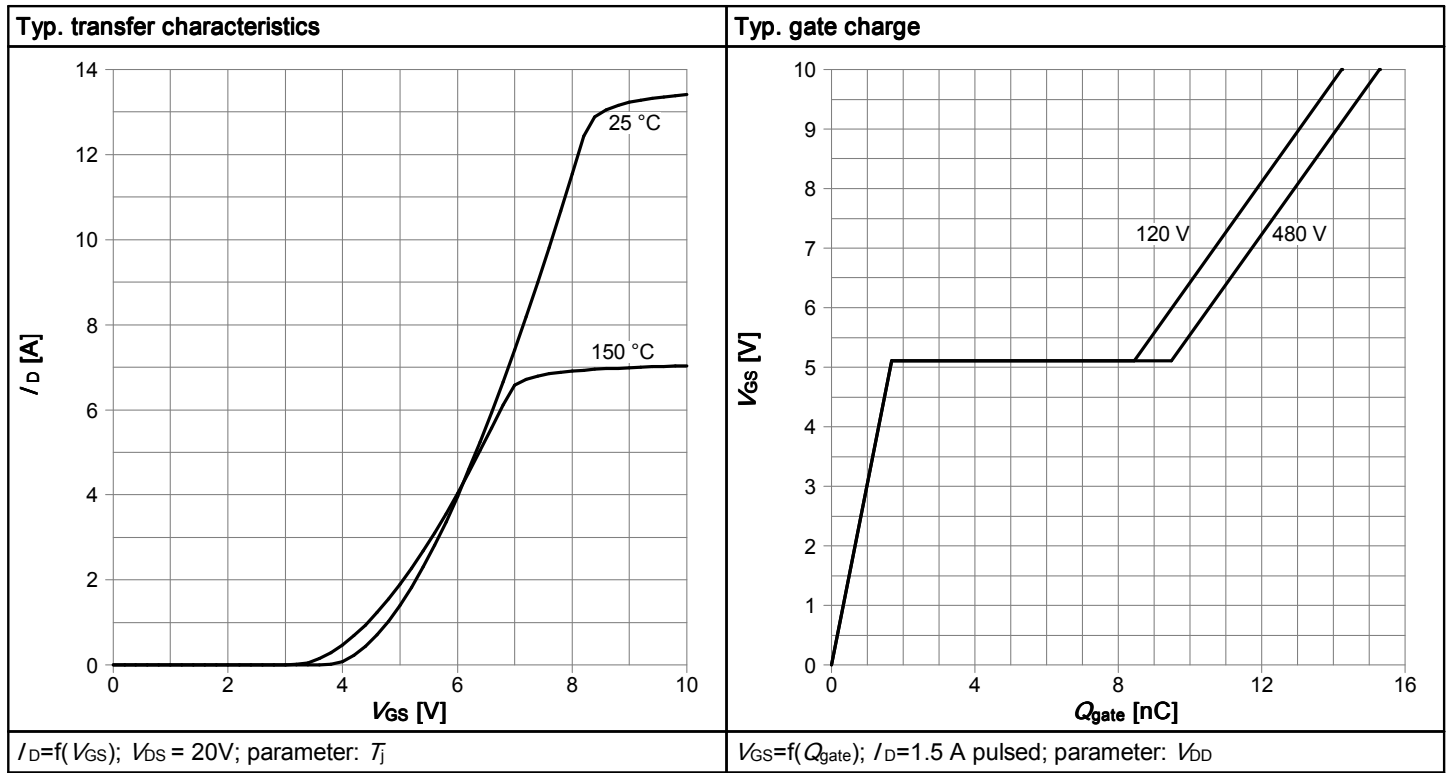


Table 13

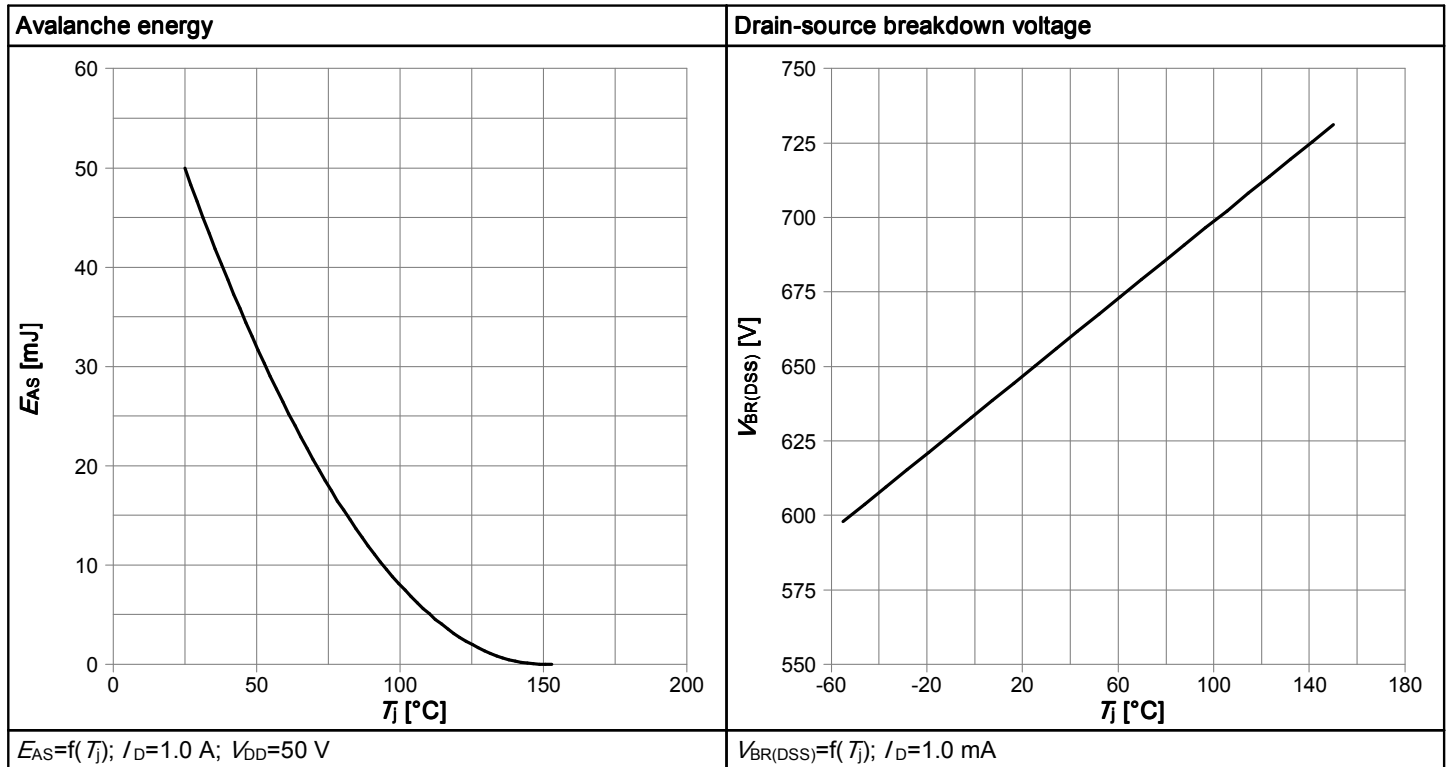


Table 14

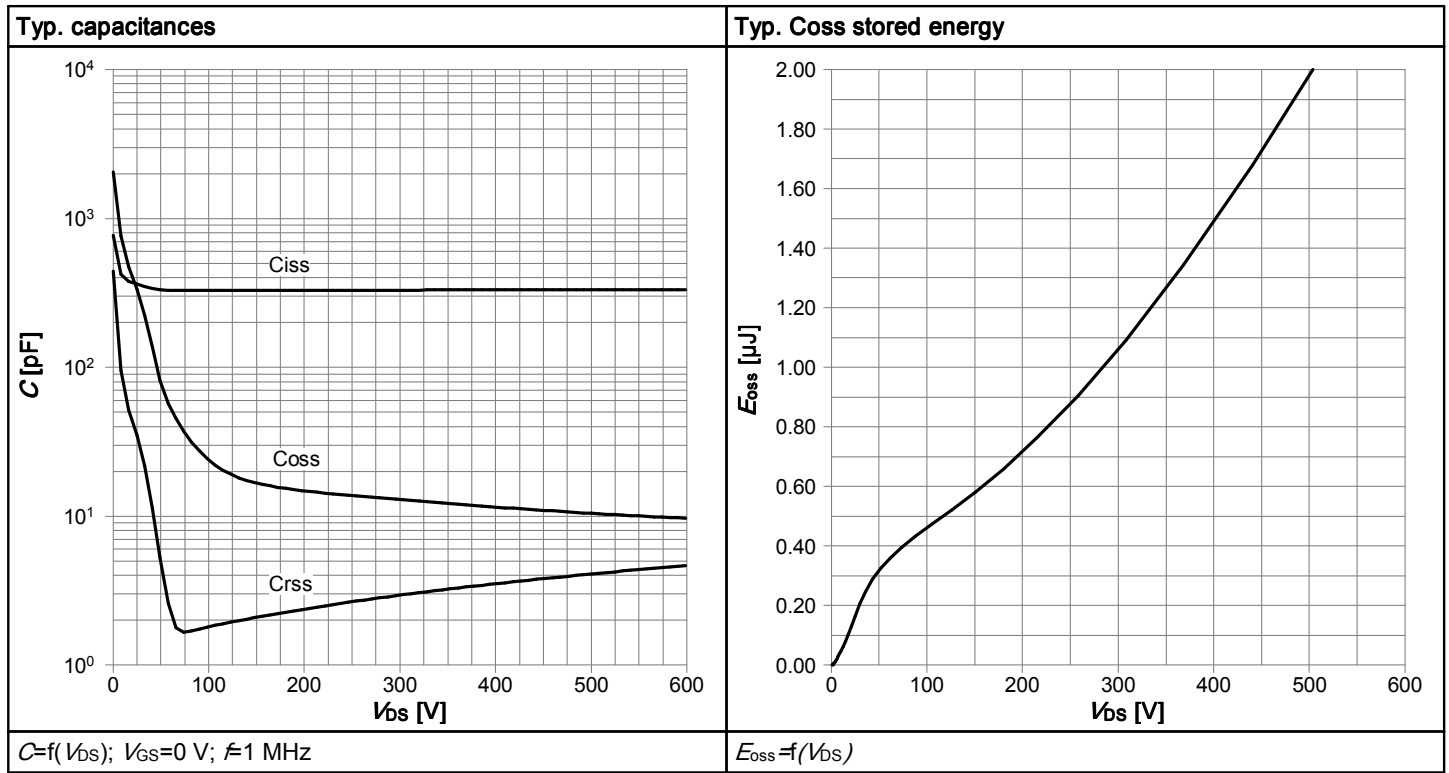
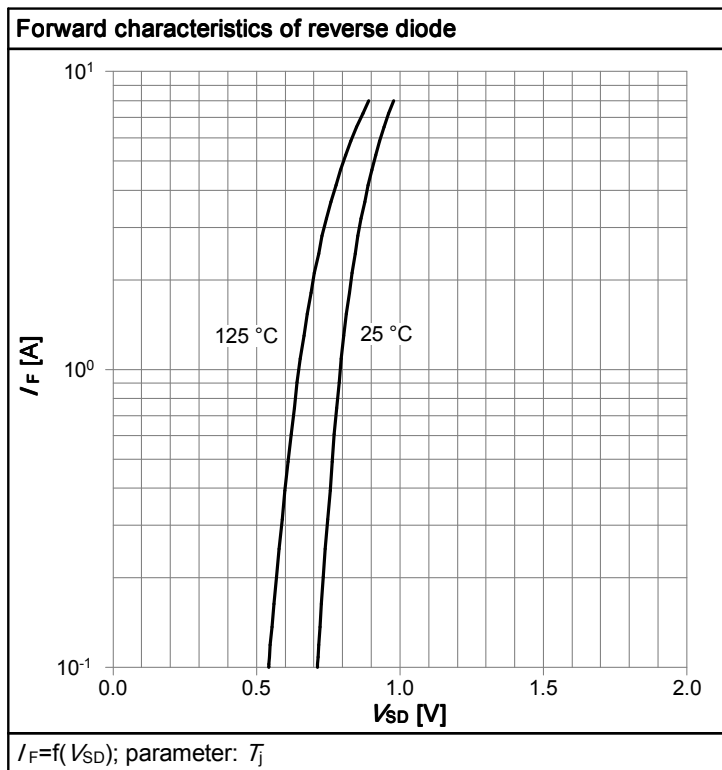


Table 15



6 Test Circuits

Table 16 Diode characteristics

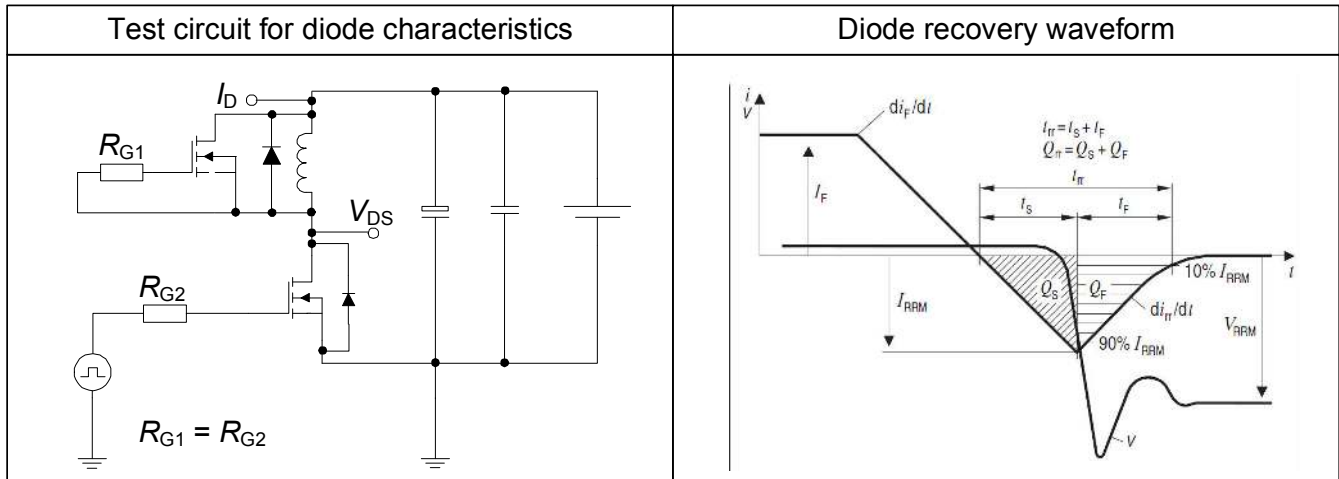


Table 17 Switching times

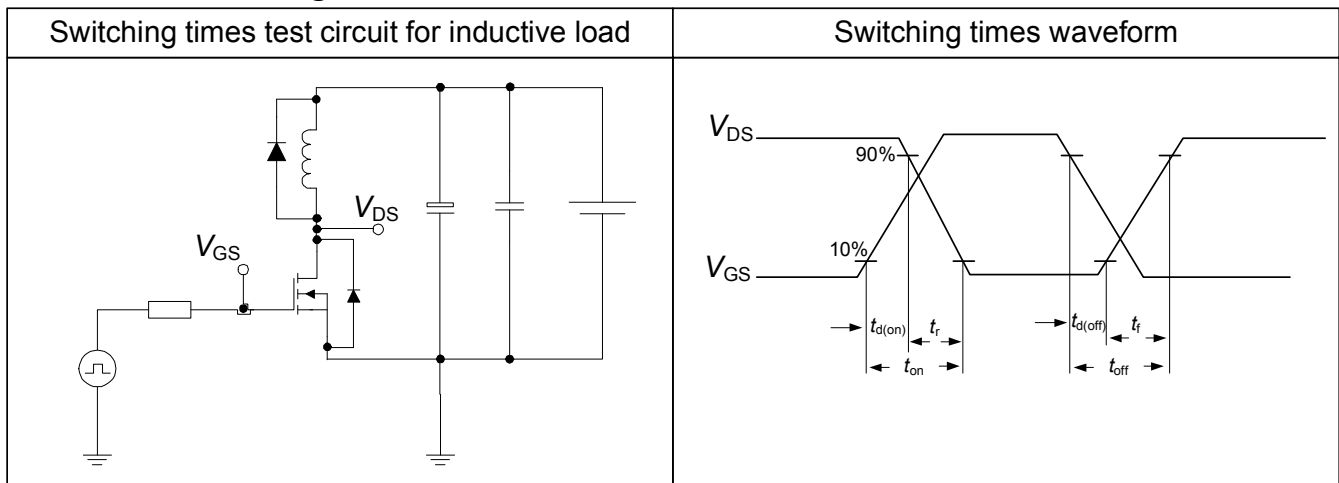
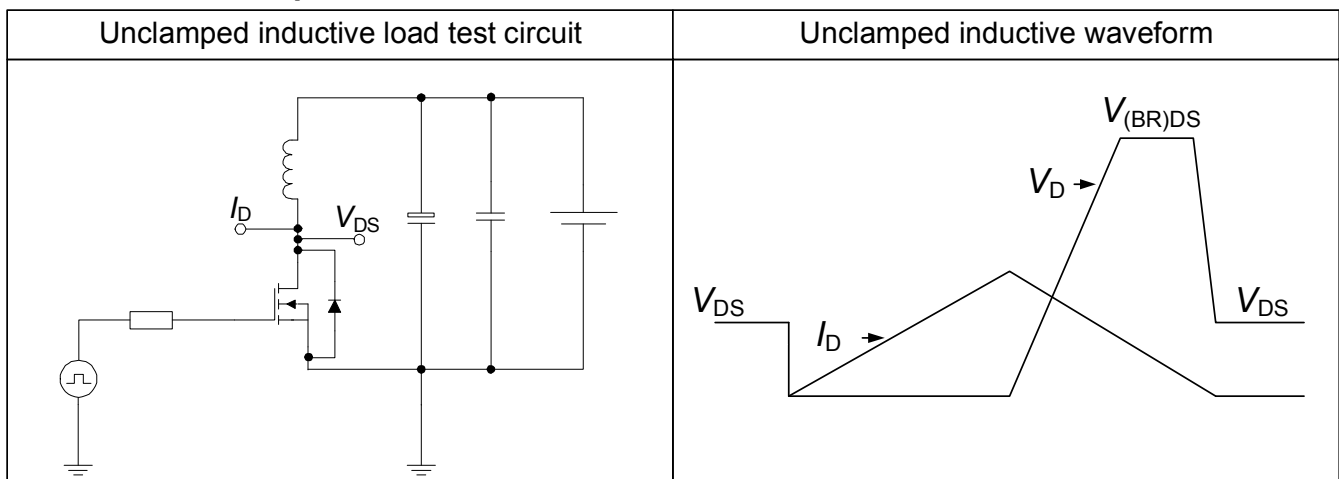
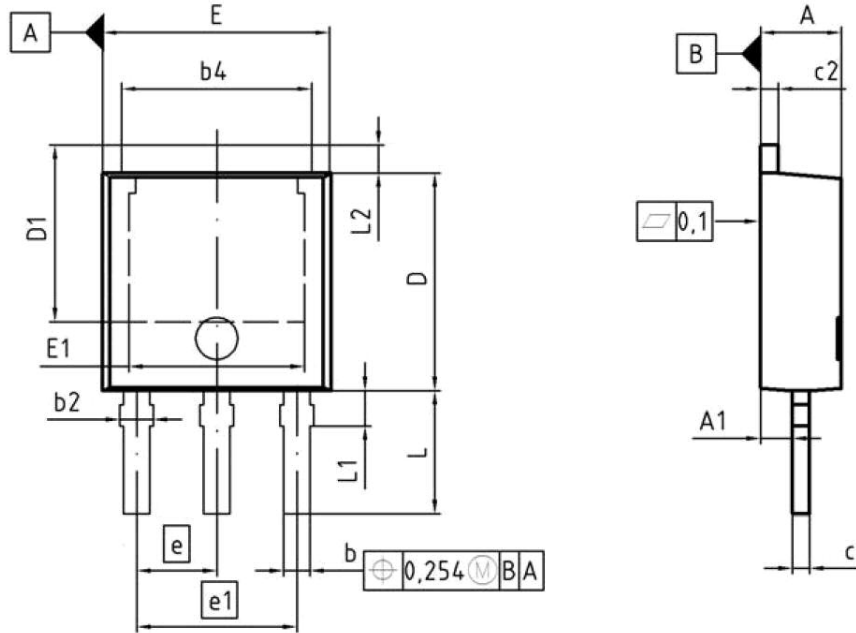


Table 18 Unclamped inductive



7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.58	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.44	0.198	0.214
E	6.35	6.73	0.250	0.265
E1	4.90	5.10	0.193	0.201
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.30	3.50	0.130	0.138
L1	0.90	1.10	0.035	0.043
L2	0.90	1.10	0.035	0.043

DOCUMENT NO.
Z8B00003329

SCALE

EUROPEAN PROJECTION

ISSUE DATE
05-07-2012

REVISION
04

Figure 1 Outline PG-TO 251, dimensions in mm/inches

8 Appendix A

Table 19 Related Links

- **IFX C6 Product Brief:**

<http://www.infineon.com/dgdl/Product+Brief+600V+CoolMOS+C6+.pdf?folderId=db3a3043156fd5730115939eb6b506db&fileId=6891a111111111111111111111111111>

- **IFX C6 Portfolio:**

http://www.infineon.com/cms/en/product/findProductTypeByName.html?q=ip*c6

- **IFX CoolMOS Webpage:**

<http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8>

- **IFX Design Tools:**

<http://www.infineon.com/cms/en/product/promopages/designtools/index.html>

Revision History

IPS65R950C6

Revision: 2012-07-06, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.9	2011-12-19	Release of target datasheet
2.0	2012-07-06	Release of final version

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