LITIX™ Pixel Rear
Multi-channel LED driver

RoHS

AEC Qualified

ISO 26262 compliant

Features

- 16 channel device with integrated and protected output stages, optimized to drive LEDs
- High regulated output current up to 76.5 mA per channel
- Parallel output operation for higher load currents
- 16 independent 6-bit configurable global output current configurations ranging from 5.625 mA to 76.5 mA
- 16 independent 14-bit PWM engines from 100 Hz up to 2 kHz
- Configurable thermal derating
- Configurable LED Open, Short and Single-LED-Short thresholds
- Digital feedback of external two voltage measurements (NTC/PTC)
- Integrated HSLI transceiver, CAN-FD physical-layer compatible up to 2 MBit/s
- Developed according to ISO26262 with process complying to ASIL-B

Potential applications

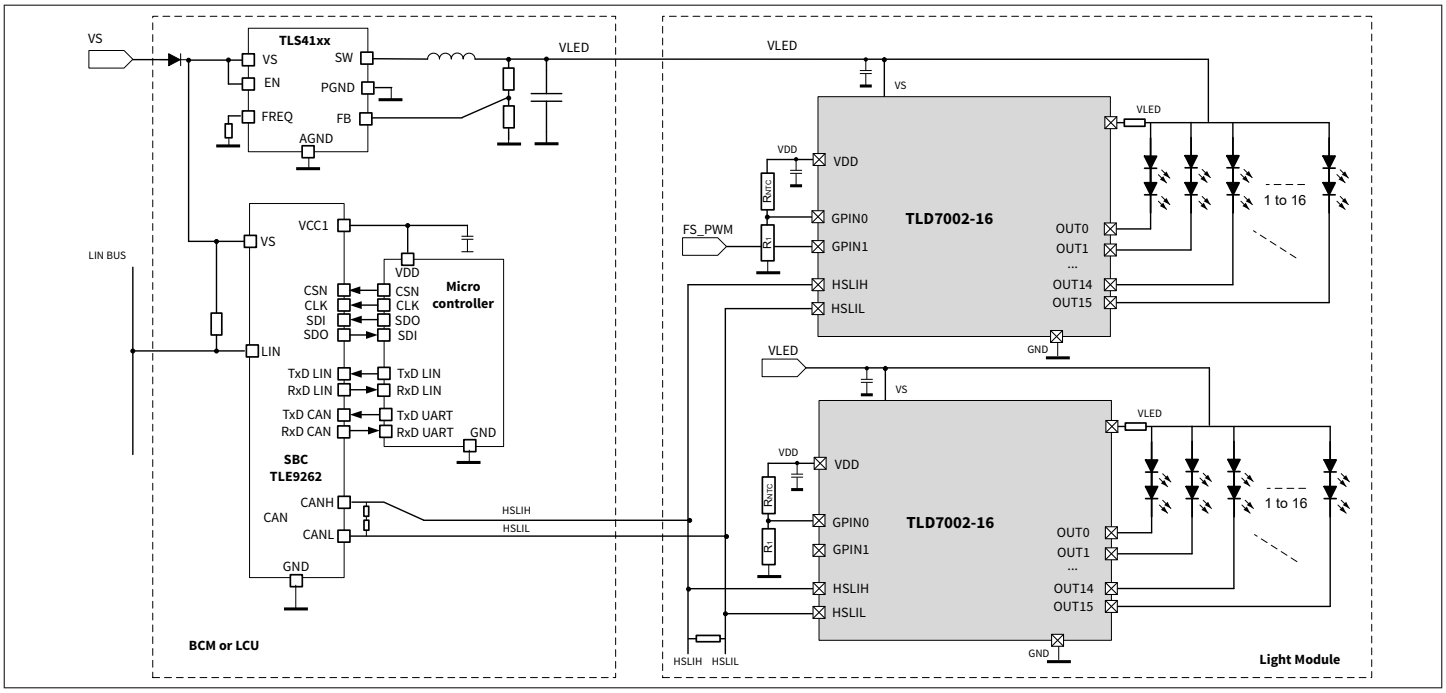
- Open-drain LED driver with high-speed lighting interface (HSLI - UARToverCAN)
- Automotive rear light functions such as tail, stop and sequential (dynamic) turn indicator
- Animated light functions like “welcome/goodbye” functions
- Interior lighting functions for ambient lighting (RGB color control), illumination and dash board lighting
- LED panels for industrial applications and instrumentation

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLD7002-16ES is a 16 channel device with integrated and protected output stages. It is designed to control LEDs with a current up to 76.5 mA as linear current sink (LCS). The power stages can be configured in parallel for higher load currents. Each individual power output stage is configured to a 6-bit current set value stored in the OTP. 16 independent and individual PWM configurations can be set. A high-speed lighting interface is used for device OTP programming, configuration, control and diagnostic feedback.



Parameter	Symbol	Values
Power supply operating voltage	$V_{S(OP)}$	6.0 V ... 20 V
Maximum output voltage	V_{OUT_max}	35 V
Nominal load current (Linear current sink)	I_{L_NOM}	75 mA, V_{LED} = 5 V
Output current accuracy T_J = 25°C	$A_{IOUT,25}$	±5%
Minimum dropout voltage	V_{dr_min}	600 mV at 50 mA

Further features include the following:

- Configurable thermal derating to protect the LED load at high ambient temperature conditions
- Configurable LED Open, Short and Single-LED-Short thresholds for LED fault detection
- Digital feedback of external NTC/PTC temperature measurement and up to two separate LED forward voltage measurements
- High-speed lighting interface for LED control
- Integrated HSLI transceiver, CAN-FD physical-layer compatible and electrical characteristics compliant to ISO11898-2:2016
- Protocol based on UART with baud rate up to 2 MBit/s
- Integrated transceiver with very low electromagnetic emission (EME) allows the use without additional common mode choke
- Developed according to ISO26262 with process complying to ASIL-B
- Optimized for Electromagnetic Compatibility (EMC)
- Optimized for high immunity against Electromagnetic Interference (EMI)
- Green Product (RoHS compliant)
- AEC Qualified

Safety relevant features

- Configurable V_{FWD} monitoring
- Programmable output current monitoring
- PWM duty cycle monitoring
- HSLI bus watchdog
- GPINn PWM warning
- Integrated load diagnostic features for open load, short circuit, single LED short, short between two adjacent strings detection.
- Programmable safe state in case of loss of communication
- Internal over temperature sensor
- Internal clock monitoring
- Individual fault and status flags readable via HSLI
- Configurable fault management and common open-drain output error pin ERRN

Type	Package	Marking
TLD7002-16ES	PG-TSDSO-24	TLD7002-16

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1 Block diagram and terms

1.1 Block diagram

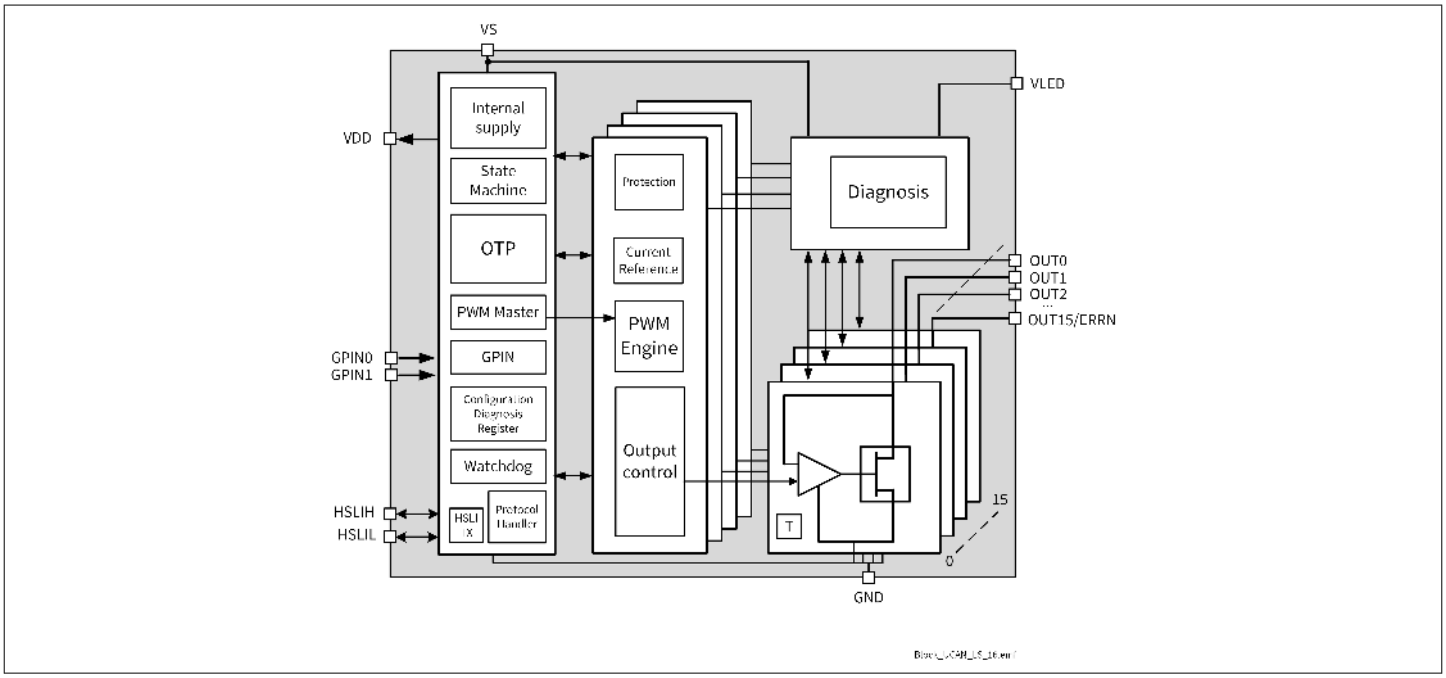


Figure 1 Block diagram of TLD7002-16ES

1.2 Terms

Figure 2 shows all terms used in this datasheet, with associated convention for positive values.

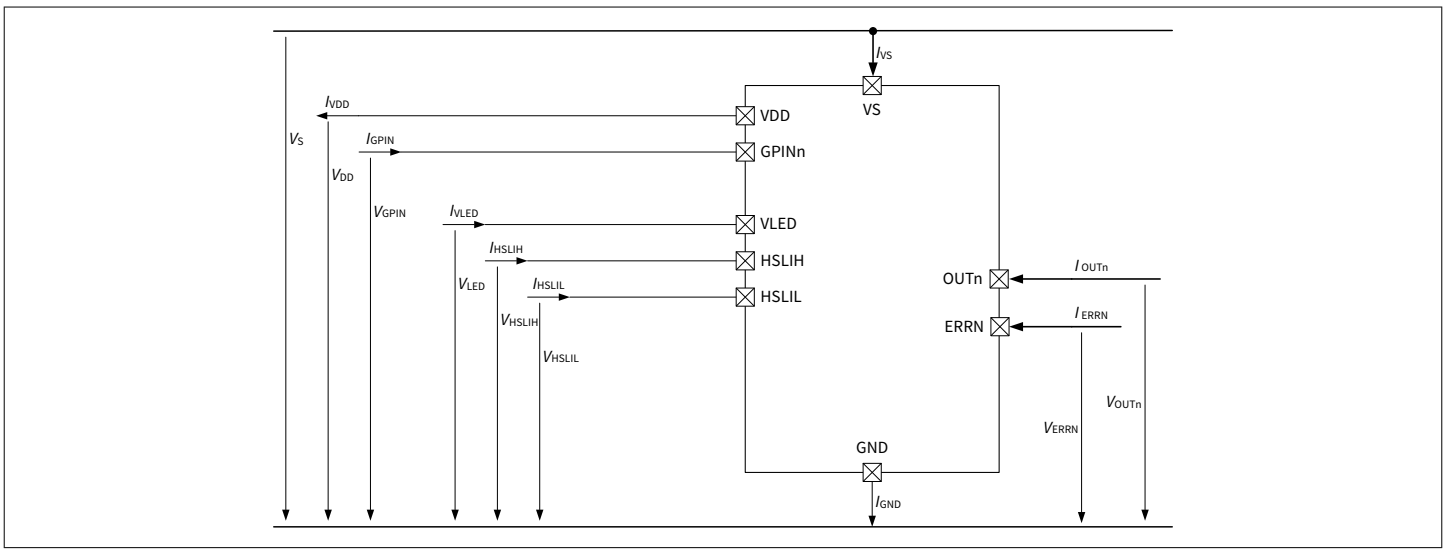


Figure 2 Terms and definitions

OUTn: n denotes the channel number from 0 to 15
GPINn: n denotes the GPIN number from 0 to 1

2 Pin configuration

2.1 Pin configuration

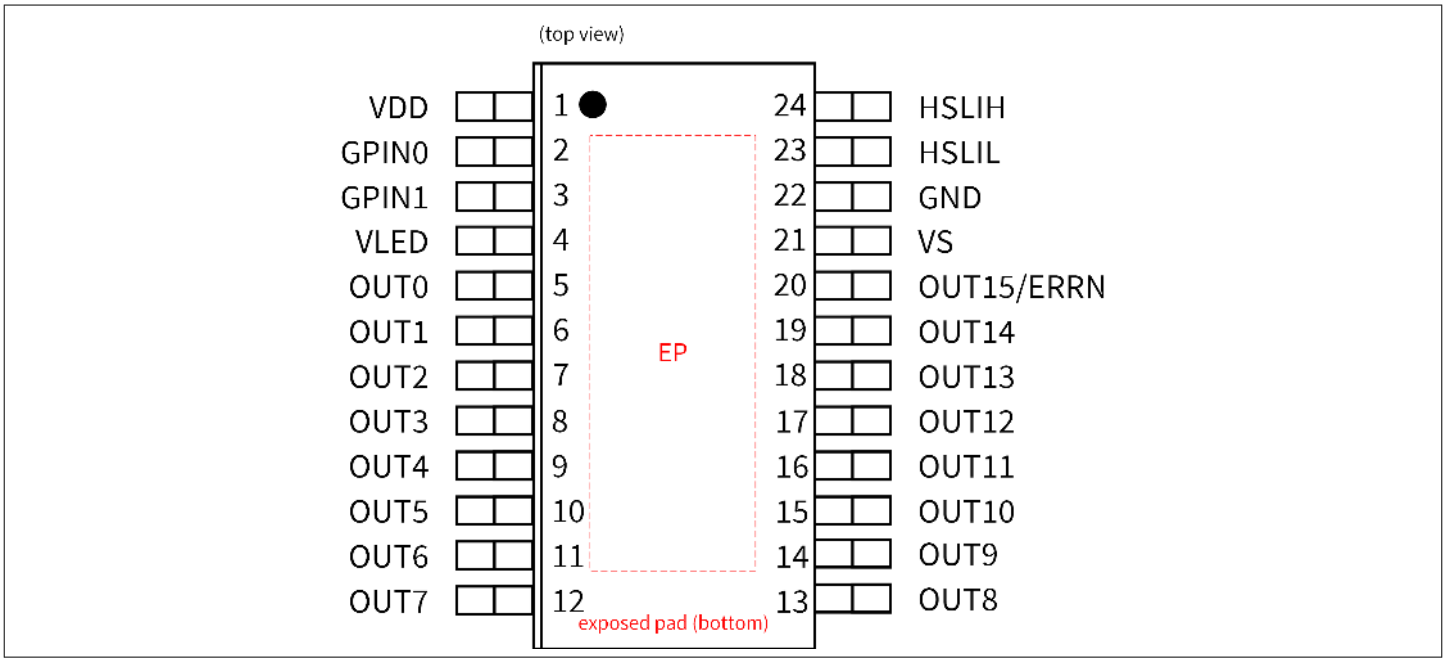


Figure 3 Pin configuration

2.2 Pin description

Table 1 Pin description

Pin	Symbol	Function
21	VS	**Power supply voltage** Supply for internal biasing and can be used for differential forward voltage measurement of the LED load
1	VDD	**Digital GPIN supply voltage output** Can be used as voltage reference for NTC/PTC thermistors and acts as HSLI bus voltage reference, thus as supply for the transceiver
22	GND	**Ground** Ground potential. Connect externally close to the chip
-	EP	**Exposed pad** Connect to external heat spreading Cu area, either electrical GND or floating potential. Recommendation is to use the GND layer of a PCB with thermal vias, The exposed pad is not replacing the electrical GND pin
5...20	OUT0...OUT15	**Output channel** Open drain linear current sink. Connect to the target load
20	ERRN	**ERROR flag I/O** Open drain active low error flag. Connect to a pull-up resistor

(table continues...)

Table 1 (continued) Pin description

Pin	Symbol	Function
2,3	GPIN0, GPIN1	**General purpose input** Can be used for voltage measurement or as function activation input source
4	VLED	**Analog input** Can be used for differential forward voltage measurement of the LED load
24	HSLIH	**High-speed lighting interface high level I/O** “high” in “dominant” state
23	HSLIL	**High-speed lighting interface low level I/O** “low” in “dominant” state

Note: Unused output pins (OUTn) shall be left open with duty cycle set to 0.

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	28	V	–	PRQ-362
Power supply load dump voltage	$V_{S(LD)}$	–	–	35	V	suppressed Load Dump acc. to ISO16750-2 (2010). R_i = 2 Ω	PRQ-686
Digital supply voltage	V_{DD}	-0.3	–	5.5	V	–	PRQ-363
Digital supply current	I_{DD}	0	–	10	mA	Not subject to production test - specified by design	PRQ-364
Output pins							
Power output voltage	V_{OUT}	-0.3	–	35	V	–	PRQ-365
Power output current	I_{OUT}	0	–	85	mA	Not subject to production test - specified by design	PRQ-366
GPIN/VLED pins							
Voltage at pin GPIN0, GPIN1	V_{GPIN}	-0.3	–	VDD	V	–	PRQ-367
Current at pin GPIN0, GPIN1	I_{GPIN}	0	–	2	mA	Not subject to production test - specified by design	PRQ-368
Voltage at pin VLED	V_{LED}	-0.3	–	35	V	–	PRQ-369
HSLI pins							
Voltage at pin HSLIL, HSLIH	V_{HSLI}	-27	–	35	V		PRQ-756
Temperatures							
Junction temperature	T_J	-40	–	150	°C	Not subject to production test - specified by design	PRQ-370

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ESD susceptibility							
ESD susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002; Not subject to production test - specified by design	PRQ-540
ESD susceptibility HSLIH, HSLIL vs GND (HBM)	$V_{ESD(HBM)}$	-8	–	8	kV	ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002; Not subject to production test - specified by design	PRQ-665
ESD susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	ESD susceptibility, Charged Device Model “CDM” according to AEC Q100-011; Not subject to production test - specified by design	PRQ-542
ESD susceptibility corner pins (CDM)	$V_{ESD(CDM)\_CR}$	-750	–	750	V	ESD susceptibility, Charged Device Model “CDM” according to AEC Q100-011; Not subject to production test - specified by design	PRQ-543

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage operating range	V_{SOP}	6	9	20	V	–	PRQ-373
Extended power supply voltage operating range	V_{SOPEXT}	6	9	29	V	t ≤ 1 min with parameter deviations	PRQ-763
Digital supply output voltage	V_{DD}	4.5	5	5.5	V	–	PRQ-372
VS capacitor range	C_{VS}	100	470	–	nF	X7R	PRQ-374
VDD capacitor range	C_{VDD}	4700	–	13000	nF		PRQ-375
VLED capacitor range	C_{VLED}	–	470	–	nF	X7R	PRQ-376
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-377
Output stage							
VLED operating range	$V_{LED(OP)}$	2	9	20	V	–	PRQ-660
Output voltage operating range	$V_{OUT(OP)}$	0.6	–	20	V	–	PRQ-378
Output current per channel	I_{OUT}	0	–	76.5	mA	Code 0x00 = 5.625 mA, Code 0x3F = 76.5 mA; OUT.DC = 0 % results into 0 mA and power stage is off.	PRQ-379
Output capacitor range	C_{OUT}	0	–	100	nF	–	PRQ-380
Output inductance range	L_{OUT}	0	–	2	µH	10 nF < C_{OUT} ≤ 100 nF	PRQ-381
Output inductance range	L_{OUT}	0	–	1	µH	C_{OUT} < 10 nF	PRQ-382

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal resistance junction to top	Ψ_{JTOP}	–	3	5	K/W	Not subject to production test - specified by design.	PRQ-618
Thermal resistance junction to soldering point	R_{thJSP}	–	3	5	K/W	simulated at exposed pad; Not subject to production test - specified by design.	PRQ-619
Thermal resistance junction to ambient	R_{thJA}	–	28	30	K/W	Not subject to production test - specified by design.	PRQ-383

Note: Specified R_{th} values are according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_{AMB} = 85°C with all channels on, $P_{DISSIPATION}$ = 2 W and a homogeneous temperature distribution across the device.

4 Power supply

The device is supplied by VS, which is used for the internal logic and the supply for the power output stages. Moreover, the high-speed lighting bus bias voltage V_{DD} is generated internally from VS and available on the VDD pin. VS has an undervoltage detection circuit, which prevents the activation of the power output stages and diagnosis in case the applied voltage is below the undervoltage threshold.

4.1 Power mode states

The device has the following operation modes:

- Idle (unsupplied and reset)
- Init mode
- Active mode
- OTP mode with substates for programming or emulation
- Fail-safe mode
- Fail-off mode

The state diagram including the possible transitions is shown below. The behavior of the device as well as some parameters may change depending on the operation mode of the device.

The state diagrams are shown in Figure 4 and Figure 5.

Note: ADC readings, and all the diagnostic related to it, are available only in ACTIVE, FAIL-SAFE and OTP modes.

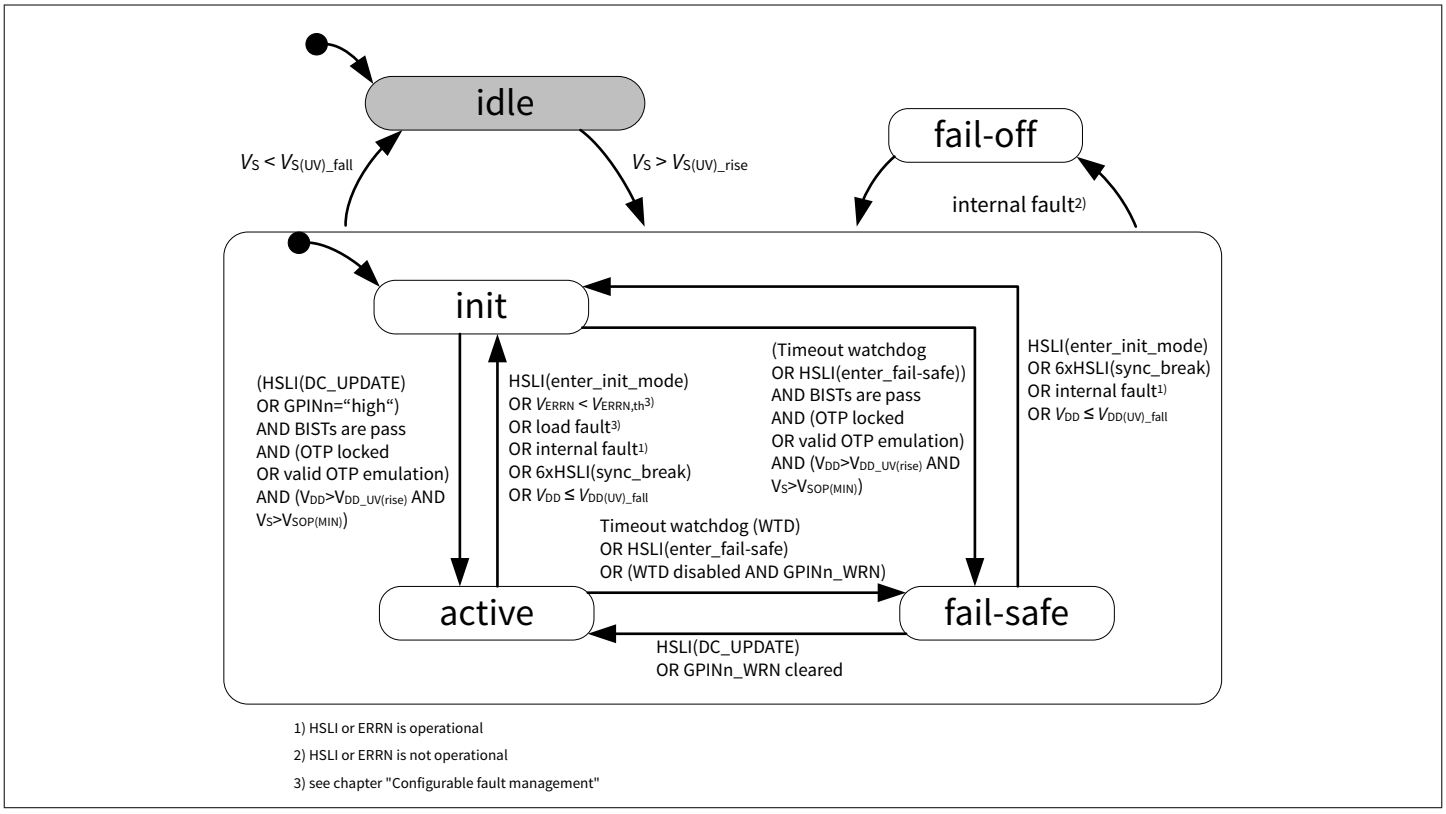


Figure 4 Power supply operation modes

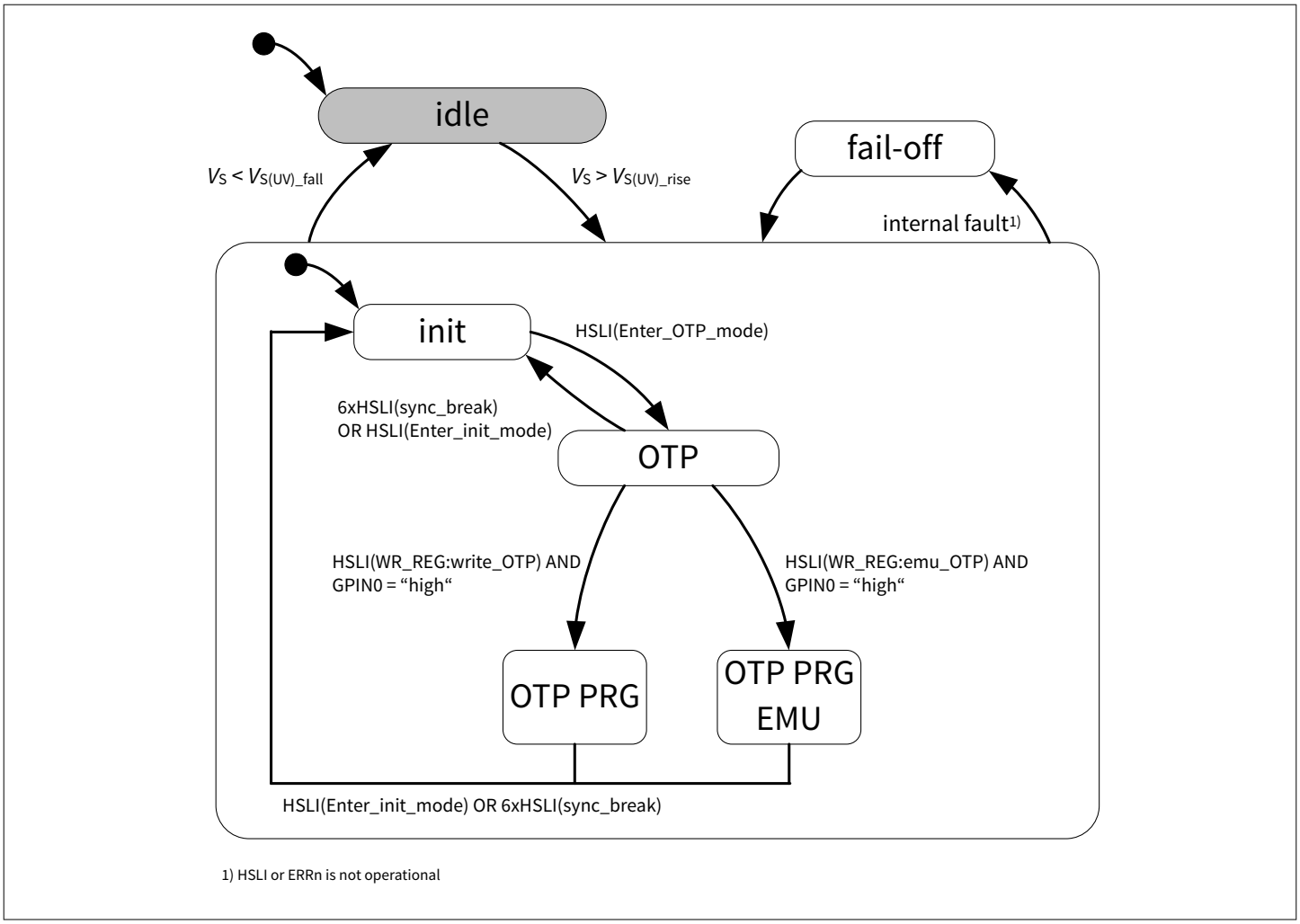


Figure 5 Power supply operation modes for OTP programming and emulation

4.2 Idle mode

In the idle mode

- all output channels are switched OFF and
- the device is reset including configuration and fault registers and
- the HSLIH and HSLIL bus interface pins are floating.

The device enters into Idle mode if the power supply voltage $V_S < V_{S(UV)\_fall}$ OR internal fault via fail-off mode occurred.

4.3 Init mode

The following functions are available in init mode:

- Sending and receiving HSLI frames if $V_{DD} > V_{DD(UV)\_rise}$
- VDD output voltage is available
- BIST safety mechanism are executed
- Power output stages are commanded to off, means the DC = 0%.

The device enters into init mode in $t_{IDLE2INIT}$ if:
$V_S > V_{S(UV)\_rise}$
OR in t_{INIT} if:

the device is in active mode AND
- an internal fault occurred and HSLI or ERRn is operational OR
- $V_{DD} < V_{DD(UV)\_fall}$

OR
PM_CHANGE(enter_init_mode) frame is received via the HSLI bus
OR
6 times sync_break is received via the HSLI bus as described in Chapter 9.1.11.9 to reset the device
OR
the device is in active mode AND a load fault has been detected
OR
the device is in active mode AND ERRN is active when $V_{ERRN} < V_{ERRN,th}$.

4.4 Fail-off mode

In the fail-off mode the device is reset, all output channels are switched OFF and the HSLIH and HSLIL bus interface pins are floating.

The device enters into fail-off mode in t_{FAIL_OFF} in case of an internal fault when HSLI or ERRN is not operational.

4.5 Fail-safe mode

In fail-safe mode each output stage enters the desired safe state either ON or OFF.

The device enters into fail-safe mode in $t_{ACTIVE2FAILSAFE}$
- if the device is in active mode and the timeout watchdog is triggered OR
- if the device is in init mode and the timeout watchdog is triggered OR
- if the device received an PM_CHANGE(enter_fail-safe) via the HSLI bus OR
- if the GPIN warning occurs and the watchdog timeout is disabled.

The device exits the fail-safe mode into init mode in $t_{FAILSAFE2INIT}$ if
- the device received a valid PM_CHANGE(enter_init_mode) frame via the HSLI OR
- a 6 consecutive HSLI sync break frames trigger a device reset.

The device exits the fail-safe mode into active mode in $t_{FAILSAFE2ACTIVE}$ if
- the device received a valid DC_UPDATE frame via the HSLI OR
- GPIN warning cleared via HSLI HWCR frame

The safe state is set on the FAIL-SAFE MODE OTP register.

If the device reaches the fail-safe state, the duty cycle values and the output current of all and only the outputs enabled in fail-safe state will be updated with the content of the OTP registers (OTP failsafe/GPIN0 DC register and OTP ISET register).

4.6 Active mode

The device enters into active mode within $t_{INIT2ACTIVE}$ if:
- the device is in init OR fail-safe mode AND
- BISTs are pass in init mode AND
- OTP is configured and locked OR OTP emulation is valid AND
- the device received a valid DC_UPDATE command via the HSLI bus OR an activation request via GPINn AND
- $V_{DD}>V_{DD\_UV(rise)}$ AND $V_S>V_{SOP(MIN)}$

Valid commands means no CRC-3 for master request, CRC-8 error and no frame structure error occurred.

4.7 OTP mode

In this mode the LCU can program or emulate the OTP configuration.

Following functions are available in OTP mode:
- Sending and receiving HSLI frames if $V_{DD} > V_{DD(UV)\_rise}$
- VDD output voltage is available
- internal fault monitoring

The device enters into OTP mode in $t_{INIT2OTP}$ if:
- the device is in init mode AND
- the device received a valid enter_OTP_mode frame via the HSLI bus

4.8 OTP programming mode

The following functions are available in OTP programming mode:
- sending and receiving HSLI frames if $V_{DD} > V_{DD(UV)\_rise}$
- VDD output voltage is available
- internal fault monitoring

The device enters into OTP programming mode in $t_{OTP2PRG}$ if:
- the device is in OTP mode AND
- the device received a WRITE_REG(write_OTP) via the HSLI bus AND
- GPIN0 is set to “high”.

In this programing mode the LCU can program the OTP configuration register and store them permanently in the OTP. In order to program the OTP, supply voltage on VS pin must remain within the VS_PROG voltage range during the entire programming procedure. The OTP is locked and secured if the LCU successfully writes all the OTP registers and the correct CRC protection word.

Note: In case GPIN0=LOW and a valid passphrase is sent, the device remains in OTP mode. A HSLI power mode change frame is required to move the device to init mode.

4.9 OTP programming emulation mode

The following functions are available in OTP programming emulation mode:
- sending and receiving HSLI frames if $V_{DD} > V_{DD(UV)\_rise}$
- VDD output voltage is available
- internal fault monitoring

The device enters into OTP programming emulation mode in $t_{OTP2PRG}$ if:
- the device is in OTP mode AND
- the device received a WRITE_REG(emu_OTP) via the HSLI bus AND
- GPIN0 is set as digital input and a “high” voltage level applied.

In this emulation mode the LCU can program a volatile copy of the OTP.

This volatile copy is not stored in the OTP. The device generates a CRC protection word for the volatile copy of the OTP and this is compared to the CRC protection word received from the LCU. The OTP volatile copy is used until the next power-up sequence in case the LCU CRC protection word matches to the OTP emulation checksum.

Note: In case GPIN0=LOW and a valid passphrase is sent, the device remains in OTP mode. A HSLI power mode change frame is required to move the device to init mode.

4.10 Electrical characteristics power supply

Table 5 Electrical characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply							
Power supply undervoltage shutdown rising edge	$V_{S(UV)\_rise}$	2.8	3.75	4.5	V	–	PRQ-387
Power supply undervoltage shutdown falling edge	$V_{S(UV)\_fall}$	1.85	2.5	2.9	V	–	PRQ-388
Power supply current consumption in init mode	$I_{VS(INIT)}$	–	–	8	mA	no bus communication; no load on VDD; init mode; LP_INIT='0'; ERRN disabled	PRQ-667
Power supply current consumption in init mode LP_INIT	$I_{VS(INIT)}$	-	3.2	3.5	mA	no bus communication; no load on VDD; init mode; LP_INIT='1'; V_S > 8 V; f_{PWM} configured to 300 Hz; GPIN0 configured as analog input; GPIN1 configured as digital input; $T_J \leq 85°C$; ERRN disabled; Not subject to production test - specified by design	PRQ-879

(table continues...)

Table 5 (continued) Electrical characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply current consumption in active mode	$I_{VS(ACTIVE)}$	–	15	20	mA	no bus communication; all output channels ON; active mode; no load on VDD	PRQ-389
Power supply current consumption in active mode with communication	$I_{VS(ACTIVE)}$	-	-	30	mA	active mode, HSLI communication, DC_UPDATE and DC_SYNC frame sent with 100 fps at 1 Mbit/s, all output channels on; no load on VDD; Not subject to production test - specified by design	PRQ-691
Power supply current consumption in programming modes	$I_{VS(PRG)}$	–	40	70	mA	OTP programming mode; OTP programming emulation mode; no load on VDD;	PRQ-390
Power supply current consumption in fail-safe mode	$I_{VS(Failsafe)}$	–	15	20	mA	no bus communication; Fail-safe mode; no load on VDD	PRQ-392
Internal voltage regulator and oscillator							
VDD output voltage	V_{VDD}	4.9	5	5.1	V	no communication; $0 < I_{VDD} \leq 10$ mA; init mode; active mode; fail-safe mode; OTP mode; OTP programming mode; OTP programming emulation mode;	PRQ-393

(table continues...)

Table 5 (continued) Electrical characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VDD undervoltage shutdown falling edge	$V_{DD(UV)\_fall}$	3.8	4.25	4.5	V	–	PRQ-693
VDD undervoltage shutdown rising edge	$V_{DD(UV)\_rising}$	4.5	4.75	4.9	V		PRQ-730
Absolute oscillator frequency accuracy	af_{OSC}	-1	-	1	%	-20°C ≤ T_J < 125°C, not subject to production test; $a_{fOSC} = f_{OSCmax}$-f_{OSCmin}/ $f_{OSCaverage}$	PRQ-726
Timings							
Idle to Init delay	$t_{IDLE2INIT}$	-	-	5	ms	C_{VDD} ≤ 4.7 µF	PRQ-668
Init to Active delay	$t_{INIT2ACTIVE}$	–	–	250	µs	GPIN is processed after HSLI communication is finished; Not subject to production test - specified by design	PRQ-394
Init mode delay	t_{INIT}	-	-	250 + 2 (1/f_{PWM})	µs	Not subject to production test - specified by design	PRQ-694
Fail-off mode delay	t_{fail_off}	–	–	250	µs	Not subject to production test - specified by design	PRQ-765
Init to OTP delay	$t_{INIT2OTP}$	-	-	1	ms	Not subject to production test - specified by design	PRQ-728
OTP to programming delay	$t_{OTP2PRG}$	–	–	1	ms	transition to OTP programming mode; transition to OTP programming emulation mode; Not subject to production test - specified by design	PRQ-395

(table continues...)

Table 5 (continued) Electrical characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Active to fail-safe delay	$t_{ACTVE2FAILSAFE}$	–	–	4	ms	I_{OUT} ≥ 90% of desired output current after watchdog timeout triggered; f_{PWM} ≥ 300 Hz; Not subject to production test - specified by design	PRQ-397
Fail-safe to init delay	$t_{FAILSAFE2INIT}$	–	–	250 + 2 ($1/f_{PWM}$)	µs	Not subject to production test - specified by design	PRQ-398
Fail-safe to active delay	$t_{FAILSAFE2ACTIVE}$	–	–	250	µs	Not subject to production test - specified by design	PRQ-855

5 General Purpose Input (GPI)

5.1 Overview and features

The device provides two general purpose input pins GPIN0 and GPIN1. The GPINs can be used as

- digital input for direct drive feature to operate the device without the HSLI interface
- analog inputs connected to the internal ADC multiplexer for external NTC/PTC measurements

Accepted input signals for the direct drive feature can be either static voltage level or PWM decoded duty cycle

5.2 Digital Input

The GPINn pins integrate an internal pull-down function when set as digital input, where the pull-down current is defined by I_{PD}.

The digital input is set by default on GPIN0 and disabled on GPIN1. If the GPINn is used as analog input, the pull-down current is disabled as described in Chapter 5.5.

If GPINn is set as digital input it can be used to move the device in active mode. This is valid also if no outputs are mapped to GPINn. An activation request is either a static input high voltage level (Vih) or a PWM input high duty cycle (dc_hi) with GPINn set as digital input.

5.3 Direct drive

The direct drive function can be used to operate the device without the HSLI interface. A valid PWM signal on GPIN overwrites the HSLI request. One or both inputs drive one to all power output channels defined with a GPINn to OUTn mapping stored in the OTP.

GPIN0OUTn MAP - Group0	GPIN1OUTn MAP - Group1
0b aaaa aaaa aaaa aaaa	0b bbbb bbbb bbbb bbbb

Definition for a,b

"0" ... input is not mapped to the corresponding power output stage

"1" ... input is mapped to the corresponding power output stage

Each GPIN is mapped to one set of 16 duty cycle configuration with a resolution of 8-bit. The configuration is stored in the OTP. The GPIN0 duty cycle configuration shares the fail-safe duty cycle configuration.

In case two GPINs are mapped to the same OUTn both GPINs demands are combined by a logical OR.

A GPIN1 ON demand has higher priority than a GPIN0 ON demand to resolve the duty cycle configuration conflict.

Application example:

GPIN1 is used to active a stop light function, where OUTn is configured to 100% duty cycle

GPIN0 is used to active a tail light function, where OUTn is configured to 6% duty cycle

Table 6 Application example

GPIN0 (tail light)	GPIN1 (stop light)	Output duty cycle
Low	Low	0%
Low	High	100%
High	Low	6%

(table continues...)

Table 6 (continued) Application example

GPIN0 (tail light)	GPIN1 (stop light)	Output duty cycle
High	High	100%

The device resolves duty cycle request conflicts between GPIN activation and HSLI activation according to following table:

Table 7 GPIN priority configuration

Output mapped to GPIN	GPIN	GPINn_WRN	HSLI_WDT	Priority configuration
no	–	–	not triggered	HSLI
no	–	–	triggered	Fail-safe (OTP)
no	–	–	disabled	HSLI
yes	static low	–	not triggered	HSLI
yes	static low	–	triggered	Fail-safe (OTP)
yes	static low	–	disabled	GPIN, output OFF
yes	static high	–	–	GPIN, output ON
yes	PWM low	no	not triggered	HSLI
yes	PWM low	no	triggered	Fail-safe (OTP)
yes	PWM low	no	disabled	GPIN, output OFF
yes	PWM high	no	–	GPIN, output ON
yes	PWM low/high	yes	not triggered	HSLI
yes	PWM low/high	yes	triggered	Fail-safe (OTP)
yes	PWM low/high	yes	disabled	Fail-safe (OTP)

Note: *In case of a transition from GPIN control back to HSLI control a DC_SYNC frame is needed to synchronize to the last configured duty cycle.*

5.4 Output enable

The GPIN0 enables or disables all power output stages if the ouput enable (OE) feature is configured via the OTP.
The output power stages are enabled if the GPIN0="high", disabled if the GPIN0="low".

A "high" state is when VGPIN0 ≥ V_{IH} OR as in case of a PWM encoding as described in Chapter 5.6.
A "low" state is when VGPIN0 ≤ V_{IL} OR as in case of a PWM encoding as described in Chapter 5.6.
The output enable function is not effective for

- OUT15, when used as ERRn
- OUT0, when used as DCDC feedback channel.

5.5 Analog input

The GPINs can be configured with the OTP as analog input pins for external voltage measurements, (e.g. for external NTC/PTC temperature measurements).
The pull-down function is disabled in case the GPINn is configured as analog input pin.

The GPIN ADC measurement is described in Chapter 7.3.

5.6 GPIN PWM decoding

The GPINs can decode an input PWM signal with a frequency of f_{PWM_GPINn} where

- a duty cycle dc_{LO} is detected as OFF activation OR
- a duty cycle dc_{HI} is detected as ON activation OR
- a duty cycle outbound of dc_{LO} OR dc_{HI} is detected as fault and reported via the HSLI interface or ERRn.

The GPIN decoding can be enabled or disabled via the OTP configuration for each GPINn.

In case of active mode the GPIN warning flag (GPINn_WRN) is reported via the HSLI output status byte OR activating ERRN with a PWM.DC = 100%.
In case of fail-safe mode the fault state is reported by activating ERRN with a PWM.DC = 100%.
A GPIN warning on ERRN is reported, when fault management configuration is set to "0" - no state change.

Note: The device interprets an immediate warning recovery as OFF activation. At least two GPIN PWM periods are required to detect an ON activation after a GPIN warning.
The GPIN_WRN flag is cleared with an explicit HWCR frame from LCU.

Note: If both GPINs are used for direct control and GPIN decoding enabled a phase shift between 10 µs and 1/fPWM and same frequency are required.
If the phase shift constraint is not granted, a GPIN short (GPIN_SHORT) is detected by the device and reported in the output status byte FAULT bit.

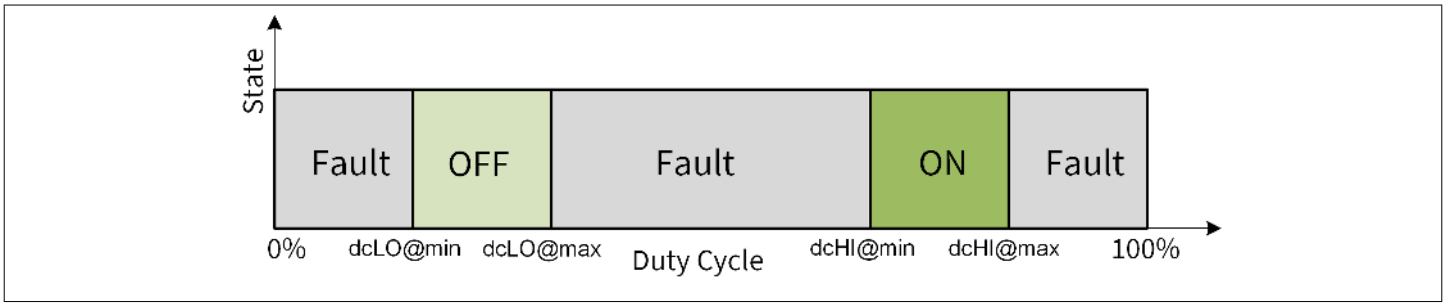


Figure 6 GPIN PWM decoding scheme

5.7 Electrical characteristics

Table 8 Electrical characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GPINn							
Input low voltage	V_{IL}	0	–	0.8	V	–	PRQ-407
Input high voltage	V_{IH}	2.0	–	5.5	V	Internally clamped to 5.5 V if the input current is ≤ I_{GPINn}	PRQ-408

(table continues...)

Table 8 (continued) Electrical characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Analog input voltage range	V_{AIN}	0	–	VDD+0.3	V	–	PRQ-409
Input pull-down current	I_{PD}	3	10	25	µA	V_{GPIN} = 5 V	PRQ-411
Input leakage current	I_{IL}	-10	–	10	µA	V_{GPIN} = 5 V; configured as analog input	PRQ-412
PWM decoding							
GPINn PWM decode frequency	f_{PWM_GPINn}	25.5	–	2000	Hz	Not subject to production test - specified by design	PRQ-670
Input low duty cycle	dc_{LO}	12.5	25	37.5	%	Not subject to production test - specified by design	PRQ-671
Input high duty cycle	dc_{HI}	62.5	75	87.5	%	Not subject to production test - specified by design	PRQ-672

6 Power Stage

6.1 Features

- 16 output power stages
- one master PWM frequency ranging from 100 Hz to 2 kHz for LED dimming
- 16 individual configurable edge-aligned PWM engines with 14-bit duty cycle resolution
- one configurable 5-bit phase shift function for improved EME and supply stabilization
- parallel output operation
- integrated thermal overload protection
- thermal protection by derating of the output current
- 16 independent 6-bit configurable global output current configuration ranging from 5.625 mA to 76.5 mA

6.2 Current sink operation

The output stage sinks an individual configurable 6-bit output current I_{OUT} where the desired output current is configurable via the OTP or via HSLI in runtime.

The following table is related to the configurable output current configurations:

Table 9 Output current configurations

I_{OUT} step	I_{OUT} [mA]	I_{OUT} step	I_{OUT} [mA]	I_{OUT} step	I_{OUT} [mA]	I_{OUT} step	I_{OUT} [mA]
0	5.625	16	23.625	32	41.625	48	59.625
1	6.75	17	24.75	33	42.75	49	60.75
2	7.875	18	25.875	34	43.875	50	61.875
3	9	19	27	35	45	51	63
4	10.125	20	28.125	36	46.125	52	64.125
5	11.25	21	29.25	37	47.25	53	65.25
6	12.375	22	30.375	38	48.375	54	66.375
7	13.5	23	31.5	39	49.5	55	67.5
8	14.625	24	32.625	40	50.625	56	68.625
9	15.75	25	33.75	41	51.75	57	69.75
10	16.875	26	34.875	42	52.875	58	70.875
11	18	27	36	43	54	59	72
12	19.125	28	37.125	44	55.125	60	73.125
13	20.25	29	38.25	45	56.25	61	74.25
14	21.375	30	39.375	46	57.375	62	75.375
15	22.5	31	40.5	47	58.5	63	76.5

6.3 HSLI configurable output current

The 6-bit output current I_{OUT} can be configured also runtime via the HSLI in init mode, OTP programming emulation mode and active mode.

6.4 PWM Generator

6.4.1 PWM function

The device operates each power output stage with a PWM function containing

- one configurable duty cycle per channel
- one global PWM frequency and
- one global PWM phase shift

The device sinks current on HSLI request or GPIN request on each output channel in ≤tON time.

This delay depends on the PWM frequency and on the phase shift according to the following approximate formula:

$t_{ON}=1/f_{PWM}+n*t_{PHS}$

6.4.2 PWM frequency

The PWM engine operates with one master PWM frequency setting f_{PWM} stored in the OTP. The configuration steps should cover multiples of 50 Hz and 60 Hz in the range from 100 Hz to 2 kHz according to following table:

Table 10 Configuration example

Step	Frequency [Hz]	Step	Frequency [Hz]
0	99.90	8	662.08
1	200.32	9	723.38
2	239.65	10	781.25
3	300.48	11	899.50
4	359.78	12	1199.00
5	399.89	13	1502.40
6	539.03	14	1799.00
7	600.96	15	1997.00

6.4.3 PWM duty cycle

The PWM engine provides 16 individual configurable edge-aligned PWM duty cycle settings configurable

- via the OTP in fail-safe mode OR
- the HSLI interface in active mode
- GPINn direct control as described in Chapter 5.3

The updated duty cycle values are applied to the power stages synchronous to the internal PWM period. e.g. the power output duty cycle change is seen latest after one PWM period ($1/f_{PWM}$) independently if the change was triggered by the HSLI, fail-safe mode or GPINn control.

6.4.4 PWM duty cycle configuration - linear or power-law relation

The duty cycle setting can be configured as

- non-linear 8-bit duty cycle configuration by using the DC_UPDATE frame and DLC=0x4, which is related to the 8-bit configuration with a power law relation to the 14-bit resolution OR
- linear 14-bit duty cycle configuration by using the DC_UPDATE frame and DLC=0x6.

The applied power law is defined as:

DC_14bit = 16383 * (DC_8bit/255)$^{1/gamma}$, where gamma is set to 0.4545 and the result is round up away from 0. The graphical representation is shown in Figure 7.

DC_14bit ... duty cycle in 14-bit representation

DC_8bit ... duty cycle in 8-bit representation

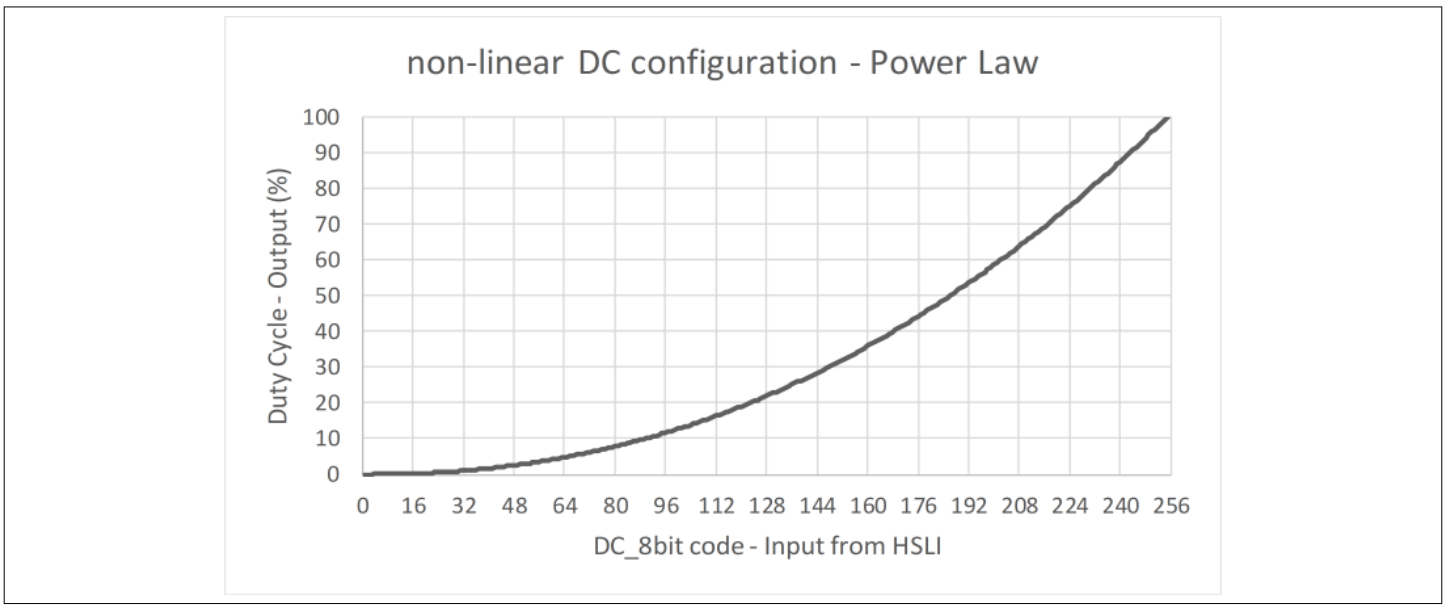


Figure 7 Power law - 8-bit to 14-bit

6.4.5 PWM phase shift

The PWM generator provides one global 5-bit PWM phase shift configuration stored in the OTP.

The phase shift can be enabled or disabled for each power output stage via the OTP.

In case the phase shift is enabled, OUT_n turns on with a delay of t_{PHS}=n * n_{PSH}*1/f_{PWM}, where n=0 to 15.

In case the phase shift is disabled, OUT_n turns on simultaneously with OUT_{n-1}. Both cases are shown in following Figure 8.

The 5-bit phase-shift configuration is related to the 14-bit duty cycle reference from bits 9:5 as shown in table below. This results into a phase shift range of n_{PSH} referred to the PWM period.

Table 11 Duty cycle to phase shift bit weight relation

bit	Duty cycle (14-bit)	Phase shift (5-bit)	bit	Duty cycle (14-bit)	Phase shift (5-bit)
13	x		06	x	x
12	x		05	x	x
11	x		04	x	
10	x		03	x	
09	x	x	02	x	
08	x	x	01	x	
07	x	x	00	x	

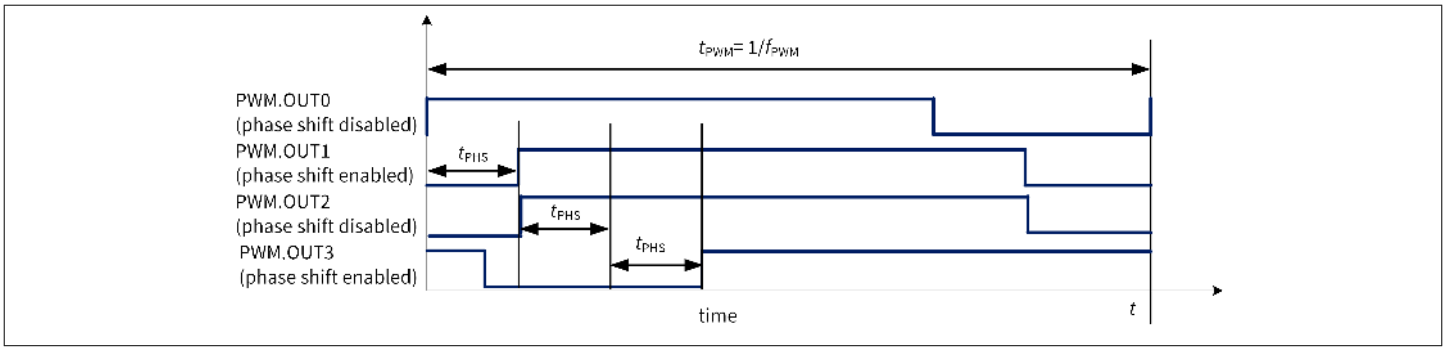


Figure 8 Timing diagram and parameter for PWM pulse

6.5 Power shift

The device can limit the internal power dissipation by balancing one load current branch with two power stages and an external resistance.

The primary output channel OUTn and secondary output channel OUTn+1 provide the output current $I_{OUT} = I_{OUTn} + I_{OUTn+1}$, where I_{OUTn+1} linearly increases until V_{OUTPS_HI} threshold is reached. If $V_{OUTn} > V_{OUTPS\_HI}$ then $I_{OUT} = I_{OUTn+1}$ - 5.625 mA and I_{OUTn} = 5.625 mA. The sum of I_{OUTn} and I_{OUTn+1} remains constant while V_{OUTn} rises.

The external resistance is connected to the secondary output channel.

The primary and secondary output channels are defined according to following table:

Table 12 Primary and secondary output channels

Primary	Secondary
OUT0	OUT1
OUT2	OUT3
OUT8	OUT9
OUT10	OUT11

The power shift threshold V_{OUTPS_HI} is programmable by a 2-bit OTP register with 4 options as shown below with an accuracy of a a_{VOUT_PS} per configuration step.

Table 13 V_{OUTPS_HI} configuration steps

Configuration step	V_{OUTPS_HI}
0	2 V
1	3 V
2	6 V
3	10 V

The power shift needs to be enabled via the OTP configuration.

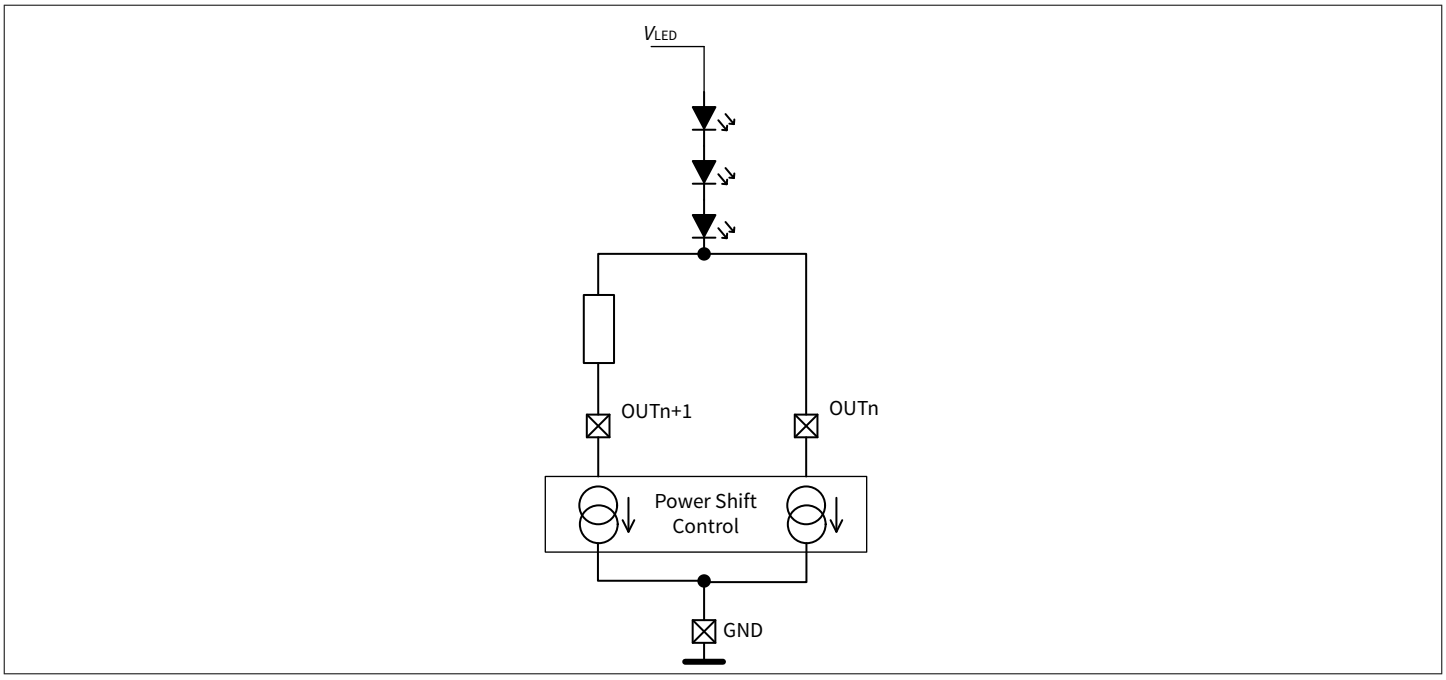


Figure 9 Power shift principle

In case the thermal derating feature is enabled, the power shift feature is not available.

The target output current, which is the sum of the primary and the secondary channels, shall be set in the primary channel OTP current register.

The secondary channel OTP current register shall be set to the minimum value.

6.6 Parallel output configuration

Up to all output stages can be used in parallel to achieve a higher output current without any dedicated configuration needs.

6.7 Thermal overload

The output stage integrates an individual thermal overload protection.

The output stage turns off if the junction temperature exceeds $T_{J(ABS)}$ with a hysteresis of $T_{HYS(ABS)}$ and reports the thermal overload event in a fault register.

The LCU can poll the OVLD flag in the output status byte or by reading the channel status byte OUTn with the READ_OST command. The OVLD flag is cleared after the fault has been acknowledged with an explicit HWCR frame from the LCU.

6.8 Thermal derating

6.8.1 Thermal derating with integrated temperature sensor

The output stage provides a configurable thermal derating (thermal foldback) of the output current based on the integrated device temperature measurement. Each output stage starts to decrease the current linearly when $T_J \geq T_{Jstart}$ until T_{Jstop} is reached, where

$$I_{OUTDER} = \quad I_{OUT} - (T_J - T_{Jstart}) \times k_{DER} \tag{1}$$

$$k_{DER} = \frac{(I_{OUT} - 5.625mA)}{T_{JDER}} \quad (2)$$

$TJ_{start} = T_{Jstop} - TJ_{DER}$, where TJ_{DER} is configured globally and is stored in the OTP.

TJ_{DER} is programmable by a 3-bit register with 5 options as shown below with an accuracy of a_{TJDER} for each step:

Table 14 Thermal derating configuration

TJ_{DER} step	TJ_{DER} temperature
0	20°C
1	30°C
2	40°C
3	50°C
4	60°C

The thermal derating function can be enabled or disabled via the OTP configuration.
In case the thermal derating feature is enable, the power shift feature is not available.

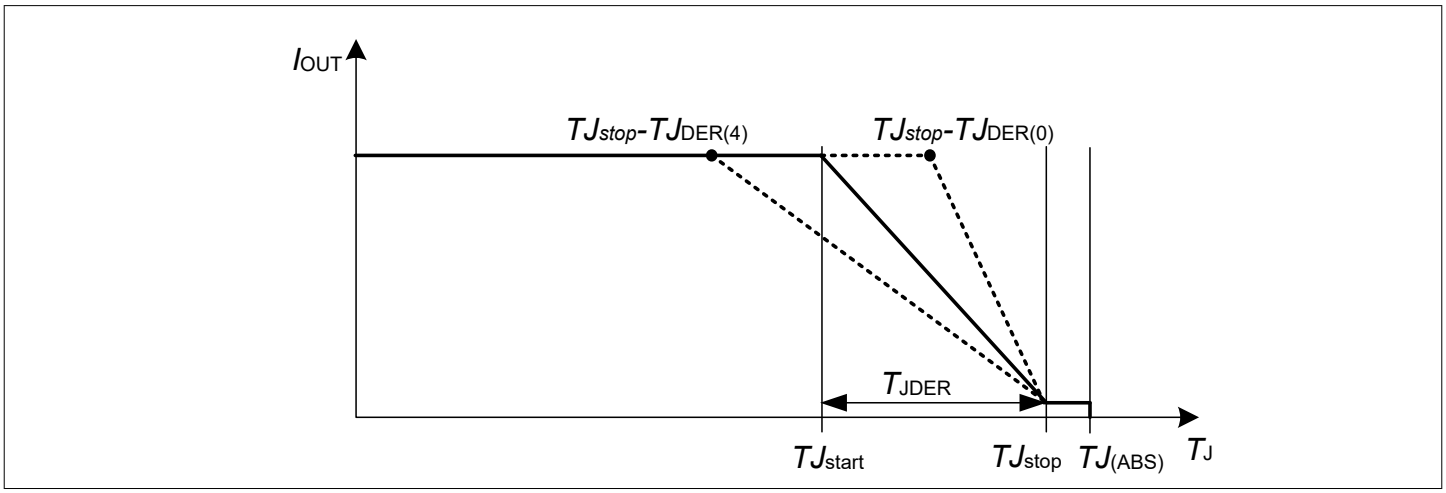


Figure 10 Thermal derating

Thermal derating it is an integrated protection feature intended to avoid a light off condition at high junction temperature.
The output current is reduced applying discrete current steps, with magnitude depending on the thermal derating configuration.
Optical performance and perceived light variation during derating has to be tested in the final application.
The device provide the value of the internal temperature sensor in the DTS status register.
The sensor is not reading the peak junction temperature but an average die temperature.

6.8.2 Thermal derating with GPIN0

The output stage provides a configurable derating of the output current based on the voltage on GPIN0. Each output stage starts to decrease the current linearly when $V_{GPIN0} \geq V_{DER\_start}$ until V_{DER_stop} is reached, where

$$I_{\mathrm{OUTDER}} = I_{\mathrm{OUT}} - (V_{\mathrm{GPIN0}} - V_{DER\_START}) \times k_{\mathrm{DER}}$$
$$k_{\mathrm{DER}} = (I_{\mathrm{OUT}} - 5.625 \quad \mathrm{mA}) / (V_{\mathrm{DER\_STOP}} / V_{DER\_START}) \quad (3)$$

$V_{\mathrm{DER\_start}}$ and $V_{\mathrm{DER\_stop}}$ are configured globally and stored in the OTP.

The GPIN0 derating function can be enabled or disabled via the OTP configuration.
In case the GPIN0 derating feature is enable, the power shift feature is not available.

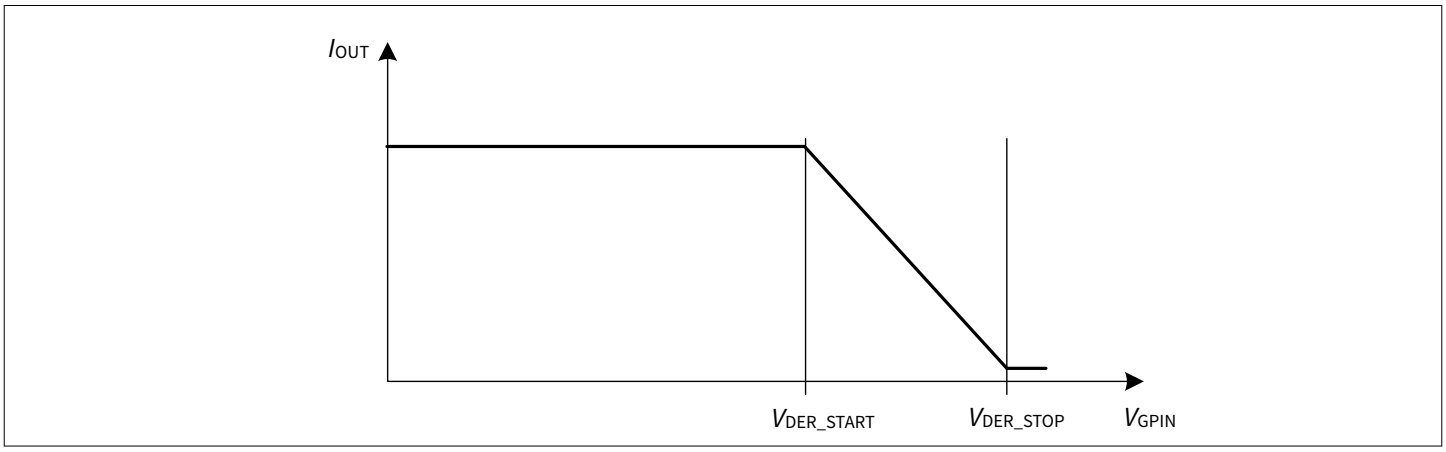


Figure 11 GPIN0 output current derating feature

6.9 Thermal overload retry strategy

The output stage contains a configurable retry strategy for the thermal overload fault event. The retry strategy consists of two options, 1) latch off and 2) retry mode.

1. Latch OFF(default configuration): The output stage remains off after a thermal overload event. The output stage remains off until HWCR.RESET_OVERLOAD is applied AND T_J is lower than $T_{J(ABS)}$ - $T_{HYS(ABS)}$.
2. Retry Mode: The output stage turns on after a thermal overload event if T_J is lower than $T_{J(ABS)}$ - $T_{HYS(ABS)}$. The device needs a DC_SYNC or GPINn = "high" condition to restart when T_J is lower than $T_{J(ABS)}$ - $T_{HYS(ABS)}$ after a thermal overload event.

The retry behavior can be configured for each individual output stage via the HSLI interface.

In both retry strategy options, the thermal overload flag OVLD has to be cleared with a HWCR.RESET_OVERLOAD except during the reconfirmation cycle when fault management configuration is set to 1, where it is cleared automatically

6.10 Normal and fast switching mode

The power output stage provides an individual configurable normal and fast switching mode (slew rate) where the turn-on and turn-off timings are defined in PWM output timing and the timing definition is shown in Figure 12.
The normal switching mode is the default configuration and can be changed to fast-mode with the HSLI interface.

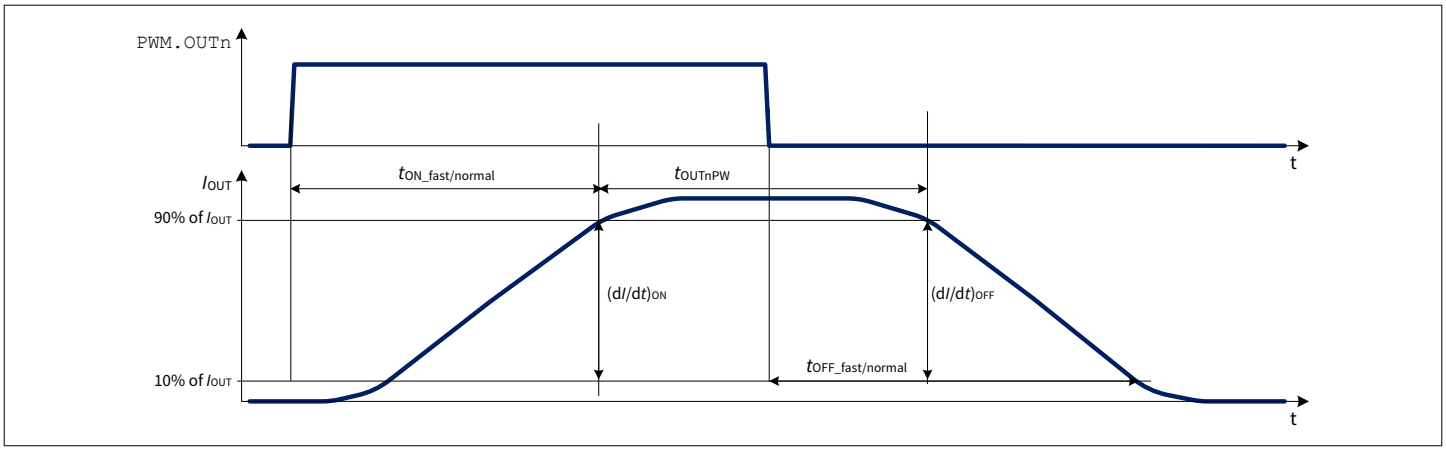


Figure 12 Output stage timing definition

6.11 Electrical characteristics

Table 15 Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage currents							
Output leakage current	I_{OUT_LEAK}	-	–	3	µA	T_J = 85°C, V_{OUT} ≤ 20 V, idle mode	PRQ-428
Output leakage current	I_{OUT_LEAK}	-	–	7	µA	T_J ≤ 150°C, V_{OUT} ≤ 20 V, idle mode	PRQ-429
Output current accuracy and drop-out voltage							
Output current accuracy	$A_{IOUT,25}$	-5	–	5	%	T_J ≥ 25°C full scale range, where 10.125 mA (code 0x4) ≤ I_{OUT} < 76.5 mA (code 0x3F)	PRQ-430
Output current accuracy	A_{IOUT}	-10	–	10	%	-40°C ≤ T_J < 150°C full scale range, where 5.625 mA (code 0x00) ≤ I_{OUT} < 76.5 mA (code 0x3F)	PRQ-431
Output current ripple	ΔI_{OUT}	-1.8	–	1.8	mA	$I_{OUTn\_tPWMn-1}$ - I_{OUTn_tPWMn}, output current difference between two consecutive periods	PRQ-436

(table continues...)

Table 15 (continued) Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output current channel matching	I_{OUTn},I_{OUTn+1}	-5	–	5	%	(I_{OUTn} - $I_{average}$) / $I_{average}$, 10.125 mA (code 0x4) ≤ IOUT ≤ 76.5 mA (code 0x3F)	PRQ-434
Drop out voltage	$V_{DR,1}$		–	600	mV	T_J ≤ 105°C, one channel active, I_{OUT} ≥ 90% of 76.5 mA (code 0x3F)	PRQ-435
Drop out voltage - all channels active	$V_{DR,all}$		–	850	mV	T_J < 105°C, all channels active, I_{OUT} ≥ 90% of 76.5 mA (code 0x3F)	PRQ-604
Power shift threshold voltage accuracy	a_{VOUT_PS}	-0.1	–	0.1	V	two adjacent channels OUT_n and OUT_{n+1} are configured for power shift operation, where n=0,2,8,10	PRQ-689
PWM engine							
Number of PWM channels	n_{PWM}	16	–	–	–	–	PRQ-437
PWM frequency	f_{PWM}	99	–	2020	Hz	Not subject to production test - specified by design	PRQ-438
Duty cycle resolution	n_{DC}	14	–	–	Bit	Not subject to production test - specified by design	PRQ-440
PWM frequency drift	f_{DRIFT}	-1	–	1	%	-20°C ≤ T_J < 125°C, not subject to production test	PRQ-441
PWM phase shift resolution	$n_{PWM\_PH,Res}$	5	–	–	Bit	Not subject to production test - specified by design	PRQ-442
PWM phase shift	n_{PSH}	0	-	6.05	%	Not subject to production test - specified by design	PRQ-688

(table continues...)

Table 15 (continued) Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWM output timing							
PWM turn on time (fast)	t_{ONfast}	–	300	900	ns	fast switching mode; I_{OUT}=90% of 50.625 mA (code 0x28); see Figure 12	PRQ-443
PWM turn on time (normal)	$t_{ONnormal}$	15	20	25	µs	normal switching mode, I_{OUT}=90% of 76.5 mA (code 0x3F), see Figure 12	PRQ-444
Current rise slew rate (normal)	dI/dt_{ON}	2.4	–	4	mA/µs	normal switching mode, I_{OUT} rising from 10% to 90% of 76.5 mA (code 0x3F), see Figure 12	PRQ-698
Current falling slew rate (normal)	dI/dt_{OFF}	-4	–	-2.4	mA/µs	normal switching mode, I_{OUT} falling from 90% to 10% of 76.5 mA (code 0x3F), see Figure 12	PRQ-699
PWM turn off time (fast)	$t_{OFFfast}$	–	300	900	ns	fast switching mode; I_{OUT}=10% of 50.625 mA (code 0x28); see Figure 12	PRQ-445
PWM turn off time (normal)	$t_{OFFnormal}$	15	20	25	µs	normal switching mode; I_{OUT}=10% of 76.5 mA (code 0x3F); see Figure 12	PRQ-446
Turn-on time	t_{ON}	-	-	5	ms	I_{OUT} > 90% of desired output current after DC_SYNC frame at f_{PWM} ≥ 300 Hz and t_{PHS} < 100 µs	PRQ-679

(table continues...)

Table 15 (continued) Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Turn-on time (GPIN)	t_{ON}	–	–	5	ms	I_{OUT} > 90% of desired output current after GPIN="high" at f_{PWM} ≥ 300 Hz and t_{PHS} < 100 µs; GPIN encoding enabled; GPIN is processed after HSLI communication is finished	PRQ-834
Protection							
Thermal current derating accuracy	a_{TJDER}	-5	–	5	K	Not subject to production test - specified by design	PRQ-451
Thermal current derating stop temperature	TJ_{STOP}	155	165	175	°C	specified by design - not subject to production test	PRQ-452
Thermal shutdown temperature	$T_{J(ABS)}$	150	175	200	°C	Not subject to production test - specified by design	PRQ-449
Thermal shutdown hysteresis	$T_{HYS(ABS)}$	5	10	15	K	specified by design	PRQ-450

7 Load Diagnostic

7.1 Features

Several load diagnostic features are integrated in the device for all of the output channels OUTn:

- Open load detection (OL)
- Forward voltage warning to detect short to supply
- Single LED Short detection (SLS)
- Short between two adjacent output channels
- Digital feedback of VS, GPINn, VLED, min(VOUTn) and VFWDn
- ERRn feedback, if enabled
- Configurable fault management, reporting, latching or retry behavior

7.2 VFWD measurement

The device provides an analog to digital conversion of V_{FWD} voltage with a resolution of $n_{VRES,Hi}$, accessible with the HSLI interface when OUTn pulse width (t_{OUTnPW}) fulfills:

- $t_{OUTnPW} > t_{diag\_dly} + t_{DIAG\_ON}$ in case phase shift is enabled OR
- $t_{OUTnPW} > t_{diag\_dly} + N * t_{DIAG\_ON}$ in case phase shift is disabled, where N is equal to the number of preceding channels with phase shift disabled.

V_{FWD} is defined as V_{LED}-V_{OUT} or V_S-V_{OUT} depending on the load configuration stored in the OTP. All 16 V_{FWD} voltage measurements are sampled sequentially starting from OUT0 to OUT15. One channel starts sampling after t_{diag_dly} and the result is available after t_{DIAG_ON} as shown in the Figure 13.

In case of phase shift disabled between two adjacent channels, the t_{diag_dly} is skipped.

The phase shift shall be set to $t_{phs} > t_{diag\_dly} + 2*t_{DIAG\_ON}$ for proper supplies and output voltages sampling.

The conversion is done once per PWM period and continuously updated. New data is signaled with a dedicated VALID flag which is reset after reading completion.

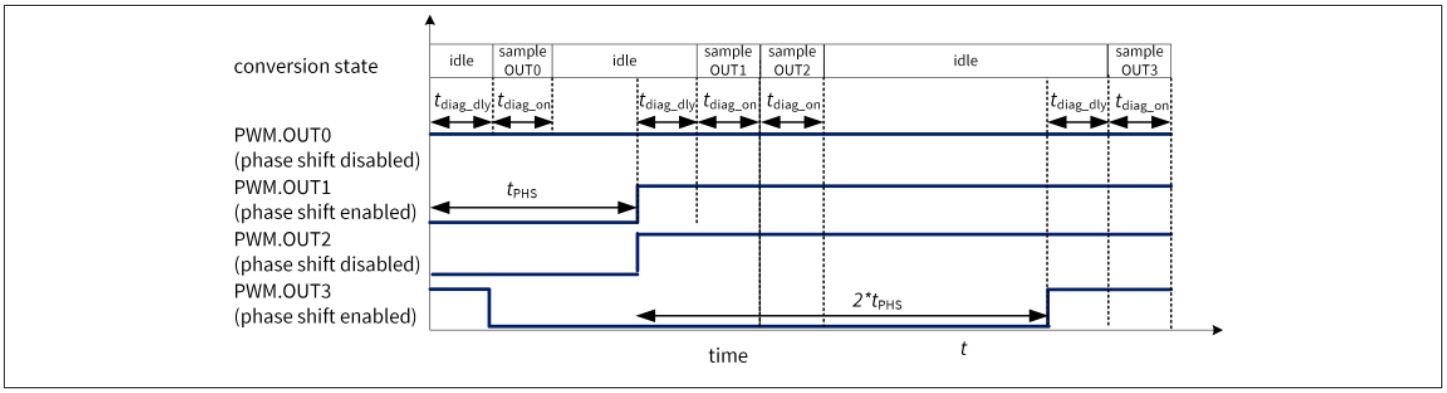


Figure 13 Timing diagram for ON-state diagnostics synchronized to the PWM

7.3 VGPIN measurement

The device provides an analog to digital conversion of V_{GPIN} voltage with a resolution of $n_{VRES,Lo}$, accessible with the HSLI interface. The device samples the V_{GPIn} and stores the result in a VGPIN register. New data is signaled with a dedicated VALID flag which is reset after reading completion.

Note: *The sampling period depends on the phase-shift configuration according to following table.*

Table 16 Sample period relation to phase shift configuration

> 4 output channels enable phase shift	≤ 4 output channels enable phase shift
sampling requires one PWM period	sampling requires up to 4 PWM periods

7.4 VLED measurement

The device provides an analog to digital conversion of V_{LED} voltage with a resolution of $n_{VRES,Hi}$, accessible with the HSLI interface. The device samples the V_{LED} and stores the result in a VLED register. New data is signaled with a dedicated VALID flag, which is reset after reading completion.

Note: *The sampling period depends on the phase-shift configuration according to following table.*

Table 17 Sample period relation to phase shift configuration

> 4 output channels enable phase shift	≤ 4 output channels enable phase shift
sampling requires one PWM period	sampling requires up to 4 PWM periods

7.5 VS measurement

The device provides an analog to digital conversion of V_S voltage measurement with a resolution of $n_{VRES,Hi}$, accessible with the HSLI interface. The device samples the V_S and stores the result in a VS result register. New data is signaled with a dedicated VALID flag, which is reset after reading completion.

Note: *The sampling period depends on the phase-shift configuration according to following table.*

Table 18 Sample period relation to phase shift configuration

> 4 output channels enable phase shift	≤ 4 output channels enable phase shift
sampling requires one PWM period	sampling requires up to 4 PWM periods

7.6 Minimum VOUT measurement

The device provides an analog to digital conversion of the minimum of its 16 V_{OUT} voltage measurements with a resolution of $n_{VRES,Hi}$, accessible with the HSLI interface. The device samples the min(V_{OUTn}) once per PWM period and stores the result in a result register. New data is signaled with a dedicated VALID flag, which is reset after reading completion.

OUT0 can be masked out from the minimum calculation via an OTP configuration bit. This allows to use OUT0 as feedback current sink to an external DC-DC to its adjustable voltage input pin.

OUT15 is masked out from the minimum calculation when used as ERRN pin.

7.7 Voltage regulator feedback

The LCU can use OUT0 to control a current to a feedback network of an external voltage regulator. This feature can be enabled via an OTP configuration bit. In case output channel is configured as feedback path following diagnostic mechanism are masked out

- exclusion from min(VOUT) measurement
- open load detection
- Forward voltage warning (VFWD_WRN)

Additionally the VFWD measurement register for output channel holds the output voltage VOUT instead of the forward voltage VFWD to directly provide the feedback voltage.

7.8 Open load detection

The device detects an open load fault if

- output stage is in ON-state AND
- $V_{OUTn} \leq V_{OUT,OL\_th}$ for more than $n_{debounce}$ consecutive PWM periods AND
- $V_S \geq V_{DEN\_threshold}$ for VS related diagnostic AND
- $V_{LED} \geq V_{DEN\_threshold}$ for VLED related diagnostic.

The open load (OL) is reported in the channel status byte OUTn and, if it is enabled, via ERRN. The OL flag is cleared after the fault has been acknowledged with an explicit HWCR frame from the LCU.

7.9 Single LED Short (SLS) detection

The device provides a single LED short (SLS) detection based on the V_{FWD} conversion result.

A SLS is detected if

- $0 \leq V_{FWDn} \leq V_{SLSth\_m}$ for more than $n_{debounce}$ consecutive PWM periods, where m=0,1 which denotes the diagnostic group AND
- OUTn pulse width as specified for VFWD measurement AND
- $V_S \geq V_{DEN\_threshold}$ for VS related diagnostic AND
- $V_{LED} \geq V_{DEN\_threshold}$ for VLED related diagnostic.

The two default SLS threshold voltages V_{SLSth_m} are configured via the OTP and can be changed in active mode via the HSLI with 256 steps from 0V to 20.067 V.

The device reports the SLS event in a channel status byte OUTn and, if enabled, via ERRN. The SLS flag is cleared after the fault has been acknowledged with an explicit HWCR frame from the LCU.

7.10 OUT_SHORT_WRN, CUR_WRN, DC_WRN, VFWD_WRN warnings

The device reports a violation of the forward voltage (VFWD_WRN), based on the VFWD measurement, in the output status byte and channel status byte OUTn and, if it is enabled, via ERRN. The VFWD warning (VFWD_WRN) thresholds are stored in the OTP. The loads can use two different sensing pins for the anode voltage: VS and VLED. The sensing input to be used is selected in the diagnostic group OTP register. If the forward voltage is too low for more than ndebounce, then the VFWD_WRN.OUTn is set on the HSLI channel status byte OUTn. If at least one VFWD_WRN.OUTn bit is set, the VFWD_WRN bit is set in the output status byte. The VFWD_WRN flag is cleared with an explicit HWCR frame from the LCU.

The OUT_SHORT_WRN flag indicates a possible short between adjacent outputs. The fail is reported in the channel status byte OUTn and, if enabled, via ERRN. If at least one OUT_SHORT_WRN.OUTn bit is set, the OUT_SHORT_WRN bit is set in the output status byte. The OUT_SHORT_WRN can be enabled individually for each output via OTP. The OUT_SHORT_WRN is a safety feature. Detailed operational conditions are presented in the safety manual.

The current warning mechanism monitors the regulated current on each power output channel in ON state condition if ton is above 100 µs. The channels that are OFF are not monitored. The current warning flag CUR_WRN is reported in case the measured current is lower than 15 mA (max) of the set OTP current value for more than n_debounce consecutive periods.

Further information on the current warning settings can be found in the user manual.

In case the OTP current value is set equal or below 14.625 mA (I_{OUT} step=08) the output status byte can report an unintended current warning flag. It is recommended to set an OTP current value higher of equal than 15.75 mA (I_{OUT} step = 09) to avoid unintended current warning flags.

The CUR_WRN is reported in the channel status byte OUTn and, if enabled, via ERRN. If at least one CUR_WRN.OUTn bit is set, the CUR_WRN bit is set in the output status byte. The CUR_WRN flag is cleared after the warning has been acknowledged with an explicit HWCR frame from the LCU. An additional OTP parameter disables the report of the current warning on the ERRN output. This can be used to avoid warnings on applications where thermal derating or power offload is applied.

The duty cycle warning (DC_WRN) compares the duty cycle for each power output channel witht the target stored in the OTP, when controlled via GPIN, or the one set with a DC_UPDATE command. It reports a deviation of the duty cycle bigger than 20% for more than $n_{debounce}$ consecutive periods. The DC_WRN.OUTn is reported on the channel status byte OUTn and, if enabled, via ERRN. If at least one DC_WRN.OUTn bit is set, the DC_WRN bit is set in the output status byte. The DC_WRN flag is cleared after the warning has been acknowledged with an explicit HWCR frame from the LCU. In case of DC_UPDATE with DLC=0x4 (8-bit format) is applied, the output status byte can report an unintended DC_WRN due to the power-law relation. It is recommended to ignore a DC_WRN when using DC_UPDATE with DLC=0x4 and to use DC_UPDATE with DLC=0x6 if the DC_WRN safety mechanism is needed.

7.11 Diagnostic group

Each output stage is assigned to a diagnostic group to select the anode voltage reference and SLS reference voltage.

OUTnDIAG group
0b aaaa aaaa aaaa aaaa

Definition for a

"0" ... output is mapped to group 0, VS is taken as LED load anode voltage

"1" ... output is mapped to group 1, VLED is taken as LED load anode voltage

7.12 Configurable fault management

The device provides configuration options to define the output behavior on detected LED load faults (OL, SLS, OVLD) and ERRn reaction. The fault management configuration can be set in OTP according to the following table:

Table 19 Fault management

Fault management configuration	Device power mode state change
0 (default)	no state change
1	change to init mode (power stages are turned off)

The fault management configuration is valid in active mode only.

If the Fault management is set to 1, and a load fault (OL, SLS, OVLD) or ERRn is recognized, the device will move to INIT switching off all the outputs and it is ready to perform a reconfirmation cycle. Load warnings (CUR_WRN, DC_WRN, VFWD_WRN, OUT_SHORT_WRN) do not trigger an INIT transition unless the ERRn is enabled in OTP. In this last case, the INIT transition happens due to the ERRn reaction. If Fault Management is set to 0, the outputs are not turned off in case of OL, SLS and ERRn, and the device does not moves to INIT. The LCU can take care of disabling the failing output based on the application diagnostic strategy.

7.13 Load fault reconfirmation cycle

A load fault reconfirmation cycle consist of a wait time followed by a re-activation of the failing output. This in order to check if the fault condition persist, while keeping the rest of the outputs off. This allows reduced current consumption during fault. A reconfirmation cycle consist on 2 phases

- An INIT phase where all the channels are switched OFF
- An ACTIVE phase where the failing output can be turned ON

A reconfirmation cycle is performed if

- fault management configuration is set to "1" AND
- a load fault is detected in the previous ACTIVE phase

The reconfirmation cycle starts after a fault detection by moving the device in the INIT phase with outputs OFF. The INIT phase persist for at least t_{reconf} time.

In case of HSLI control, the ACTIVE phase is trigger by a DC_UPDATE command with a delay of t_{reconf}. The DC_UPDATE command will also clear the fault flags to allow the reconfirmation procedure. Once in ACTIVE phase, a DC_SYNC command is needed to turn on only the failing output for ((2 + $n_{debounce}$) x PWM period) time.

In case of direct control via GPIN, the ACTIVE phase is trigger by a GPIN HIGH with a delay of t_{reconf}. The fault flags (OL, SLS, OVLD) are cleared automatically at the beginning of the t_{reconf}. Once in ACTIVE phase only the failing output is turned on for ((2 + $n_{debounce}$) x PWM period) time in order to reconfirm the load fault. In case the failure is reconfirmed, the device moves to the INIT phase again. If the fault condition is not detected during ACTIVE ON, for more than ($n_{debounce}$ x PWM period) time, the device will enable also the other outputs

The status of the reconfirmation cycle can be checked via HSLI in the reconfirmation status register.

Note: In an HSLI application (no GPINn activations requests), the load fault shall be read with a READ_OST frame before the DC_UPDATE frame.

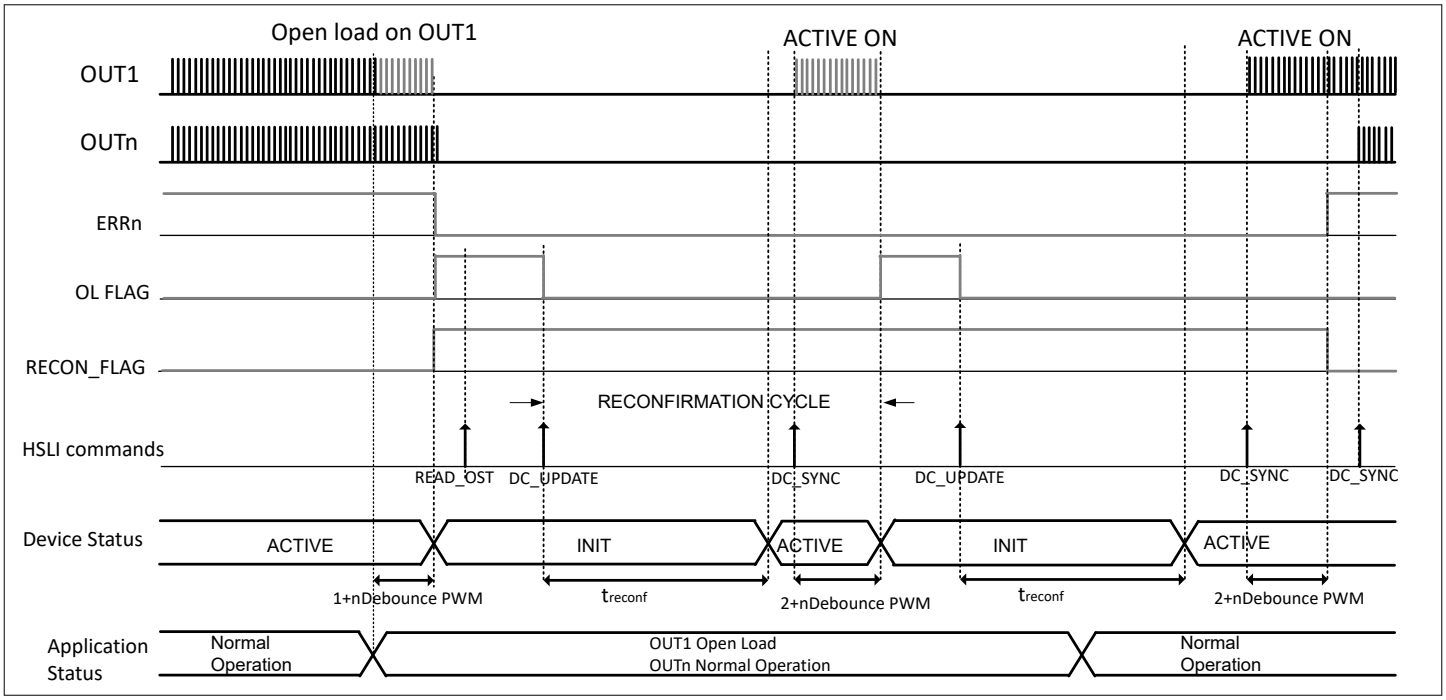


Figure 14 Load fault reconfirmation cycle with HSLI

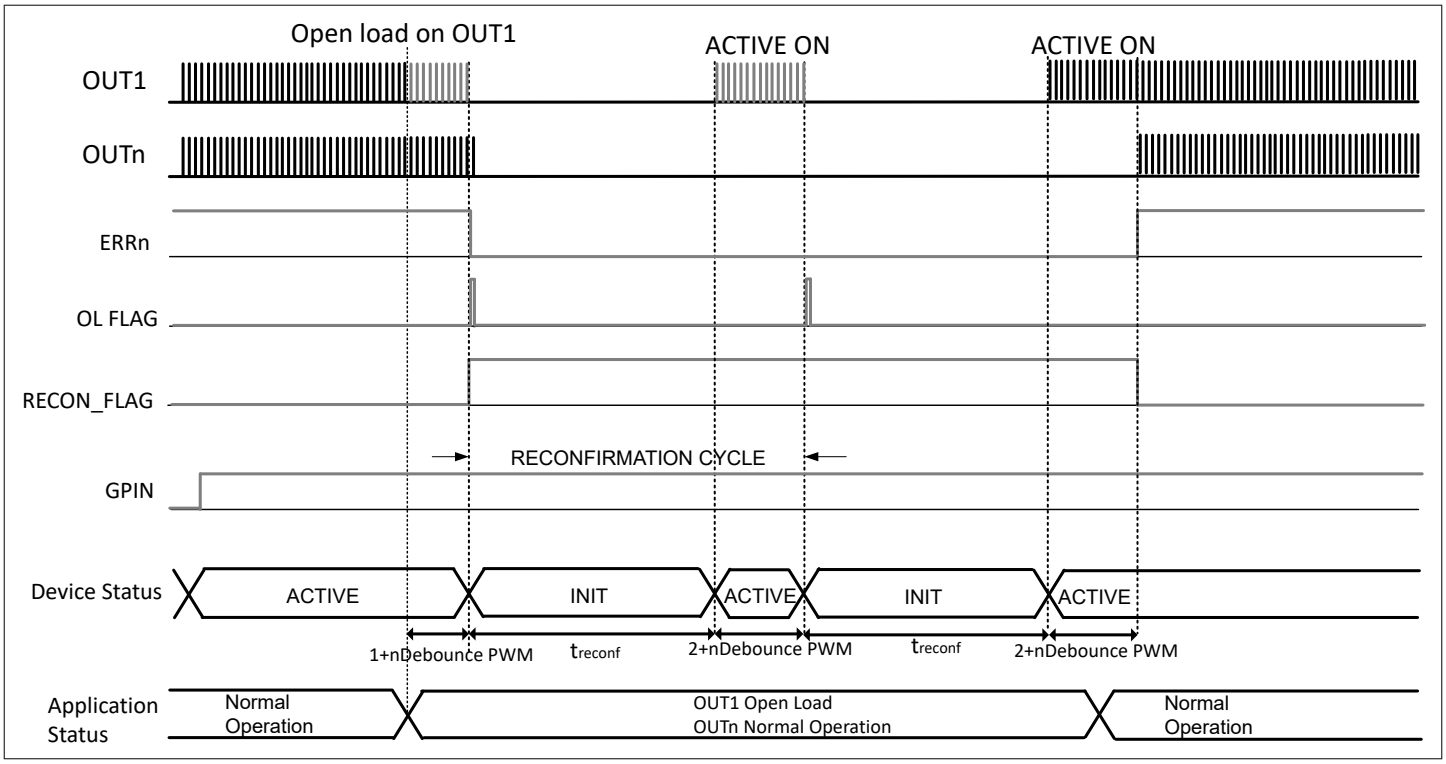


Figure 15 Load fault reconfirmation cycle with GPIN

7.14 Diagnostic enable

An unintended LED open or SLS fault can be detected on OUTn in low supply condition on VS or VLED depending on the Diagnostic group configuration.

The device provides one diagnostic enable threshold related to VS and one diagnostic enable threshold related to VLED according to following table:

Table 20 Diagnostic enable threshold

Code	$V_{DEN\_threshold}$ [V]	Code	$V_{DEN\_threshold}$ [V]	Code	$V_{DEN\_threshold}$ [V]	Code	$V_{DEN\_threshold}$ [V]
0	0	8	5.017	16	10.034	24	15.050
1	0.627	9	5.644	17	10.661	25	15.677
2	1.254	10	6.271	18	11.288	26	16.305
3	1.881	11	6.898	19	11.915	27	16.932
4	2.508	12	7.525	20	12.542	28	17.559
5	3.135	13	8.152	21	13.169	29	18.186
6	3.763	14	8.779	22	13.796	30	18.813
7	4.390	15	9.406	23	14.423	31	19.440

Both diagnostic enable thresholds are stored in the OTP.

Load diagnostic is only available for active-ON channel (duty cycle DC>0%). Set DC=0% on unused output will prevent from receiving spurious warnings. Exception is OUT_SHORT_WRN which is also available with DC=0%, but it can be disabled via OTP.

If the device is in ACTIVE, FAIL-SAFE or OTP modes and VS or VLED are below their respective VDEN_THRESHOLD, the device reports an VLED_VS_UV in the output status byte.

The VLED_VS_UV flag is cleared with an explicit HWCR frame from LCU.

7.15 Diagnostic sample delay

The device provides a configurable diagnostic sample delay t_{diag_dly} according to following table:

Table 21 Diagnostic sample delay

Code	t_{diag_dly} [µs]
0	8
1	16
2	24
3	48
4	96
5	192
6	300
7	600

The diagnostic sample delay is stored in the OTP.

7.16 Load diagnostic debouncing

The device provides a configurable load diagnostic debouncing counter $n_{debounce}$ according to following table:

Table 22 Diagnostic sample delay

Code	$n_{debounce}$
0	reserved
1	2 (default)
2	4
3	6

The load diagnostic debouncing counter $n_{debounce}$ is configurable via the OTP.

7.17 ERRN reaction

With the use of an external pull-up resistor multiple devices can share the open drain diagnosis line as shown in Figure 16.

The device detects an ERRN condition when $V_{ERRN} \leq V_{ERRN,th}$ and VS OR VLED is above the related VDEN_threshold.

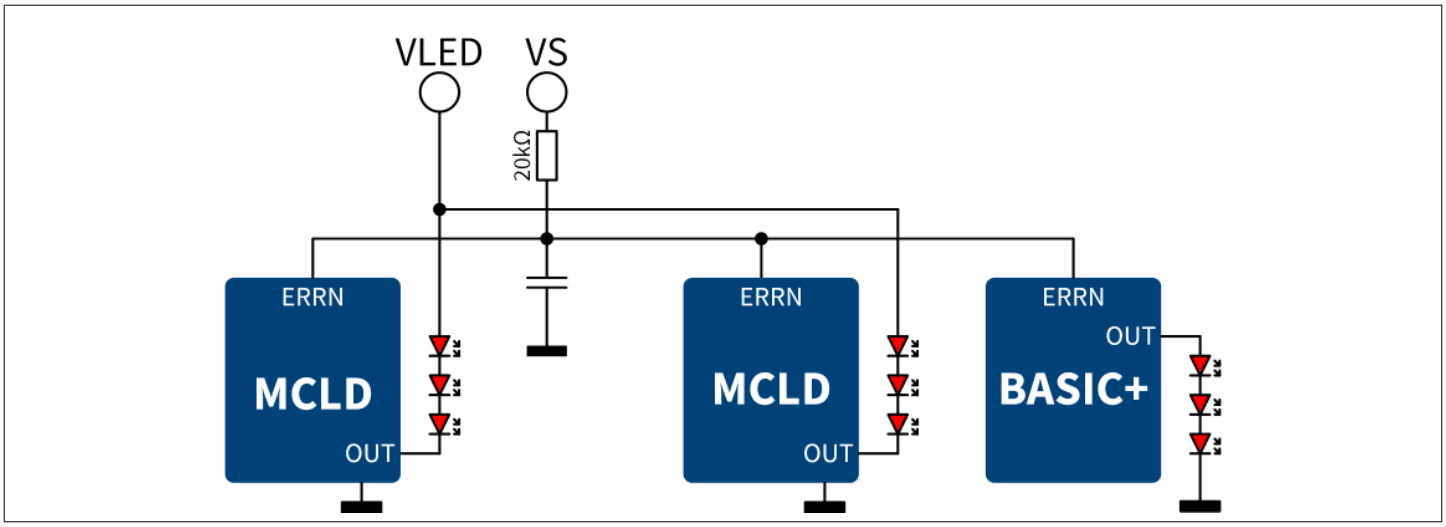


Figure 16 Shared error network principle

7.18 ERRN report

The device is able to report a detected load fault with the ERRN pin.

The open-drain ERRN pin sinks a pull-down current I_{ERRN} in ≤ t_{ERRN} when

- the device is in init OR fail-safe mode OR active mode AND
- a load fault OR internal fault OR warning has been detected AND
- the ERRN is enabled via the OTP

Following diagnostic is disabled on OUT15, when it is used as ERRN feedback:

- min(VOUT) measurement
- open load detection
- single led short detection
- VFWD warning
- PWM duty cycle monitoring only for channel 15
- current monitor
- short between adjacent channels

7.19 ERRn reporting sources

The ERRn reports following faults:

Table 23 List of fault sources for the ERRn reporting

Fault source group	Fault Short description	Fault Long description
Load faults	OVLD	thermal overload
	SLS	Single LED Short
	OL	open load
Warnings	CUR_WRN	current too low
	DC_WRN	duty cycle out of range
	VFWD_WRN	forward voltage out of range
	OUT_SHORT_WRN	short to adjacent channel
	GPINn_WRN	GPINn warning

(table continues...)

Table 23 (continued) List of fault sources for the ERRn reporting

Fault source group	Fault Short description	Fault Long description
Internal faults	UV&OV	under/overvoltage of internal supply
	IREF	reference current out of range
	OTP_CHECKSUM	OTP checksum error
	BIST_FAIL	BIST failed
	GPIN_SHORT	GPIN short

7.20 HSLI diagnostic flag handling

Application shall take care to clear the diagnostic flags during operation in order to allow new fault events detection.

List of Output status and READ_OST flags and the relation with HWCR frame

Output status/READ_OST fields		Clearable by HWCR	Need HWCR to restart the output if the failure disappears
OL		YES	NO
SLS		YES	NO
OVLD		YES	Based on thermal overload retry strategy
OUT_SHORT_WRN		YES	NO
DC_WRN		YES	NO
CUR_WRN		YES	NO
VFWD_WRN		YES	NO
OUT_STAT		NO (since not latched)	NO
VLED_VS_UV		YES	NO
GPIN_WRN		YES	NO
FAULT	Internal supply UV/OV	NO (since not latched)	NO
	OTP checksum warning	YES	YES
	Internal BIST error	YES	YES
	Internal reference current warning	YES	YES
	GPIN short	YES	YES

The FAULT Flag forces the device in INIT or FAIL OFF based on fault type so it may need HWCR or 6 consecutive HSLI sync break frames to move the device in to an active condition.

When HSLI is not available to provide an HWCR (e.g. GPIN direct drive application), special care has to be taken in order to reduce FAULT events.

A diode and a 470nF capacitor applied on VS reduce the risk of internal faults due to transient on the VS supply pin.

7.21 Electrical characteristics

Table 24 Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Open load detection threshold	V_{OUT,OL_th}	300	400	500	mV	Not subject to production test - specified by design	PRQ-731
Voltage measurement							
Voltage high-range conversion resolution	$n_{VRES,Hi}$	10	–	–	Bit	full scale 20.034 V; V_S, V_{LED}, V_{OUT} < 19.75 V	PRQ-471
Voltage low-range conversion resolution	$n_{VRES,Lo}$	10	–	–	Bit	full scale 5.496 V; V_{GPIN} < 5V	PRQ-685
ADC Differential nonlinearity	DNL	-1	–	2	LSB	–	PRQ-476
ADC Integral nonlinearity	INL	-2	–	2	LSB	–	PRQ-477
ADC offset	$VADC_{offset}$	-4	–	3	LSB	–	PRQ-709
ADC gain error	$e_{ADCgain}$	-1	–	1	%	–	PRQ-710
ERRN fault feedback							
ERRn fault current	I_{ERRn}	4	–	–	mA	V_{ERRn} ≥ 0.8 V	PRQ-700
ERRn input threshold	$V_{ERRn,th}$	0.8	–	2	V	–	PRQ-701
Timing							
Diagnostic on sample time	t_{DIAG_ON}	–	–	20	µs	Not subject to production test - specified by design	PRQ-687
Reconfirmation delay time	t_{reconf}	80	–	120	ms	Not subject to production test - specified by design	PRQ-875
ERRN activation delay	t_{ERRn}	-	-	2*t_{PWM}	ms	Not subject to production test - specified by design	PRQ-708

8 OTP

8.1 Features

The device contains a one-time programmable memory (OTP) to store the device configuration and provides following features:

- Programming mode for bus-ID and configuration section
- Emulation modes
- CRC checksum to verify consistency

It can be programmed during end of line production step at customer site.

8.2 Electrical characteristics

Table 25 Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Programming cycles	N_{PRG}	1	–	–	–	One time programmable memory (OTP)	PRQ-494
OTP programming voltage supply	V_{S_PRG}	15.5	17.5	20	V	–	PRQ-495
OTP programming cycle time	t_{PRG}	–	–	64	ms	500 µs per 16 bit cycle time; not subject to production test - specified by design	PRQ-496

9 Communication interface

The device provides a UART-based protocol HSLI, where the LCU can write and read registers to and from each device sharing the same bus.

The device provides the OTP programming and OTP emulation functions via the HSLI interface.

9.1 Protocol layer - High Speed Lighting Interface

9.1.1 General description

The High-speed Lighting Interface (HSLI) is a digital interface for high performance automotive applications. The interface data link layer is based on a standard universal asynchronous receiver transmitter (UART) bit stream. The protocol is designed to support direct device-to-µC connections as well as CAN-FD transceivers to implement a robust connection scheme for remote control applications. Thanks to the lean protocol implementation, high update rates can be achieved despite limited bandwidth especially with remote interfaces.

9.1.2 Main features

The HSLI is a cost efficient interface for high performance automotive applications. HSLI can be used as highly flexible interface for transferring data.

- Single master, multiple slave concept
- Synchronization of single or multiple slaves
- Supports bus configurations with up to 31 addressable slaves and 1 broadcast address
- Bidirectional communication
- Auto-bit rate detection within the range from 200 kbit/s up to 2 Mbit/s when LP_INIT='0' or up to 500 kbit/s when LP_INIT='1'.

9.1.3 Frame structure

The frame consists of a number of bytes:

- one sync byte
- one master request
- followed by 0 to n master data bytes
- and 0 to n slave data bytes

The structure of a full communication frame is shown below:

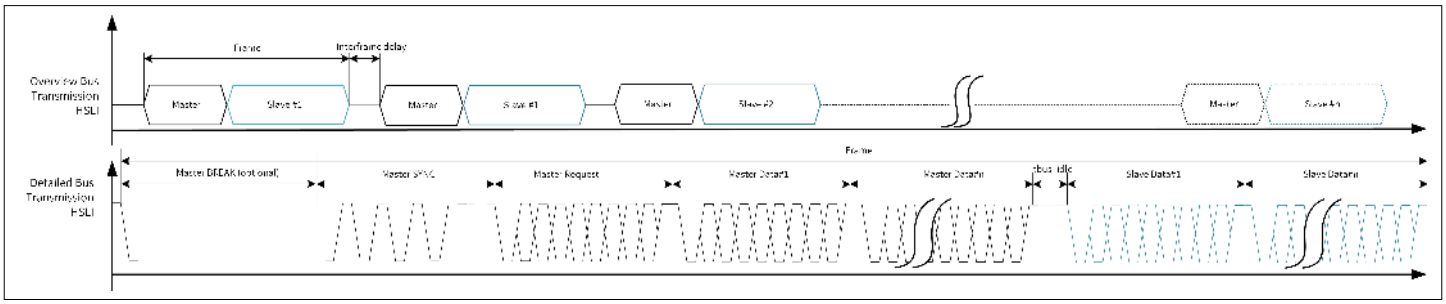


Figure 17 Structure of a frame

9.1.4 HSLI interframe delay

The HSLI aborts processing the communication when no dominant ("0") bus communication occurred longer than the interfame delay $t_{framedly}$. The master needs to wait longer than $t_{framedly}$ between two consecutive frames.

The interframe delay is configurable via the OTP according to following table:

Table 26 HSLI interframe delay

Step	$t_{framedly}$
0	50 µs
1	100 µs
2	250 µs
3	500 µs
4 (default)	1 ms
5	2.5 ms

The device starts counting the interframe delay from the last received dominant bit and not at the end of the byte transmitted.

In case of a 0xFF byte transmission the counting starts from the start bit.

9.1.5 Slave response bus idle time

The slave responds to a valid master request within t_{bus_idle} when requested by the master.

9.1.6 UART byte field

The next figure shows the standard UART byte field. This structure is the basis for data transfer between slave and master. The LSB of the data is transmitted first and the MSB last. The start bit is encoded as a low and the stop bit is encoded as a high bit.

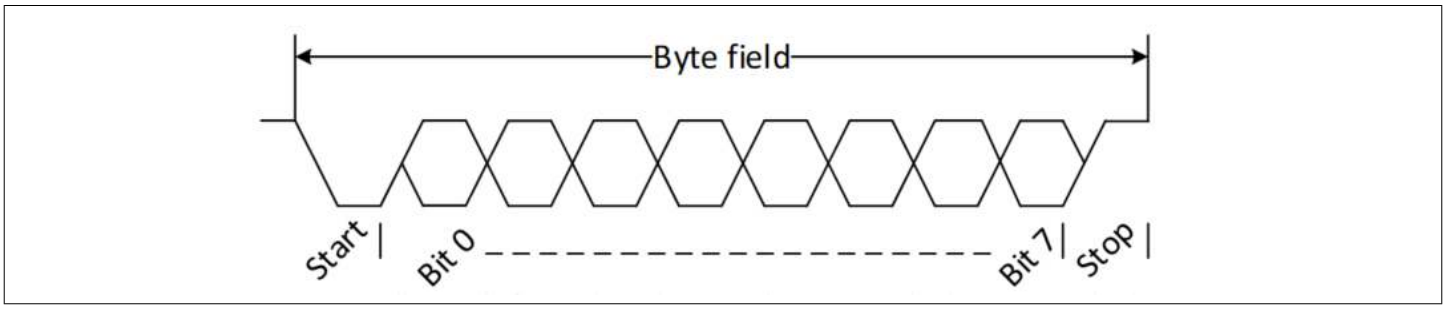


Figure 18 UART byte field

9.1.7 HSLI baud rate auto detection

The HSLI supports Baud rates in the range of n_{Baud}. The Baud rate configuration is automatically detected based on the master request.

9.1.8 HSLI bit timing

The HSLI uses a variable oversampling for the RX signal within 16 quanta with a configurable bit sample timing stored in the OTP.

Table 27 HSLI bit timing

Step	n_{BST}
0 (default)	7,8,9
1	8,9,10
2	9,10,11
3	10,11,12

9.1.9 HSLI watchdog timeout

The watchdog is used to monitor the HSLI bus activity and to trigger a state change to fail-safe mode in case of a communication timeout.

The watchdog recognizes a successful watchdog trigger when receiving a valid HSLI command within less than $t_{WD} \pm a_{tWD\_Tol}$ since the previous successful watchdog trigger as shown in the following figure.

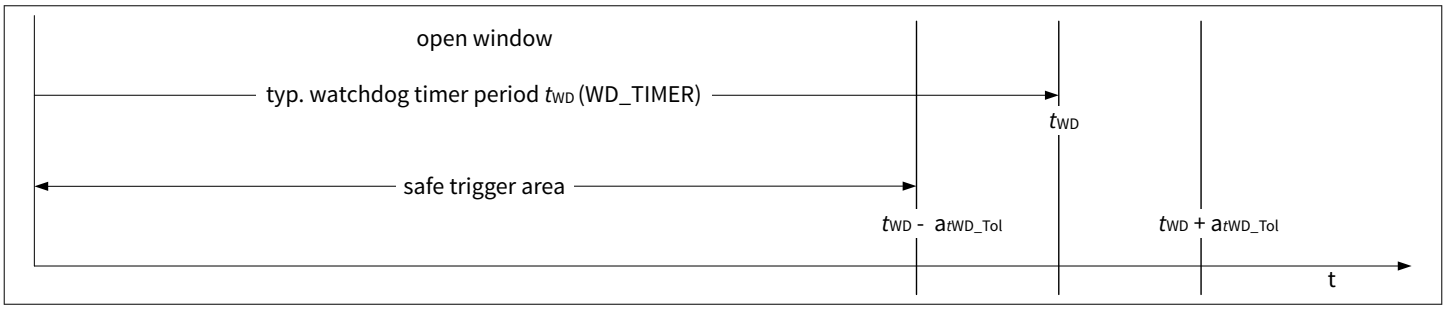


Figure 19 Watchdog timeout trigger definition

The watchdog timer period t_{WD} (WD_TIMER) can be configured via the OTP according to following table:

Table 28 WD_TIMER configuration

WD_TIMER	t_{WD} [ms] , where LP_INIT = '0'	t_{WD} [ms] , where LP_INIT = '1' AND device is in init mode
0	disabled	disabled
1	20	60
2	50	150
3	100	300
4	200	600
5	500	1500
6	1000	3000
7	2000 (default)	6000 (default)

9.1.10 Electrical characteristics

Table 29 Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Baud rate	n_{BAUD}	0.2	-	2	MBaud	LP_INIT = '0'; Not subject to production test - specified by design	PRQ-737
Baud rate LP_INIT	n_{BAUD}	0.1	-	0.5	MBaud	init mode; LP_INIT = '1'; Not subject to production test - specified by design	PRQ-880
Slave response bus idle time	t_{bus_idle}	0.1	-	15	µs	active mode, OTP programming and emulation modes, fail-safe mode; not subject to production test - specified by design	PRQ-738
Slave response bus idle time in init mode	t_{bus_idle}	1	–	100	µs	init mode; not subject to production test - specified by design	PRQ-781
Timeout watchdog tolerance	a_{tWD_Tol}	-10	–	10	%	Not subject to production test - specified by design	PRQ-820

9.1.11 Master Frame Types

9.1.11.1 Overview

The frame type describes the different configuration of frames. Some of the frame types are only for specific purpose, which will be defined in the following subsections. The master request frames are issued by the LCU and provide address information for the connected slave. The slave will receive every master request frame and compare the address information to its reference address stored in the OTP. If the address issued by the master matches the slave reference address, the slave takes action according the master request frame; otherwise the entire frame will be ignored.

When setting up a network it has to be taken care that all slaves connected to the network are assigned a unique address to avoid bus collisions. One particular slave address is used to implement a broadcast synchronization feature, which will cause all connected slaves to change their duty cycle output control configuration at the same point in time.

The data transfer from the LCU to the slave is organized in dedicated master request frames, namely

- Broadcast duty cycle update synchronization - DC_SYNC
- Update duty cycle shadow register - DC_UPDATE
- Power mode change - PM_CHANGE
- Hardware control - HWCR
- Read diagnostics - READ_OST
- Write register content - WRITE_REG
- Read register content - READ_REG
- Sync break reset - SYNC_BREAK

The following sequence diagram shows the write and read register frame sequence for two nodes.

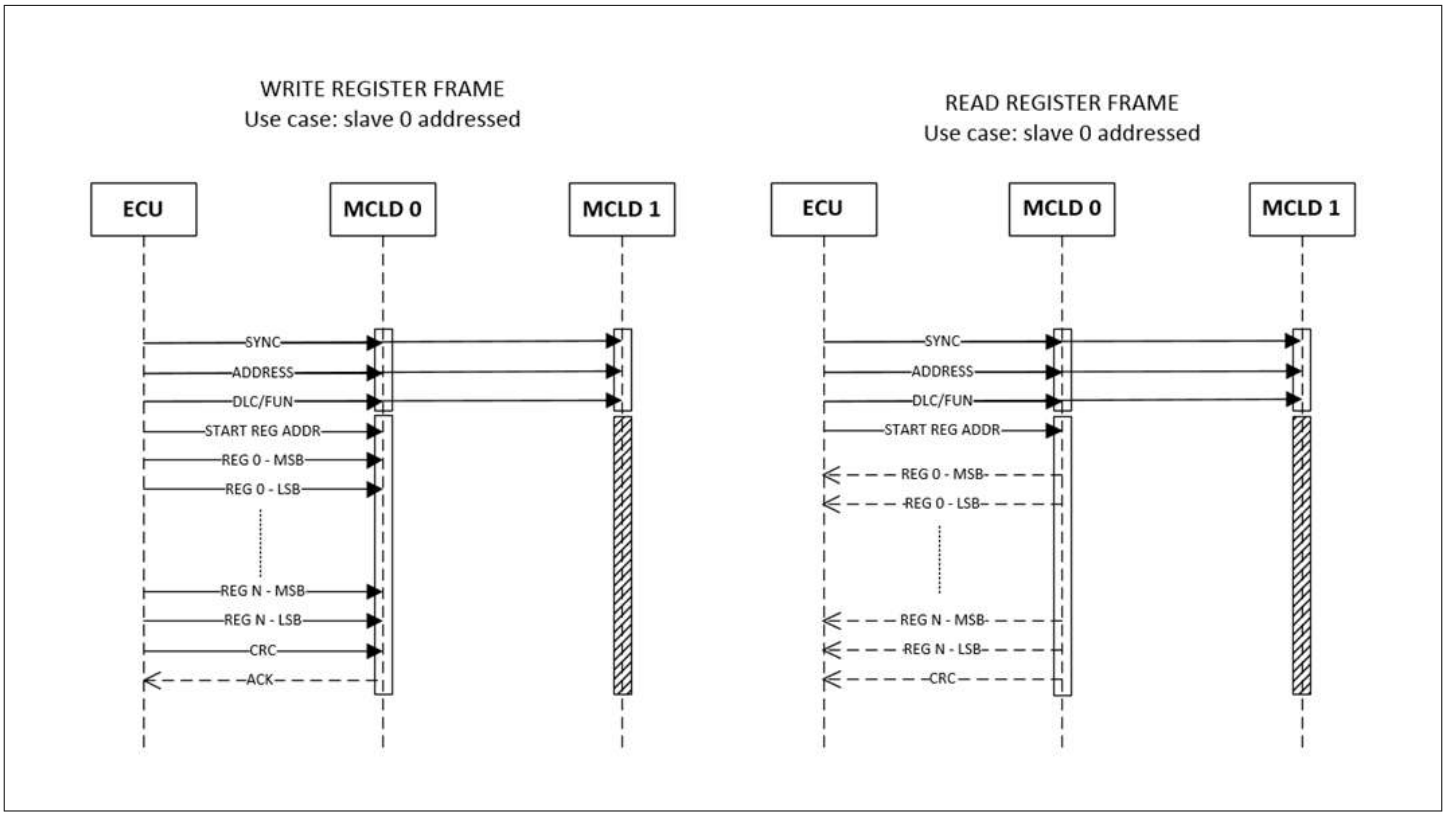


Figure 20 Sequence diagram - write and read registers

Table 30 Master frame overview table

SYNC	ADDRESS	MRC		DLC		FUN		DATA_0 ... DATA_n	Ouptut Status Byte	ACK Byte
0x55	0x0	x	x	0x0	0 words	0x0	Broadcast duty cycle synchronization	not applicable for broadcast command		
0x55	0x1	x	x	0x1	1 word	0x1	Duty cycle shadow register update	data by the master	Diagnostic feedback (slave)	CRC-3, MODE, RC, TER (slave)
0x55	0x2	x	x	0x2	2 words	0x2	Request diagnostics	data by the slave	Diagnostic feedback (slave)	CRC-3, MODE, RC, TER (slave)

(table continues...)

Table 30 (continued) Master frame overview table

SYNC	ADDRESS	MRC		DLC		FUN		DATA_0 ... DATA_n	Ouptut Status Byte	ACK Byte
0x55	0x3	x	x	0x3	4 words	0x3	Hardware control	data by the master	Diagnostic feedback (slave)	CRC-3, MODE, RC, TER (slave)
0x55	0x4	x	x	0x4	8 words	0x4	Write register	data by the master	Diagnostic feedback (slave)	CRC-3, MODE, RC, TER (slave)
0x55	0x5	x	x	0x5	12 words	0x5	Read register	data by the slave	Diagnostic feedback (slave)	CRC-3, MODE, RC, TER (slave)
...	...	...	...	0x6	16 words	0x6	Power mode change	data by the master	Diagnostic feedback (slave)	CRC-3, MODE, RC, TER (slave)
0x55	0x1F	x	x	0x7	32 words	0x7	reserved			

9.1.11.2 DC_SYNC - broadcast duty cycle update synchronization

Some applications require a synchronous change of the output duty cycle configuration of all connected slaves on the bus.

The protocol provides a broadcast duty cycle update synchronization command (DC_SYNC) to trigger a synchronous sampling event at multiple slaves. The sampling event can trigger the duty cycle update process, where the duty cycle data from the shadow register is transferred to the hardware control register synchronized to the start of the next PWM period. An updated output channel completes the actual PWM pulse before changing to the new duty cycle configuration to avoid glitches on the output.

The frame description is shown in Figure 21.

The DC_SYNC frame requires following field configurations:

- Address[4:0] = 0x00
- DLC[5:3] = 0x0
- FUN[2:0] = 0x0

There is no response from the slave to the master given in case of the broadcast duty cycle update synchronization frame.

The CRC [7:5] is calculated as described in Chapter 9.1.11.11.

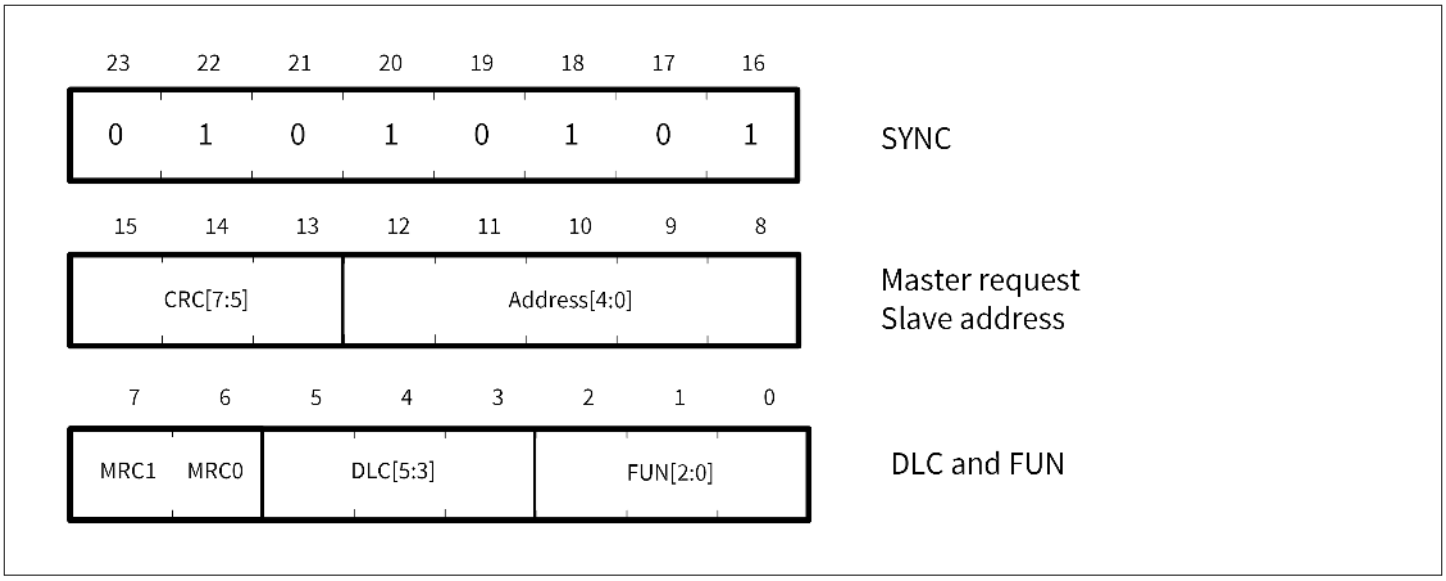


Figure 21 Broadcast synchronization frame

9.1.11.3 DC_UPDATE - update duty cycle shadow register

The purpose of the master request frame update duty cycle is to refresh the duty cycle for each channel within one master request. The data transfer to the slave is organized in dedicated write frame, containing

- the sync byte, provided by the master,
- the address byte, provided by the master,
- the MRC_DLC_FUN byte, provided by the master,
- the DutyCycleOUTn bytes representing the desired duty cycle, DLC times words provided by the master,
- the safety byte (CRC-8), provided by the master,
- the output status bytes, provided by the slave and the
- Acknowledge byte (ACK) provided by the slave.

The DC_UPDATE frame requires following field configurations to update the duty cycle:

- DLC[5:3] = 0x4 for 8 words respectively 16 bytes for 8-bit duty cycle configuration OR
- DLC[5:3] = 0x6 for 16 words respectively 32 bytes for 14-bit duty cycle configuration
- FUN[2:0] = 0x1

The slave ignores and discards frames in case of an unexpected DLC or FUN data as described in Chapter 9.1.11.10. In addition a broadcast frame with DLC[5:3] = 0x0 is ignored.

The DC_UPDATE frame requires following field configurations to retrieve diagnostics only:

- DLC[5:3] = 0x0 for output status bytes only
- FUN[2:0] = 0x1

The slave response bytes "output status byte and acknowledge byte" are skipped in case the frame is sent to the broadcast address. Consequently there is no response from the slave to the master provided.

The DC_UPDATE frame is shown in Figure 22.

The master request CRC[7:5] is calculated as described in CRC-3 for master requests.
The safety byte CRC[7:0] is calculated as described in CRC-8 for safety byte.

The slave response CRC[7:5] is calculated as described in CRC-3 for slave response.

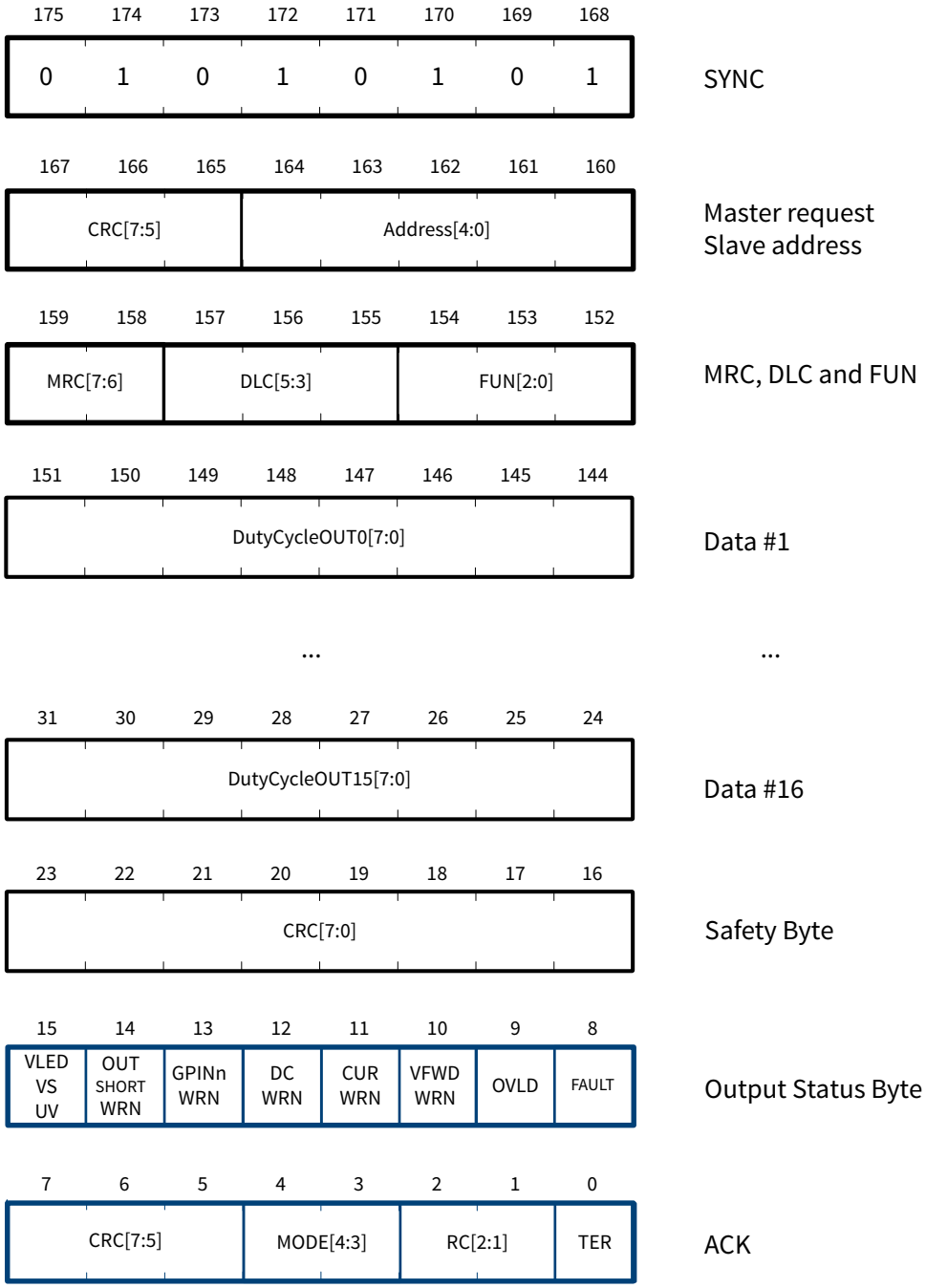


Figure 22 Update duty cycle (DC_UPDATE) for DLC = 0x04

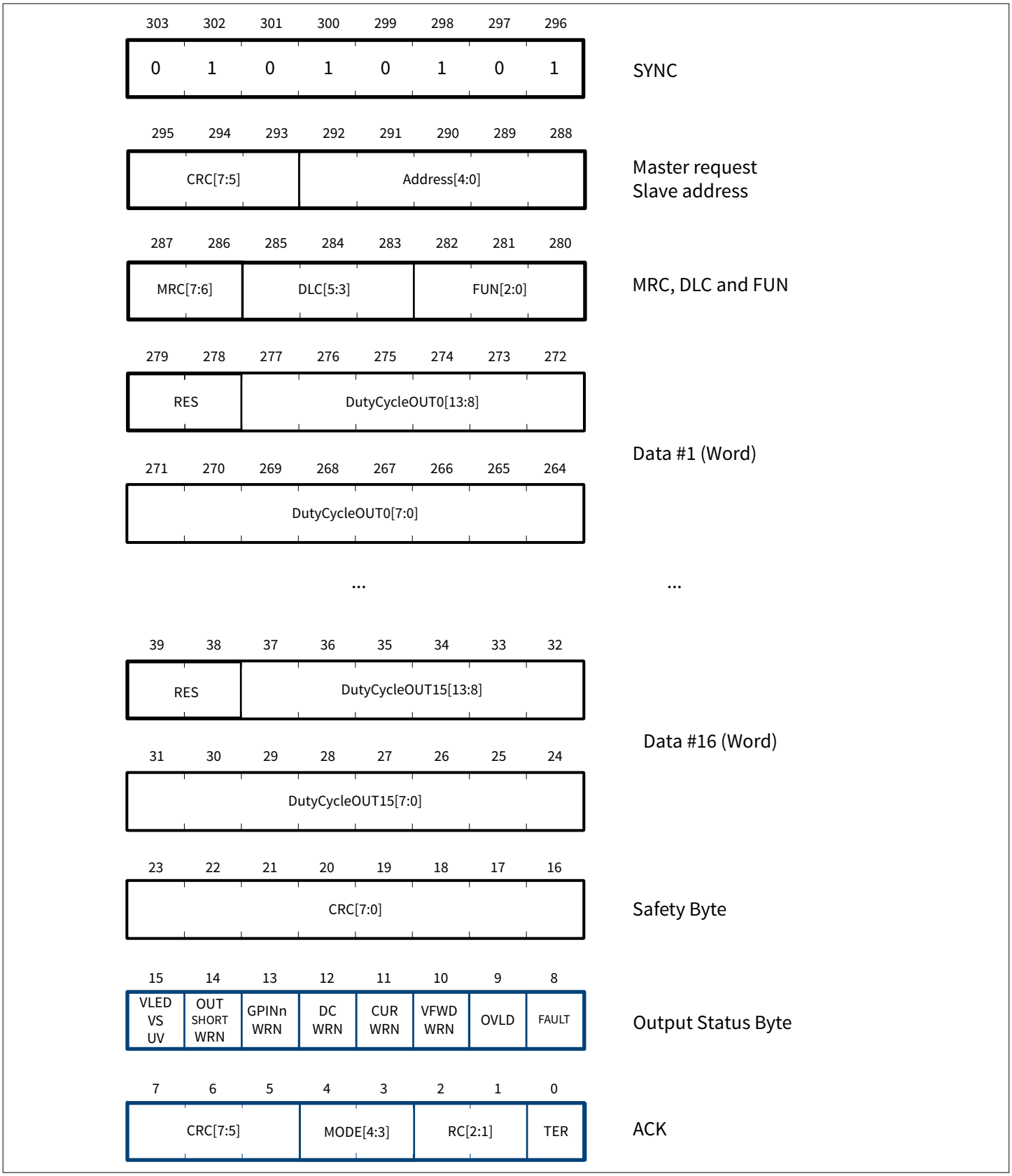


Figure 23 Update duty cycle (DC_UPDATE) for DLC = 0x06

9.1.11.4 READ_OST - request diagnostic

The purpose of this frame is to retrieve the output power stage status (Channel status Byte OUTn) within one master request. The data transfer to the slave is organized in a dedicated write frame containing

- the sync byte, provided by the master,
- the address byte, provided by the master,
- the function (FUN = 0x2) and data length code (DLC = 0x4) information, provided by the master,
- data bytes representing the output stage status, provided by the slave, and the
- safety byte (CRC-8), provided by the slave.

The READ_OST byte frame is shown in Figure 24 and requires following fields to read the Channel Status OUT:

- DLC[5:3] = 0x4 for 8 words respectively 16 bytes
- FUN[2:0] = 0x2

The slave ignores and discards frames in case of an unexpected DLC or FUN data as described in Chapter 9.1.11.10.

The master request CRC[7:5] is calculated as described in CRC-3 for master requests.
The safety byte CRC[7:0] is calculated as described in CRC-8 for safety byte.
The slave response CRC[7:5] is calculated as described in CRC-3 for slave response.

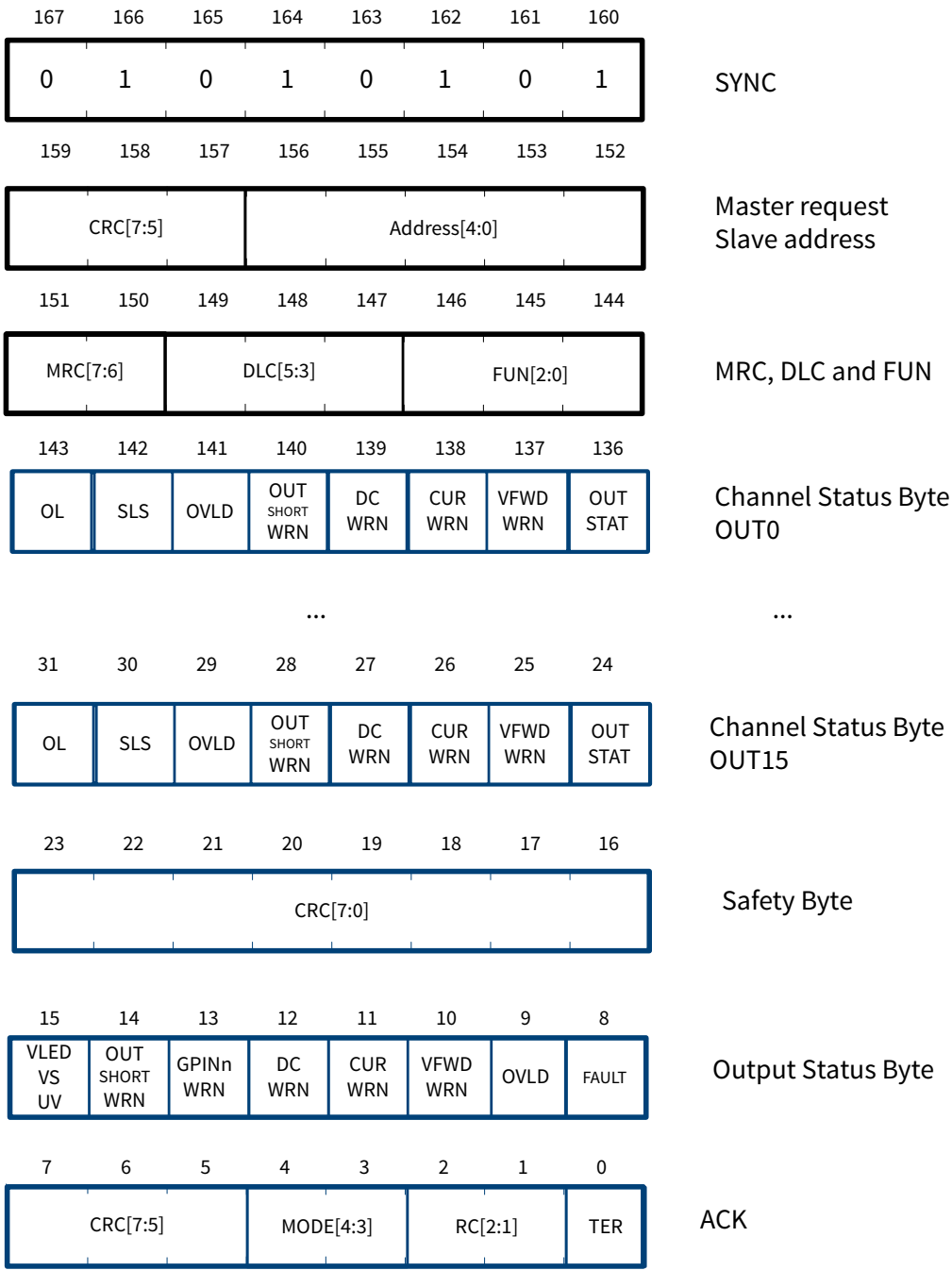


Figure 24 Request diagnostic frame

9.1.11.5 HWCR frame

The purpose of the hardware control frame is to clear the diagnostic flags. The data transfer to the slave is organized in dedicated write frame, containing

- the sync byte, provided by the master
- the address byte, provided by the master
- the MRC_DLC_FUN byte, provided by the master
- the RESET diagnostic words (RESET_OVERLOAD, RESET_OPENLOAD, RESET_SLS, RESET_STATUS), provided by the master
- the safety byte (CRC-8), provided by the master
- the output status byte, provided by the slave and the
- Acknowledge byte (ACK) provided by the slave.

The HWCR frame requires following field configurations:

- DLC[5:3] = 0x3 for 4 words respectively 8 bytes for the reset diagnostic words
- FUN[2:0] = 0x3

The slave response bytes "output status byte and acknowledge byte" are skipped in case the frame is sent to the broadcast address. Consequently there is no response from the slave to the master provided.

The slave ignores and discards frames in case of an unexpected DLC or FUN data as described in Chapter 9.1.11.10.

The HWCR frame requires following field configurations to retrieve diagnostics only:

- DLC[5:3] = 0x0 for output status bytes only
- FUN[2:0] = 0x3

The HWCR frame is shown in Figure 25.

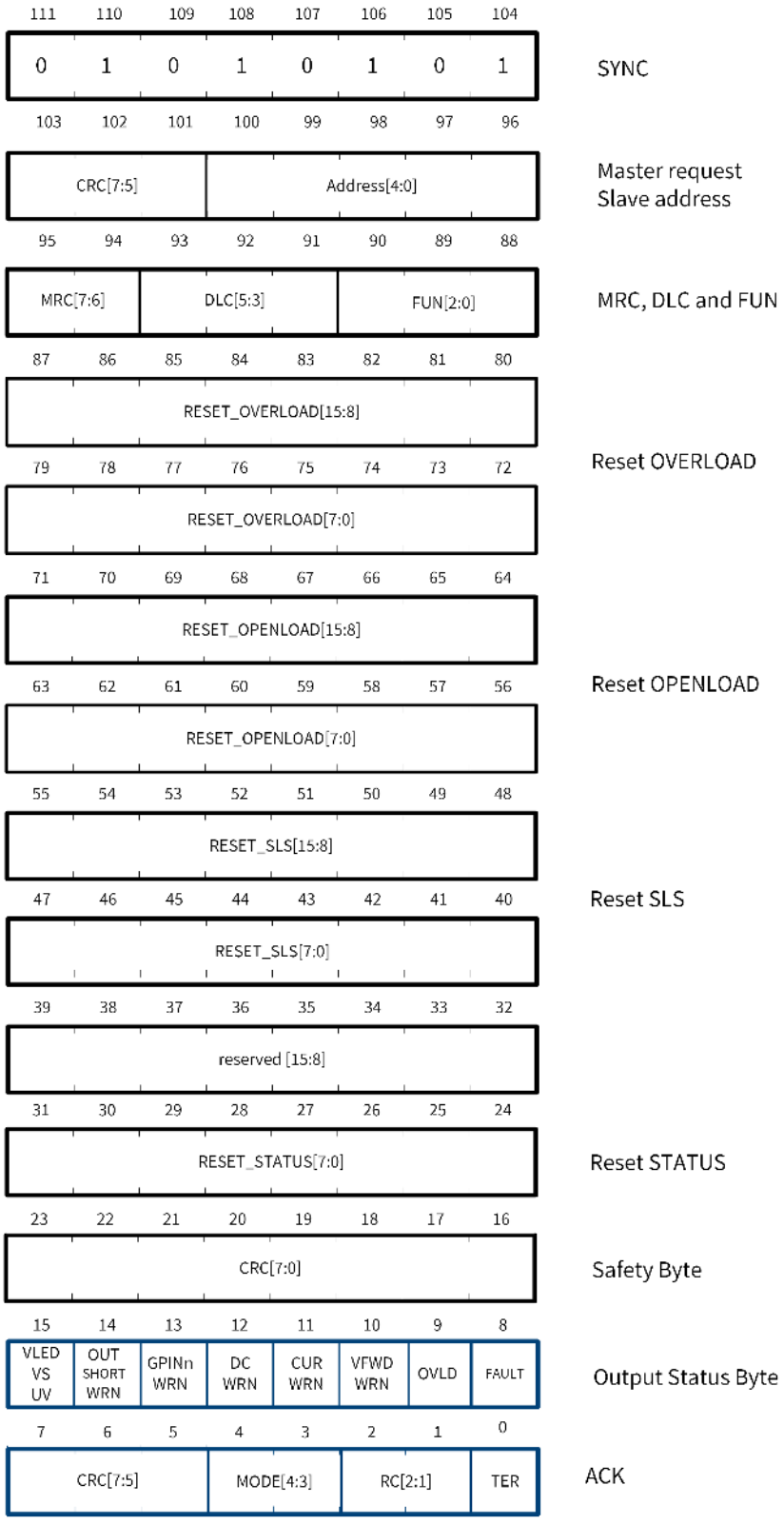


Figure 25 Hardware control frame

9.1.11.6 PM_CHANGE - power mode change

The purpose of the master request frame power mode change is to initiated a transition to the commanded power state. The data transfer to the slave is organized in dedicated write frame, containing

- the sync byte, provided by the master,
- the address byte, provided by the master,
- the MRC_DLC_FUN byte, provided by the master,
- the power mode provided by the master,
- the safety byte (CRC-8), provided by the master,
- the output status byte, provided by the slave and the
- Acknowledge byte (ACK) provided by the slave.

The slave response bytes "output status byte and acknowledge byte" are skipped in case the power mode change is sent to the broadcast address. Consequently there is no response from the slave to the master given in case of the broadcast address contains the power mode change frame.

The PM_CHANGE frame requires following field configurations to perform the power mode change:

- DLC[5:3] = 0x1 for 1 word respectively 2 bytes
- FUN[2:0] = 0x6

The slave ignores and discards frames in case of an unexpected DLC or FUN data as described in Chapter 9.1.11.10.

The master request CRC[7:5] is calculated as described in CRC-3 for master requests.
The safety byte CRC[7:0] is calculated as described in CRC-8 for safety byte.
The slave response CRC[7:5] is calculated as described in CRC-3 for slave response.

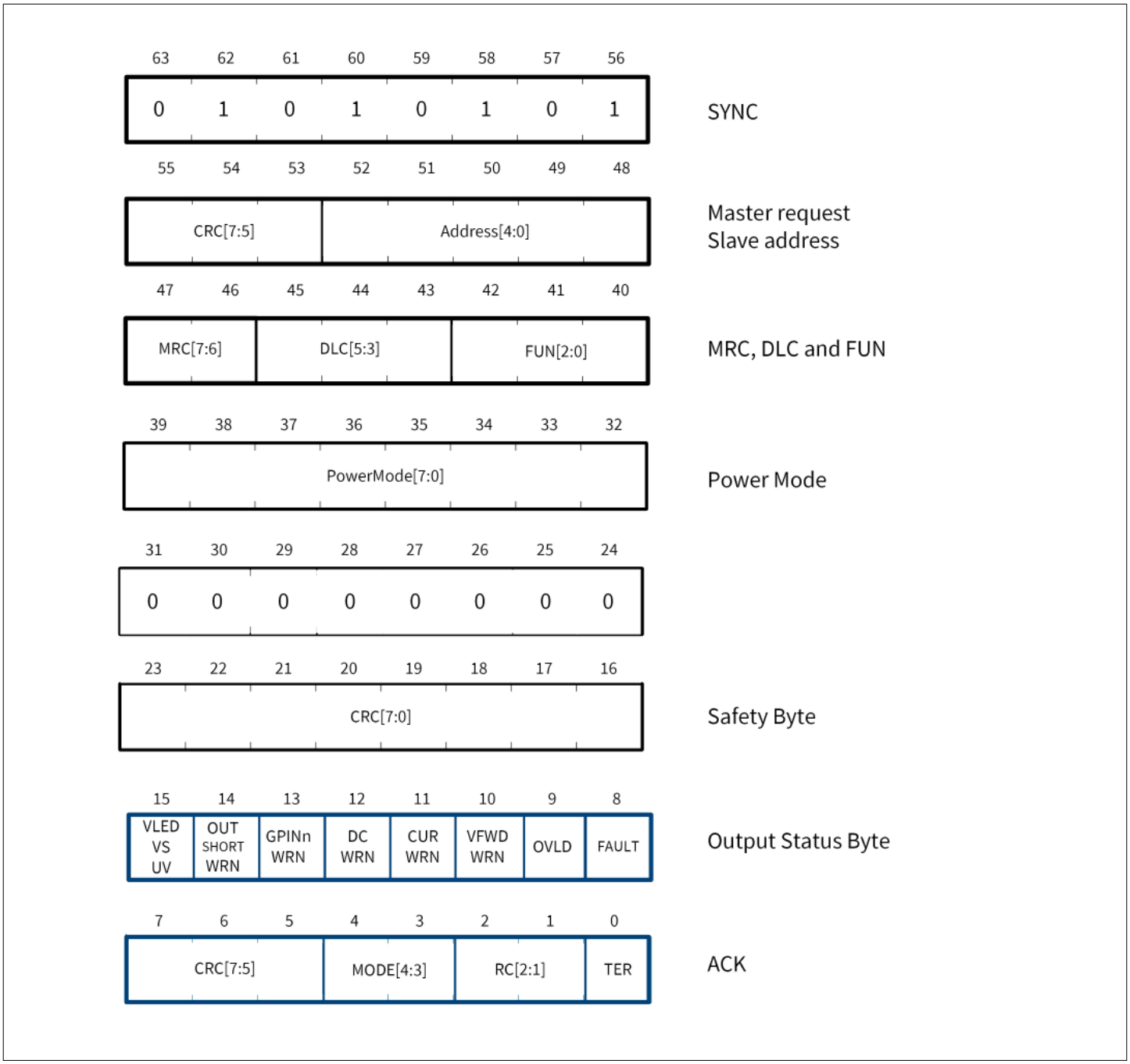


Figure 26 Power mode change frame

9.1.11.7 WRITE_REG - Write register

The purpose of the master request frame write register (WRITE_REG) is to access the devices 16-bit registers.

The data transfer to the slave is organized in dedicated write frame, containing
- the sync byte, provided by the master,
- the address byte, provided by the master,
- the MRC_DLC_FUN byte, provided by the master,
- the start address, provided by the master,
- the data words representing the register content, DLC times provided by the master,
- the safety byte (CRC-8), provided by the master,
- the output status bytes, provided by the slave and the
- Acknowledge byte (ACK) provided by the slave.

The WRITE_REG frame requires following field configurations:
- DLC[5:3] = n > 0, for the number of words
- FUN[2:0] = 0x4

The WRITE_REG frame is shown in Figure 27.

The write register can access consecutive register depending on the start address and DLC.

The master request CRC[7:5] is calculated as described in CRC-3 for master requests.
The safety byte CRC[7:0] is calculated as described in CRC-8 for safety byte.
The slave response CRC[7:5] is calculated as described in CRC-3 for slave response.

Accessing an invalid address, a DLC or FUN error leads to an invalid frame. Consequently the slave reacts as described in Chapter 9.1.11.10.

In case the address byte is 0 (broadcast address), the device does not provide the output status byte and acknowledge byte.

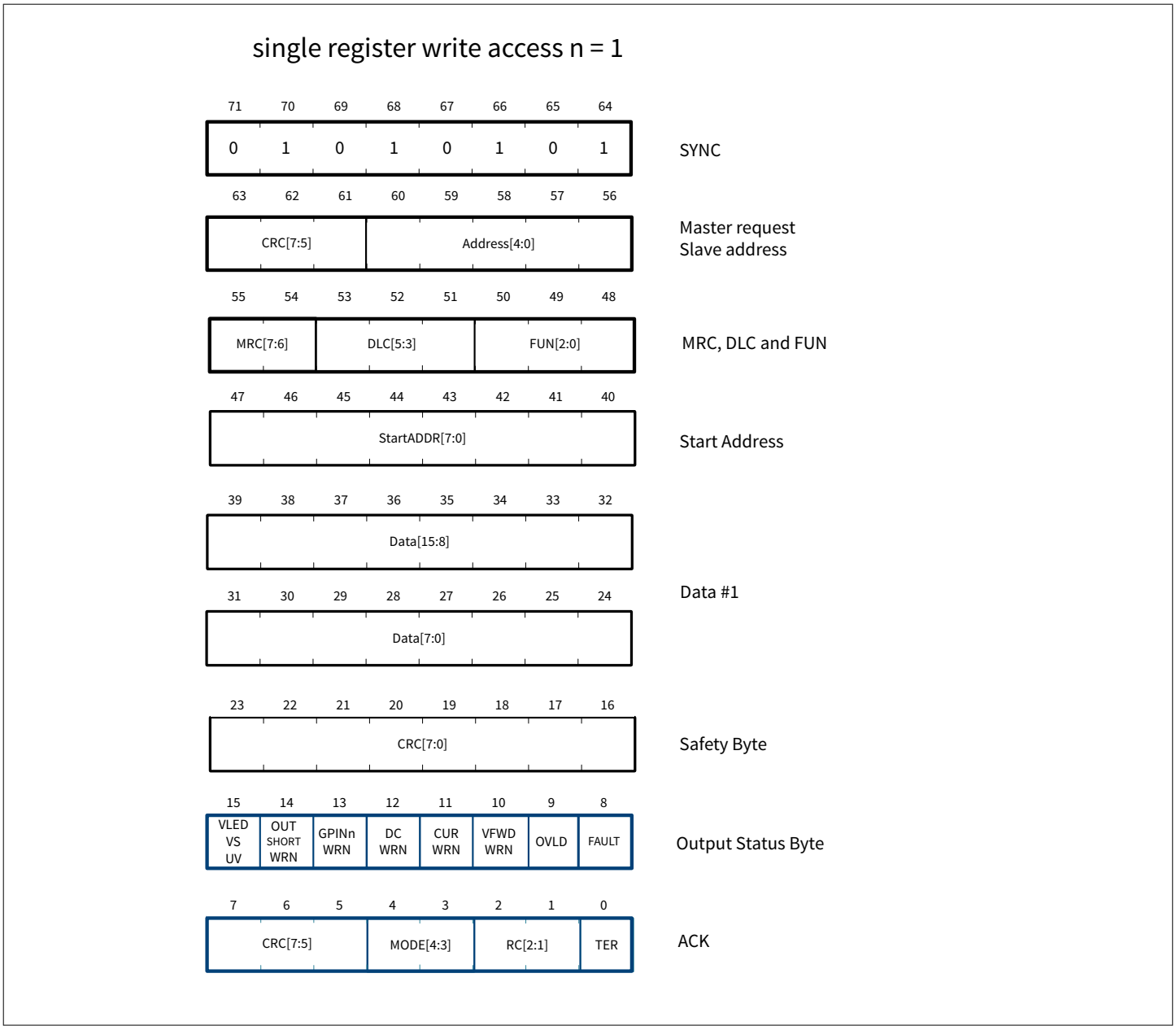


Figure 27 Master request frame - write single register

9.1.11.8 READ_REG - Read register

The purpose of the master request frame read register is to access the devices 16-bit registers.

The data transfer is organized in dedicated frame, containing
- the sync byte, provided by the master
- the address byte, provided by the master
- the MRC_DLC_FUN byte, provided by the master,
- the start address,
- the data words, DLC times words provided by the slave,
- the safety byte (CRC-8), provided by the slave
- the output status bytes, provided by the slave and the
- Acknowledge byte (ACK) provided by the slave.

The READ_REG frame requires following field configurations:
- DLC[5:3] = n > 0, for the number of words
- FUN[2:0] = 0x5

The READ_REG frame is shown in Figure 28.

The read register can access consecutive register depending on the start address and DLC.

Accessing an invalid address, a DLC or FUN error leads to an invalid frame. Consequently the slave reacts as described in Chapter 9.1.11.10.

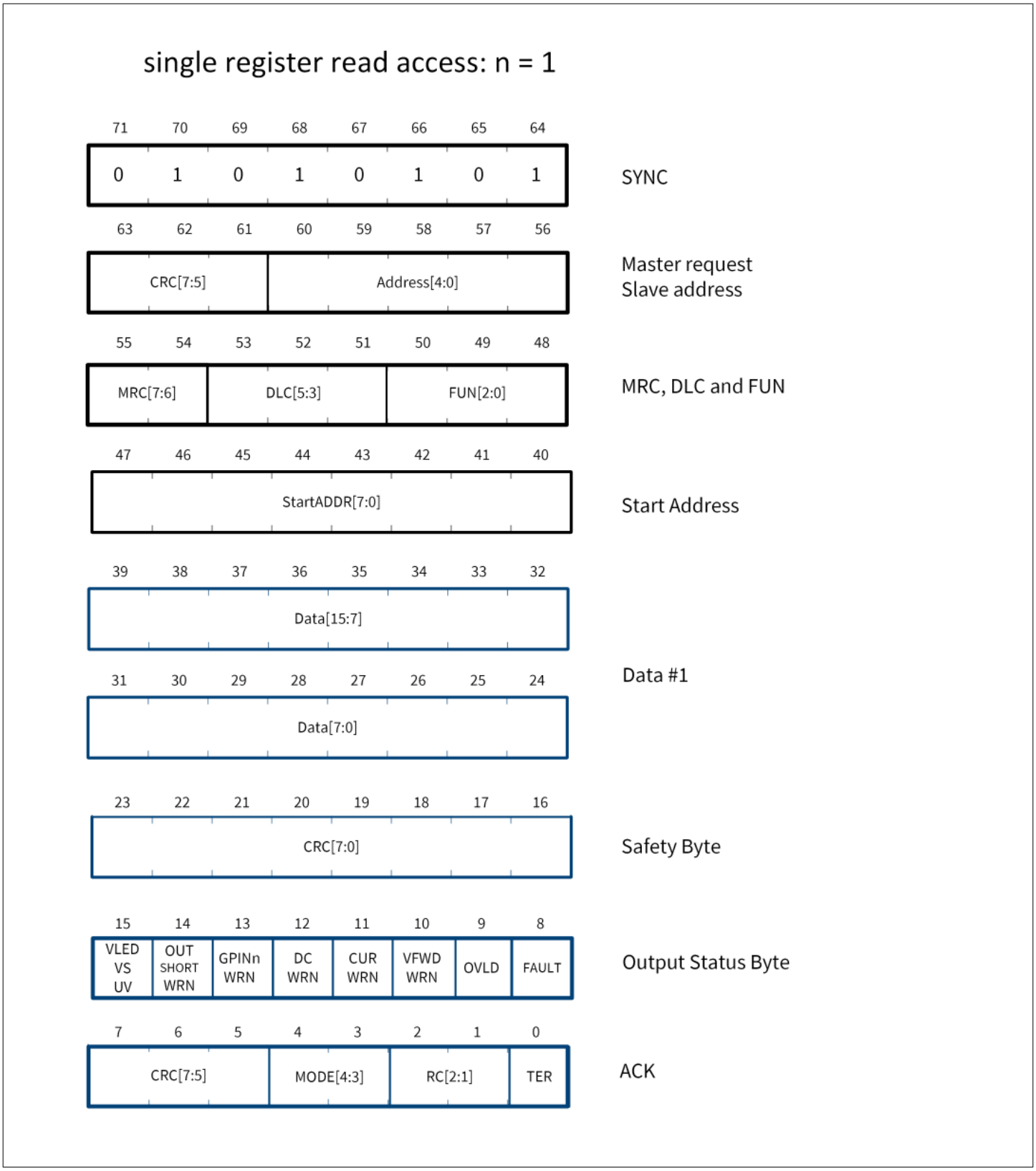


Figure 28 Read single register frame

9.1.11.9 SYNC_BREAK

The LCU can initiate a sync break to reset the protocol handler.

The device detects a sync break if the HSLI bus is dominant ≥ t_{SYNC_BREAK} and then recessive again.
Every received sync break reset signal is counted by the device. The sync break counter is reset on a valid HSLI communication frame.

t_{SYNC_BREAK} can be configured by the OTP according to table below.

Table 31 t_{SYNC_BREAK} configuration

Step	t_{SYNC_BREAK}
0	100 µs
1	250 µs
2	750 µs
3 (default)	1 ms

If the sync break is detected a reset of the protocol handler is initiated where,
- master rolling counter (MRC) and slave rolling counter (RC) is reset to its default value (0) and
- all pending transmissions are interrupted.

If the sync break counter is equal to 6 the slave performs a reset of the devices and enters init mode after $t_{IDLE2INIT}$ time. This reset mechanism is available in init mode, active mode, fail-safe mode and OTP mode

9.1.11.10 Handling of invalid frame requests

The slave can receive invalid request frames from the LCU master. Potential root causes for invalid frames can be
- Programming error at the LCU
- Distorted communication
- Loss of synchronization between slave and LCU causing the interpretation of a data frame as slave request frame.

Following mechanisms are integrated to avoid, detect and report invalid master request frames:
- In case of a valid frame but a CRC-8 error occurred, the slave reports an invalid received frame with ACK.TER = '1' as described.
- In case of an invalid frame or syntax error the slave ignores and discards the received frame.

In case of a CRC-8 error the slave reports an invalid received frame with ACK.TER = '1' . The received frame is discarded and the communication watchdog is not served.

In case of an invalid frame error the slave ignores and discards the received frame and the time out watchdog is not served. No feedback is given to the LCU to prevent further potential bus collision or loss of data frames.

An invalid frame is considered if
- stop bit is low
- unrecognized sync byte
- unspecified register in REG_WRITE or REG_READ frames
- unspecified DLC and FUN combination
- wrong master rolling counter MRC
- CRC-3 for master request error

9.1.11.11 CRC overview

The CRC-3 for master request (CRC[7:5]) in the master request is calculated over the Address[4:0], MRC[7:6], DLC[5:3] and FUN[2:0]. The generator polynom is $x^3 + x + 1$ and the seed is 0x5.

The CRC-3 for slave response (CRC[7:5]) in the slave response is calculated over the output status byte, MODE[4:3], RC[2:1] and TER. The generator polynom is $x^3 + x + 1$ and the seed is 0x5.

The CRC-8 for the safety byte (CRC[7:0]) for the safety byte is defined with the generator polynom according to CRC-8-AUTOSAR and SAE J1850: 0x8e = x^8 +x^4 +x^3 +x^2 +1 and the seed is 0xFF.

The CRC-8 is used in following frames and calculated over dedicated bytes or words :

Frame	Words
DC_UPDATE	DutyDycleOUT0 to DutyCycleOUT15
PM_CHANGE	PowerMode and 0x00
WRITE_REG	StartADDR + Data * DLC
READ_REG	StartADDR + Data * DLC

9.1.11.12 Byte Field Description

9.1.11.12. MASTER_REQ_ADDR 1

The master request address byte comprises the slave address information and a CRC[7:5] bit field to secure the data transmission as shown in Figure 29.

Table 32 Master request byte overview

Field	Bits	Type	Description
Address	[4:0]	w	Slave Address
CRC	[7:5]	w	Cyclic Redundancy Check

The composition of a master request field is shown above. Bits Address[4:0] represent the slave address information and the broadcast address as shown in table below. To avoid an incorrect arbitration of the bus in case of disturbances, the master request frame includes 3-bit CRC[7:5] as described in CRC-3 for master requests.

Table 33 Slave address overview

Slave Address					Function
A4	A3	A2	A1	A0	
0	0	0	0	0	Broadcast
N					Slave n [1..31]

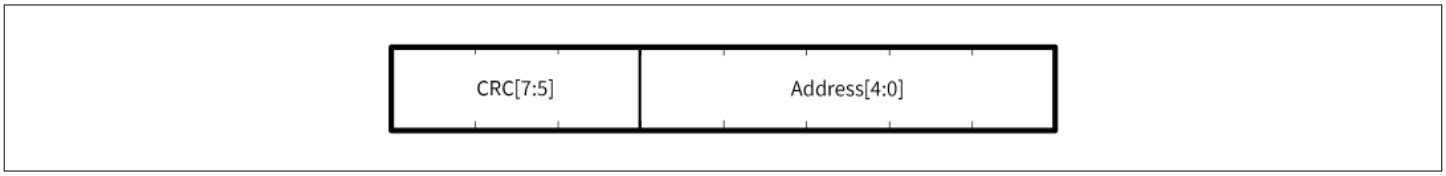


Figure 29 Master request byte to address the slaves

9.1.11.12. DutyCycleOUTn byte 2

The DutyCycleOUTn byte comprises the desired output PWM duty cycle in a compact 8-bit format as shown in DutyCycleOUTn byte. The device converts the 8-bit format to the 14-bit internal hardware duty cycle setting. The relation between the compact 8-bit and the 14-bit representation follows a power law as described in Figure 7 and Chapter 6.4.4.

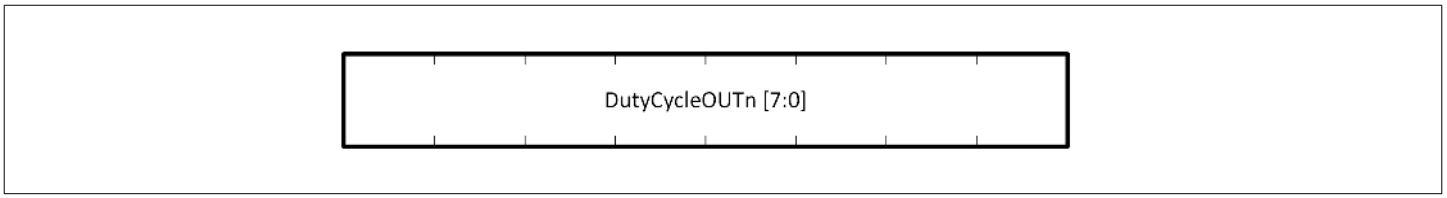


Figure 30 Duty cycle update byte

Table 34 Output conversion result byte overview

Field	Bits	Type	Description
DutyCycleOUTn	[7:0]	w	Desired PWM Duty Cycle for OUTn (n=0..15)

Figure 31 Duty cycle update word

Table 35 Output conversion result byte overview

Field	Bits	Type	Description
DutyCycleOUTn	[13:0]	w	Desired PWM Duty Cycle for OUTn (n=0..15)

9.1.11.12. MRC_DLC_FUN byte 3

The MRC_DLC_FUN byte comprises the master issued rolling counter, the data length code and the desired function as shown in Figure 32.

The composition of a function request and data length code byte is shown in the table below.

Table 36 Master request byte overview

Field	Bits	Type	Description
MRC	[7:6]	w	Rolling Counter, 2 bit counter value, master needs to increment in every data transmission 0x00 default (start) value
DLC	[5:3]	w	Data Length Code
FUN	[2:0]	w	Function

The bits DLC[5:3] represent the data length code and is defined as shown in the next table.

Table 37 DLC field overview

DLC - Data Length Code			data length in words - multiple of 2 bytes
D2	D1	D0	
0	0	0	0 words, 0 bytes
0	0	1	1 word, 2 bytes
0	1	0	2 words, 4 bytes
0	1	1	4 words, 8 bytes
1	0	0	8 words, 16 bytes
1	0	1	12 words, 24 bytes
1	1	0	16 words, 32 bytes
1	1	1	32 words, 64 bytes

The bits FUN[2:0] represent the desired function request as listed in the table below.

Table 38 Function request field overview

Function bits			Function
F2	F1	F0	
0	0	0	Broadcast duty cycle synchronization
0	0	1	Duty cycle shadow register update
0	1	0	Request diagnostics
0	1	1	Hardware control frame
1	0	0	Write register
1	0	1	Read register
1	1	0	Power mode change
1	1	1	Reserved

The device increments the 2-bit master rolling counter MRC counter on every received valid master request frame despite the address field.

A MRC fail is detected if there is a mismatch between the received MRC and the internal MRC counter.

The internal MRC counter is loaded after a mismatch condition with the received MRC.

In case of an reset condition the MRC counter default value is set to 0.

Figure 32 Master rolling counter, function request and data length code byte

9.1.11.12. StartADDR byte 4

The start address byte is used for writing or reading up to 32 consecutive register locations starting from the defined start address register in a single command as shown in Figure 33. The number of successive write or read events is defined with the DLC.

Table 39 Start address byte overview

Field	Bits	Type	Description
Start Address	[7:0]	w	Single byte start address for the 16-bit register write or read operation

Figure 33 Start address byte

9.1.11.12. Data Word 5

The two data bytes comprises the downloaded data from the master to the slave or the responded feedback from the slave to the master as shown in Figure 34.

Table 40 Data word - word structure overview

Field	Bits	Type	Description
Data	**[15:8]**	**w/r**	**Data** Contains the MSB(byte) of the data to written to the slave or read from the master
Data	**[7:0]**	**w/r**	**Data** Contains the LSB(byte) of the data to written to the slave or read from the master

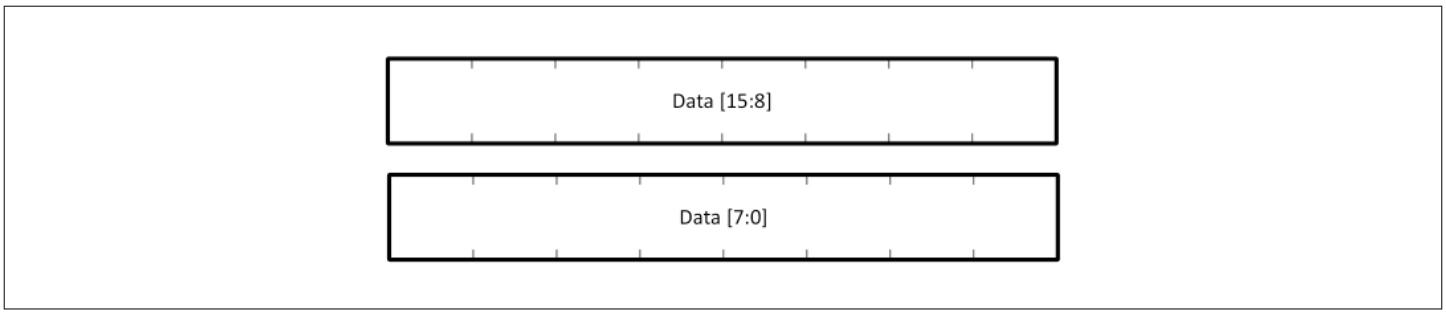


Figure 34 Data word

9.1.11.12. Power Mode 6

The master power mode change byte comprises the commanded power mode state as shown in Figure 35.

Table 41 Power mode byte overview

Field	Bits	Type	Description
Power Mode	[2:0]	w	Power mode 000 ... enter_init_mode 001 ... reserved 010 ... enter_fail-safe 011 ... enter_OTP_mode 1xx ... reserved
reserved	[7:3]	w	–

Figure 35 Power mode byte

9.1.11.12. Output Status Byte 7

The output status byte comprises the status overview for all power output channels and is shown in Figure 36.
The bit fields are described below, further details are available in the safety and user manuals.

Table 42 Bit field description

Field	Bits	Type	Description
VLED_VS_UV	7	r	**VLED/VS under voltage flag** 0 ... if (V_{LED} AND V_S) is above VDEN_threshold 1 ... there was at least one under voltage condition event detected

(table continues...)

Table 42 (continued) Bit field description

Field	Bits	Type	Description
OUT_SHORT_WRN	6	r	**short between adjacent output warning** 0 .. no short between adjacent output warning detected 1 .. there was at least one short between an adjacent output warning detected
GPINn_WRN	5	r	**GPINn warning flag** 0 ... GPIN0 and GPIN1 are not in a fault condition 1 ... there was at least one GPINn fault condition
DC_WRN	4	r	**Duty cycle warning flag** 0 ... no duty cycle warning for OUT0 to OUT15 detected 1 ... there was at least one duty cycle warning condition
CUR_WRN	3	r	**Output current warning flag** 0 ... no output current warning for OUT0 to OUT15 detected 1 ... there was at least one output current warning condition
VFWD_WRN	2	r	**Forward voltage warning flag** 0 ... no forward voltage warning for OUT0 to OUT15 detected 1 ... there was at least one forward voltage warning condition
OVLD	1	r	**Over load flag** 0 ... no thermal overload condition detected on OUT0 to OUT15 1 ... there was at least one thermal overload condition detected
Fault	0	r	**Internal fault flag** 0 ... no internal fault detected 1 ... internal fault condition detected

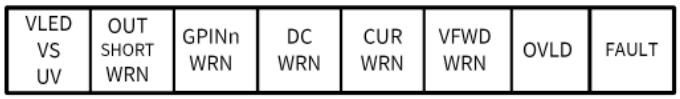


Figure 36 Output status byte

Note: In case of GPIN short condition is detected, the Fault bit is set.

9.1.11.12. Channel status Byte – OUTn

8

The Channel status Byte - OUTn comprises the status overview for a single power output channel OUTn and is shown in Figure 37.

The bit fields are described below, where the warning conditions are described in Chapter 7.10 and in the safety manual

Table 43 Bit field description

Field	Bits	Type	Description
OL	7	r	**Open load flag** 0 ... no open load condition detected 1 ... there was at least one open load condition detected
SLS	6	r	**Single LED Short (SLS) flag** 0 .. no SLS condition detected 1 .. there was at least one single LED short detected
OVLD	5	r	**OVLD flag** 0 ... no thermal overload condition detected 1 ... there was at least one thermal overload condition detected
OUT_SHORT_WRN	4	r	**short between adjacent output warning flag** 0 .. no short between adjacent output warning detected 1 .. there was at least one short between an adjacent output warning detected
DC_WRN	3	r	**Duty cycle warning flag** 0 ... no duty cycle warning detected 1 ... there was at least one duty cycle warning condition detected
CUR_WRN	2	r	**Output current warning flag** 0 ... no output current warning detected 1 ... there was at least one output current warning condition detected
VFWD_WRN	1	r	**Forward voltage warning flag** 0 ... no forward voltage warning detected 1 ... there was at least one forward voltage warning condition detected
OUT_STAT	0	r	**Output state flag** 0 ... power output channel is in ON state or device in INIT mode 1 ... power output channel is in OFF state

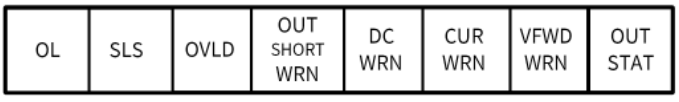


Figure 37 Channel status Byte - OUTn

Note: The output state flag (OUT_STAT) reports an on-state ("0") in case of a duty cycle ≥ 6.25% and no fault occured. In case of a duty cycle set to 0%, the output state flag reports off-state ("1") and no fault occured. In case of a duty cycle >0% and < 6.25% the output state flag reports either on-state or off-state.

OUT_STAT reports the proper status of the channel with a delay of 2 PWM after the duty cycle update (DC_UPDATE+DC_SYNC)

9.1.11.12. RESET diagnostic words 9

The two bytes comprise reset request for the reported thermal overload condition for each output channel.

Table 44 RESET_OVERLOAD word - structure overview

Field	Bits	Type	Description
RESET_OVERLOAD	**[15:8]**	**w**	**Reset OVERLOAD flag** Contains the MSB(byte) for the reset thermal overload request. The bit RESET_OVERLOAD[n] is mapped to fault flag reported for OUTn .
RESET_OVERLOAD	**[7:0]**	**w**	**Reset OVERLOAD flag** Contains the LSB(byte) for the reset thermal overload request. The bit RESET_OVERLOAD[n] is mapped to fault flag reported for OUTn.

The two bytes comprise reset request for the reported open load condition for each output channel.

Table 45 RESET_OPENLOAD word - structure overview

RESET_OPENLOAD	**[15:8]**	**w**	**Reset OPENLOAD flag** Contains the MSB(byte) for the reset open load request. The bit RESET_OPENLOAD[n] is mapped to fault flag reported for OUTn.
RESET_OPENLOAD	**[7:0]**	**w**	**Reset OPENLOAD flag** Contains the LSB(byte) for the reset open load request. The bit RESET_OPENLOAD[n] is mapped to fault flag reported for OUTn.

The two bytes comprise reset request for the reported SLS condition for each output channel.

Table 46 RESET_SLS word - structure overview

Field	Bits	Type	Description
RESET_SLS	**[15:8]**	**w**	**Reset SLS flag** Contains the MSB(byte) for the reset SLS request. The bit RESET_SLS[n] is mapped to the fault flag reported for OUTn.
RESET_SLS	**[7:0]**	**w**	**Reset SLS flag** Contains the LSB(byte) for the reset SLS request. The bit RESET_SLS[n] is mapped to the fault flag reported for OUTn.

The byte comprises the reset request for the reported status conditions for the device.

Table 47 RESET_STATUS - structure overview

Field	Bits	Type	Description
RESET_VLED_VS_UV	**[7]**	**w**	**Reset VLED_VS_UV flag** Resets the VLED_VS_UV flag.
RESET_OUT_SHORT_WRN	**[6]**	**w**	**Reset OUT_SHORT_WRN** Resets the OUT_SHORT_WRN flag.
RESET_GPINn_WRN	**[5]**	**w**	**Reset GPINn_WRN** Resets the GPINn_WRN flag.

(table continues...)

Table 47 (continued) RESET_STATUS - structure overview

Field	Bits	Type	Description
RESET_DC_WRN	**[4]**	**w**	**Reset DC_WRN** Resets the DC_WRN flag.
RESET_CUR_WRN	**[3]**	**w**	**Reset CUR_WRN** Resets the CUR_WRN flag.
RESET_VFWD_WRN	**[2]**	**w**	**Reset VFWD_WRN** Resets the VFWD_WRN flag.
RESERVED	**[1]**	**w**	Reserved
RESET_FAULT	**[0]**	**w**	**Reset FAULT** Resets the FAULT flag.

9.1.11.12. ACK byte 10

The device increments the 2-bit slave rolling counter RC counter on every sent response frame.
In case of an reset condition the RC counter default value is set to 0.
The ACK byte comprises the response to the master including diagnostic feedback as shown in Figure 38.

Table 48 ACK byte - structure overview

Field	Bits	Type	Description
CRC	[7:5]	r	**CRC**, details see CRC-3 for slave response
MODE	[4:3]	r	**MODE**, power mode state 00 ... init mode 01 ... active mode 10 ... fail-safe mode 11 ... programming or emulation mode
RC	[2:1]	r	rolling counter, incremented every slave response
TER	[0]	r	**TER** 0 ... current frame has been successfully received 1 ... the received frame resulted in a CRC-8 error

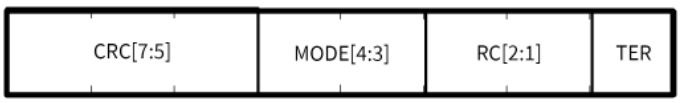


Figure 38 slave ACK byte

9.2 Physical layer

9.2.1 CAN-FD compliance

The integrated CAN transceiver is electrically compliant to ISO11898-2:2016 and CAN FD up to 2 Mbit/s.

9.2.2 Transceiver block diagram

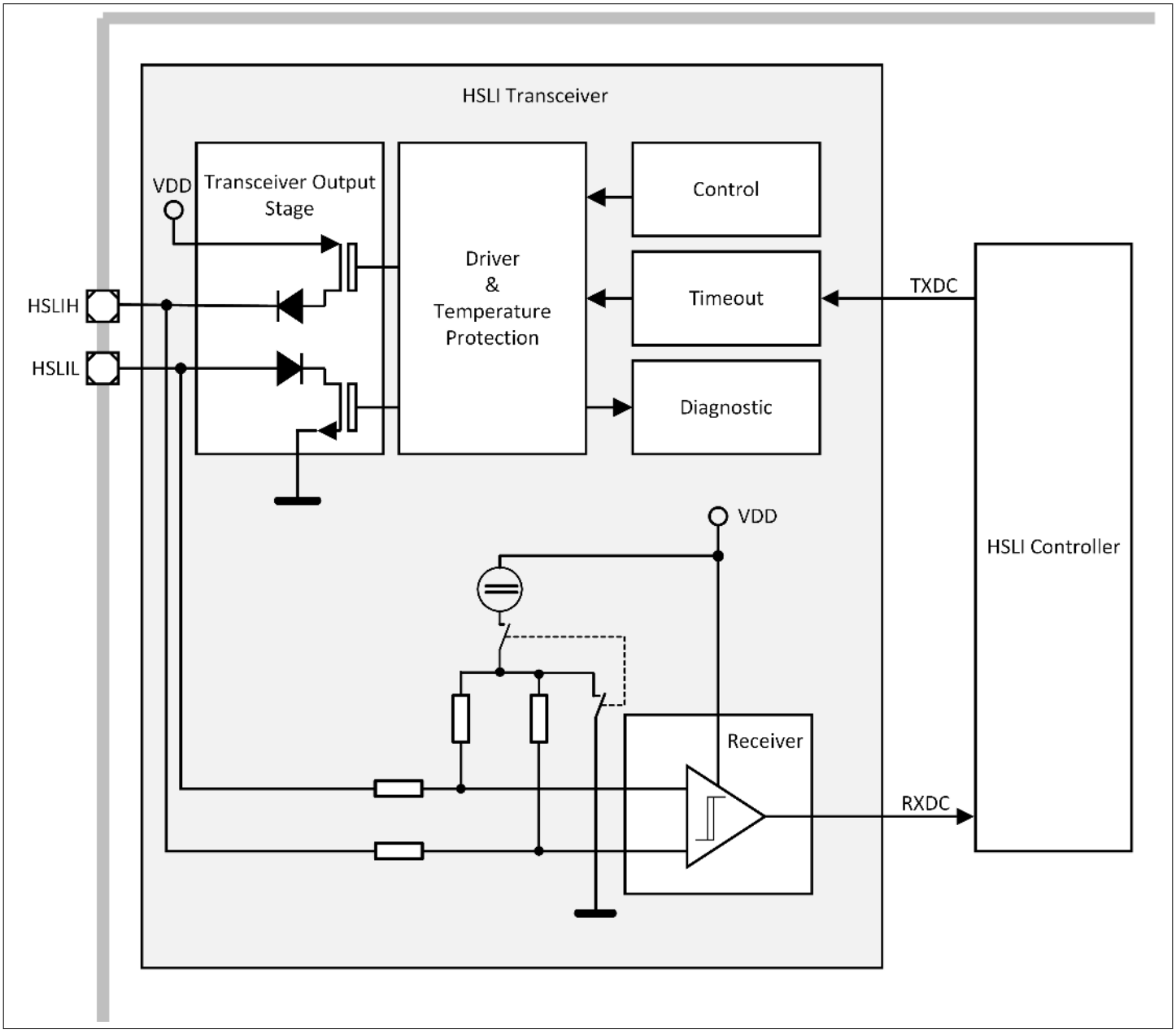


Figure 39 Functional block diagram

9.2.3 Electrical characteristics

Table 49 Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
HSLI bus receiver							
Differential receiver: threshold voltage, recessive to dominant edge	$V_{diff\_rd(active)}$	–	0.8	0.9	V	$V_{diff} = V_{HSLIH} - V_{HSLIL}$; - 12 V < $V_{CM(HSLI)}$ < 12 V; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-504
Differential receiver: threshold voltage, dominant to recessive edge	$V_{diff\_dr(active)}$	0.5	0.6	–	V	$V_{diff} = V_{HSLIH} - V_{HSLIL}$; - 12 V < $V_{CM(HSLI)}$ < 12 V; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-505
Common mode range	CMR	-12	–	12	V	–	PRQ-506
HSLIH, HSLIL input resistance	R_i	20	40	50	kΩ	Recessive state	PRQ-507
Differential input resistance	R_{diff}	40	80	100	kΩ	Recessive state	PRQ-508
Input resistance deviation between HSLIH and HSLIL	DR_i	-3	–	3	%	Recessive state, Not subject to production test - specified by design	PRQ-509
Input capacitance HSLIH, HSLIL versus GND	C_i	–	20	40	pF	–	PRQ-510
HSLI bus transmitter							
HSLIH/HSLIL recessive output voltage	$V_{HSLIH/L(active)}$	2.0	–	3.0	V	init mode, active mode, fail-safe mode, OTP programming and emulation modes; no load	PRQ-511
HSLIH/HSLIL recessive output voltage difference	$V_{diff\_r(active)}$	-500	–	50	mV	$V_{diff} = V_{HSLIH} - V_{HSLIL}$; init mode, active mode, fail-safe mode, OTP programming and emulation modes; no load	PRQ-513

(table continues...)

Table 49 (continued) Electrical Characteristics

V_S = 6 V to 20 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive currents flowing as described in Figure 2 (unless otherwise specified). Typical values: V_S = 9 V, T_J = 25°C

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
HSLIL dominant output voltage	V_{HSLIL}	0.5	–	2.25	V	VDD = 5 V, 50 Ω < R < 65 Ω; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-515
HSLIH dominant output voltage	V_{HSLIH}	2.75	–	4.5	V	VDD = 5V, 50 Ω < R < 65 Ω; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-516
HSLIH dominant output voltage difference	$V_{diff\_d(active)}$	1.5	–	3.0	V	Vdiff = VHSLIH - VHSLIL, VDD = 5V, 50 Ω < R < 65 Ω; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-517
Driver symmetry	V_{SYM}	4.5	–	5.5	V	V_{DD} = 5 V; 50 Ω < R < 65 Ω; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-518
HSLIH short circuit current	$HSLIH_{SC}$	-100	-80	-50	mA	$V_{HSLIHshort}$ = 0 V; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-519
HSLIL short circuit current	$HSLIL_{SC}$	50	80	100	mA	$V_{HSLILshort}$ ≤ 18 V; init mode, active mode, fail-safe mode, OTP programming and emulation modes	PRQ-520
HSLIH leakage current	$HSLIH_{(leak)}$	–	5	7.5	µA	idle mode; 0 V ≤ V_{HSLIH} < 5 V;	PRQ-521
HSLIL leakage current	$HSLIL_{(leak)}$	–	5	7.5	µA	idle mode; 0 V ≤ V_{HSLIL} < 5 V;	PRQ-522

10 Application Information

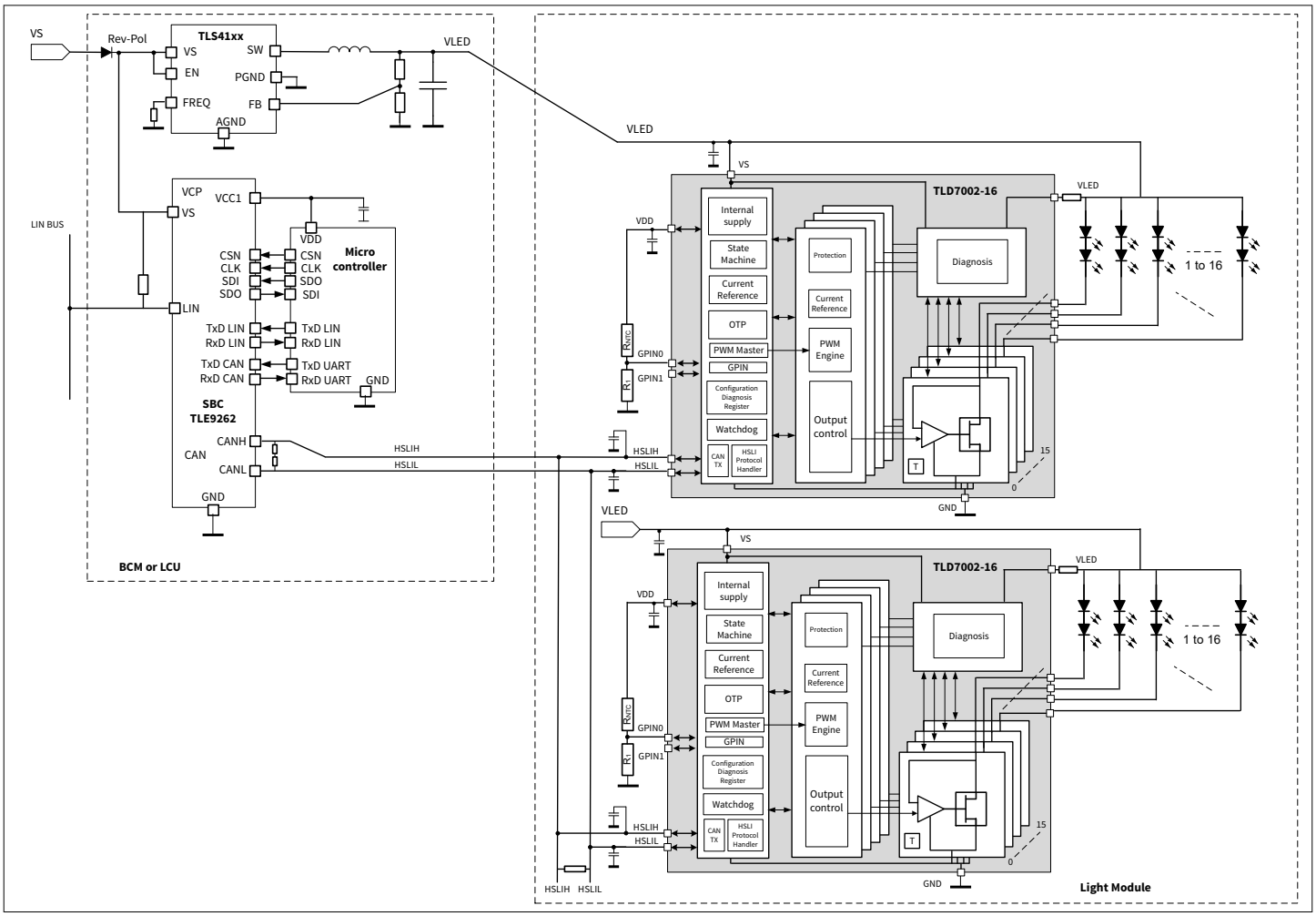
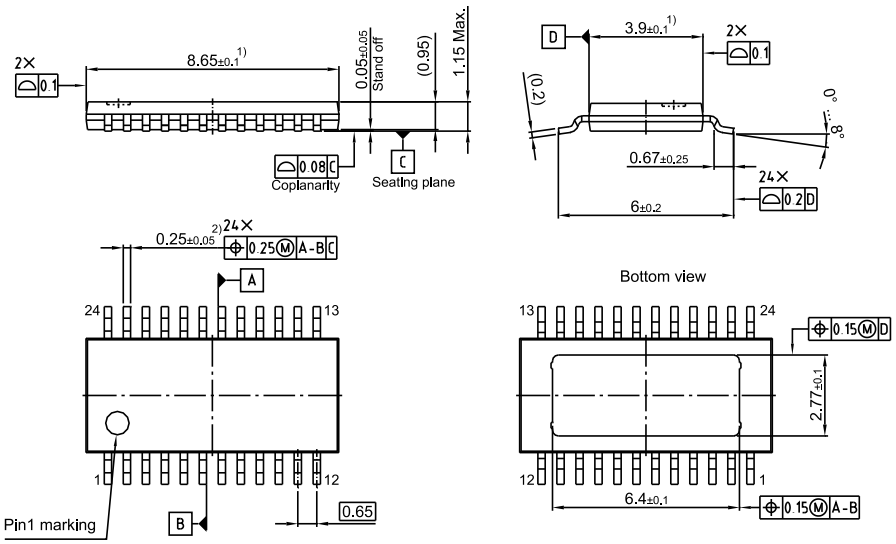


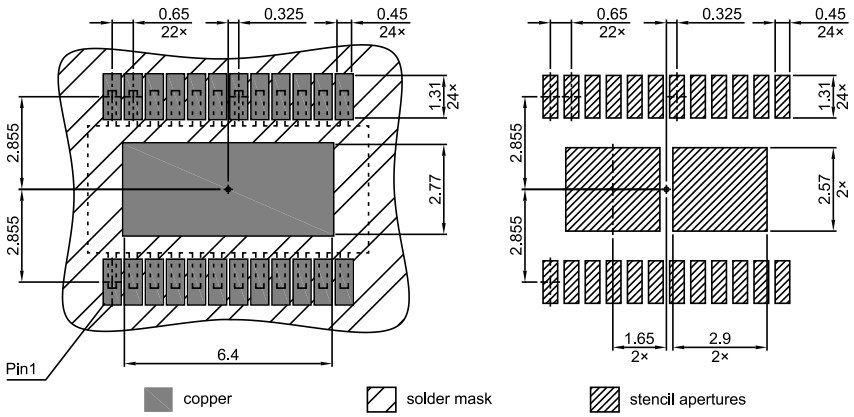
Figure 40 Application diagram

11 Package dimensions



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊕]
Drawing according to ISO 8015, general tolerances ISO 2768-mk

Figure 41 PG-TSDSO-24 package outline



All dimensions are in units mm

Figure 42 PG-TSDSO-24 package pads and stencil

Note: ***Green product (RoHS compliant)***

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).
For further information on packages, please visit our website: https://www.infineon.com/packages

Revision history

Document version	Date of release	Description of changes
Rev.1.00	2022-05-03	• Initial Datasheet

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