Evaluation Board User Guide
UG-591

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Evaluating the ADP5134 Micropower Management Unit (PMU)

FEATURES

Full-featured evaluation board for the ADP5134
Standalone capability
Simple device measurements, including line and load regulation, demonstrable with
- **A single voltage supply**
- **A voltmeter**
- **An ammeter**
- **Load resistors**

Easy access to external components
Cascading options to supply the low dropout (LDO) from BUCK1 or BUCK2
Dedicated precision enable option on each channel for easier power sequencing
Factory programmable soft start options
Factory programmable UVLO options
Power good pin for monitoring
Mode option to change bucks from PFM to PWM operation

GENERAL DESCRIPTION

This user guide describes the hardware for the evaluation of the ADP5134 and includes detailed schematics and PCB layouts. The ADP5134 is available in a 24-lead 4 mm × 4 mm LFCSP package.

The ADP5134 LFCSP evaluation board has two step-down regulators with two LDOs that enable evaluation of the ADP5134. The evaluation board is available with an adjustable voltage option.

Full details on the parts are provided in the ADP5134 data sheet, which should be consulted in conjunction with this evaluation board user guide.

ADP5134 EVALUATION BOARD

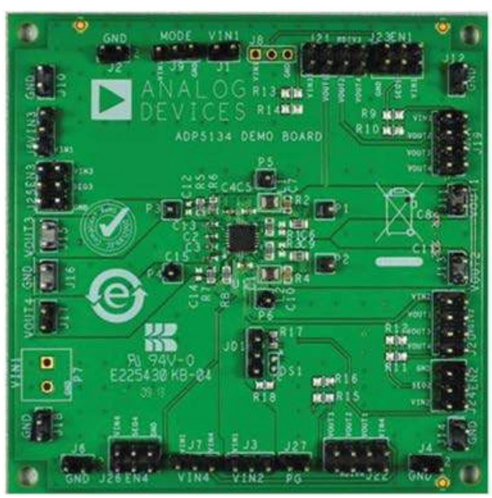

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Figure 1.

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REVISION HISTORY

11/13—Revision 0: Initial Version

SETTING UP THE HARDWARE

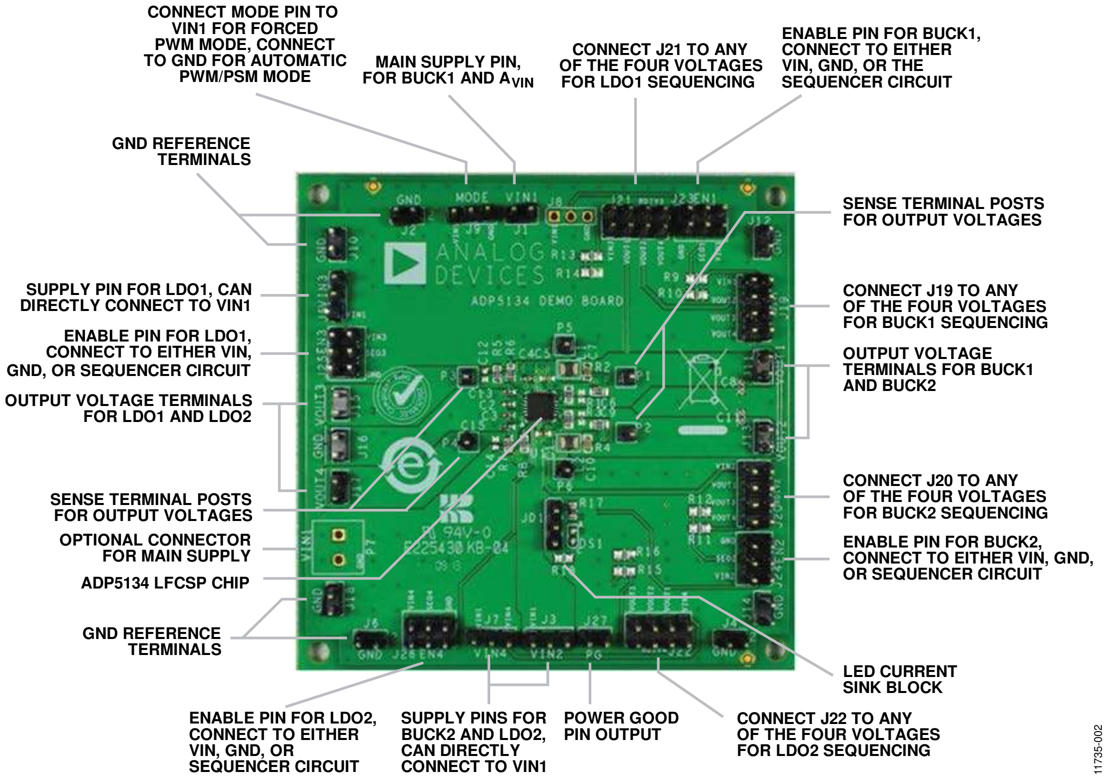


Figure 2. Evaluation Board Overview

The ADP5134 evaluation board is supplied fully assembled and tested.

Before applying power to the evaluation board, follow the procedures in this section.

ENABLE

Each channel has its own enable pin, which must be pulled high to enable that channel (see Table 1).

Table 1. Channels of the Enable Pins

Channel	Enable Pin
1	J23
2	J24
3	J25
4	J26

JUMPER J9 (MODE)

The Jumper J9, as shown in Figure 2, is used to connect the MODE pin of the device to either ground or VIN1. To force BUCK1 and BUCK2 into forced PWM operation, shunt the center contact of Jumper J9 (MODE) to the left pin header to pull the MODE pin high to VIN1. To allow BUCK1 and BUCK2 to operate in automatic PWM/PSM operation, shunt the center contact of J9 (MODE) to the right pin header to pull the MODE pin low to GND1.

INPUT POWER SOURCE

If the input power source includes a current meter, use that meter to monitor the input current. The board allows easy connection of all power supply pins to the main power source (VIN1).

To do this, shunt the center contact of Jumper J3 (VIN2) to the left pin header to connect VIN2 to VIN1. Then, shunt Jumper J5 to connect VIN3 to VIN1. You can also shunt Jumper J7 to connect VIN4 to VIN1.

Connect the positive terminal of the power source to J1 (VIN1) on the evaluation board and the negative terminal of the power source to J2 (GND).

If the power source does not include a current meter, connect a current meter in series with the input source voltage. Connect the positive lead (+) of the power source to the ammeter positive (+) connection, the negative lead (−) of the power source to J2 (GND) on the evaluation board, and the negative lead (−) of the ammeter to J1 (VIN1) on the board. Be aware that the current meters add resistance to the input source, and this voltage reduces with high output currents.

OUTPUT LOAD

Connect an electronic load or resistor to set the load current. If the load includes an ammeter, or if the current is not measured, connect the load directly to the evaluation board, with the positive (+) load connected to one of the channels. For example, connect BUCK1, J11 (VOUT1), and the negative (−) load connection to J12 (GND)

If an ammeter is used, connect it in series with the load. Connect the positive (+) ammeter terminal to the evaluation board for BUCK1, J11 (VOUT1), the negative (−) ammeter terminal to the positive (+) load terminal, and the negative (−) load terminal to the evaluation board at J12 (GND).

INPUT AND OUTPUT VOLTMETERS

Measure the input and output voltages with voltmeters. Make sure that the voltmeters are connected to the appropriate evaluation board terminals and not to the load or power sources themselves.

If the voltmeters are not connected directly to the evaluation board, the measured voltages will be incorrect due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

Connect the input voltage measuring voltmeter positive terminal (+) to the evaluation board at J1 (VIN1), and input voltage measuring voltmeter negative (−) terminal to the evaluation board at J2 (GND).

Connect the output voltage measuring voltmeter positive (+) terminal to the evaluation board at P1 (VOUT1) for measuring the output voltage of BUCK1, and the output voltage measuring voltmeter negative (−) terminal to the evaluation board at J12 (GND).

POWERING UP THE EVALUATION BOARD

When the power source and load are connected to the evaluation board, the board can be powered for operation.

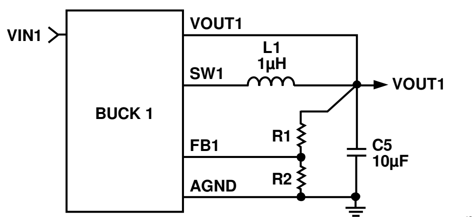
Before doing so, ensure that

- The power source voltage for the bucks (VIN1, VIN2) is >2.5 V to <5.5 V.
- The power source voltage for the LDOs (VIN3, VIN4) is from V_{OUT} LDO + 0.5 V or 1.7 V (whichever is greater) to 5.5 V.
- The desired channel is enabled and monitors the output voltage.

If the load is not enabled, enable the load; check that it is drawing the proper current and that the output voltage maintains voltage regulation.

SETTING THE OUTPUT VOLTAGE OF THE BUCKS

The buck output voltage is set through external resistor dividers shown in Figure 3 for BUCK1. Optionally, the output voltage can be factory programmed to default values as indicated in the data sheet. In this event, R1 and R2 are not needed, and FB1 can be left unconnected. In all cases, VOUT1 must be connected to the output capacitor. FB1 is 0.5 V.

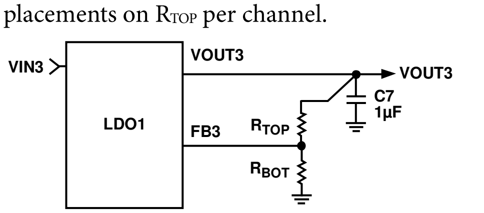


$$V_{OUT1} = V_{FB1}\left(\frac{R1}{R2} + 1\right)$$

Figure 3. BUCK1 External Output Voltage Setting

SETTING THE OUTPUT VOLTAGE OF THE LDOS

Each LDO output voltage is set through external resistor dividers as shown in Figure 4 for LDO1. Optionally, the output voltage can be factory programmed to default values as indicated in the data sheet. In this event, FB3 must be connected to the top of the capacitor on VOUT3 by placing a 0 Ω resistor on R_{TOP}, and leaving R_{BOT} unpopulated. Refer to Table 2 for the corresponding 0 Ω resistor placements on R_{TOP} per channel.



$$V_{OUT3} = V_{FB3}\left(\frac{R_{TOP}}{R_{BOT}} + 1\right)$$

Figure 4. LDO1 External Output Voltage Setting

EXTERNAL RESISTOR DIVIDER SETTING FOR BUCKS AND LDOS

The ADP5134 demo boards are supplied with fixed resistors with values chosen for a target output voltage. Varying the resistor values of the resistor divider networks varies the output voltage accordingly.

Table 2. External Resistor Dividers (Fixed)

Resistor Divider	BUCK1	BUCK2	LDO1	LDO2
R_{TOP}	R1	R3	R5	R7
R_{BOT}	R2	R4	R6	R8

REGULATOR SEQUENCING USING EXTERNAL RESISTORS

The ADP5134 demo board also houses sequencing circuits for each of the four regulator channels. These allow the user to dictate which regulator turns On and Off first, and which regulators are triggered in sequence.

Taking BUCK1, for example, and referring to Figure 5, the enable pin (EN1) can be tied to the sequencer circuit (SEQ1) by shunting Pin 3 to Pin 4 of Jumper J23. The pull-up voltage for R9 can be connected to any of the available voltage rails on J19. If the top of R9 (RDIV1) is connected to VOUT2, then BUCK1 is enabled only after BUCK2 output voltage ramps to the desired level.

To allow for regulator sequencing where BUCK1 turns on, followed by BUCK2, then LDO1, and then LDO2, follow these steps:

1. Shunt J23 to VIN1 and leave J19 unconnected to enable BUCK1.
2. Shunt J24 to SEQ2.
3. Shunt RDIV2 to VOUT1 on J20.
4. Shunt J25 to SEQ3.
5. Shunt RDIV3 to VOUT2 on J21.
6. Shunt J26 to SEQ4.
7. Shunt RDIV4 to VOUT3 on J22.

The sequencing resistors, R9 and R10 as shown in Figure 5, should be computed to generate approximately 1.1 V to the ENx pin to go above the enable threshold.

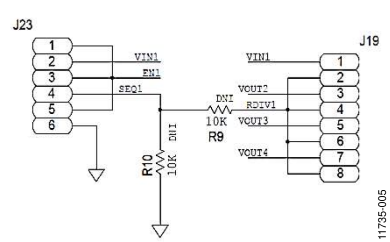


Figure 5. BUCK1 Sequencing Circuit

POWER GOOD PIN FOR OUTPUT VOLTAGE MONITORING

A power good output is available at Pin 6 of the LFCSP package to monitor the output voltage of the four regulators by default. The PG output can also be factory programmed to monitor a specific regulator channel. The PG pin is set to logic low when the monitored VOUTx falls below 90% of the nominal VOUTx level. The PG function also allows sequencing and enabling of external regulators tied to the PG pin.

As shown in Figure 6, the ADP5134 boards have provisions for a pull-up resistor tied between the open-drain PG pin and VIN or to an LED to monitor the state of the PG pin. To connect to a pull-up resistor, shunt the center contact of Jumper JD1 to the top pin header to pull the PG pin high to VIN1 through Resistor R17. In this configuration, the PG pin can be used to enable external regulators.

To connect to the LED circuit, shunt the center contact of Jumper JD1 to the bottom pin header. Since the PG pin will short to ground when the output goes out of regulation, a current sink path will be available for the LED, thus turning it on. In this configuration, a red LED is preferred to signal a fault condition. The value of the limiting resistor, RLIM (R18), is set by the forward voltage and current requirements of the LED; a typical LED would require 2 V with 20 mA forward current. To limit the current at 20 mA, RLIM should be around 167 Ω as shown in the sample calculation.

$$RLIM = \frac{VIN - VDROP - VDS}{ISINK}$$

$$= \frac{(5.5 - 2.0 - .1614)}{0.02}$$

$$= \approx 167\ \Omega$$

where:
RLIM refers to the value of the limiting resistor.
VIN = 5.5 V.
VDROP (LED voltage drop) is 2 V.
ISINK (LED bias current) is 20 mA.
VDS = 161.4 mV (typical).

By default, R18 and the LED (DS1) are not installed. Only R17 is populated on the demo board, making an available connection for a pull-up option.

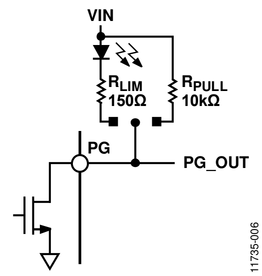


Figure 6. Power Good Pin Circuit

MEASURING PERFORMANCE

MEASURING OUTPUT VOLTAGE RIPPLE OF THE BUCK REGULATOR

To observe the output voltage ripple of BUCK1, place an oscilloscope probe across the output capacitor (C7) with the probe ground lead at the negative (−) capacitor terminal and the probe tip at the positive (+) capacitor terminal.

Set the oscilloscope to ac, 10 mV/division, and 2 µs/division time base, with BW set to 20 MHz to avoid noise that may interfere with the measurements. It is recommended to shorten the ground loop of the oscilloscope probe to minimize coupling.

A good way to measure the output voltage ripple is to solder a wire to the negative (−) capacitor terminal and wrap it around the barrel of the probe, while the tip directly connects to the positive (+) capacitor terminal as shown in Figure 7.

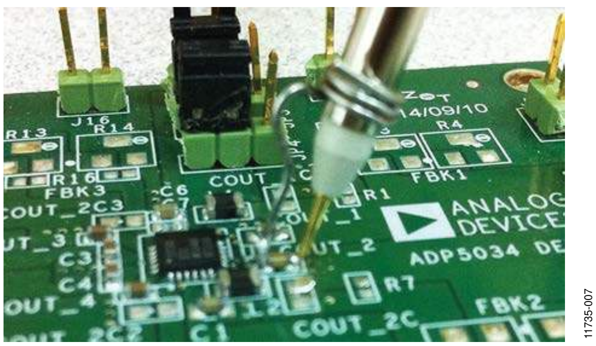


Figure 7. Measuring Output Voltage Ripple

MEASURING THE SWITCHING WAVEFORM OF THE BUCK REGULATOR

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at the end of the inductor with the probe ground at GND. Set the oscilloscope to dc, 2 V/division, and 200 ns/division time base.

When the MODE pin is set to high, the buck regulators operate in forced PWM mode. When the MODE pin is set to low, the buck regulators operate in PWM mode when the load is above a predefined threshold. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM), improving the light load efficiency. Typical PSM and PWM switching waveforms are shown in Figure 8 and Figure 9, respectively.

MEASURING THE LOAD REGULATION OF THE BUCK REGULATOR

Test the load regulation by increasing the load at the output and looking at the change in output voltage. The input voltage must be held constant during this measurement. To minimize voltage drop, use short low resistance wires, especially for loads approaching maximum current.

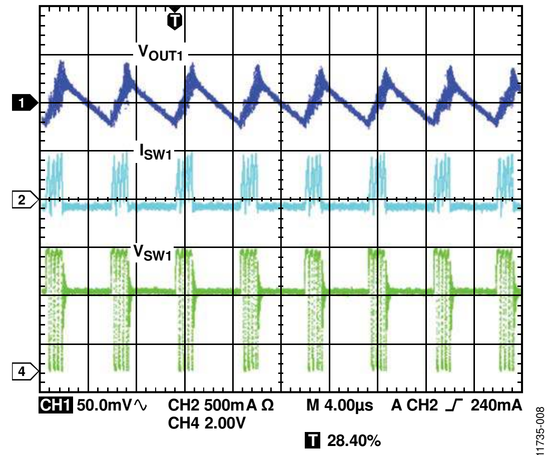


Figure 8. Typical Waveforms, V_{VOUT1} = 3.3 V, I_{VOUT1} = 30 mA, PSM Mode

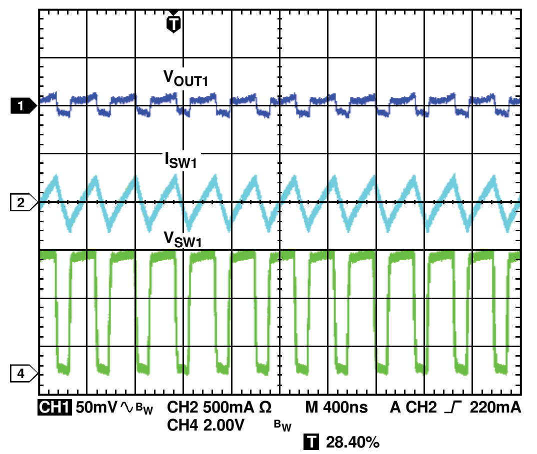


Figure 9. Typical Waveforms, $V_{VOUT}1$ = 3.3 V, $I_{VOUT}1$ = 30 mA, PWM Mode

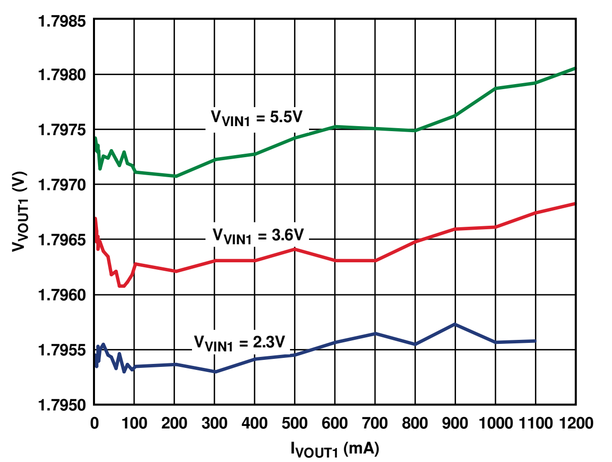


Figure 10. Buck Load Regulation

MEASURING LINE REGULATION OF BUCK

Vary the input voltage and examine the change in the output voltage.

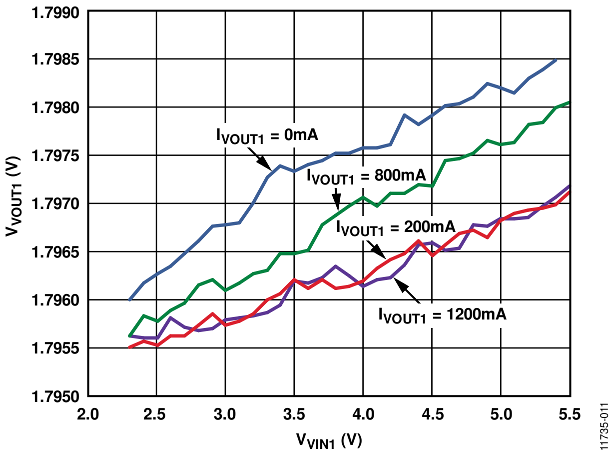


Figure 11. Buck Line Regulation

MEASURING BUCK EFFICIENCY

Measure the efficiency, η, by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of IR drops.

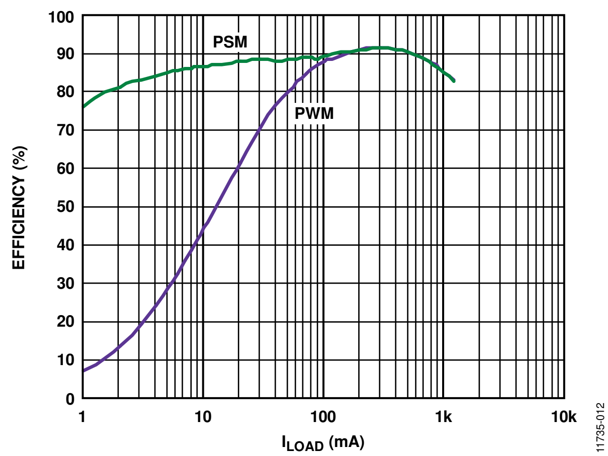


Figure 12. Buck Efficiency, V_{VIN1} = 3.6 V, V_{VOUT1} = 1.8 V

MEASURING INDUCTOR CURRENT

Measure the inductor current by removing one end of the inductor from its pad and connecting a current loop in series. A current probe can be connected to this wire.

MEASURING LINE REGULATION OF LDO

For line regulation measurements, the output of the regulator is monitored while its input is varied. For good line regulation, the output must change as little as possible with varying input levels. To ensure that the device is not in dropout mode during this measurement, V_{IN} must be varied between V_{OUT} nominal + 0.5 V (or 2.3 V, whichever is greater) and V_{IN} maximum. For example, a fixed 3.3 V output needs V_{IN} to be varied between 3.8 V and 5.5 V. This measurement can be repeated under different load conditions. Figure 13 shows the typical line regulation performance of the LDO with a fixed 3.3 V output.

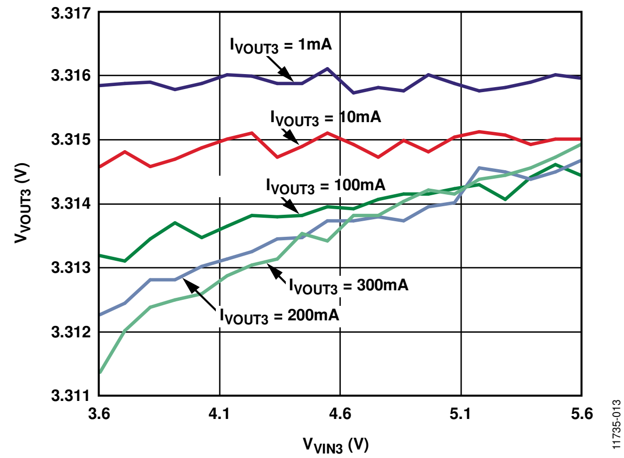


Figure 13. LDO Line Regulation

MEASURING LOAD REGULATION OF LDO

For load regulation measurements, the regulator output is monitored while the load is varied. For good load regulation, the output must change as little as possible with varying loads. The input voltage must be held constant during this measurement. The load current can be varied from 0 mA to 300 mA. Figure 14 shows the typical load regulation performance of the LDO with a 3.3 V output for different input voltages.

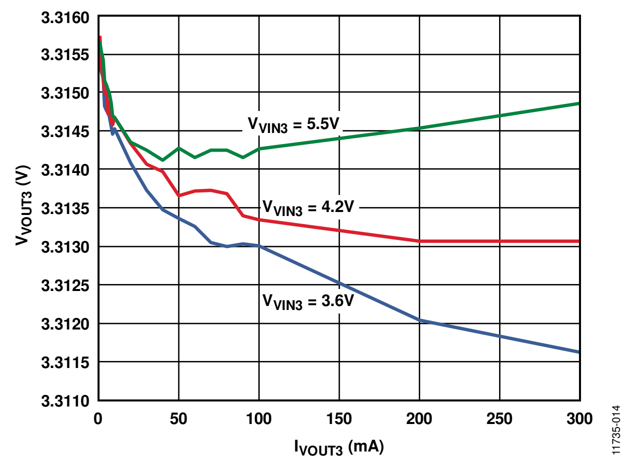


Figure 14. LDO Load Regulation

MEASURING DROPOUT VOLTAGE OF LDO

Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. One way to measure dropout voltage is to get the output voltage (V_{OUT} nominal) with V_{IN} initially set to V_{OUT} nominal + 0.5 V; output load can be set to 100 µA. Then, force the input voltage equal to V_{OUT} nominal, and measure the output voltage accordingly (V_{OUT} dropout). Dropout voltage is then calculated as V_{OUT} nominal − V_{OUT} dropout. This applies only for output voltages greater than 1.7 V. Dropout voltage increases with larger loads. For more accurate measurements, a second voltmeter can be used to monitor the input voltage across the input capacitor. The input supply voltage may need to be adjusted to account for IR drops, especially if large load currents are used.

MEASURING GROUND CURRENT CONSUMPTION OF LDO

Ground current measurements can determine how much current the internal circuits of the regulator consume while the circuits perform the regulation function. To be efficient, the regulator needs to consume as little current as possible. Typically, the regulator uses the maximum current when supplying its largest load level (300 mA). When the device is disabled, the ground current drops to less than 1 µA. Refer to Figure 18 for detailed instructions on how to perform ground current measurements.

CASCADING AN LDO FROM THE BUCK REGULATOR

For certain applications, such as analog circuit supplies, LDOs are preferred over bucks because of better noise performance. When not all buck outputs are being used, the input supply of the LDO can be taken from these outputs. An example demo board connection is shown in Figure 15 where VOUT1 is tied to VIN3 at Jumper J21, which is the supply of LDO1. In this configuration, the output voltage of the buck regulator should have enough headroom with the desired output voltage of the LDO to guarantee the LDO operate within specifications.

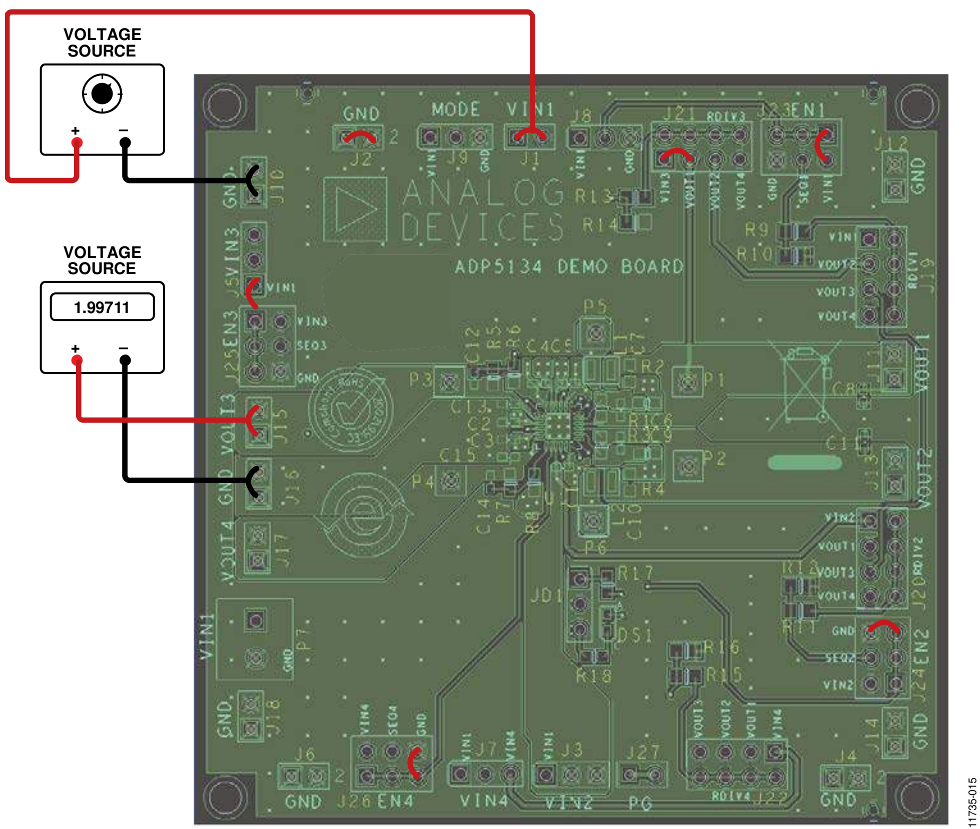


Figure 15. Cascading LDO from Buck

CONNECTING REGULATORS IN SEQUENCE

Figure 16 shows the jumper connections when regulators are powered up in sequence. The EN1 pin of BUCK1 is tied to VIN1 through Jumper J23. This allows automatic start-up for BUCK1, whereas the ENx pins of the other regulators are tied in sequence.

Shunting the J20 and J24 jumpers ties the EN2 pin of BUCK2 to VOUT1 via the sequencing circuit. This allows activation of BUCK2 once BUCK1 reaches its target level. Shunting the J21 and J25 jumpers ties the EN3 pin of LDO1 to VOUT2, and shunting jumpers J22 and J26 as shown connects EN4 of LDO2 to VOUT3.

In this setup, the regulators start-up are controlled in such a way that BUCK1 turns on first, followed by BUCK2, then LDO1, and finally LDO2. By changing the jumper connections, a different start-up sequence can be achieved.

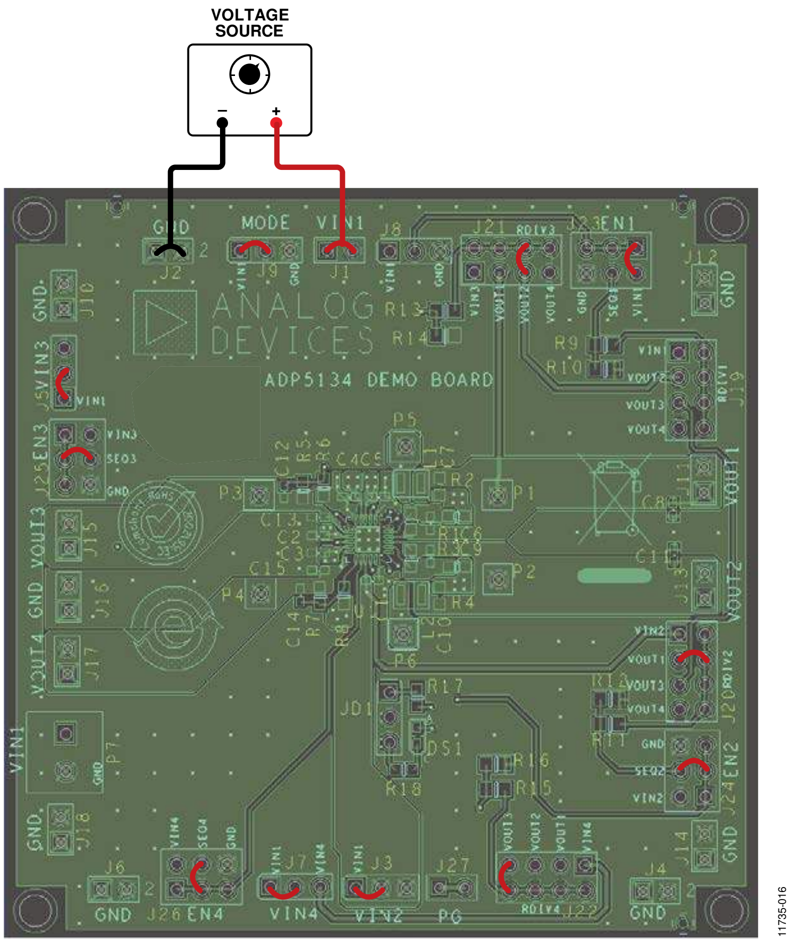


Figure 16. Regulators Connected in Sequence

MEASURING OUTPUT VOLTAGE

Figure 17 shows how the evaluation board can be connected to a voltage source and a voltmeter for basic output voltage accuracy measurements.

Figure 17 shows a voltage source connected to VIN1 and a voltmeter connected to VOUT1, which is the output of BUCK1. EN1 is connected to VIN1 via a shunt, which enables BUCK1, and EN2, EN3, EN4 are connected to ground, disabling the other channels. When measuring the voltages on VOUT2, VOUT3, and VOUT4, make sure that the respective channels are enabled, and the voltmeters are connected to the respective outputs.

A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating adequate to handle the power expected to be dissipated across it. An electronic load can also be used as an alternative. Ensure that the voltage source can supply enough current for the expected load levels.

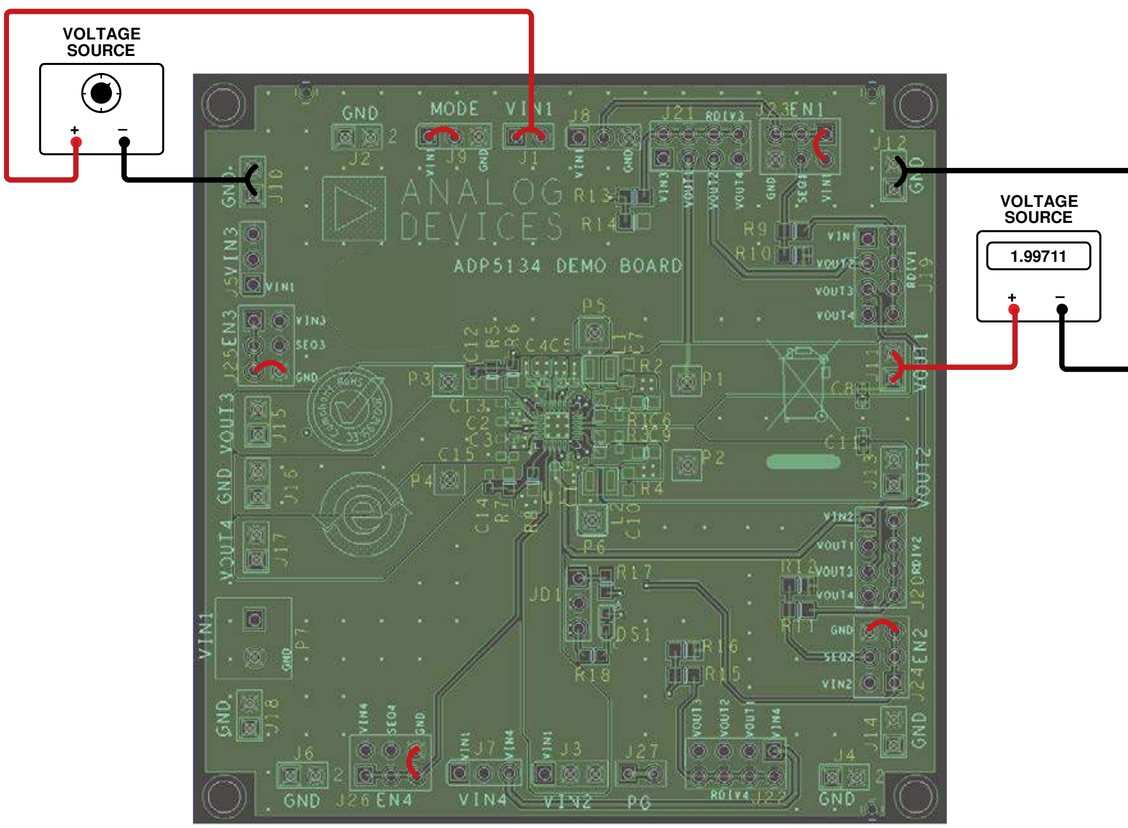


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Figure 17. Output Voltage Measurement

MEASURING GROUND CURRENT

Figure 18 shows the evaluation board connected to a voltage source and an ammeter for ground current measurements. A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating that is adequate to handle the power expected to be dissipated across it. An electronic load can be used as an alternative. Ensure that the voltage source used can supply enough current for the expected load levels.

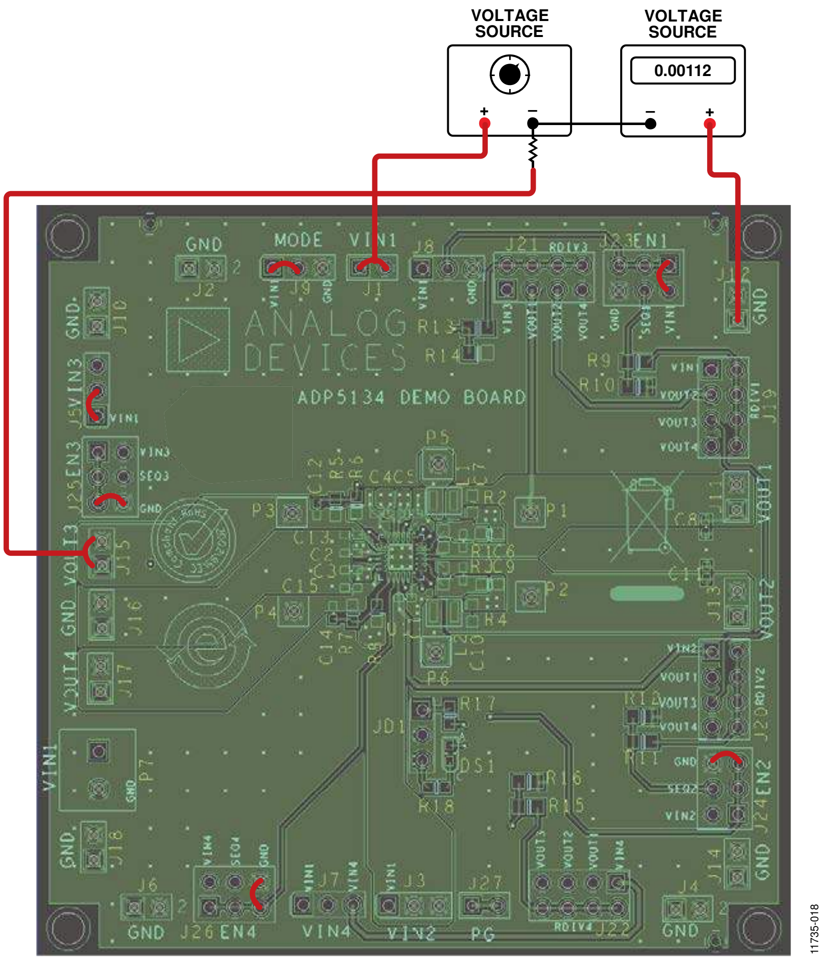

Figure 18. Ground Current Measurement

EVALUATION BOARD SCHEMATICS AND ARTWORK

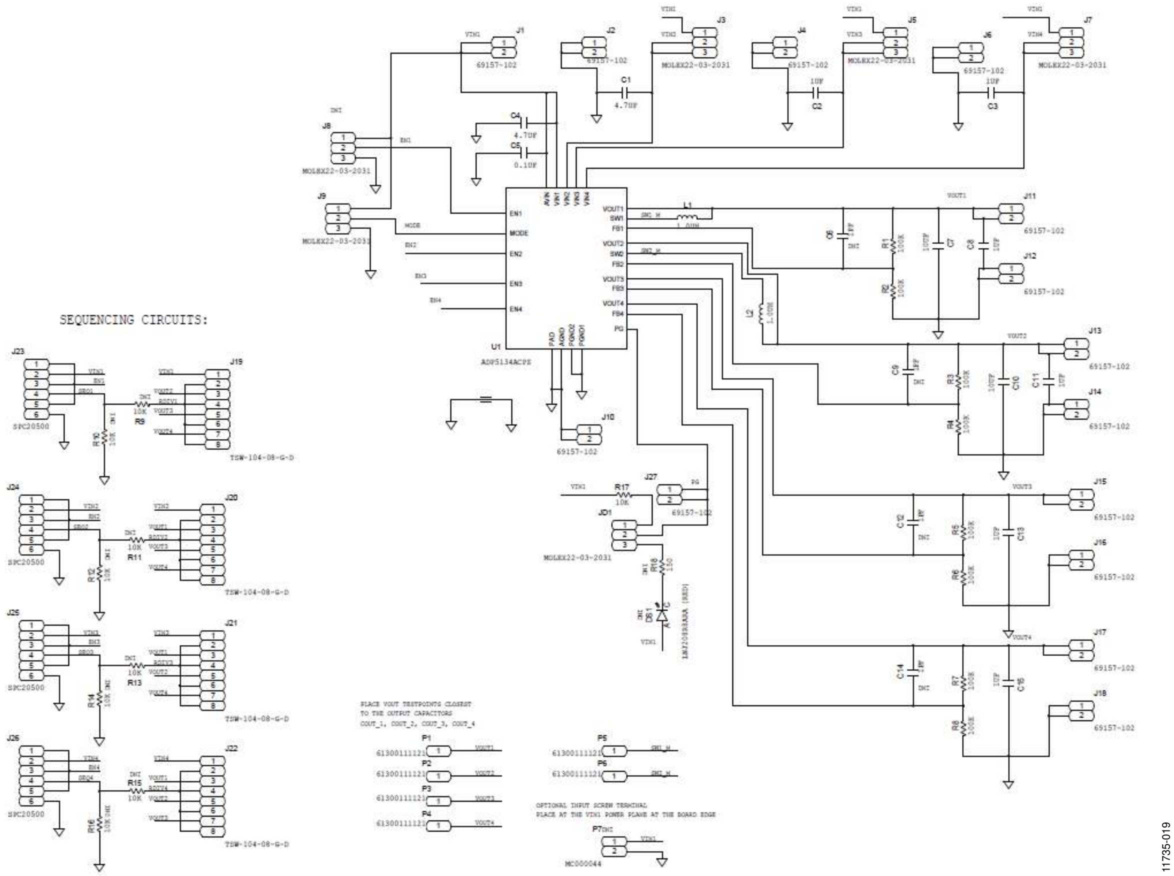

Figure 19. Evaluation Board Schematic of the ADP5134

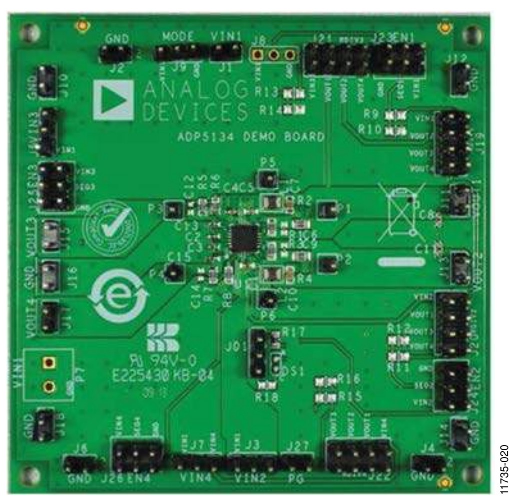

Figure 20. Evaluation Board for the ADP5134

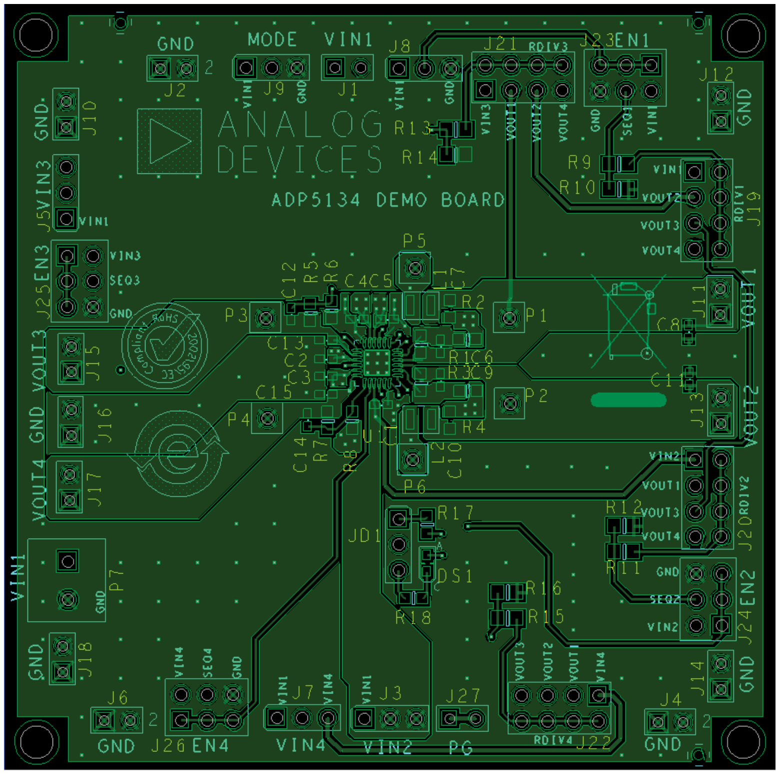

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Figure 21. Top Layer, Recommended Layout for ADP5134

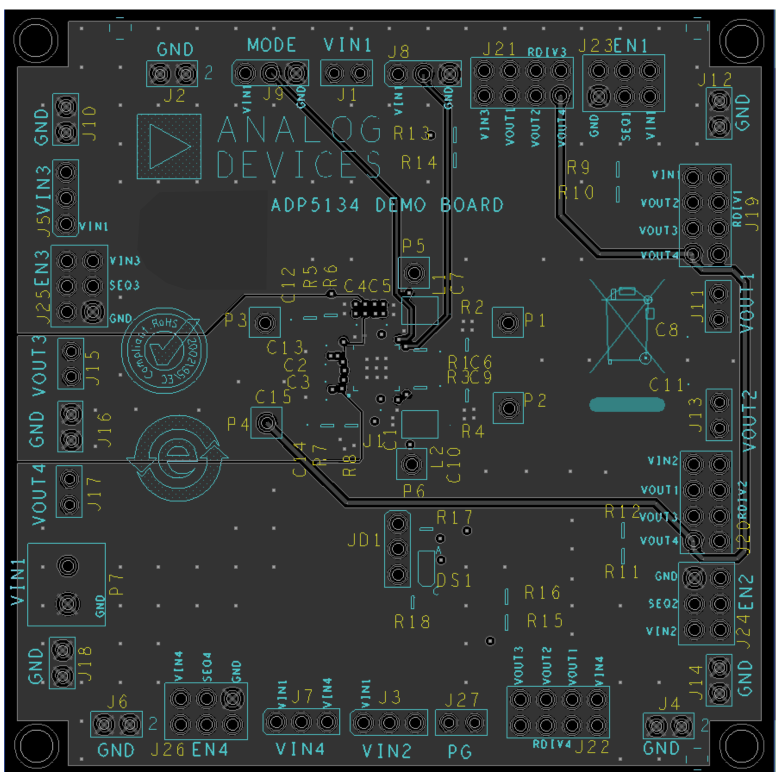

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Figure 22. Layer 2 (GND PLANE), Recommended Layout for ADP5134

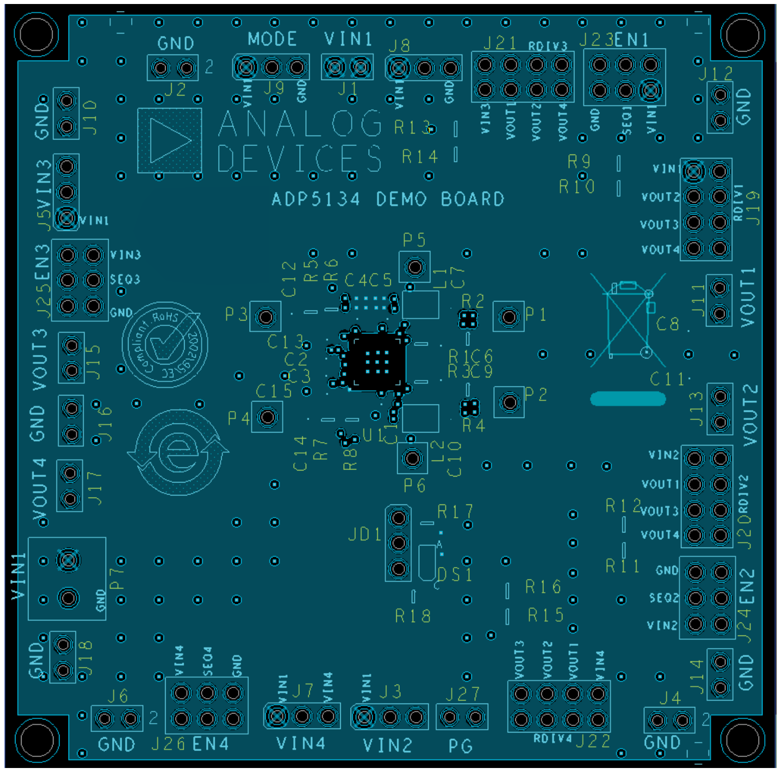

Figure 23. Layer 3 (PWR PLANE), Recommended Layout for ADP5134

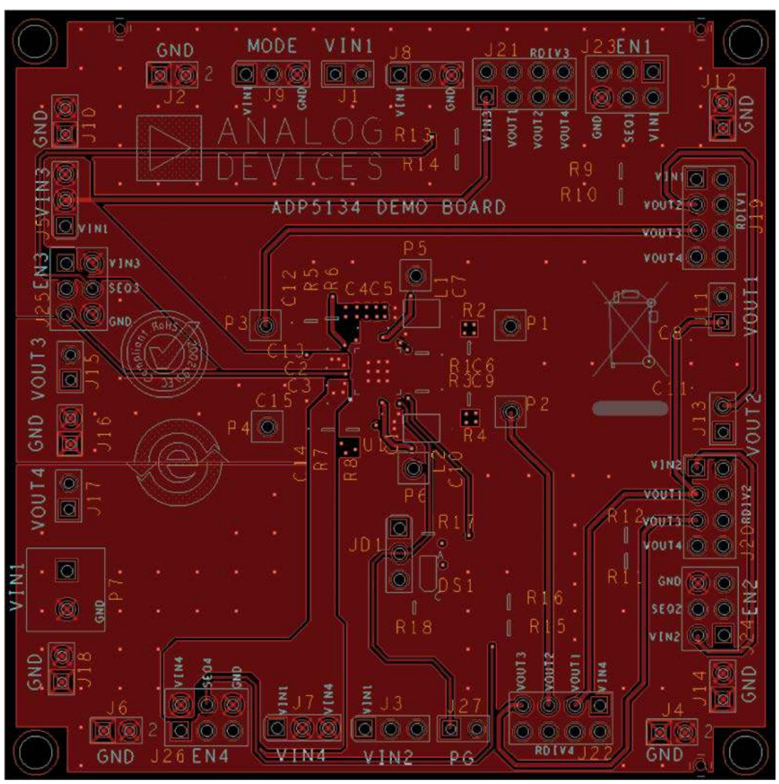

Figure 24. Bottom Layer, Recommended Layout for ADP5134

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	U1	Micro PMU	Analog Devices, Inc.	ADP5134
2	C1, C4	Capacitor, MLCC, 4.7 µF	Murata	GRM155R60J475ME87D
2	C7, C10	Capacitor, MLCC, 10.0 µF	Murata	GRM188R60J106ME47D
6	C2, C3, C8, C11, C13, C15	Capacitor, MLCC, 1.0 µF	Murata	GRM155R60J105KE19D
1	C5	Capacitor, MLCC, 0.1 µF	Murata	GRM155R71C104KA88D
4	C6, C9, C12, C14	Capacitor, MLCC, 1 pF	Not fitted	Not fitted
2	L1, L2	Inductor, 1.0 µH	Murata	LQM2HPN1R0MJ0L
8	R1 to R8	Resistor, 0603, 100 kΩ	Panasonic	ERJ-3EKF1003V
1	R17	Resistor, 0603, 10 kΩ	Panasonic	ERA-3YEB103V
9	R9 to R16, R18	Not fitted	Not fitted	Not fitted
1	DS1	LED, red	Not fitted	Not fitted

RELATED LINKS

Resource	Description
ADP5023	Dual 3 MHz, 800 mA Buck Regulator with One 300 mA LDO
ADP5024	Dual 3 MHz, 1200 mA Buck Regulators with One 300 mA LDO
ADP5034	Dual 3 MHz, 1200 mA Buck Regulator with Two 300 mA LDOs
ADP5037	Dual 3 MHz, 800 mA Buck Regulators with Two 300 mA LDOs

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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