

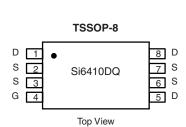
N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	
30	0.014 at V _{GS} = 10 V	± 7.8	
	0.021 at V _{GS} = 4.5 V	± 6.3	

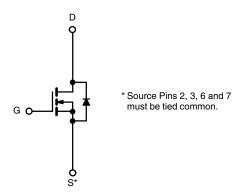
FEATURES

- · Halogen-free
- TrenchFET® Power MOSFETs





Ordering Information: Si6410DQ-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unles	ss otherwise no	ted	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	± 20	v
Continuous Dusin Comment /T 150 9008	T _A = 25 °C	1	± 7.8	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C	ID	± 6.2	
Pulsed Drain Current		I _{DM}	± 30	Α
Continuous Source Current (Diode Conduction) ^a		I _S	1.5	
	T _A = 25 °C	В	1.5	10/
Maximum Power Dissipation ^a	T _A = 70 °C	P _D	1.0	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	83	°C/W	

Notes:

a. Surface Mounted on FR4 board, $t \le 10$ s.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm.

Si6410DQ

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted									
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static									
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1			V			
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA			
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	T			
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			25	μΑ			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α			
Durin Course On Olate Besidence	B-a	$V_{GS} = 10 \text{ V}, I_D = 7.8 \text{ A}$		0.011	0.014	Ω			
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		0.015	0.021				
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 7.8 A		27		S			
Diode Forward Voltage ^a	V_{SD}	I _S = 1.5 A, V _{GS} = 0 V		0.7	1.1	V			
Dynamic ^b									
Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 7.8 \text{ A}$		22	33				
Total Gate Charge	Q _{gt}			43	60	nC			
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 7.8 \text{ A}$		9.0					
Gate-Drain Charge	Q_{gd}			7.0					
Turn-On Delay Time	t _{d(on)}			15	30				
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		10	20				
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		70	120	ns			
Fall Time	t _f			20	50				
Source-Drain Reverse Recovery Time	t _{rr}	$I_F = 1.5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		50	80				

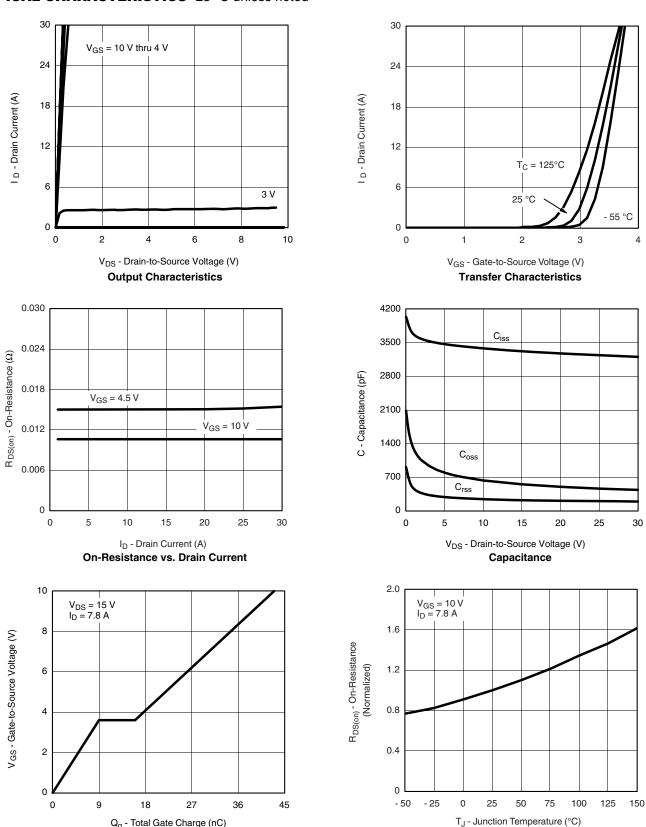
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.





TYPICAL CHARACTERISTICS 25 °C unless noted



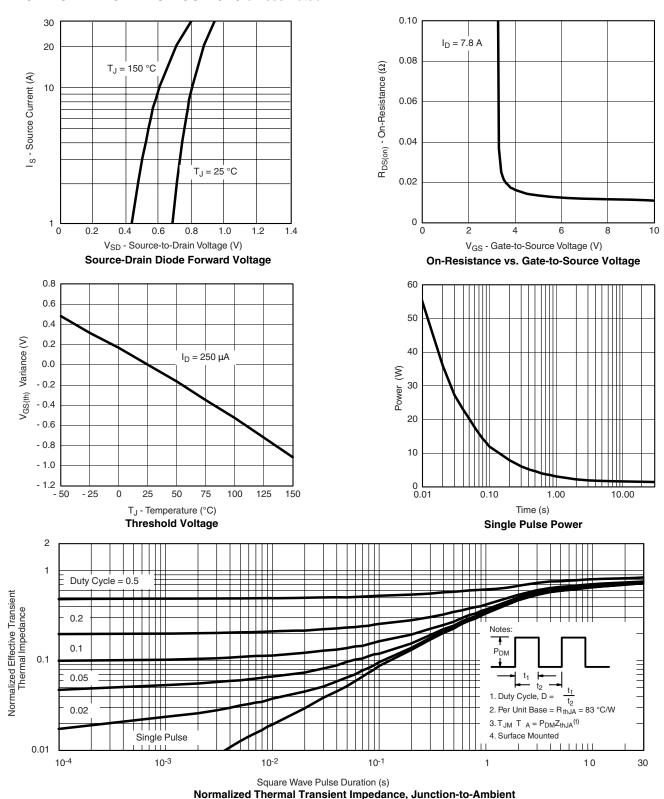
 Q_g - Total Gate Charge (nC) **Gate Charge**

On-Resistance vs. Junction Temperature

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TYPICAL CHARACTERISTICS 25 °C unless noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70661.



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