High-Speed Dual Precision CCD Driver

ISL55112

The ISL55112 is a high-speed CCD array driver comprising 2 Horizontal drivers with high current output drive and 2 ancillary signal drivers with lower current output drive.

The devices can be used in pairs to drive and control two halves of a high pixel count CCD array as used in high end Digital Cameras or Camcorders. The device has a largely symmetric pinout about a center axis to facilitate the placement of the devices on either side of a large CCD array with minimal signal routing disruption.

The ISL55112 can accommodate split asymmetric voltage supplies up to 8V total for each of the 4 drivers and has significant flexibility in the selection of these supply voltages within this range. All 4 drivers have their own High and Low level supply lines to minimize interference between drivers caused by shared current paths.

Special circuitry for the high current drivers is included to ensure the highest degree of stability of the driver output resistance over varying supply voltage, temperature and semiconductor process variations, resulting in highly consistent, predictable waveform crossover points.

The ISL55112 can drive high capacitance loads at pixel clock rates exceeding 30MHz with low propagation delays, and skews between channels of better than ±500ps.

The ISL55112 is available in 24 Ld exposed pad TQFN package and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55112IRTZ	55112 IRTZ	-40 to +85	24 Ld TQFN	L24.4x5C

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL55112. For more information on MSL please see techbrief TB363.

Features

- 2 Horizontal Row Drivers (High Current)
- 2 Ancillary Drivers (Lower Current)
- Up to 8V Signal Swing
- Unipolar and Bipolar Supply Capability
- Adjustable Output Impedance for EMI Control
- 3V Logic Interface
- Low Propagation Delays
- Low Skew: ±500ps
- High Clock Rates: 30MHz+
- Stand-by and Power-Down Modes

Applications* (see page 20)

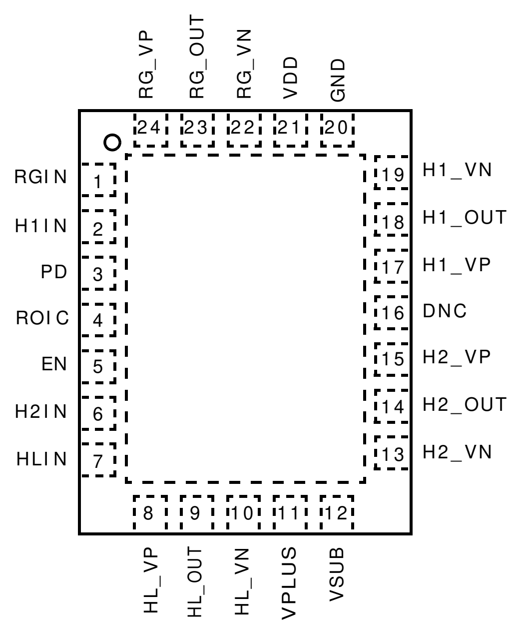
- Digital Still Cameras
- High Definition Digital Camcorders
- Industrial Vision Systems
- Medical Imaging
- Semiconductor Wafer and Mask Inspection Equipment
- High Definition Security Systems
- Home Security Systems

Related Literature* (see page 20)

- See AN1495 “ISL55112 High Speed Dual Precision CCD Driver Evaluation Board User Guide”

Pin Configuration

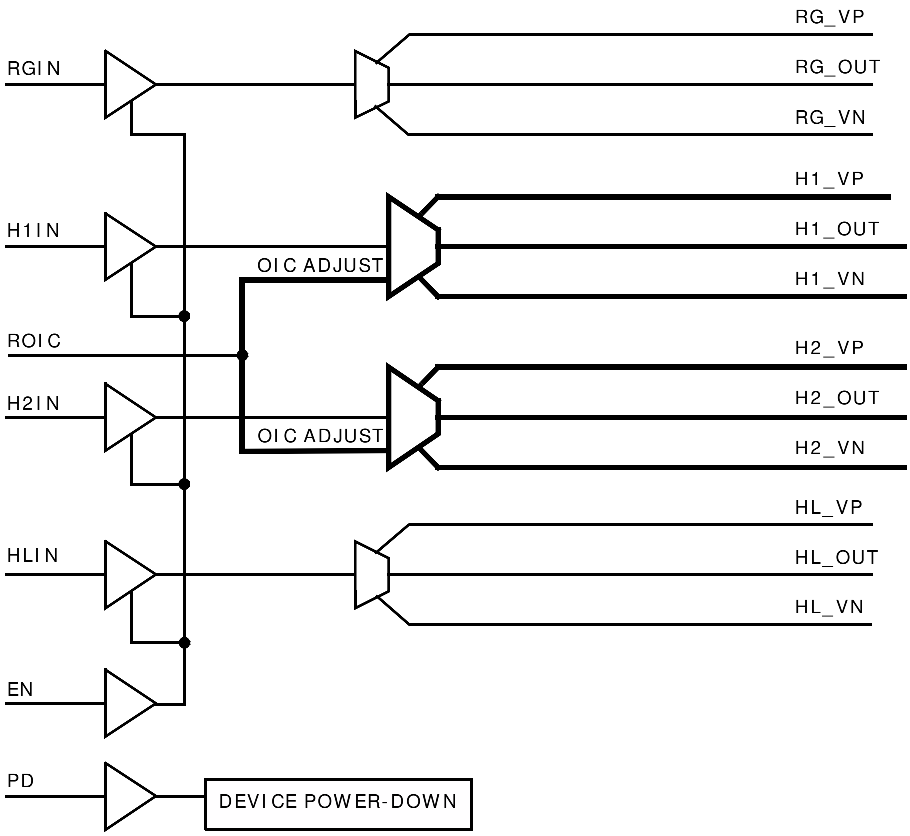
ISL55112
(24 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1	RGIN	Logic input for the Reset Gate (low capacitance) driver.
2	H1IN	Logic input for the H1 (high capacitance) driver.
3	PD	Logic input for placing device in Power-Down State.This is a static input and should never be toggled above 1Hz.
4	ROIC	A resistor to VSUB, sets the output impedance of the High Current Drivers.
5	EN	Logic input for placing device in the enabled state.
6	H2IN	Logic input for the H2 (high capacitance) driver.
7	HLIN	Logic input for the HL Driver (low capacitance) driver.
8	HL_VP	Low current driver (HL) upper supply voltage connection.
9	HL_OUT	Low current driver (HL) output connection.
10	HL_VN	Low current driver (HL) lower supply voltage connection.
11	VPLUS	Bias connection. Tie to most positive supply line on device.
12	VSUB	Bias connection. Tie to most negative supply line on device. Note: This potential is also on the exposed pad of the device.
13	H2_VN	High current driver (H2) lower supply voltage connection. (Connect to same voltage as H1_VN).
14	H2_OUT	High current driver (H2) output connection.
15	H2_VP	High current driver (H2) upper supply voltage connection.
16	DNC	Do not connect, leave open.
17	H1_VP	High current driver (H1) upper supply voltage connection.
18	H1_OUT	High current driver (H1) output connection.
19	H1_VN	High current driver (H1) lower supply voltage connection (Connect to same voltage as H2_VN).
20	GND	Device ground connection.
21	VDD	Logic supply voltage connection.
22	RG_VN	Low current driver (RG) lower supply voltage connection.
23	RG_OUT	Low current driver (RG) output connection.
24	RG_VP	Low current driver (RG) upper supply voltage connection.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (V_{PLUS} and V_{SUB}). 16.0V
Supply Voltage (H1_VP/H2_VP/RG_VP/HL_VP - H1_VN/ H2_VN/RG_VN/HL_VN) 16.0V
Supply Voltage (V_{DD} V_{LOGIC}) . . . . -0.3V to 6.0V
Maximum Output Current H1-H2 . . . . 200mA
Maximum Output Current RG/HL 20mA
Input Voltages
H1/H2/RG/HL/EN/PD . . . . . (GND -0.5V) to (V_{LOGIC} +0.5V)
Output Voltages
H1/H2//RG/HL . . . . (VN -0.5V) to (VP +0.5V)
All Pin Voltages: (Note 6) . . . . (V_{SUB} - 0.5V) to (V_{PLUS} + 0.5V)
Latch-up . . . . Class II, Level A AT +85°C
ESD Ratings
Human Body Model (HBM) 3kV
Machine Model (MM) 300V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN Package (Notes 4, 5) . .	37	1.5

Maximum Junction Temperature (Plastic Package). . . +150°C
Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature. . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features and is based on 6 Thermal Vias. See Tech Brief TB379 for details. Adding additional vias can improve thermal performance. See Tech Brief TB389.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. Dynamic over/undershoot characteristics should be examined to ensure this condition is never exceeded. Driver undershoot with respect to V_{SUB} is especially important. In applications where extremely high driver current is needed, V_{SUB} may require a voltage below the most negative driver rail to avoid driver under shoot falling below V_{SUB}.

Recommended Operating Specifications

Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Driver Positive Supply	VPn	H1, H2, RG, HL	Full	-2.5		8.0	V
Driver Negative Supply	VNn	H1, H2, RG, HL	Full	-8.0		2.5	V
Driver Differential Supply Range	VPn-VNn	H1, H2, RG, HL	Full	5.5		8.0	V
Logic Positive Supply Voltage	V_{DD}		Full	2.7		5.5	V

NOTE: V_{PLUS} must be connected to most positive voltage rail, V_{SUB} must be connected to the most negative voltage rail. V_{SUB} should be connected to ground where driver negative supplies are at or above ground. No voltage should occur on any pin less than V_{SUB} - 0.5V or greater than V_{PLUS} +0.5V. In applications where extremely high driver current is needed, V_{SUB} may require a voltage below the most negative driver rail to avoid driver under shoot falling below V_{SUB}.

Electrical Specifications

Test Conditions: XX_VP = 4V, XX_VN = -4V, VDD = 3.3V, V_{PLUS} = 4V, V_{SUB} = -4V, R_{OIC} = 68kΩ; Unless Otherwise specified. Full (-40°C to +85°C) limits are established by characterization and are not production tested. Boldface limits apply over the operating temperature range, -40°C to +85°C.

SYMBOL	PARAMETER	TEST CONDITIONS (Note 9)		TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
LOGIC INPUT CHARACTERISTICS H1/H2/RG/HL DRIVER INPUTS								
V_{IH}	Input High Threshold Voltage	H1, H2, R_G, H_L (Note 11)	V_{DD} = 3.3V	25	2.0			V
				Full	2.0			V
V_{IL}	Input Low Threshold Voltage	H1, H2, R_G, H_L (Note 11)	V_{DD} = 3.3V	25			1.2	V
				Full			1.2	V
I_{IH}	Logic "1" Input Current	H1, H2, R_G, H_L	V_{INPUT} = 5.5V, V_{DD} = 5.5V	25		56	63	µA
				Full	45		65	µA

Electrical Specifications

Test Conditions: XX_VP = 4V, XX_VN = -4V, VDD = 3.3V, V_{PLUS} = 4V, V_{SUB} = -4V, R_{OIC} = 68kΩ; Unless Otherwise specified. Full (-40°C to +85°C) limits are established by characterization and are not production tested. Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS (Note 9)		TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
I_{IL}	Logic "0" Input Current	H1, H2, R_G, H_L	V_{INPUT} = 0.0V, V_{DD} = 5.5V	25		30	175	nA
				Full			200	nA
C_{IN}	Input Capacitance (Gnd)	H1, H2, R_G, H_L		25		3.5		pF
R_{IN}	Input Resistance (Gnd)	H1, H2, R_G, H_L		25		100k		Ω
LOGIC INPUT CHARACTERISTICS EN (Enable) and PD (Power-Down) DRIVER INPUT								
V_{IH}	Input High Threshold Voltage	EN, PD (Note 12)	V_{DD} = 3.3V	25	2.0			V
				Full	2.0			V
V_{IL}	Input Low Threshold Voltage	EN, PD (Note 12)	V_{DD} = 3.3V	25			1.2	V
				Full			1.2	V
I_{IH}	Logic "1" Input Current	EN, PD	V_{INPUT} = 5.5V, V_{DD} = 5.5V	25		3	5	µA
				Full			5.5	µA
I_{IL}	Logic "0" Input Current	EN, PD	V_{INPUT} = 0.0V, V_{DD} = 5.5V	25			45	nA
				Full			50	nA
C_{IN}	Input Capacitance (Gnd)	EN, PD		25		3.5		pF
R_{IN}	Input Resistance (Gnd)	EN, PD		25		2M		Ω
DRIVER SIGNAL OUTPUT CHARACTERISTICS H1 and H2 (Note 13)								
V_{OH}	Driver Output High Voltage	H1, H2: I_{OUT} = -10mA		25	3.91	3.93	4	V
V_{OL}	Driver Output Low Voltage	H1, H2 I_{OUT} = 10mA		25	-4	-3.93	-3.91	V
R_{OH}	Driver Source Output Resistance	H1, H2: I_{OUT} = -100mA		25		2.8	14	Ω
R_{OL}	Driver Sink Ouput Resistance	H1, H2: I_{OUT} = -100mA		25		2.0	12	Ω
I_{PK+}	Peak Sourcing Current	H1, H2: C_L = 0.022µF (Note 14)	R_{OIC} = 40k	25		2.66		A
			R_{OIC} = 68k	25		2.04		A
			R_{OIC} = 80k	25		1.96		A
			R_{OIC} = 120k	25		1.66		A
I_{PK-}	Peak Sinking Current	H1, H2: C_L = 0.022µF (Note 14)	R_{OIC} = 40k	25		2.18		A
			R_{OIC} = 68k	25		1.72		A
			R_{OIC} = 80k	25		1.64		A
			R_{OIC} = 120k	25		1.52		A
t_R	Driver Rise Time	H1, H2: C_L = 300pF: V_P = +6V, VN = -1V		25		2.8	4.2	ns
				Full			4.3	ns
t_F	Driver Fall Time	H1, H2: C_L = 300pF: V_P = +6V, V_N = -1V		25		2.8	4.2	ns
				Full			4.3	ns
t_{PD+}	Propagation Delay Rising Edge	H1, H2: C_L = 300pF: V_P = +6V, V_N = -1V		25		7.7	10.1	ns
				Full			10.5	ns
t_{PD-}	Propagation Delay Falling Edge	H1, H2: C_L = 300pF: V_P = +6V, V_N = -1V		25		7.7	10.1	ns
				Full			10.5	ns
t_{SKEW+}	Driver Skew, H1 to H2 Rising Edge	H1, H2: C_L = 300pF		25		0		ns
				Full	-0.50		0.50	ns

Electrical Specifications

Test Conditions: XX_VP = 4V, XX_VN = -4V, VDD = 3.3V, V_{PLUS} = 4V, V_{SUB} = -4V, R_{OIC} = 68kΩ; Unless Otherwise specified. Full (-40°C to +85°C) limits are established by characterization and are not production tested. Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS (Note 9)		TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
t_{SKEW-}	Driver Skew, H1 to H2 Falling Edge	H1, H2: C_L = 300pF		25		0		ns
				Full	-0.50		0.50	ns
$t_{SKEW\pm}$	Skew: H1 Rising H2 Falling	H1, H2: C_L = 300pF		25		0		ns
				Full	-0.50		0.50	ns
$t_{SKEW\pm}$	Skew: H2 Rising H1 Falling	H1, H2: C_L = 300pF		25		0		ns
				Full	-0.50		0.50	ns
F_{MAX}	Max Operating Frequency	H1, H2: C_L = 300pF: V_P= +6V, V_N = -1V		25	40			MHz
		H1, H2: C_L = 300pF	R_{OIC} = 40k	25		70		MHz
			R_{OIC} = 120k	25		55		MHz
C_{HINT}	Calculated Empirical Internal H Driver capacitance	H1, H2: C_L = 0	40MHz, R_{OIC} = 68k	25		60		pF
t_{MIN}	Min Pulse Width	C_L = 0pF		25		2.5		ns
t_{MIN}	Min Pulse Width	C_L = 300pF V_P = 6, V_N = -1V		25	4	5.5	8	ns
DRIVER SIGNAL OUTPUT CHARACTERISTICS RG and HL								
V_{OH}	Driver Output High Voltage	R_G, H_L: I_{OUT} = -1mA		25	3.96	3.97	4	V
V_{OL}	Driver Output Low Voltage	RG, HL; I_{OUT} = 1mA		25	-4	-3.97	-3.96	V
R_{OH}	Driver Source Output Resistance	RG, HL: I_{OUT} = -10mA		25		22	55	Ω
				Full			56	Ω
R_{OL}	Driver Sink Ouput Resistance	R_G, H_L: I_{OUT} = -10mA		25		17	55	Ω
				Full			56	Ω
t_R	Driver Rise Time	R_G, H_L: C_L = 22pF		25		3		ns
				Full	2.5		3.5	ns
t_F	Driver Fall Time	R_G, H_L: C_L = 22pF		25		3.4		ns
				Full	3.1		3.7	ns
t_{PD+}	Propagation Delay Rising Edge	R_G, H_L: C_L = 22pF (Note 15)		25		7.6		ns
				Full	7		8.2	ns
t_{PD-}	Propagation Delay Falling Edge	R_G, H_L: C_L = 22pF (Note 15)		25		8.5		ns
				Full	7.9		9.0	ns
t_{SKEW+}	Driver Skew, RG to HL Rising Edge	R_G, H_L: C_L = 22pF		25		0		ns
				Full	-0.5		0.50	ns
t_{SKEW-}	Driver Skew, RG to HL Falling Edge	R_G, H_L: C_L = 22pF		25		0		ns
				Full	-0.5		0.50	ns
F_{MAX}	Max Operating Frequency	R_G. H_L: C_L = 90pF: V_P = +6V, V_N = -1V		25	40			MHz
		R_G, H_L: C_L = 22pF		Full		60		MHz
t_{MIN}	Min Pulse Width	C_L = 0pF		25		3.6		ns
t_{MIN}	Min Pulse Width	C_L = 22pF		25		6.5		ns
POWER-DOWN AND DRIVER ENABLE TIMING								
$t_{PD\ ON}$	Active Mode to Power Down Time	Time V_{DD} Current Drops to < 100µA		25		25	50	µs

Electrical Specifications Test Conditions: XX_VP = 4V, XX_VN = -4V, VDD = 3.3V, V_{PLUS} = 4V, V_{SUB} = -4V, R_{OIC} = 68kΩ; Unless Otherwise specified. Full (-40°C to +85°C) limits are established by characterization and are not production tested. Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS (Note 9)		TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
$t_{PD\ OFF}$	Power Down to Active Mode Time	Time H-Drivers $t_{PD}/t_R/t_F$ Takes to Stabilize		25		25	50	µs
$t_{EN\ ON}$	Driver Enable to Disable Mode Time	CLK Running at 30MHz		25		33		ns
$t_{EN\ OFF}$	Drivers Disable to Enable Mode Time			25		33		ns
STANDBY SUPPLY CURRENT: EN = 1:PD = 0								
I_{SB}	Current on Each Pin Type, Input = 0Hz	H1_VP, H2_VP	+4.0V	25		2.5	4.75	mA
				Full			5	mA
		H1_VN, H2_VN	-4.0V	25	-5	-2.5		mA
				Full	-5.5			mA
		RG_VP, HL_VP	+4.0V	25		0.25	1.5	mA
				Full			1.7	mA
		RG_VN, HL_VN	-4.0V	25	-1.5	-0.25		mA
				Full	-1.7			mA
		V_{DD}	3.3V	25		.75	1.2	mA
				Full			1.3	mA
		V_{PLUS}	+4.0V	25		1.0	1.8	mA
				Full			2.0	mA
		V_{SUB}	-4.0V	25	-2.2	-1.4		mA
				Full	-2.5			mA
POWER-DOWN SUPPLY CURRENT: EN = X, PD = 1								
I_{PD}	Current on Each Pin Type	H1_VP, H2_VP	+4.0V	25		70	450	µA
				Full			500	µA
		H1_VN, H2_VN	-4.0V	25	-450	-70		µA
				Full	-500			µA
		RG_VP, HL_VP	+4.0V	25		10	200	µA
				Full			250	µA
		RG_VN, HL_VN	-4.0V	25	-200	-10		µA
				Full	-250			µA
		V_{DD}	3.3V	25		30	300	µA
				Full			320	µA
		V_{PLUS}	+4.0V	25		70	400	µA
				Full			450	µA
		V_{SUB}	-4.0V	25	-400	-70		µA
				Full	-450			µA

Electrical Specifications Test Conditions: XX_VP = 4V, XX_VN = -4V, VDD = 3.3V, V_{PLUS} = 4V, V_{SUB} = -4V, R_{OIC} = 68kΩ; Unless Otherwise specified. Full (-40°C to +85°C) limits are established by characterization and are not production tested. Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS (Note 9)		TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
ACTIVE SUPPLY CURRENT: EN = 1, PD = 0								
I_{ACT}	Current on Each Pin Type; 40MHz input: Note 16	H1_VP, H2_VP	+4.0V	25		118		mA
		H1_VN, H2_VN	-4.0V	25		-118		mA
		RG_VP, HL_VP	+4.0V	25		15		mA
		RG_VN, HL_VN	-4.0V	25		-15		mA
		V_{DD}	3.3V, All driver inputs running	25		3.8		mA
		V_{PLUS}	+4.0V	25		0.9		mA
		V_{SUB}	-4.0V	25		-0.9		mA

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Full Temperature limits established by characterization and are not production tested.
8. The algebraic convention, where by the most negative value is the minimum and the most positive a maximum, is used in the data sheet.
9. All load capacitances are with respect to Gnd.
10. PD (Power-Down) is a static control. Do not allow toggle frequency above 1Hz. PD should be used in combination with EN pin during Active and Inactive state changes. (See “Power Supply Sequencing” on page 10).
11. H1, H2, EN, R_G, H_L V_{IH} and V_{IL} Thresholds established while toggling @10MHz.
12. PD V_{IH} and V_{IL} Thresholds established while toggling @ 1Hz.
13. ATE test conditions limit r_{ON} measurement capability. Refer to Characterization tables for typical r_{ON} Values. The Output Impedance Control active circuitry adjusts r_{ON} characteristics dynamically.
14. Peak current as measured with evaluation board with 1Ω resistor in series with 0.022µF capacitor. Measurements as characterized with ISL55112 Evaluation board. VP-VN = 12V.
15. Dynamic FULL/MIN/MAX data recorded with ISL55112 Evaluation board. Series inductance of decoupling, loads and interconnect will greatly influence this measurement. See section on “Power Supply Bypassing and Printed Circuit Board Layout” on page 10.
16. As measured using evaluation board with H1_OUT, H2_OUT = 300pF load on each output and RG_OUT, HL_OUT = 22pF load on each output.

Test Circuits and Waveforms

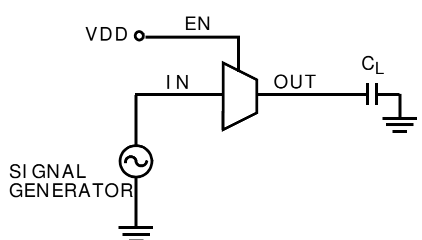


FIGURE 1A. TEST CIRCUIT

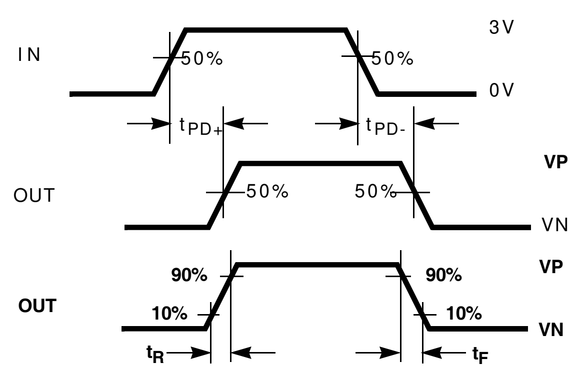


FIGURE 1B. MEASUREMENT POINTS

FIGURE 1. DRIVER PROPAGATION DELAY AND RISE AND FALL TIMES

Test Circuits and Waveforms (Continued)

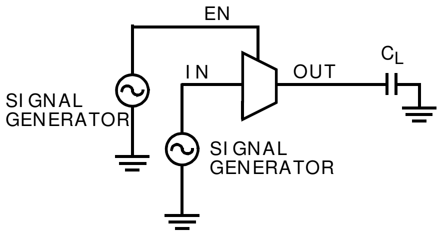


FIGURE 2A. TEST CIRCUIT

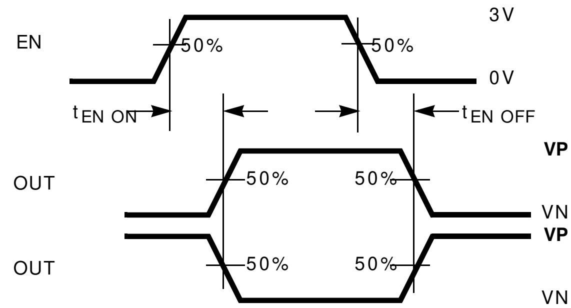


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER ENABLE AND DISABLE TIMES

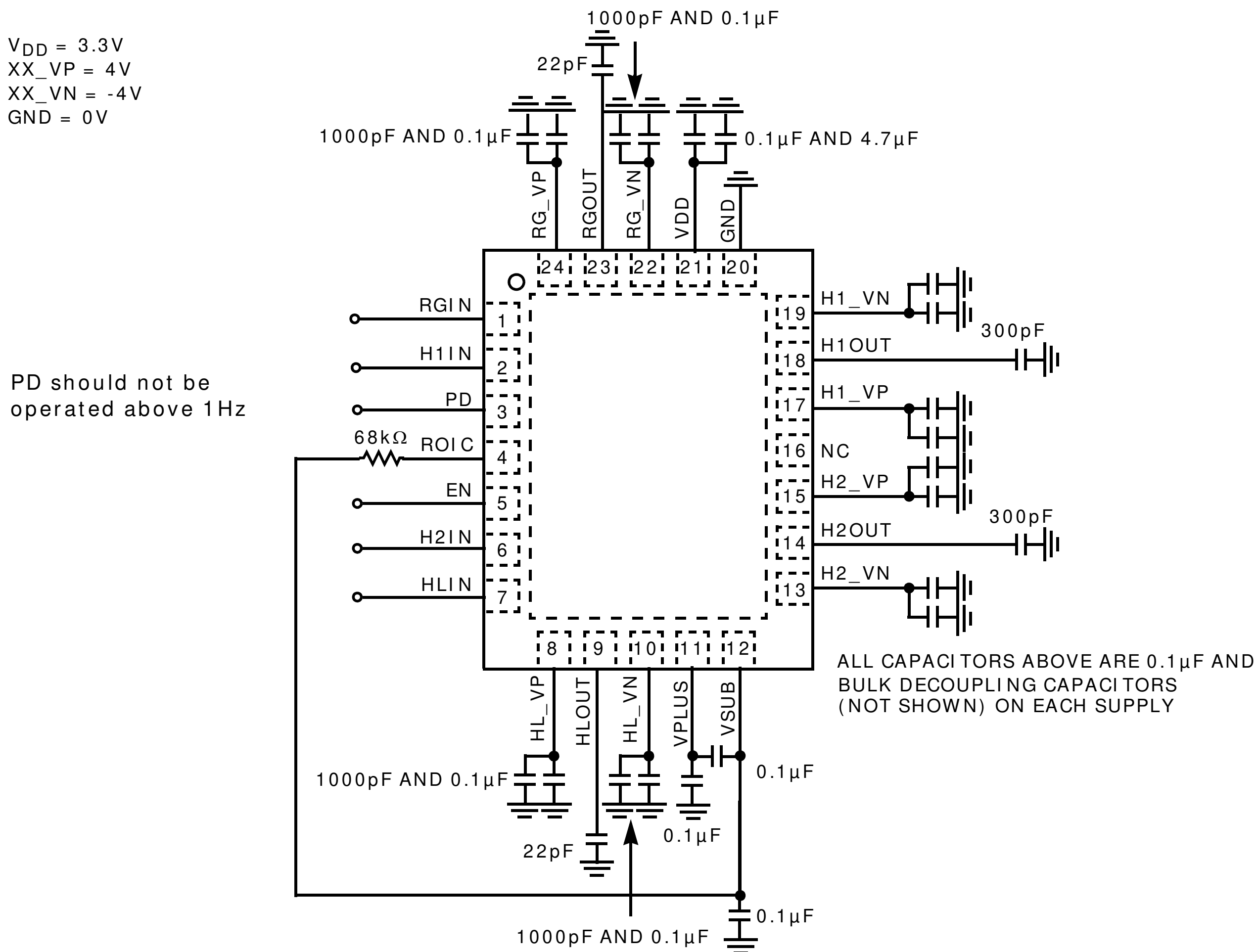


FIGURE 3. STANDARD TEST CONFIGURATION

Application Information

The ISL55112 2+2 CCD device provides four drivers for horizontal inputs of CCD arrays. It comprises two high capacitance drivers (H1/H2) and two low capacitive drivers for handling Reset Gate (RG)/Last H (HL) inputs of a CCD device.

From an applications and physical routing standpoint, the H1/H2 (high current drivers) have identical circuitry. Likewise, the HL/RG (low current drivers) circuitry is the same internally. In dual device applications, the user is free to swap driver outputs to accommodate layout requirements.

The ISL55112 H1/H2 have fast rise/fall times into large capacitive loads. H1/H2 are designed with short propagation delays and tightly controlled skew, allowing the device to be used on large, fast CCD arrays, used in image processing applications.

Supply Voltages

The ISL55112 has three types of pins when it comes to supply voltages: Logic, driver rails and device bias connections.

V_{DD} and Ground Supply Connections

The ISL55112 has a logic supply (V_{DD}) that can be set from 2.7V to 5.5V. Hence the V_{DD} supply voltage sets the operating thresholds for the digital inputs.

$H1_{IN}$, $H2_{IN}$, RG_{IN}, HL_{IN}, and EN pins are high speed digital logic connections. Typically they are logic connections coming from the master CCD timing generator. PD should have fast transitions, but should not run at frequencies above 1Hz.

CCD Driver Rails

Each of the four driver outputs has its own set of high and low rail supply connections. The positive rail connections for the drivers are RG_VP, HL_VP, H1_VP, H2_VP. The negative driver rail connections are RG_VN, HL_VN, H1_VN, H2_VN. (Note H1_VN = H2_VN and should always be at the same voltage).

Once the user has defined the “Driver” amplitudes required by the CCD, device bias connections, V_{PLUS} and V_{SUB} must be connected to the maximum and minimum voltage required.

Device Bias connections

V_{PLUS} should be connected to the most positive voltage. V_{SUB} should be connected to the most negative voltage. Accordingly, the V_{PLUS}/V_{SUB} connections can only be determined once the CCD device driver output amplitude requirements have been determined.

VSUB Discussion

The VSUB pin is connected to the device substrate. Any pin falling below the V_{SUB} voltage can reduce clamp protection performance. Most often a driver negative rail or driver output can fall below V_{SUB} voltage during high to low transitions where negative driver undershoot occurs, or ripple voltage on the VN rail might occur. The user is cautioned to take great care that the VSUB is always below the most negative swing on any pin.

If, due to the driver requirements, undershoot results in a signal falling below V_{SUB} - 0.5V, the user can consider the following options.

1. Slow rise/fall time by increasing the value of ROIC resistor.
2. Add an additional/separate bias voltage to the VSUB pin that is lower than the most negative driver under shoot. (Remember the V_{SUB} voltage is also connected to the thermal pad).
3. Add Schottky diodes on the driver outputs and driver rails for protection to the VPLUS and VSUB bias connections.
4. Always use the smallest VP-VN swing possible.

As a final note, the number one way to reduce over/ undershoot is to reduce parasitic inductance. The user must recognize that series inductance from the driver VP/VN decoupling points through the output to the load and the return path must be kept to a minimum. The faster the rise/fall times, the more the series inductance gets amplified and over/undershoot increases.

Dual Video CCD Connection Considerations

Physical placement that keeps series inductance to a minimum is important. The ISL55112 design accommodates dual device placement close to a CCD device.

H1/H2 and RG/HL drivers are internally identical. The user can rotate the device for PCB placement close to a single CCD with dual-video requirements.

Power Supply Sequencing

The ISL55112 substrate is connected to the VSUB Pin. Positive Protection is connected to the VPLUS pin.

The system supply GND connection will always be present, and is the reference to all other supply voltages. Therefore, apply V_{DD}, V_{PLUS}, V_{SUB} followed by the VP, VN busses. Digital inputs should be driven as soon as all power inputs have settled but should not be allowed to float during power-up and power-down operations.

Note: If V_{SUB} floats high when V_{DD} is applied, a 10k to 50k resistor should be added from V_{SUB} to ground. For proper power-up biasing, V_{SUB} should not be allowed to float high when only V_{DD} is applied.

Power Supply Bypassing and Printed Circuit Board Layout

Maximum current occurs during edge-transition of the driver outputs. Decoupling of the VP and VN rails for the drivers is of paramount concern. This being especially true of the high current drivers. Minimum possible lead length from the VP/VN device connections to the associated decoupling capacitors is key to device performance.

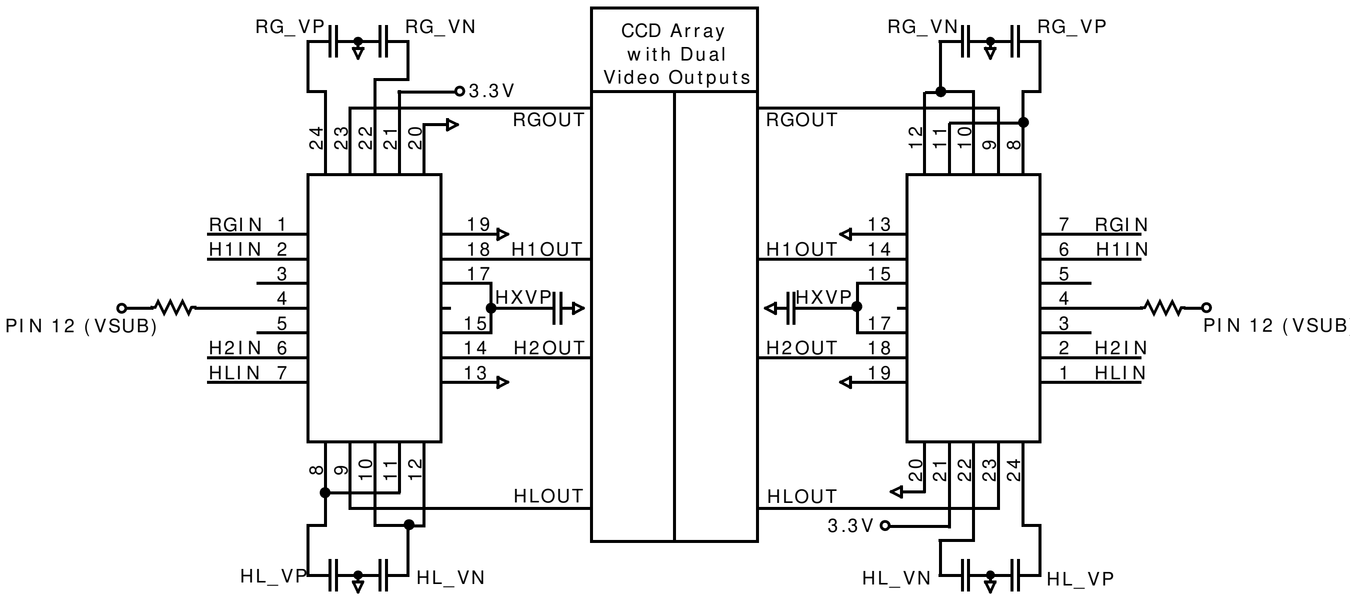


FIGURE 4. SYMMETRY ACCOMMODATES DUAL DEVICE UTILIZATION WITH A DUAL VIDEO CCD DEVICE

Given transition times are the point of maximum current, series inductance from the decoupling point to the VP/VN connections and from the VOUT connection to the CCD should be kept to the minimum possible values.

Note: The ISL55112 employs multiple bond wires on all driver rail and driver output connections. Multiple bond wires help reduce the device package internal bond wire connection inductance.

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation.

The “Evaluation Board” drawing depicts a conceptual decoupling scenario. Capacitor values, placement and quantities are subject to specific application requirements. The key to decoupling, especially during edge transitions, is to reduce the series inductance of the VP/VN supply rails.

Decoupling Discussion and Evaluation Board Information

- With split supply driver voltages, each VN and VP pin should have a separate 0.1µF capacitor to ground. The capacitors should be on the top layer of the PCB to a ground plane. This avoids the operative decoupling point having a via in series with the device pin.
- Single supply applications require fewer decoupling capacitors (VN rails are connected to ground. In this case, the top layer should also be a ground plane and VP pins should be decoupled as closely as possible.
- In both cases, the return path series inductance needs to be considered. The return current path of the load and the decoupled point should be as close as possible. Avoid/reduce Vias between driver rail decoupling points and driver output to load.

Figure 5 shows the top decoupling provides the high frequency driver rail decoupling during edge transitions (C1, C4, C6, C11). Figure 6 shows vias between bottom decoupling and the device pins on top increase series inductance. However, bottom decoupling replenishes the top decoupling before and after edge currents occur.

Additional bulk decoupling (22µF to 4.7µF) should also be used. This is low frequency decoupling and need not be located as close to the output area of the device.

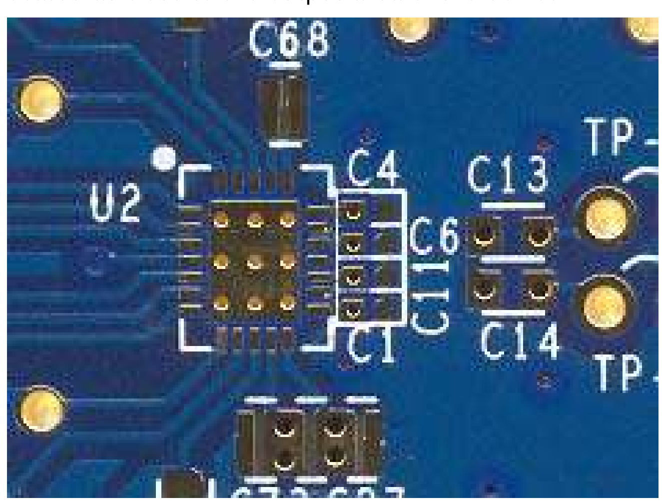


FIGURE 5. TOP COMPONENT AND PCB ARTWORK

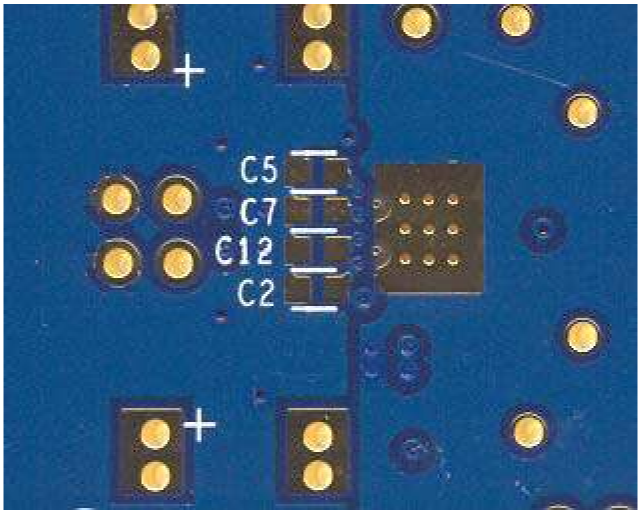


FIGURE 6. BOTTOM COMPONENT AND PCB ARTWORK

Output Impedance Control (OIC)

An external Resistor, R_{OIC}, is used to set the output impedance of the high current drivers. Selection of R_{OIC} resistance value enables the user to adjust high current H1/H2 driver operation for a specific CCD product.

Rise and Fall times can be adjusted via the R_{OIC} resistance setting. This is accomplished by selecting an ROIC resistance value from 40kΩ to 120kΩ. Actual rise/fall timing will be the product of driver loading and interconnect parasitics.

High current driver characteristics, which are normally affected by temperature and process variations, are kept to a minimum by the ISL55112 OIC feature.

Dynamic Measurements

The ISL55112 drivers require minimum series inductance to operate properly. Therefore it is not recommended that test sockets be used when evaluating driver performance. Parts should be soldered to an appropriate layout that addresses both driver load and driver rail decoupling series inductance.

Input Signals

The ISL55112 has logic signal inputs on H1,H2, RG and HL drivers. The ISL55112 also has two "mode control" pins (PD and EN) which enable the user to control power requirements. Input signals switching thresholds are set by the V_{DD} to Gnd voltage.

Power Saving Mode Control

The ISL55112 offers two methods of power reduction. The Power Down control pin is to be used in conjunction with Enable pin. (See "Mode control Power-Down sequence" on page 12 and "Mode control Power-Up sequence" on page 12).

Driver Standby (EN)

(EN: Low, PD Low) In this state the gate drive circuit is active but the front end receivers are shut off. Shorter term power savings can be realized by using the EN input.

When EN is disabled (EN: Low, PD: Low), the driver outputs will stay in their last state prior to setting the EN signal low. The "$t_{EN\ OFF}$" specification indicates the response time for the drivers to hold their present logic state.

When EN is set to the active state (High), the drivers will respond to driver inputs. Reaction time to the 1st drive pulse is defined in the electrical table as "$t_{EN\ ON}$"page 7.

During initial Power-Up, H1 and H2 Outputs will be HIz until a transition occurs on the H1 and H2 Inputs.

Device Power-Down (PD)

In Power-Down Mode, both input circuitry and gate drive circuitry is powered down. Power-down should only be used for static control. Do not exceed 1Hz of operation. The recommended sequences for Power Mode control are:

MODE CONTROL POWER-DOWN SEQUENCE

Device active (Enable High, Power Down Low)

- Stop Clock Inputs
- Set Power Down High Set Enable Low.

MODE CONTROL POWER-UP SEQUENCE

Device inactive (Enable Low, Power Down High)

- Set Enable High, Set Power Down Low
- Start Clock Inputs

Power Dissipation Considerations

Specifying continuous data rates, driver loads and driver level amplitudes are key in determining power supply requirements as well as dissipation/cooling necessities. Driver Output patterns also impact these needs. The faster the pin activity, the greater the need to supply current and remove heat.

TABLE 1. ISL55112 DETAILED POWER DISSIPATION FORMULA/EXAMPLE

FORMULA VARIABLE	EXAMPLE VALUES	UNIT	VARIABLES SQUARED	CALCULATIONS	NOTES
POWER DISSIPATION FORMULA ISL55112: OPERATION VARIABLES					
VDD	3.3	V	VDD^2	10.89	VDD^2
H_Diff	8	V	H_Diff^2	64	Hx_VP - Hx_VN
HL_Dif	8	V	HL_Diff^2	64	HL_VP-HL_VN
RG_Diff	8	V	RG_Diff^2	64	RG_VP-RG_VN

TABLE 1. ISL55112 DETAILED POWER DISSIPATION FORMULA/EXAMPLE (Continued)

FORMULA VARIABLE	EXAMPLE VALUES	UNIT	VARIABLES SQUARED	CALCULATIONS	NOTES
H1_Freq	40	MHz	Operating Frequency		
H2_Freq	40	MHz	Operating Frequency		
HL_Freq	40	MHz	Operating Frequency		
RG_Freq	40	MHz	Operating Frequency		
Driver Loads					
$H1\_C_{LOAD}$	300	pF	High Capacitance Load		
$H2\_C_{LOAD}$	300	pF	High Capacitance Load		
HL_C_{LOAD}	20	pF	Low Capacitance Load		
RG_C_{LOAD}	20	pF	Low Capacitance Load		
POWER DISSIPATION FORMULA ISL55112: DEVICE VARIABLES					
Default Currents					
IDD	1	mA	Stand By VDD Current		
IH	6	mA	Stand By IH Current		
Device Internal Capacitance					
Log_Cint	3.5	pF	Per channel internal logic switching load		
H1_Cint	60	pF	Effective Internal Driver Capacitance		
H2_Cint	60	pF	Effective Internal Driver Capacitance		
HL_Cint	6.3	pF	Effective Internal Driver Capacitance		
RG_Cint	6.3	pF	Effective Internal Driver Capacitance		
POWER DISSIPATION FORMULAS AND EXAMPLE CALCULATIONS					
Wattage Sub Totals and Formula					Example Calculation
Standby Watts	=	VDD*IDD + H_DIFF*IH			0.0513
H1_Logic_Watts	=	Log_Cint* VDD^2 * H1_Freq			0.0015
H2_Logic_Watts	=	Log_Cint* VDD^2 * H2_Freq			0.0015
HL_Logic_Watts	=	Log_Cint* VDD^2 * HL_Freq			0.0015
RG_Logic_Watts	=	Log_Cint* VDD^2 * RG_Freq			0.0015
H1_Cint_Watts	=	H1_Cint* H_Diff^2 * H1_Freq			0.1536
H2_Cint_Watts	=	H2_Cint* H_Diff^2 * H2_Freq			0.1536
HL_Cint_Watts	=	HL_Cint* HL_Diff^2 * HL_Freq			0.0161
RG_Cint_Watts	=	RG_Cint* RG_Diff^2 * RG_Freq			0.0161
H1_Cload_Watts	=	H1_Cload* H_Diff^2 * H1_Freq			0.7680
H2_Cload_Watts	=	H2_Cload* H_Diff^2 * H2_Freq			0.7680
HL_Cload_Watts	=	HL_Cload* HL_Diff^2 * HL_Freq			0.0563
RG_Cload_Watts	=	RG_Cload* RG_Diff^2 * RG_Freq			0.0563
Total Watts				Total Watts	2.0455
T_{JA}		37		Degrees over ambient	75.68

Power Dissipation Notes

Power dissipation consists of 4 contributors:

1. Contributor 1 corresponds to the Standby Current of the VDD Logic Supply (IDD) and VP-VN Driver Rails (IH)
2. Contributor 2 corresponds to the dissipation from running the H1, H2, RG and HL Inputs. Log_Cint specifies the basis for the power consumed from the VDD Supply for each input.
3. Contributor 3 corresponds to the Driver Rail Supply dissipation due to internal capacitance. The value of H1_Cint, H2_Cint, RG_Cint and HL_Cint correspond to the effective internal capacitance of the drivers.
4. Contributor 4 corresponds to the Driver Rail Supply dissipation due to load capacitance. The value of H1_Cload, H2_Cload, RG_Cload and HL_Cload correspond to the external capacitance of the device being driven.

These are approximate formulae and the actual values may be 15% to 20% off.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads. Power also depends on number of channels changing state and the frequency of operation. *The reader is cautioned against assuming the same level of thermal performance in actual applications. A careful inspection of conditions in your application should be conducted. Great care must be taken to ensure Die Temperature does not exceed +150°C Absolute Maximum Thermal Limits.*

Important Note: The ISL55112 exposed pad is used for heat sinking of the device. It must be electrically connected to the most negative supply potential needed for driver output (V_{SUB}). Therefore, when negative drive rails are used, the thermal pad (V_{SUB}) must be isolated from ground.

Typical Performance Curves

VDD = 3.3V, VH = 4V, VN = -4V, R_{OIC} = 68kΩ, C_L = 300pF for H1/2OUT, C_L = 22pF for RG/HLOUT, Unless specified otherwise. Refer to Figures 1, 2 and 3. (Information derived from ISL55112 Evaluation board characterization. See AN1495 "ISL55112 High Speed Dual Precision CCD Driver Evaluation Board User Guide).

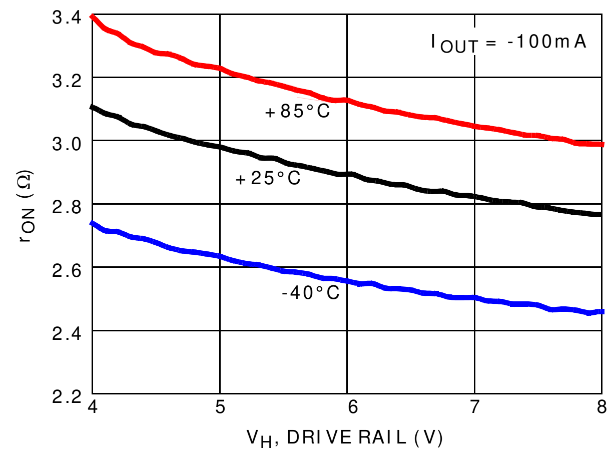


FIGURE 7. H1/H2 DRIVER SOURCE RESISTANCE vs VH

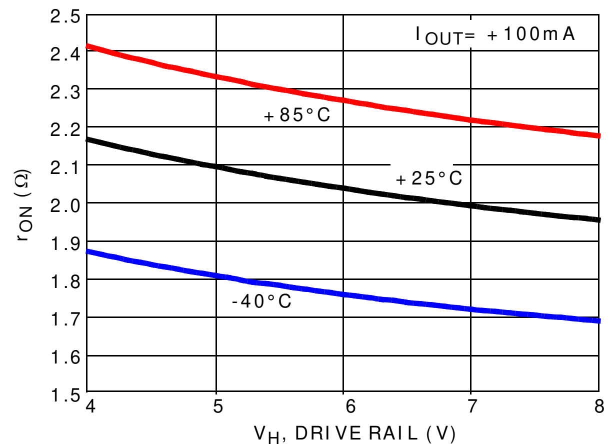


FIGURE 8. H1/H2 DRIVER SINK RESISTANCE VS VH

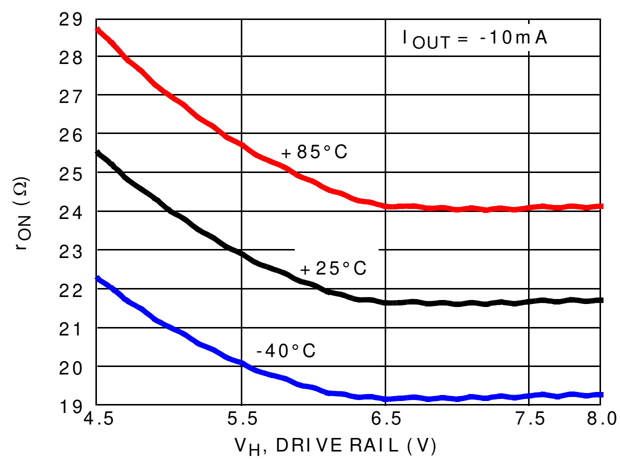


FIGURE 9. RG/HL DRIVER SOURCE RESISTANCE vs VH

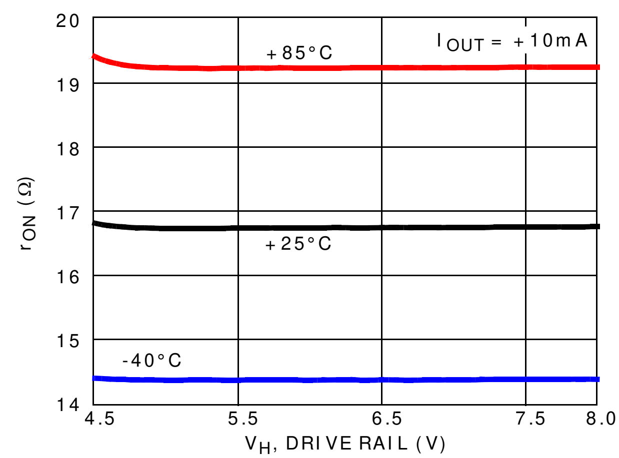


FIGURE 10. RG/HL DRIVER SINK RESISTANCE vs VH

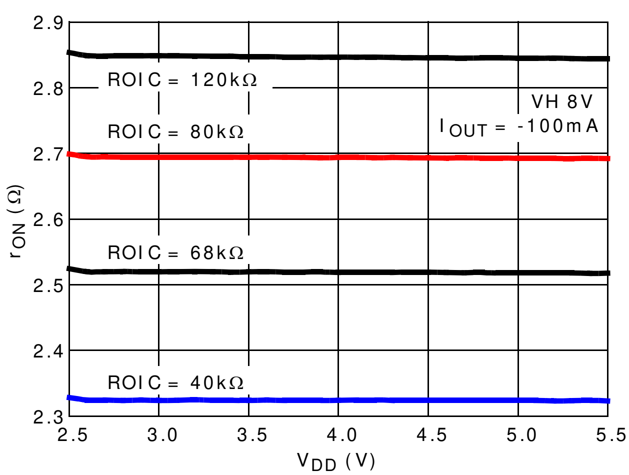


FIGURE 11. H1/H2 SOURCE RESISTANCE vs V_{DD}

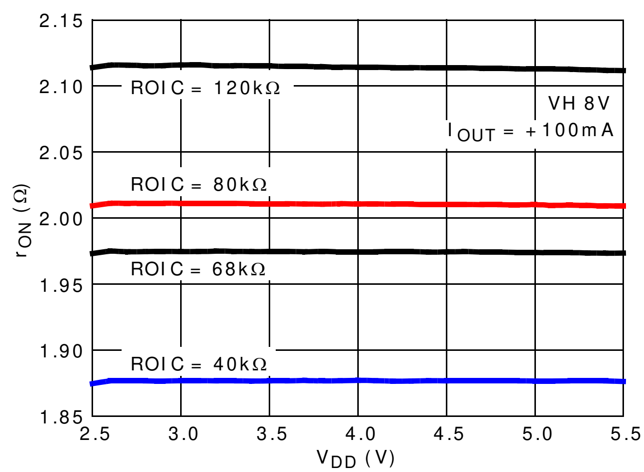


FIGURE 12. H1/H2 SINK RESISTANCE vs V_{DD}

Typical Performance Curves

VDD = 3.3V, VH = 4V, VN = -4V, R_{OIC} = 68kΩ, C_L = 300pF for H1/2OUT, C_L = 22pF for RG/HLOUT, Unless specified otherwise. Refer to Figures 1, 2 and 3. (Information derived from ISL55112 Evaluation board characterization. See AN1495 "ISL55112 High Speed Dual Precision CCD Driver Evaluation Board User Guide). (Continued)

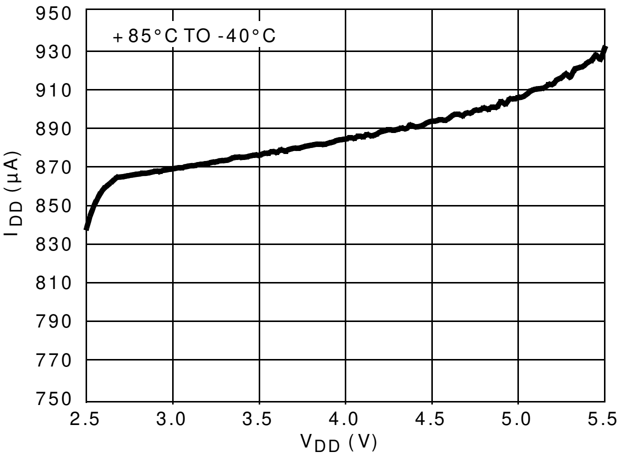


FIGURE 13. STAND BY CURRENT (Isb) I_{DD} vs V_{DD}

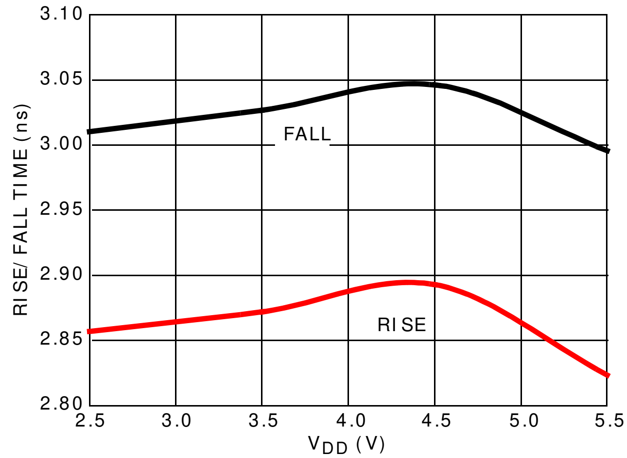


FIGURE 14. H1/H2 RISE AND FALL vs V_{DD}

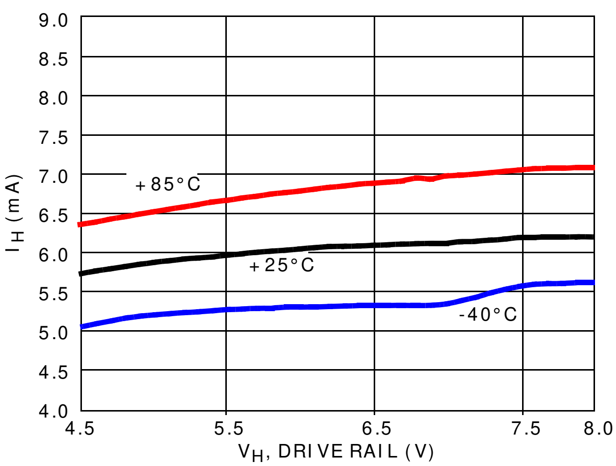


FIGURE 15. STAND BY CURRENT (Isb) I_H vs V_H

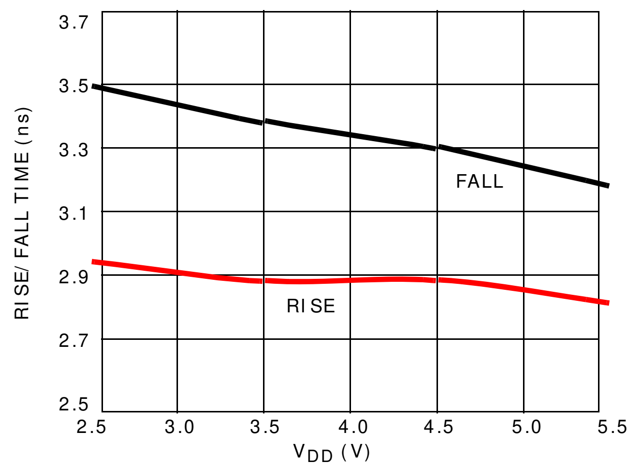


FIGURE 16. RG/HL RISE AND FALL vs V_{DD}

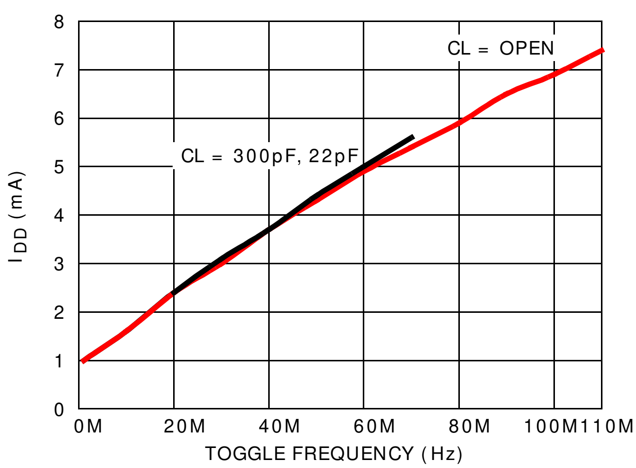


FIGURE 17. I_{DD} vs FREQUENCY (ALL OUTPUTS ACTIVE)

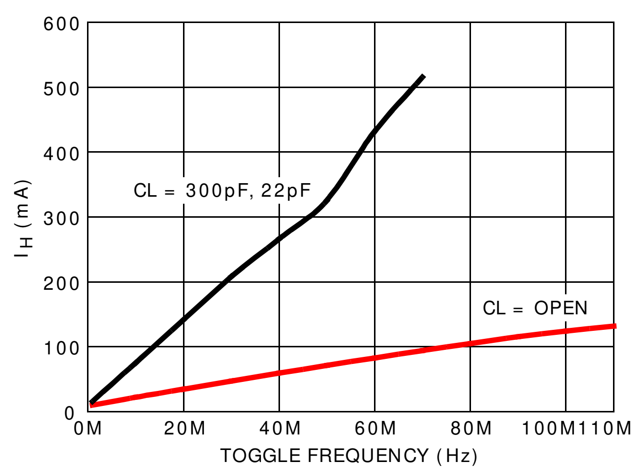


FIGURE 18. I_H vs FREQUENCY (ALL OUTPUTS ACTIVE)

Typical Performance Curves

VDD = 3.3V, VH = 4V, VN = -4V, R_{OIC} = 68kΩ, C_L= 300pF for H1/2OUT, C_L = 22pF for RG/HLOUT, Unless specified otherwise. Refer to Figures 1, 2 and 3. (Information derived from ISL55112 Evaluation board characterization. See AN1495 “ISL55112 High Speed Dual Precision CCD Driver Evaluation Board User Guide). (Continued)

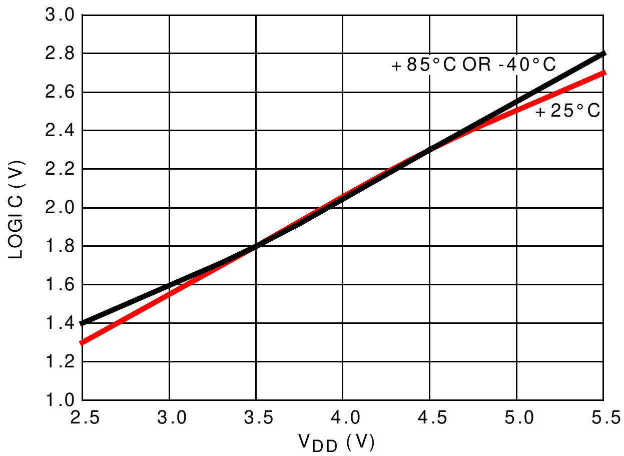


FIGURE 19. ALL INPUTS VIH LOGIC THRESHOLDS

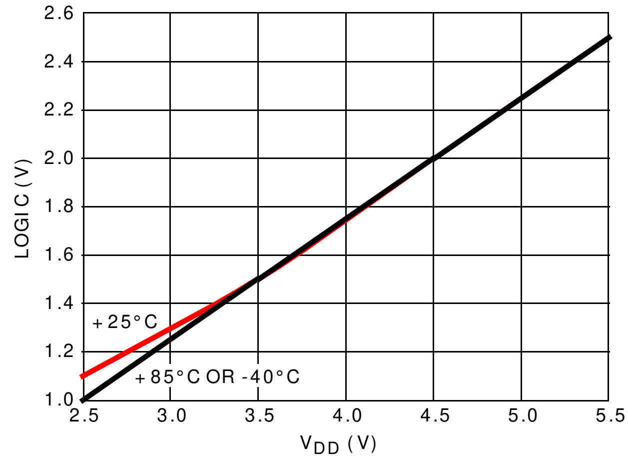


FIGURE 20. ALL INPUTS VIL LOGIC THRESHOLDS

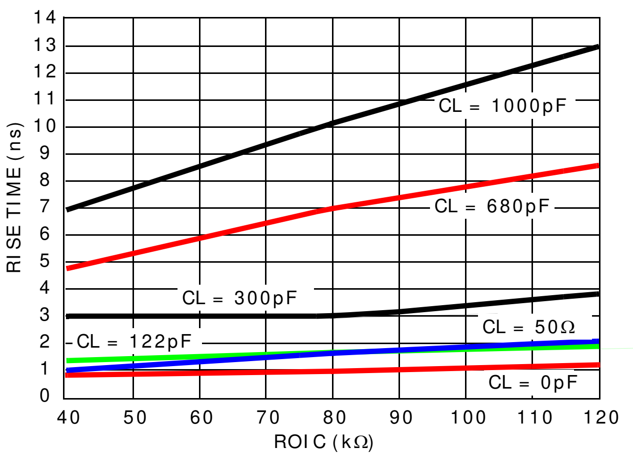


FIGURE 21. H1/H2 t_r vs ROIC vs C_L

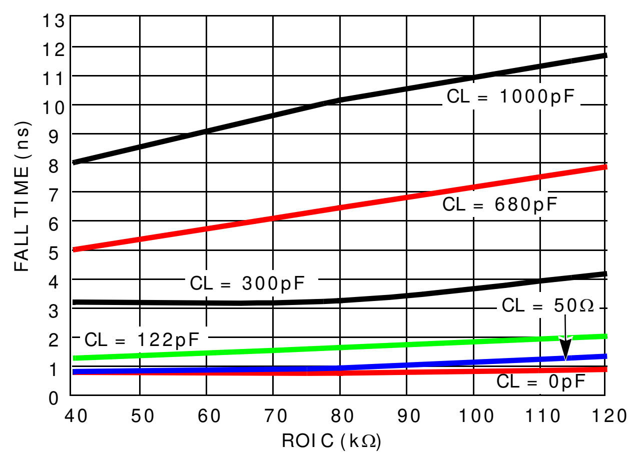


FIGURE 22. H1/H2 t_f vs ROIC vs C_L

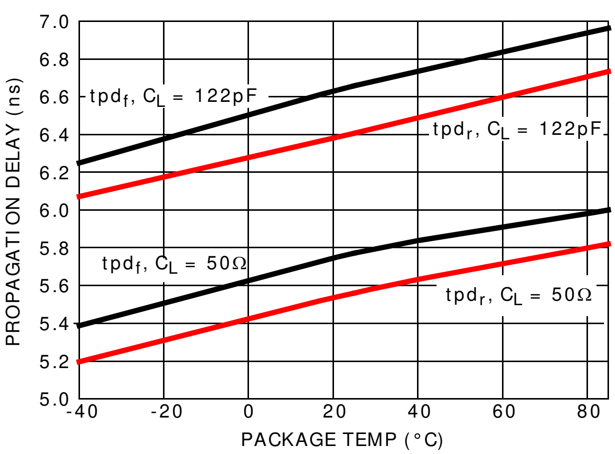


FIGURE 23. H1/H2 $tpd_{r/f}$ vs TEMPERATURE vs C_L

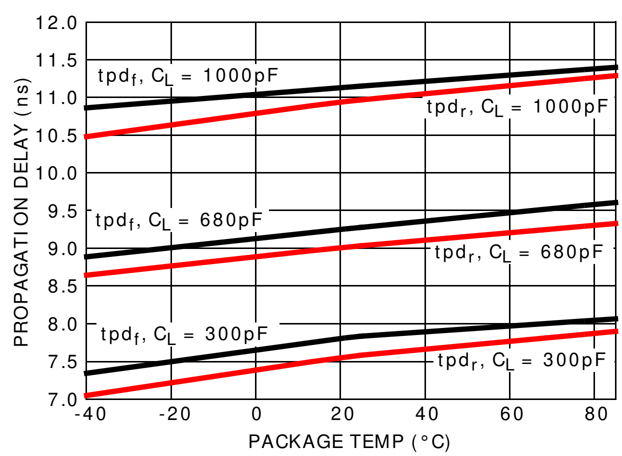


FIGURE 24. H1/H2 $tpd_{r/f}$ vs TEMPERATURE vs C_L

Typical Performance Curves

VDD = 3.3V, VH = 4V, VN = -4V, R_{OIC} = 68kΩ, C_L= 300pF for H1/2OUT, C_L = 22pF for RG/HLOUT, Unless specified otherwise. Refer to Figures 1, 2 and 3. (Information derived from ISL55112 Evaluation board characterization. See AN1495 "ISL55112 High Speed Dual Precision CCD Driver Evaluation Board User Guide). (Continued)

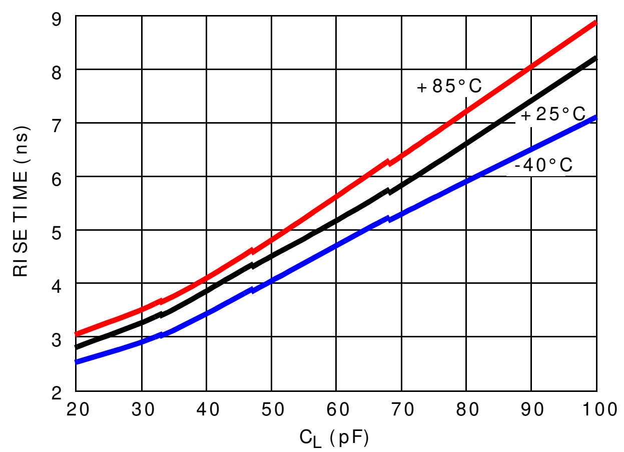


FIGURE 25. RG/HL t_r vs C_L

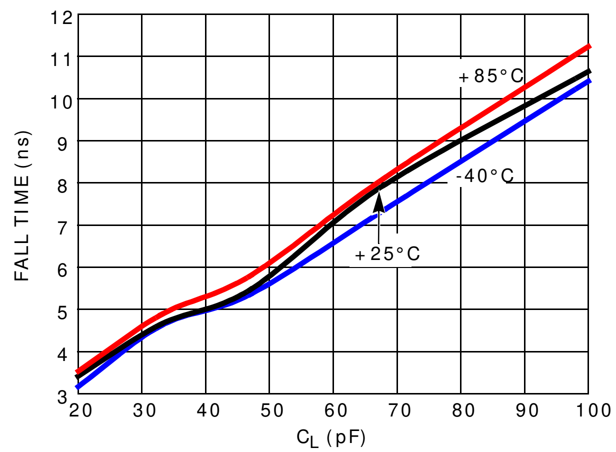


FIGURE 26. RG/HL t_f vs C_L

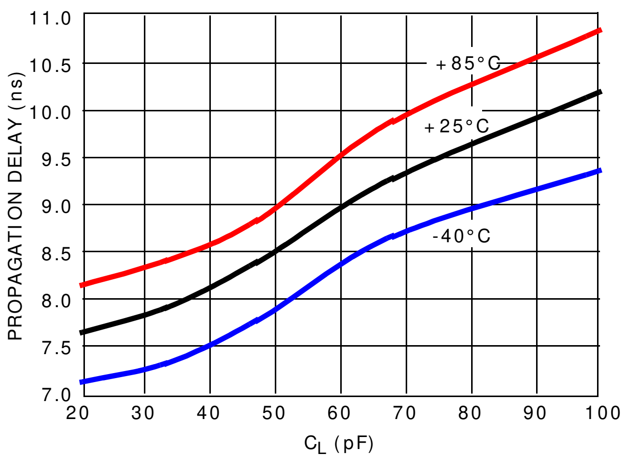


FIGURE 27. RG/HL tpd_r vs C_L

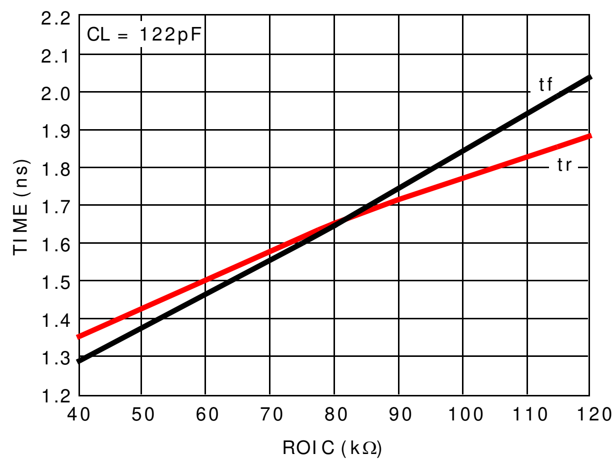


FIGURE 28. H1/H2 $t_{r/f}$ vs ROIC

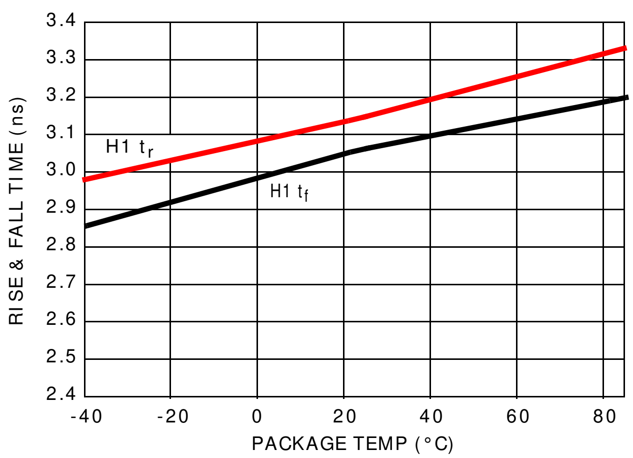


FIGURE 29. H1 t_r / t_f vs TEMPERATURE

Die Characteristics

SUBSTRATE AND TQFN THERMAL PAD POTENTIAL (POWERED UP):

VSUB

TRANSISTOR COUNT:

3900

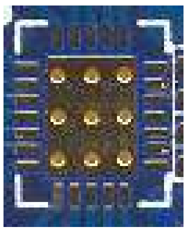
PROCESS:

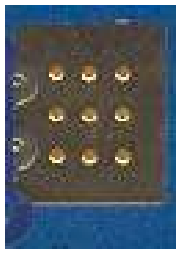
SUB MICRON CMOS

TQFN Package Discussion

Typically, power dissipation is a limiting factor in CCD array driving applications. The key tool in removing heat from the drivers is the thermal pad on the bottom of the TQFN package.

Electrically, this exposed pad is connected to the device substrate and is the most negative voltage. In applications where negative drive rails are used, this pad must be isolated from ground and connected to the negative bus. However, the size of the thermal pad and the associated voltage plane/layer it connects to determines the heat dissipation capability of the pad.


TOP VIEW


BOTTOM VIEW

The TQFN Thermal Pad is the main tool for dealing with Power Dissipation.

FIGURE 30. ISL55112 TQFN PAD LAYOUT EXAMPLE TOP AND BOTTOM VIEWS

The footprint for the ISL55112 should include a "Thermal Via Array" of through-holes. Hole size and spacing of these vias should maximize heat transfer to the bottom of the board and away from the device. Hole size should accommodate solder wicking requirements. The quantity of vias is limited by pad size and recommended spacing. Vias should also have a solid connection to the associated power plane.

Another item that affects thermal transfer is the layout on the bottom of the board. Circuit lands that run parallel with the package can actually become heat barriers. If signals are routed on the bottom, try to route signal paths (90°) away from the pad area. Make the exposed pad area as large as possible on the bottom layer. (Remember in negative voltage applications the pad needs to be electrically isolated from the ground plane.)

Reference Intersil TB389. *A grid of 1.0mm to 1.2mm pitch thermal vias, which drop down and connect to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 1.0 ounce copper. Although adding more vias (such as by decreasing via pitch) will improve thermal performance, diminishing returns will be seen as more and more vias are added. Therefore, simply use as many vias as practical for the thermal land size and your board design ground rules.*

Recommended Land Pattern (TQFN PCB Footprint)

Please refer to the Package Outline Drawing for recommended land size guidelines.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
1/26/10	FN6649.0	Added Related Documentation to page 1 On page 4: Changed Absolute Maximum rating from: "Supply Voltage (VPLUS and VSUB) . . . . 9.0V Supply Voltage (H1_VP/H2_VP/RG_VP/HL_VP - H1_VN/H2_VN/RG_VN/HL_VN)...9.0V" to: "Supply Voltage (VPLUS and VSUB) . . . . 16.0V Supply Voltage (H1_VP/H2_VP/RG_VP/HL_VP - H1_VN/H2_VN/RG_VN/HL_VN)...16.0V" Added "All Pin Voltages: (Note 6).....(VSUB - 0.5V) to (VPLUS + 0.5V)" Added Note 6 (Dynamic over/undershoot characteristics should be examined to ensure this condition is never exceeded. Driver undershoot with respect to V_{SUB} is especially important. In applications where extremely high driver current is needed, V_{SUB} may require a voltage below the most negative driver rail to avoid driver under shoot falling below V_{SUB}.) On page 4: Changed Note in "Recommended Operating Specifications" from: "NOTE: V_{PLUS} must be connected to most positive Driver Voltage Rail, V_{SUB} must be connected to the most negative voltage rail. V_{SUB} should be connected to ground where Driver Negative Supplies are above ground. H1_VN and H2_VN should be connected to each other and operated at the same voltage." to: NOTE: "V_{PLUS} must be connected to most positive voltage rail, V_{SUB} must be connected to the most negative voltage rail. V_{SUB} should be connected to ground where driver negative supplies are at or above ground. No voltage should occur on any pin less than V_{SUB} - 0.5V or greater than V_{PLUS} +0.5V. In applications where extremely high driver current is needed, V_{SUB} may require a voltage below the most negative driver rail to avoid driver under shoot falling below V_{SUB}." Updates to Electrical Specifications as follows: On page 5: VOH H drivers updated from Min/Max 3.90/3.95V to 3.91/4.00V VOL H drivers updated from Min/Max -3.95/-3.90V to -4.00/-3.91V On page 5: ROH H drivers updated from Max of 9Ω to 14Ω ROL H drivers updated from Max of 8Ω to 12Ω On page 6: VOH RG/HL updated from Max of 3.99V to 4V VOL RG/HL updated from Min of -3.99V to -4V On page 8: Updated Note 14 (Peak Currents) to include VP-VN test voltage. Added "VSUB Discussion" on page 10 On page 12: Updated Power-Down/Up Sequence to include "Stop"/"Start Clock Inputs"
9/23/09	FN6649.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL55112

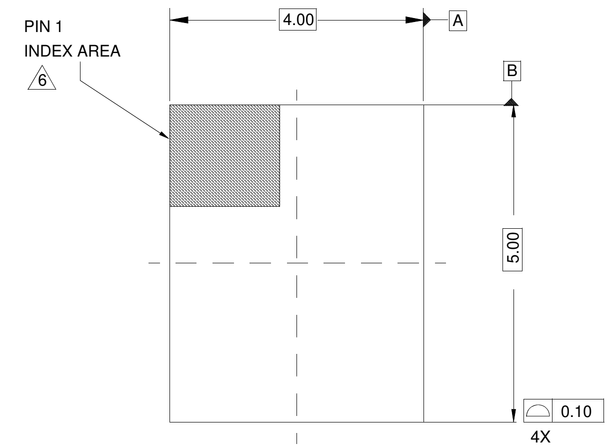
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

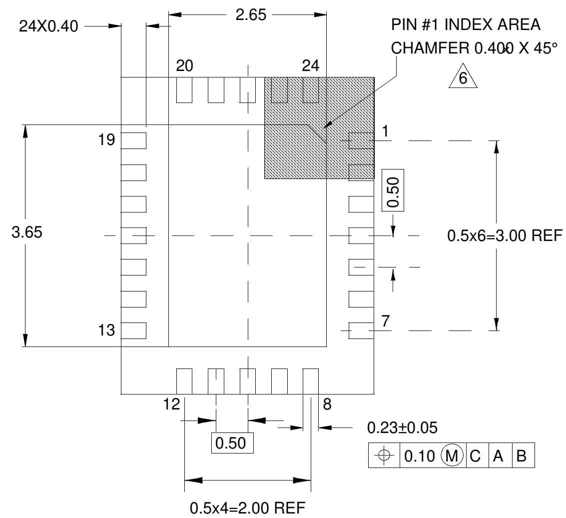
Package Outline Drawing

L24.4x5C

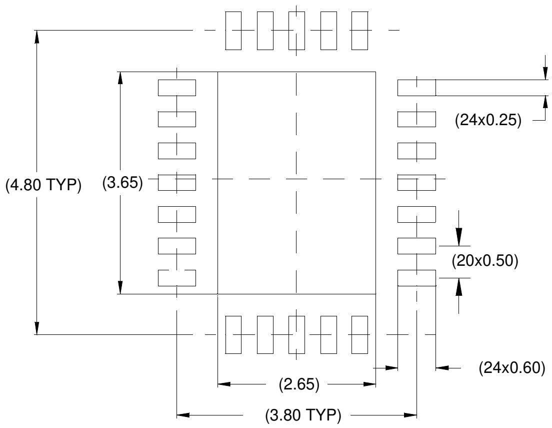
24 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 10/07



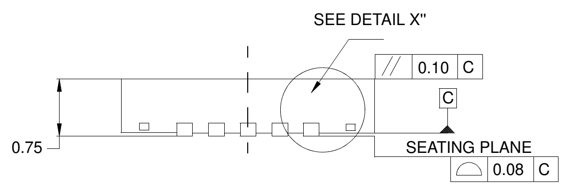
TOP VIEW



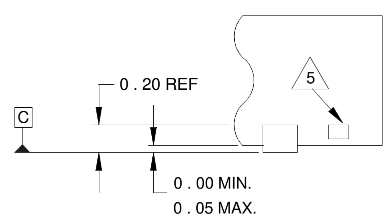
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.28mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.