Fully Digital-controlled Power Supply Control IC with Bridgeless PFC and LLC Current-resonant Circuits

MD6752

Data Sheet

Description

The MD6752 is a fully digital-controlled power supply IC, which incorporates a bridgeless PFC control circuit and an LLC current-resonant circuit. The PFC circuit, driven by continuous conduction mode (CCM), is controlled with frequencies suitable for applied input voltages and loads. The IC incorporates current mode for controlling constant voltages in the LLC stage and a floating drive circuit that drives an external high-side power MOSFET, in addition to functionally-rich protections. These digitally controlled strategies allow application-specific optimal settings. Compared to conventional analog control circuits, the IC can achieve more cost-effective, high-efficient, yet low-noise power systems with fewer external components.

Package

SOP28

Not to scale

Features

- Fully Digital-controlled PFC and LLC Current-resonant Circuits
- Soft Start
- Bridgeless PFC Circuit
- Continuous Conduction Mode (CCM) PFC Control
- Current Mode LLC Control
- Protections Include:

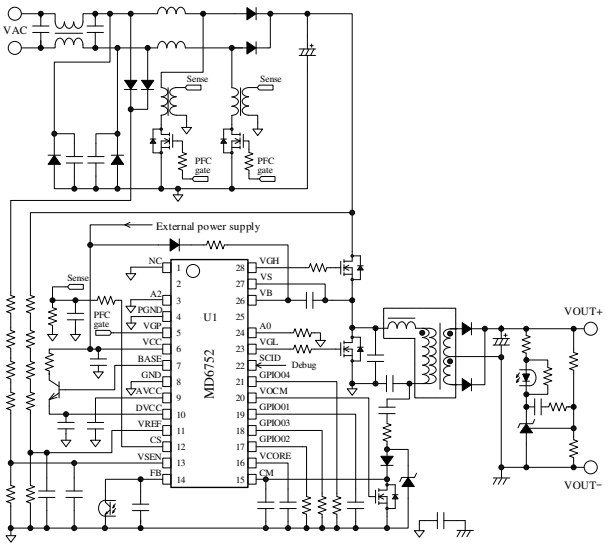
- AC Power Supply Input Undervoltage Lockout
- AC Power Supply Input Off-state Detection
- PFC Output Undervoltage Protection (PFC_UVP)
- PFC Output Overvoltage Protection (PFC_OVP)
- PFC Overcurrent Protection (PFC_OCP)
- PFC Overload Protection (PFC_OLP)
- LLC High-side Driver Undervoltage Lockout (VB_UVLO)
- LLC Overcurrent Protection (LLC_OCP)
- LLC Overload Protection (LLC_OLP)
- VCC Pin Overvoltage Protection (VCC_OVP)
- Thermal Shutdown (TSD)

Applications

For devices requiring high power supplies such as:

- Audiovisual Equipment
- Office Automation Equipment (e.g., Server, Multifunction Printer)
- Industrial Equipment
- Communication Equipment

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C. Surge withstand capability (HBM) of the MD6752 is guaranteed up to 2000 V. Note that the following pins are guaranteed to withstand surges up to 1000 V: 26, 27, 28.

Parameter	Symbol	Pin	Rating	Unit
A0 Pin Voltage	V_{A0}	24−8	−6.0 to 6.0	V
A2 Pin Voltage	V_{A2}	3−8	−6.0 to 6.0	V
PGND Pin Voltage	V_{PGND}	4−8	−0.3 to 0.3	V
VGP Pin Voltage	V_{GP}	5−8	−0.3 to V_{CC} + 0.3	V
VGP Pin Voltage ($t_W \leq 50$ ns)	$V_{GP(PULSE)}$	5−8	−1.5	V
VCC Pin Voltage	V_{CC}	6–8	−0.3 to 20	V
BASE Pin Voltage	V_{BASE}	7–8	−0.3 to 6.0	V
AVCC Pin Voltage[1][2]	V_{AVCC}	9–8	−0.3 to 3.6	V
DVCC Pin Voltage[2]	V_{DVCC}	10–8	−0.3 to 3.6	V
VREF Pin Voltage[3]	V_{REF}	11–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
CS Pin Voltage[3]	V_{CS}	12–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
VSEN Pin Voltage	V_{SEN}	13–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
FB Pin Voltage	V_{FB}	14–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
CM Pin Voltage	V_{CM}	15−8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
VCORE Pin Voltage[4]	V_{CORE}	16–8	−0.3 to 2.0[5]	V
GPIO02 Pin Voltage[6]	V_{GPIO02}	17–8	−0.3 to 5.5	V
GPIO02 Pin Current[6]	I_{GPIO02}	17–8	−4.0 to4.0	mA
GPIO03 Pin Voltage[6]	V_{GPIO03}	18–8	−0.3 to 5.5	V
GPIO03 Pin Current[6]	I_{GPIO03}	18–8	−4.0 to 4.0	mA
GPIO01 Pin Voltage[6]	V_{GPIO01}	19–8	−0.3 to 5.5	V
GPIO01 Pin Current[6]	I_{GPIO01}	19–8	−4.0 to 4.0	mA
VOCM Pin Voltage	V_{OCM}	20–8	−0.3 to 5.5	V
VOCM Pin Current	I_{VOCM}	20–8	−4.0 to 4.0	mA
GPIO04 Pin Voltage[6]	V_{GPIO04}	21–8	−0.3 to 5.5	V
GPIO04 Pin Current[6]	I_{GPIO04}	21–8	−4.0 to 4.0	mA
SCID Pin Voltage	V_{SCID}	22–8	−0.3 to 5.5	V
VGL Pin Voltage	V_{GL}	23–8	−0.3 to V_{CC} + 0.3	V
VB–VS Pin Voltage	V_{BS}	26–27	−0.3 to 20.0	V
VS Pin Voltage	V_S	27–8	−1 to 600	V
VGH Pin Voltage	V_{GH}	28–8	V_S − 0.3 to V_B + 0.3	V
Operating Ambient Temperature	T_{OP}	—	−40 to 85	°C
Storage Temperature	T_{STG}	—	−40 to 125	°C
Junction Temperature	T_J	—	125	°C

[1] The AVCC pin is the 3.3 V power supply output pin dedicated for the internal LSI chip. Do not apply external voltage to this pin.
[2] Electric potential difference between the AVCC and DVCC pins should be maintained within ±0.3 V （t > 1 ms).
[3] Refers to an analog input pin for 3.3 V systems.
[4] The VCORE pin is the 1.8 V power supply output pin dedicated for digital circuits of the internal LSI chip. Do not apply external voltage to this pin.
[5] Should be rated from −0.3 V to 2.4 V when t < 1 ms (e.g., at startup).
[6] Refers to a digital output pin for 3.3 V systems.

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 17 V.

The checkmark in the Chg. column indicates that the item is dedicated GUI-changeable. In addition, the characteristic value in this column is a reference value.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
Startup Circuit, Circuit Current								
Operation Start Voltage	$V_{CC(ON)}$		6–8	13.0	14.0	15.0	V	
Operation Stop Voltage[1]	$V_{CC(OFF)}$		6–8	7.4	8.3	9.2	V	
Circuit Current in Operation	$I_{CC(ON)}$		6–8	—	1.8	4.0	mA	
Circuit Current in Non-operation	$I_{CC(OFF)}$	V_{CC} = 11 V	6–8	—	0.5	1.0	mA	
VCC Pin Protection Release Threshold Voltage[1]	$V_{CC(P.OFF)}$		6–8	7.4	8.3	9.2	V	
Circuit Current in Protection Operation	$I_{CC(P)}$	V_{CC} = 10 V	6–8	—	0.5	1.0	mA	
VCORE Pin Supply Voltage	V_{CORE}		16–8	1.72	1.80	1.88	V	
SCID Pin High Level Detection Voltage[2]	V_{SCID_IH}		22–8	2.0	—	—	V	
SCID Pin Low Level Detection Voltage[2]	V_{SCID_IL}		22–8	—	—	0.8	V	
3.3 V Analog Internal Regulator	V_{AVCC}		9–8	3.233	3.300	3.366	V	
3.3 V Digital Internal Regulator	V_{DVCC}		10–8	3.135	3.300	3.465	V	
External Transistor Drive Voltage for DVCC Pin	V_{BASE}	I_{BASE} = −1 mA	7–8	3.6	—	4.4	V	
VSEN Pin Input UVP Threshold Voltage	$V_{SEN(OFF)}$		13–8	0.43	0.47	0.51	V	✓
VSEN Pin Input UVP Release Voltage	$V_{SEN(ON)}$		13–8	0.52	0.56	0.60	V	✓
VSEN Pin AC Input Voltage Off-state Detection Voltage	$V_{SEN(AC\_OFF)}$		13–8	0.16	0.19	0.22	V	✓
Delay Time of VSEN Pin Input UVP Detection	$t_{VSEN(OFF)}$		13–8	9.5	10.0	10.5	ms	✓
Delay Time of VSEN Pin AC Input Voltage Off-state Detection	$t_{VSEN(AC\_OFF)}$		13–8	21.8	23.0	24.2	ms	✓
PFC Stage								
PFC Drive Current (Source)	$I_{GP(SRC)}$	V_{CC} = 17 V, V_{GP} = 0 V	5–4	—	−500	—	mA	
PFC Drive Current (Sink)	$I_{GP(SNK)}$	V_{CC} = 17 V, V_{GP} = 17 V	5–4	—	1	—	A	
CS Pin OCP Threshold Voltage (Low)	$V_{CS(LO)}$	V_{IN} = 90 VAC	12–8	1.60	1.69	1.78	V	✓

[1] $V_{CC\ (OFF)} = V_{CC\ (P.OFF)}$

[2] Guaranteed by design.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
CS Pin OCP Threshold Voltage (High)	$V_{CS(HI)}$	V_{IN} = 260 VAC	12–8	0.65	0.71	0.77	V	✓
Number of OVP Operation Times	$N_{OPP(AC)}$		5–8	—	32	—	Times	✓
VREF Pin Threshold Voltage for PFC Output Control	V_{REF}		11–8	2.009	2.096	2.183	V	✓
Maximum PFC Oscillation Frequency	f_{MAX_PFC}		5–8	190	200	210	kHz	✓
Minimum PFC On-time	$t_{ON(MIN)\_PFC}$		5–8	0.28	0.30	0.32	µs	✓
Minimum PFC Off-time	$t_{OFF(MIN)\_PFC}$		5–8	0.28	0.30	0.32	µs	✓
Maximum PFC On-time	$t_{ON(MAX)\_PFC}$		5–8	20.8	21.9	23.0	µs	✓
Maximum PFC Off-time	$t_{OFF(MAX)\_PFC}$		5–8	14.2	14.9	15.7	µs	✓
VREF Pin PFC_UVP Start Voltage	$V_{REF(UVD)}$		11–8	—	V_{REF}−0.08	—	V	
VERF Pin PFC_UVP Oscillation Stop Voltage	$V_{REF(UVP)}$		11–8	1.05	1.10	1.15	V	✓
VREF Pin PFC_UVP Release Voltage	$V_{REF(UVP\_R)}$		11–8	0.51	0.55	0.59	V	✓
PFC_UVP Recovery Delay Time	$t_{(UVP\_R)}$		—	778	819	860	ms	✓
VREF Pin PFC_OVP Start Voltage	$V_{REF(OVD)}$		11–8	—	V_{REF}+0.08	—	V	
VREF Pin PFC_OVP Oscillation Stop Voltage	$V_{REF(OVP)}$		11–8	2.14	2.23	2.33	V	✓
VREF Pin PFC_OVP Oscillation Stop Release Voltage	$V_{REF(OVP\_R)}$		11–8	2.09	2.18	2.27	V	✓
LLC Stage								
Maximum FB Pin Source Current	$I_{FB(MAX)}$	V_{FB} = 0 V	14–8	−440	−330	−250	µA	
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		26–27	5.8	6.8	7.8	V	
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		26–27	5.4	6.4	7.4	V	
LLC Drive Current (Source)	$I_{GL(SRC)}$ $I_{GH(SRC)}$	V_{CC} = 17 V, V_B = 17 V, V_{GL} = 17 V, V_{GH} = 17 V	23–4 28–8	—	–300	—	mA	
LLC Drive Current (Sink)	$I_{GL(SNK)}$ $I_{GH(SNK)}$	V_{CC} = 17 V, V_B = 17 V, V_{GL} = 0 V, V_{GH} = 0 V	23–4 28–8	—	550	—	mA	
VREF Pin LLC Operation Start Voltage	$V_{REF(LLC\_ON)}$		11–8	1.85	1.93	2.01	V	✓
VREF Pin LLC Operation Stop Voltage	$V_{REF(LLC\_OFF)}$		11–8	1.26	1.32	1.39	V	✓
LLC Maximum Oscillation Frequency during Soft Start Operation	$f_{MAX\_LLC(SS)}$		23–4 28–8	385	405	426	kHz	✓
Current Mode Operation Start LLC Oscillation Frequency during Soft Start Operation	$f_{LLC(CM)}$		23–4 28–8	190	200	210	kHz	✓
Lowest LLC Oscillation Frequency	f_{MIN_LLC}		23–4 28–8	55.7	58.6	61.5	kHz	✓

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
Highest LLC Oscillation Frequency	f_{MAX_LLC}		23–4 28–8	190	200	210	kHz	✓
Minimum LLC Dead Time	$t_{d(MIN)}$		23–4 28–8	0.44	0.47	0.49	µs	✓
Maximum LLC Dead Time	$t_{d(MAX)}$		23–4 28–8	0.53	0.56	0.59	µs	✓
Current Mode Control Minimum CM Pin Voltage	$V_{CM(MIN)}$		15–8	0.06	0.10	0.15	V	✓
Current Mode Control Maximum CM Pin Voltage	$V_{CM(MAX)}$		15–8	1.90	2.00	2.10	V	✓
Current Mode Control Maximum CM Pin Voltage during LLC Undervoltage	$V_{CM(UV\_MIN)}$		15–8	2.66	2.78	2.91	V	✓
OLP Operation Start FB Pin Voltage	$V_{FB(OLP)}$		14–8	2.89	3.00	3.12	V	✓
OLP Delay Time 1	t_{OLP1}		15–8	4.7	5.0	5.3	ms	✓
OLP Delay Time 2	t_{OLP2}		15–8	0.1	0.2	0.3	ms	✓
Protection Recovery Time	t_{AR}		15–8	2850	3000	3150	ms	✓
Overvoltage Protection (OVP)								
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		6–8	18.1	19.0	19.7	V	
External Shutdown								
A0 Pin Operation Stop Threshold Voltage	V_{A0}		24–8	1.18	1.25	1.32	V	✓
A0 Pin Protection Delay Time	t_{A0}		24–8	—	1000	—	ms	✓
A0 Pin Offset Voltage[3]	$V_{A0(OFS)}$	V_{A0} = 0 V	24–8	—	1.65	—	V	
Digital General-purpose I/O								
A2 Pin Offset Voltage[4]	$V_{A2(OFS)}$	V_{A2} = 0 V	3–8	—	0.6	—	V	
GPIO Pin High Level Detection Voltage	V_{IH}		[5]	2.0	—	—	V	
GPIO Pin Low Level Detection Voltage	V_{IL}		[5]	—	—	0.8	V	
Digital Pull-up Resistor	R_{PUP}		[5]	20	60	100	kΩ	
Analog Pull-up Resistor (FB, CM)	R_{PUP2}		14–8 15–8	7.9	10.0	12.4	kΩ	
Input Leakage Current	I_L	V_{REF} = 0 V V_{SEN} = 0 V	11–8 13–8	−2	±1	2	µA	
GPIO Pin High Level Output Voltage	V_{OH4}	I_{OH} = −4 mA	[5]	2.4	—	—	V	
GPIO Pin Low Level Output Voltage	V_{OL4}	I_{OH} = 4 mA	[5]	—	—	0.4	V	
Clock Operation								
Internal IRC Oscillation Frequency	f_{IRC}		—	11.64	12.00	12.18	MHz	
Thermal Shutdown (TSD)								

[3] See Figure 2-2.
[4] See Figure 2-1.
[5] Refers to voltage between the GND pin and all the following pins: GPIO02, GPIO03, GPIO01, GPIO04.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
TSD Operating Temperature[6]	$T_{J(TSD)}$		—	125	—	—	°C	
Thermal Characteristic								
Junction-to-Air Thermal Resistor	θ_{J-A}		—	—	—	85	°C/W	

[6] Guaranteed by design.

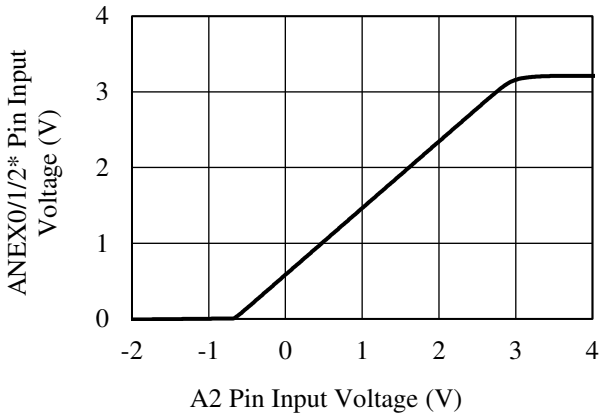


Figure 2-1. A2 Pin Offset

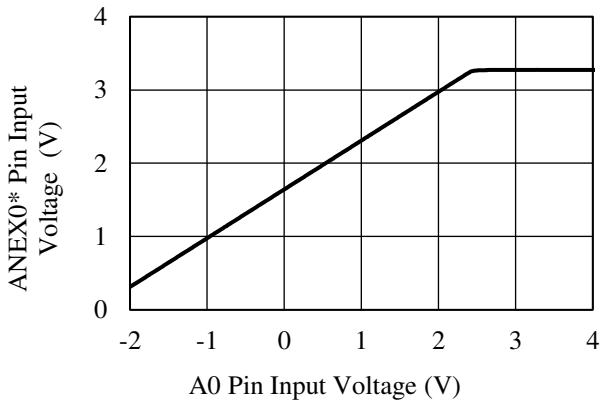
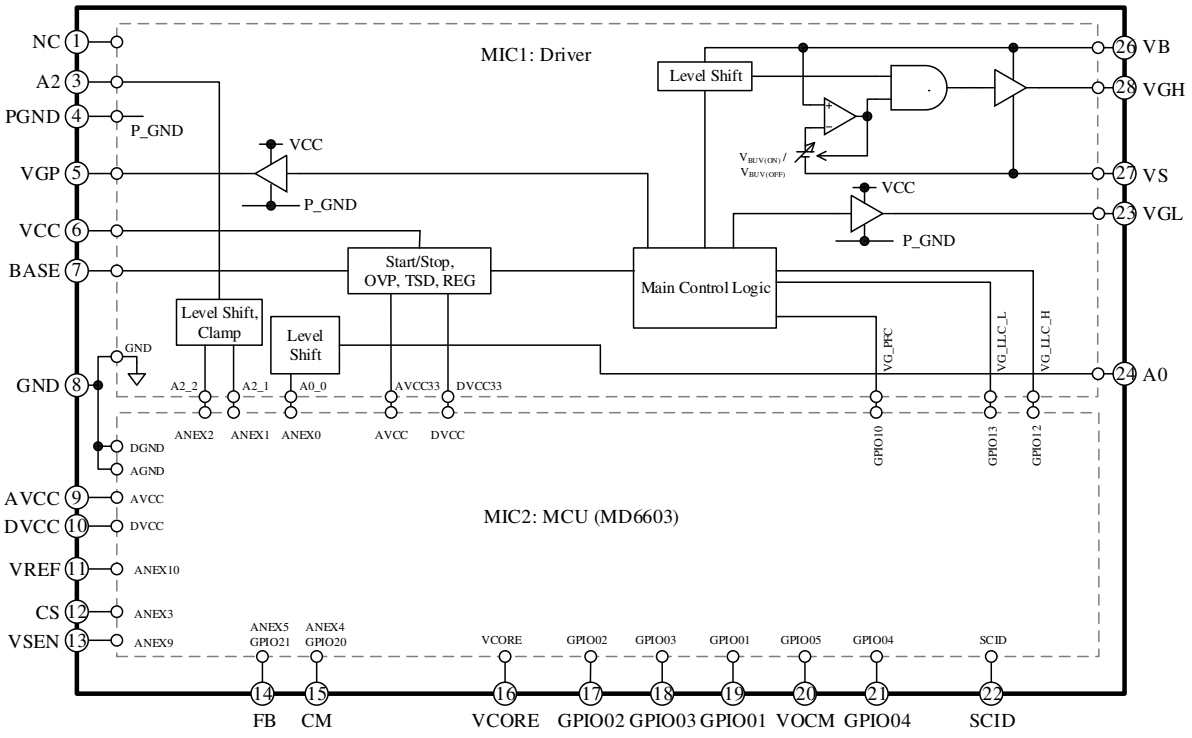


Figure 2-2. A0 Pin Offset

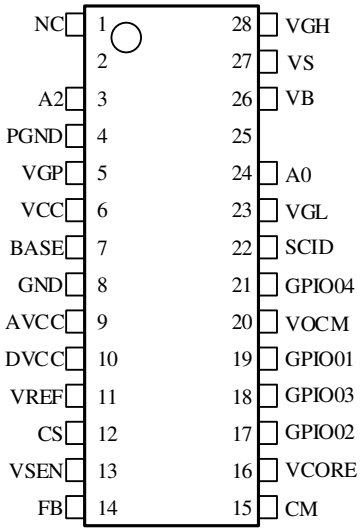
* Indicates voltages inside the IC; see the block diagram in Section 3.

3. Block Diagram



4. Pin Configuration Definitions

Top View



No.	Name	Description
1	NC	No connection (connect to the logic ground)
2	—	Pin removed
3	A2	Analog input
4	PGND	Power ground
5	VGP	PFC gate drive output
6	VCC	Logic power supply input; VCC_OVP
7	BASE	External transistor base voltage output for the DVCC pin
8	GND	Ground
9	AVCC	3.3 V analog power supply
10	DVCC	3.3 V digital power supply
11	VREF	PFC constant voltage control signal input; PFC_UVP / PFC_OVP
12	CS	PFC_OCP signal input
13	VSEN	Input voltage detection signal input
14	FB	Power MOSFET control signal input; LLC_OLP
15	CM	Current mode detection signal input, LLC overcurrent protection (OCP) detection signal input
16	VCORE	Capacitor connection for internal digital circuit supplies
17	GPIO02	General-purpose I/O pin
18	GPIO03	General-purpose I/O pin
19	GPIO01	General-purpose I/O pin
20	VOCM	Current mode control signal input
21	GPIO04	General-purpose I/O pin
22	SCID	Debugging pin (left open if not used)
23	VGL	LLC low-side gate drive output
24	A0	Analog input (External Shutdown Input)
25	—	Pin removed
26	VB	Power supply input for LLC high-side gate drive with UVLO; VB_UVLO signal input
27	VS	Floating ground of LLC high-side driver
28	VGH	LLC high-side gate drive output

5. Typical Application

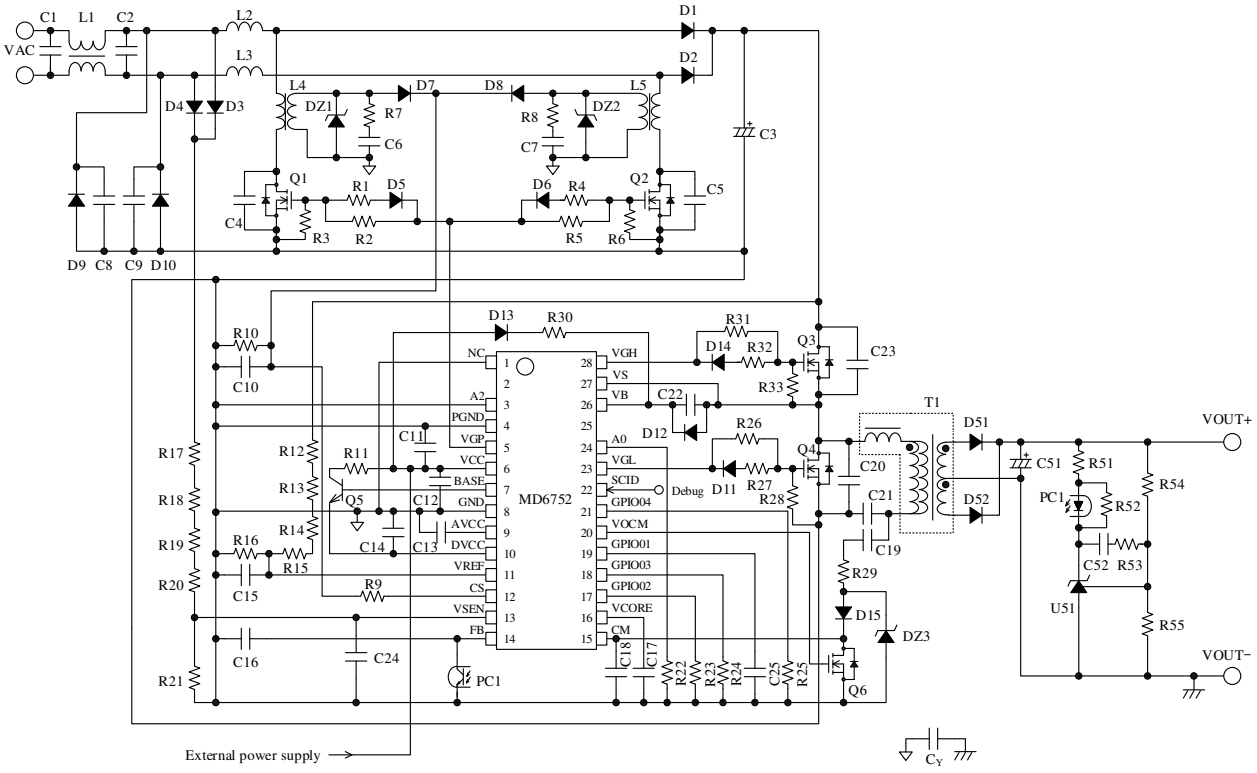


Figure 5-1. Typical Application

6. Physical Dimensions

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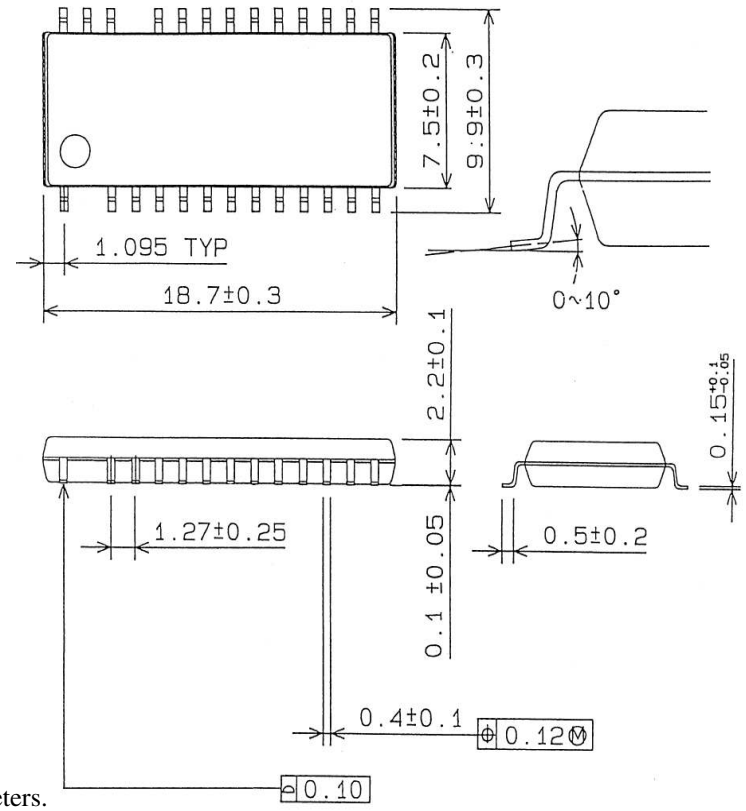
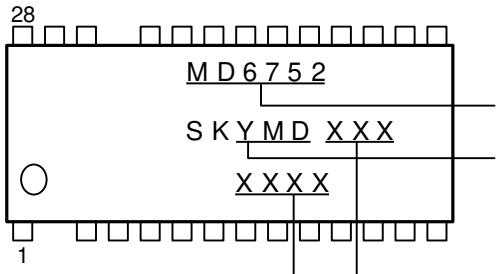


NOTES:
- Dimension is in millimeters.
- Pb-free

7. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is the period of days represented by:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

8. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 2 and the electronic symbol names of the typical application in Section 5.

8.1. General Description

The MD6752 digitally controls a PFC circuit and an LLC current-resonant circuit.

The PFC circuit embedded in the IC requires no input rectifier bridge for its own controlling. The PFC circuit, driven by continuous conduction mode (CCM) in normal operation, is controlled with the frequencies suitable for applied input voltages and loads. By monitoring the output voltage of the PFC circuit with the VREF pin, the IC controls the VGP pin on-time and provides regulated outputs.

The IC has a built-in high-side driver that drives the LLC half-bridge circuit. By monitoring the secondary output voltage through an optocoupler, which is connected to the FB pin, the IC controls the oscillation frequencies of the VGH and VGL pins to provide regulated outputs (Section 8.10). Moreover, software-supported dead time setting is available for the MD6752 (Section 8.11).

Protections in the PFC stage include the overcurrent and overload protections (Section 8.7), the overvoltage protection (Section 8.8), and the undervoltage protection (Section 8.9). Protections in the LLC stage include the high-side driver undervoltage lockout (Section 8.12), and the overcurrent and overload protections (Section 8.13).

In addition to the protections above, the IC also has the following functions: the soft start function (Section 8.4), the VCC pin overvoltage protection (to prevent secondary outputs from overvoltage; see Section 8.6), and the thermal shutdown (Section 8.14).

8.2. Pin Descriptions

8.2.1. A0

This pin is used for analog input and external shutdown input. The A0 pin should be used within the range of absolute maximum ratings (see Section 1). When the A0 pin voltage, V_{A0} = 1.25 V or more, and remains in this condition for 1000 ms or longer, the oscillation operations of the VGH, VGL, and VGP pins are stopped. When the Protection Recovery Time, t_{AR} = 3000 ms or longer, elapses after that, the IC releases the protection and restarts to operate.

Connect the pull-down resistor, R22 (about 1 kΩ), to the logic ground, if not used.

8.2.2. A2

This is the input pin for analog signals. The A2 pin is internally connected to the comparator and the AD converter. Connect this pin to the logic ground or a capacitor of about 0.01 µF, if not used. For more details, refer to the MD6603 data sheet.

8.2.3. GND and PGND

The GND pin is the logic ground pin of the IC; the PGND pin is the power ground pin where driving currents for an external power MOSFET flow through. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, extreme care should be taken in designing a PCB so that currents from the power ground do not affect these pins. For the notes on PCB pattern layouts, see Section 10.

8.2.4. VGP

This is the drive output pin for driving the power MOSFETs (Q1, Q2) in the PFC stage. The pin should be connected to the gates of Q1 and Q2. Respective drive currents are defined as follows: the PFC Drive Current (Source), $I_{GP(SRC)}$ = −500 mA; the PFC Drive Current (Sink), $I_{GP(SNK)}$ = 1 A.

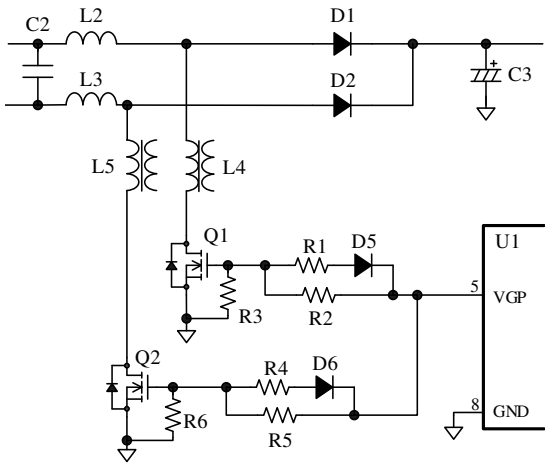


Figure 8-1. VGP Pin and Its Peripheral Circuit

The description hereafter holds up the peripheral circuit of Q1 as an example (but is also applicable to Q2). To increase a rising speed of the gate at power MOSFET turn-off, connect the diode D5 as shown in Figure 8-1. D5, R1, and R2 should be adjusted based on

the operation performance checked with an actual board, including a loss in the power MOSFET, gate waveform (e.g., ringing due to pattern layout), and EMI noise. To prevent malfunction caused by steep dv/dt at power MOSFET turn-off, connect R3, of about 10 kΩ to 100 kΩ, between the gate and source of the power MOSFET with a minimal length of traces.

8.2.5. VCC

This is the power supply pin for the built-in control MICs, and is connected to an external power supply. When the VCC pin voltage increases to $V_{CC(ON)}$ or more, the IC starts operating. When the VCC pin voltage decreases to $V_{CC(OFF)}$ or less, the IC stops operating. This sequence of operations is the VCC pin undervoltage lockout (VCC_UVLO). In addition to this function, the VCC pin also has the VCC pin overvoltage protection (VCC_OVP).

Section 8.3 describes the startup operation of the IC; Section 8.6 provides more details on the VCC_OVP. To prevent malfunction induced by supply ripples or other factors, connect 0.01 µF to 0.1 µF ceramic capacitors, C11 and C12, between the VCC and PGND pins, and between the VCC and GND pins, respectively, with a minimal length of traces.

8.2.6. DVCC and BASE

The DVCC pin is the internal 3.3 V digital power supply pin. As Figure 8-2 illustrates, the DVCC pin power is supplied from the external power supply through an external transistor. The BASE pin is connected to the base of this external transistor. To reduce noises on the DVCC pin, connect the capacitor C14 with a capacitance of about 0.47 µF.

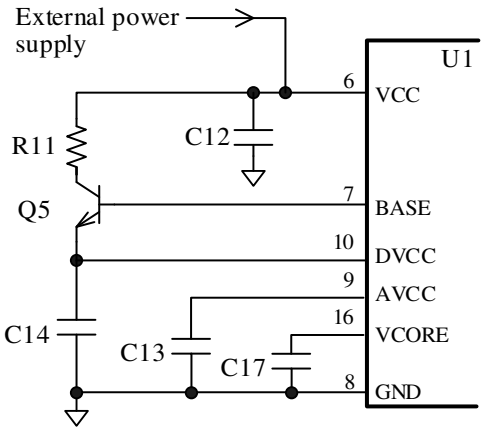


Figure 8-2. Power Stage and Its Peripheral Circuit

8.2.7. AVCC

The AVCC pin is the internal 3.3 V analog power supply pin. The capacitor C13 in Figure 8-2 should have a capacitance of about 0.47 µF. Do not connect anything but C13 to the AVCC pin.

8.2.8. VREF

As shown in Figure 8-3, the output voltage of the PFC stage, $V_{OUT(PFC)}$, divided by the detection resistors is applied to the VREF pin. Signals input to the VREF pin are used for the constant voltage control in the PFC stage, the overvoltage protection (Section 8.8), and the undervoltage protection (Section 8.9). $V_{OUT(PFC)}$ is determined by the detection resistors, R12 to R16, and can be calculated by the equation below:

$$V_{OUT(PFC)} = \left(\frac{R_{REF1}}{R_{REF2}} + 1\right) \times V_{REF} . \quad (1)$$

Where:

V_{REF} is the VREF pin threshold voltage (2.10 V),
R_{REF1} is the combined resistance of the resistors R12 to R15, and
R_{REF2} is the resistance of R16 (≈ 10 kΩ to 68 kΩ).

The resistors of R_{REF1} are set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure R_{REF1} with some serial resistors to reduce each applied voltage.

R16 should be adjusted based on the operation performance checked with an actual board, including a PFC output, overvoltage protection, and undervoltage protection.

To reduce switching noises, connect the capacitor C15 with a capacitance of about 100 pF to 1000 pF, as near as possible to the VREF pin.

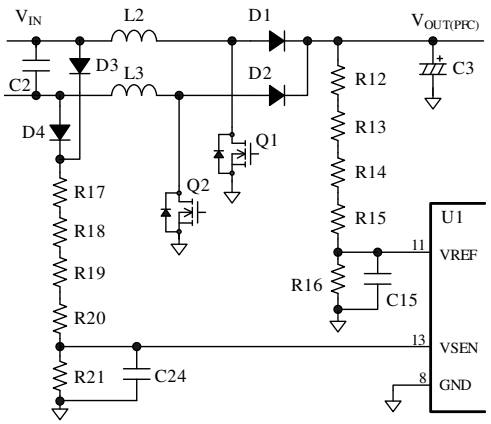


Figure 8-3. VREF and VSEN Pins and Their Peripheral Circuit

8.2.9. CS

This pin serves as a drain current detector of the power MOSFET in the PFC circuit. In the PFC circuit, which supports high-power applications, current through the power MOSFET is usually detected by the current transformers (L4, L5) as in Figure 8-4. Then, a detection signal is input to the CS pin. Current detection signals transmitted from the CS pin are used for the protections against overcurrent and overload conditions. Section 8.7 provides detailed descriptions on the setting of constants for the CS pin peripheral circuit, the PFC overcurrent protection, and the PFC overload protection.

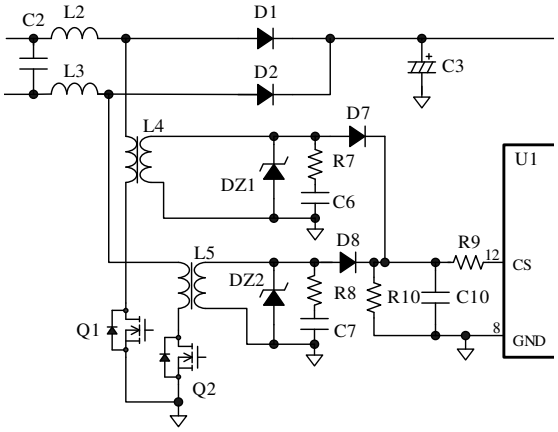


Figure 8-4. CS Pin and Its Peripheral Circuit

8.2.10. VSEN

As shown in Figure 8-3, the input voltage, V_{IN}, divided by the detection resistors is applied to the VSEN pin. Signals input to the VSEN pin are used for the undervoltage lockout and the input voltage off-state detection. For more detailed functional descriptions and the setting of peripheral constants for the VSEN pin, see Section 8.5.

8.2.11. FB

This pin is used for controlling LLC output voltage to be constant. As Figure 8-5 shows, the optocoupler PC1 and the capacitor C16 should be connected to the FB pin. The FB pin controls the on-times of the high- and low-side power MOSFETs (duty cycle = 50%).

Section 8.10 provides more details on the constant voltage control.

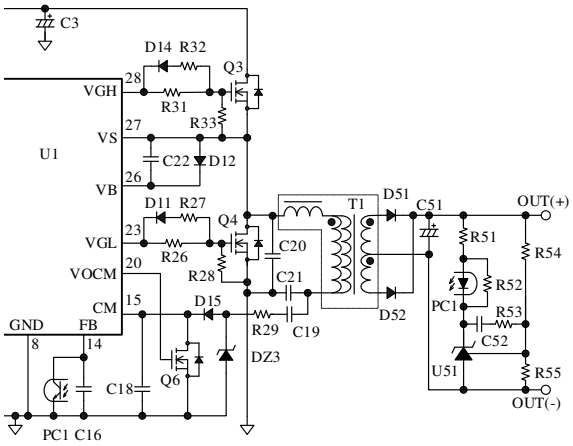


Figure 8-5. LLC Circuit

8.2.12. CM

The CM pin detects the current flowing to the power MOSFET of the LLC stage. The detected signals are used for the current mode control and the LLC overcurrent protection. Section 8.10 explains the settings of peripheral circuit for the CM pin; Section 8.13 gives a detailed explanation on the LLC overcurrent protection.

8.2.13. VCORE

The VCORE pin is the internal 1.80 V power supply pin. The capacitor C17 should have a capacitance of 0.1 µF. Do not connect anything but C17 to the VCORE pin.

8.2.14. GPIO01 to GPIO04

These pins are the general-purpose I/O pins. For more details, refer to the MD6603 data sheet.

The GPIO1 pin controls the LLC stage on/off operation. The capacitor C25 should have a capacitance of 0.01 µF. When the GPIO1 pin becomes logic high, the LLC stage turns on. When the GPIO1 pin becomes logic low, the LLC stage turns off.

The GPIO04 pin has the AC power supply input off-state detection function, which outputs a signal at AC power supply cutoff (see Section 8.5). GPIO02 to GPIO04 pins must be all connected to the GND pin if not used.

8.2.15. VOCM

The VOCM pin is connected to the gate of the power MOSFET (Q6) for small-signal used for current mode control as shown in Figure 8-5. For more detailed setting of peripheral circuit for the VOCM pin, see Section 8.10.

8.2.16. SCID

This is the debugging pin. For detailed functional descriptions, such as software debugging, and software programming (erasing and writing) to the programs on the flash memory, refer to the MD6603 data sheet. Leave this pin open if not used.

8.2.17. VGL and VGH

These pins are the drive output pins for driving the power MOSFETs in the LLC stage. The VGL pin acts as a low-side driver, whereas the VGH pin acts as a high-side driver. Respective drive currents are defined as follows: the LLC Drive Current (Source), $I_{GL(SRC)} = I_{GH(SRC)} = -300$ mA; the LLC Drive Current (Sink), $I_{GL(SNK)} = I_{GH(SNK)} = 550$ mA.

The description hereafter holds up the peripheral circuit of Q4 as an example (but is also applicable to Q3). To increase a falling speed of the gate at power MOSFET turn-off, connect the diode D11 as shown in Figure 8-5. R26, R27, and D11 should be adjusted based on the operation performance checked with an actual board, including a loss in the power MOSFET, gate waveform (e.g., ringing due to pattern layout), and EMI noise. To prevent malfunction caused by steep dv/dt at power MOSFET turn-off, connect R28, of about 10 kΩ to 100 kΩ, between the gate and source of the power MOSFET with a minimal length of traces. When adjusting gate resistances, note that gate waveforms of the power MOSFETs must be checked whether a proper amount of dead time is ensured based on the reference waveforms depicted in Figure 8-6.

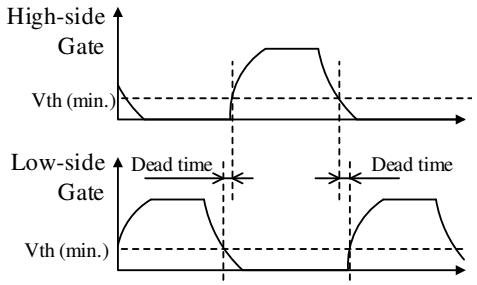


Figure 8-6. Dead Time Confirmation

8.2.18. VB and VS

The VB pin is the input of the high-side floating power supply, whereas the VS pin is the ground of the high-side floating power supply. The MD6752 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins (see Section 8.12).

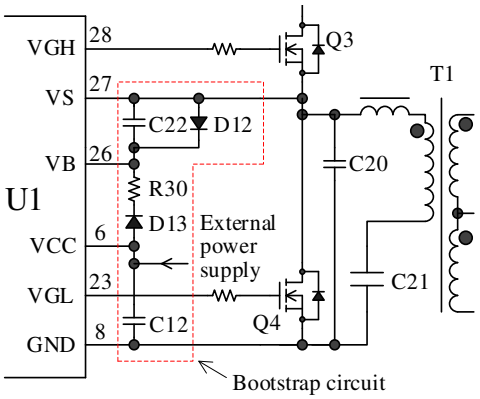


Figure 8-7. Bootstrap Circuit

Figure 8-7 is a schematic diagram of the bootstrap circuit that drives the high-side power MOSFET (Q3). In the condition where the high-side power MOSFET is turned off and the low-side power MOSFET (Q4) is turned on, the VS pin voltage has almost the same potential as the ground. Then, C22 is charged with the VCC pin. When the voltage between the VB and VS pins (hereafter "VB–VS voltage") increases to $V_{BUV(ON)} = 6.8$ V or more, the internal high-side driver starts operating. When VB–VS voltage decreases to $V_{BUV(OFF)} = 6.4$ V or less, the internal high-side driver stops operating (i.e., VB_UVLO). The VB_UVLO protects the IC in case both ends of C22 and D12 are shorted. The bootstrap circuit components must meet the following:

- **D13**

D13 should be a fast recovery diode with a short recovery time and a low reverse current. When the maximum supply input voltage is specified at 265 VAC, it is recommended to use a fast recovery diode with $V_{RM} = 600$ V.

- **C12, C22, R30**

The values of C12, C22, and R30 are determined by the following parameters: the total amount of gate charges of the external power MOSFETs, Qg; the amount of a voltage dip between the VB and VS pins during operation at the lowest oscillation frequency. C12, C22, and R30 should be adjusted according to voltages measured by a high-voltage differential probe so that VB–VS voltage exceeds $V_{BUV(ON)} = 6.8$ V. C12 and C22 should be film or ceramic capacitors with a low ESR and a low leakage current. The reference value of C12 is 0.47μF to 1 μF. The time constants of C22 and R29 should be set within 500 ns. C22 should have a capacitance of 0.047 μF to 0.1 μF; R30 should have a resistance of 2.2 Ω to 10 Ω.

- **D12**

D12 is used for protecting the VS pin from having a negative potential. D12 should be a Schottky diode with

a low forward voltage so that VB–VS voltage does not fall below −0.3 V of its absolute maximum rating.

8.3. Startup Operation

The power supply voltage for control circuit of the IC is externally applied to the VCC pin that is the power input pin. When the AC power supply is turned on and the VCC pin voltage applied from the external power supply reaches $V_{CC(ON)}$ = 14.0 V or more, the VGP pin in the PFC stage starts oscillating and the PFC output voltage rises. When 100 ms or more elapses after the VGP pin in the PFC stage starts oscillating, the VGH and VGL pins in the LLC stage start oscillating, and the secondary output voltage rises. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.3 V or less, the IC stops operation by undervoltage lockout (UVLO) circuit.

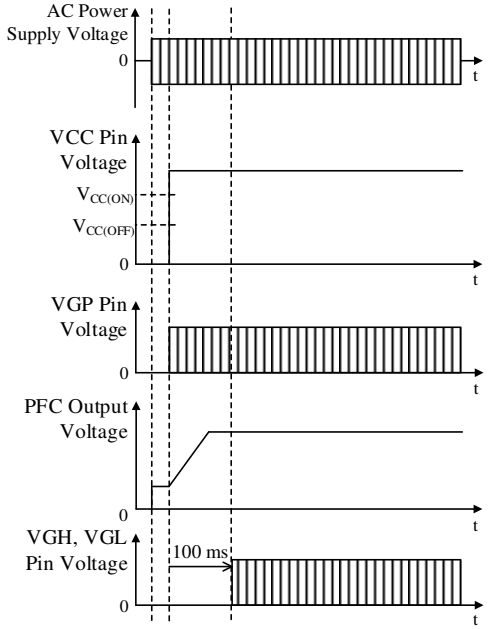


Figure 8-8. Operational Waveforms at Startup

8.4. Soft Start Function

Figure 8-9 shows operational waveforms of the soft start operation at startup. The IC has the soft start function, which reduces stresses on the peripheral components. During the soft start operation, output power increases as the switching frequencies of the VGH and VGL pins gradually decrease. After the output power increases, the IC operates with oscillation frequency control using feedback signal.

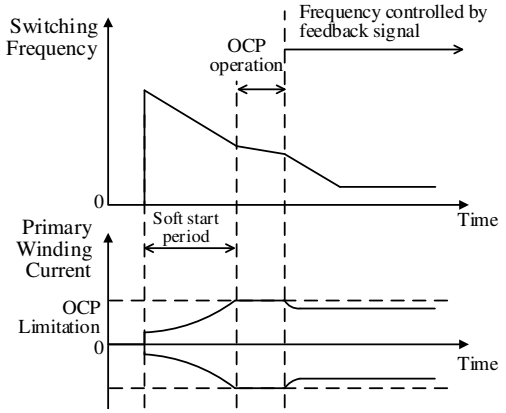


Figure 8-9. Soft Start Operation

8.5. AC Power Supply Input Undervoltage Lockout, AC Power Supply Input Off-state Detection Function

The IC incorporates the AC power supply input undervoltage lockout and the AC power supply input off-state detection function. These functions allow the IC to stop the switching operation of the VGP pin when a low AC line input voltage is detected, thus preventing from excessive input current and overheating.

As depicted in Figure 8-10, the VSEN pin monitors the AC input voltage. Each protection starts operating when either of the two conditions persists for its own fixed delay time: when the AC input voltage falls below its normal-state level and $V_{SEN} \leq V_{SEN(OFF)}$ of 0.47 V; or when VSEN stays unvaried. In either condition, the IC stops the VGP pin switching operation after a lapse of $t_{VSEN(OFF)}$ = 10.0 ms (i.e., the AC power supply input undervoltage lockout), or the GPIO04 pin becomes logic low after a lapse of $t_{VSEN(AC\_OFF)}$ = 23.0 ms (i.e., the AC power supply input off-state detection function).

Signals detected when the AC power supply is in an off state can also be transmitted to the secondary microcontroller through an optocoupler (see Figure 8-10). During the function operation, the IC controls the LLC circuit with "AC off mode".

When all the following conditions are met, the VGP pin resumes switching operation according to output load and the LLC circuit returns to normal operation: the AC input voltage is rising, the IC is in operation, and $V_{SEN} \geq V_{SEN(ON)}$ of 0.56 V.

The reference resistance of R21, the resistor to be connected to the VSEN pin, is about 20 kΩ. R17 to R21 should be selected based on the operation performance checked with an actual board. R17 to R20 are set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; connect these resistors in series to reduce each applied voltage.

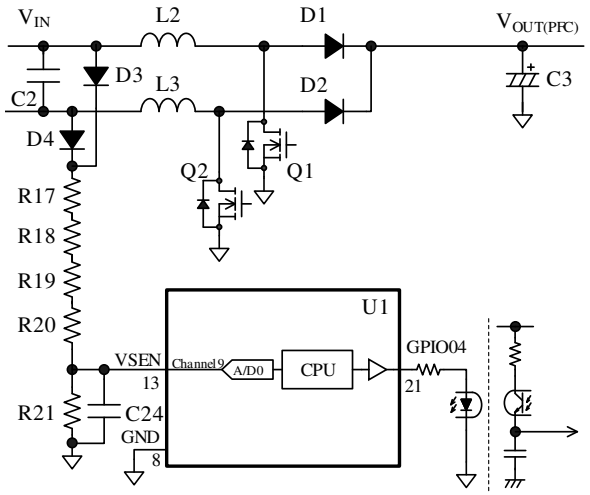


Figure 8-10. VSEN Pin and Its Peripheral Circuit

8.6. VCC Pin Overvoltage Protection

When the voltage between the VCC and GND pins increases to $V_{CC(OVP)}$ = 19.0 V or more, the VCC pin overvoltage protection (VCC_OVP) is activated. Then, the IC stops switching operation.

After that, when the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.3 V or less, the IC restarts. When the causes of the overvoltage condition are eliminated, the IC automatically returns to normal operation.

8.7. PFC Overcurrent Protection, PFC Overload Protection

The MD6752 has the PFC overcurrent protection (PFC_OCP). This function monitors the CS pin voltage to detect a peak drain current of the power MOSFET on a pulse-by-pulse basis, and limits the on-time of the VGP pin when the CS pin voltage reaches the PFC_OCP threshold voltage. The PFC_OCP threshold voltage can be set by the CS pin, with a range of $V_{CS(LO)}$ to $V_{CS(HI)}$.

As shown in Figure 8-11, when the number of the half-wave cycle of the AC input voltage with the PFC_OCP state (i.e., the CS pin voltage exceeds the PFC_OCP threshold voltage) becomes more than the fixed number of times, $N_{OPP(AC)}$ = 32 times, the PFC overload protection (PFC_OLP) is activated to stop the oscillation operations of the VGP, VGH, and VGL pins. When the Protection Recovery Time, t_{AR} = 3000 ms or longer, elapses after that, the IC releases the PFC_OLP operation and restarts to operate. When the causes of the overcurrent condition are eliminated, the IC automatically returns to normal operation.

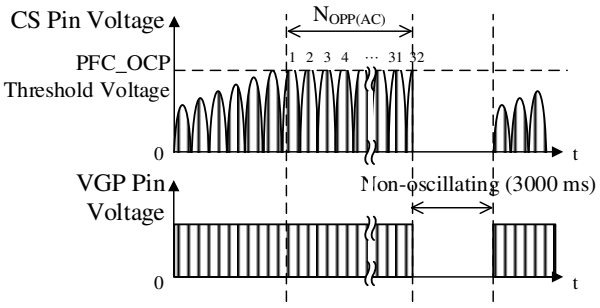


Figure 8-11. PFC_OCP Operational Waveforms

In all AC input voltage specifications, the current transformer should be set so that CS pin voltage stays within the range of $V_{CS(LO)}$ to $V_{CS(HI)}$. The winding turns ratio of the current transformer, n, is calculated as follows:

$$n = \frac{I_{D(PEAK)}}{V_{OCP}} \times R_{CS} . \quad (2)$$

Where:

$I_{D(PEAK)}$ is the drain current in the PFC_OCP operation,

R_{CS} is the current detection resistance of the current transformer (i.e., R10 in Figure 5-1), and

V_{OCP} is the PFC_OCP threshold voltage (i.e., $V_{CS(HI)}$).

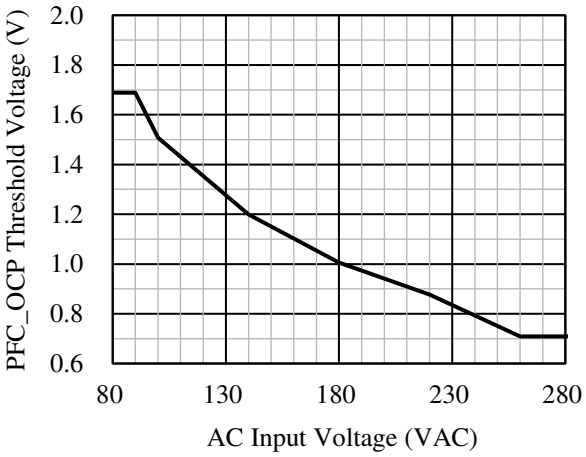


Figure 8-12. PFC_OCP Threshold Voltage vs. AC Input Voltage

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8.8. PFC Overvoltage Protection

The VREF pin detects an overvoltage condition of the PFC output. Figure 8-13 depicts operational waveforms of the PFC overvoltage protection (PFC_OVP). When the VREF pin voltage increases to $V_{REF(OVP)}$ = 2.23 V or more, the PFC_OVP is activated to stop the VGP pin oscillation and to avoid a further increase in the output voltage. When the VREF pin voltage decreases to $V_{REF(OVP\_R)}$ = 2.18 V or less along with a lowering in the output voltage, the VGP pin resumes oscillating. In this way, the intermittent operation is repeated while the overvoltage condition persists. When the causes of the overvoltage condition are eliminated, the IC automatically returns to normal operation. During the PFC_OVP operation, the VGH and VGL pins in the LLC circuit continue their switching operations.

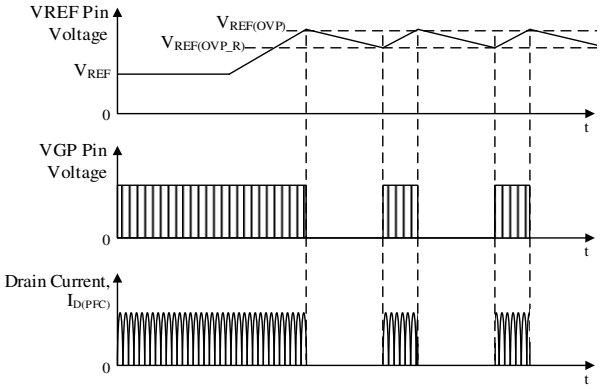

Figure 8-13. PFC_OVP Operational Waveforms

8.9. PFC Undervoltage Protection

The VREF pin also detects an undervoltage condition of the PFC output. Figure 8-14 depicts operational waveforms of the PFC undervoltage protection (PFC_UVP). When the VREF pin voltage decreases to $V_{REF(UVD)}$ = VREF−0.08 V or less, the on-time of the VGP pin is lengthened. Besides, when the VREF pin voltage still decreases $V_{REF(UVP)}$ = 1.10 V or less, the PFC_UVP is activated to stop the VGP pin oscillation. When the VREF pin voltage decreases even further to $V_{REF(UVP\_R)}$ = 0.55 V or less after that, the VGP pin resumes oscillating. During the non-oscillating period of the VGP pin, if the VREF pin voltage does not go below $V_{REF(UVP\_R)}$ within $t_{(UVP\_R)}$ = 819 ms, the VGP pin resumes oscillating at the time that $t_{(UVP\_R)}$ elapses. In this way, the intermittent operation is repeated while the output undervoltage condition persists. When the causes of the undervoltage condition are eliminated, the IC automatically returns to normal operation.

During the PFC_UVP operation, the VGH and VGL pins in the LLC circuit continue their switching operations.

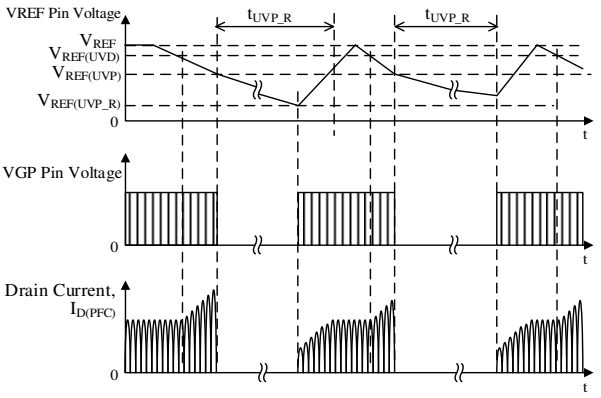

Figure 8-14. PFC_UVP Operational Waveforms

8.10. LLC Constant Voltage Control

Figure 8-15 is a schematic diagram of the FB, CM, and VOCM pins and their peripheral circuit. On-time of the VGH pin is determined by the CM pin and FB pin voltages. On-time of the VGL pin is equal to that of the VGH pin. The on-time of the VGH and VGL pins including dead time is controlled by 50% duty, and the shorter the on-time, the higher the operating frequencies.

The capacitor C18 is connected to the CM pin. When the high-side power MOSFET is turned on, the CM pin voltage, V_{CM}, increases because C18 is charged. The capacitor C16 and the optocoupler PC1 are connected to the FB pin. The feedback current is sunk from the FB pin by the optocoupler depending on the load, and then FB pin voltage, V_{FB}, is determined. The IC compares V_{CM} and V_{FB} with an internal comparator, and operates the time until V_{CM} reaches V_{FB} as on-time. When $V_{CM} \approx V_{FB}$, the IC turns the VOCM pin "H", and then Q6 is turned on. Thus, C18 is discharged, and the CM pin voltage becomes the initial value (0 V).

In light load operation, V_{FB} decreases as the feedback source current increases. The IC reduces the on-times of the VGH and VGL pins, and raises their oscillation frequencies. Conversely, V_{FB} increases in heavy load operation. The IC extends the on-times of the VGH and VGL pins, and lowers their oscillation frequencies. By regulating oscillation frequencies in this manner, the IC can stabilize an output voltage (controlled in an inductance area).

In heavy load operation, when V_{FB} rises and the peak of V_{CM} reaches Current Mode Control Maximum CM Pin Voltage, $V_{CM(MAX)}$ = 2.00 V or more, the LLC overcurrent protection (LCC_OCP) is activated to limit current on pulse-by-pulse basis. Section 8.13 provides more details on the LLC_OCP.

C18 should have a capacitance of about 1000 pF to 0.01 µF. Care should be taken in adjusting C18 because C18 value depends on the maximum output power.

The secondary error amplifier should be designed so that collector current passing through the optocoupler PC1 is higher than 330 µA, i.e., higher than the absolute maximum source current of the FB pin. In particular, the

current transfer ratio, CTR, of the optocoupler must take its performance decline over time into account in actual designing. C16 should have a capacitance of about 1000 pF.

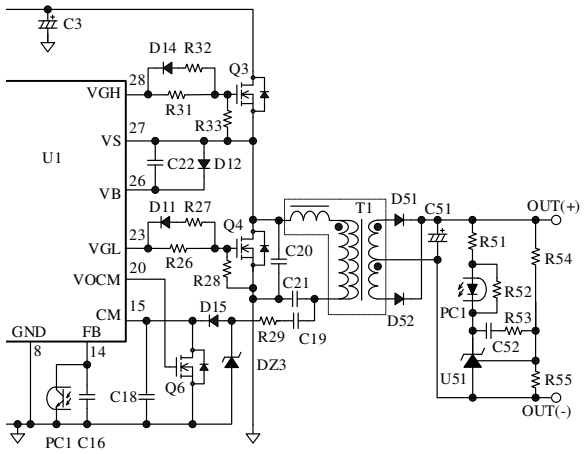

Figure 8-15. FB Pin and Its Peripheral Circuit

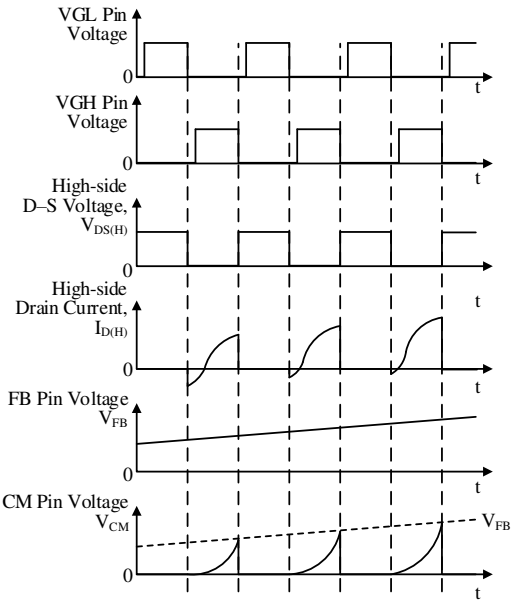

Figure 8-16. Current Mode Control Operational Waveforms

8.11. LLC Dead Time

A dead time is a period of time when both of the high- and low-side power MOSFETs in the LLC stage turn off. When the dead time is shorter than a voltage resonance period as in Figure 8-17, the power MOSFETs turn on or off during the voltage resonance period. In such case, switching loss increases due to hard switching of the power MOSFETs.

Be sure to set a dead time so that it falls within the range, from $t_{d(MIN)}$ = 0.47 µs to $t_{d(MAX)}$ = 0.56 µs, for which the power supply operates within all the allowable operating ranges and avoids the zero voltage switching (ZVS) failure shown in Figure 8-17.

Figure 8-19 depicts how a dead time varies according to the FB pin voltage. Also, ensure a margin so that period in which drain current flows through body diode in Figure 8-18 is longer than the dead time, and actual operations must be checked to ensure that power MOSFETs operate with the zero current switching (ZCS) under the following conditions:

- When an output power is minimum in a maximum input voltage specification
- When an output power is maximum in a minimum input voltage specification

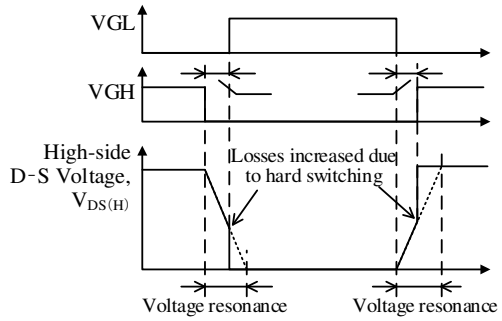

Figure 8-17. Waveforms When ZVS Failure Occurs

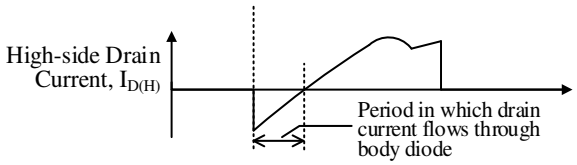

Figure 8-18. Point to Be Checked in ZCS

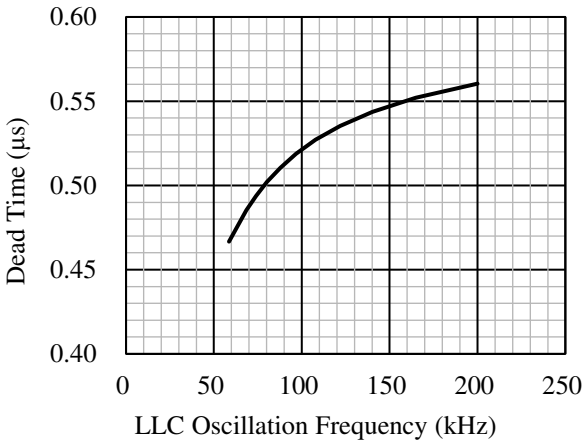

Figure 8-19. Dead Time vs. LLC Oscillation Frequency

8.12. LLC High-side Driver Undervoltage Lockout

The MD6752 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins.

When the voltage between the VB and VS pins (i.e., "VB–VS voltage") increases to $V_{BUV(ON)}$ = 6.8 V or more, the internal high-side driver starts operating. When the VB–VS voltage decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the internal high-side driver stops operating. The VB_UVLO protects the IC in case both ends of the capacitor C22 for bootstrap circuit and the protective diode D12 are shorted.

8.13. LLC Overcurrent Protection, LLC Overload Protection

The LLC overcurrent protection (LLC_OCP) detects a peak drain current of the power MOSFET on a pulse-by-pulse basis, and limits the output power. The CM pin detects the current flowing to the power MOSFET. In heavy load operation, when the FB pin voltage, V_{FB}, rises, the peak value of CM pin voltage, V_{CM} also rises. When V_{CM} reaches $V_{CM(MAX)}$ = 2.00 V or more, the LCC_OCP is activated to increase oscillation frequency and thus limits the drain current. When the LCC_OCP condition persists for a period longer than t_{OLP} = 5.0 ms, the LLC overload protection (LLC_OLP) is activated to stop the oscillation operations of the VGH, VGL, and VGP pins. When the Protection Recovery Time, t_{AR} = 3000 ms or longer, elapses after that, the IC releases the LLC_OLP operation and restarts to operate. When the causes of the overload condition are eliminated, the IC automatically returns to normal operation.

During the LLC_OCP operation, the maximum output power, P_{MAX}, depends on C18 capacitance of the CM pin. The smaller C18 capacitance, the higher the frequency and the smaller P_{MAX}. C18 should have a capacitance of about 1000 pF to 0.01 µF.

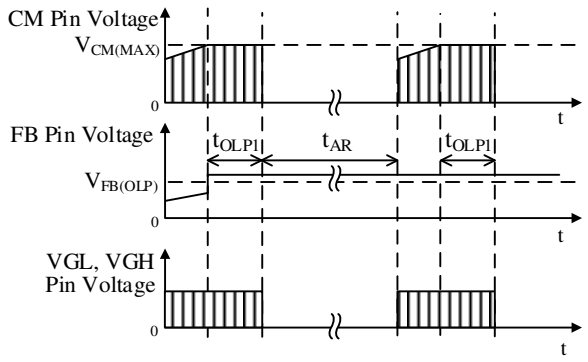

Figure 8-20. Operational Waveforms of LCC_OCP and LCC_OLP

8.14. Thermal Shutdown

When the control circuit temperature reaches $T_{J(TSD)}$ = 125 °C, the thermal shutdown (TSD) is activated. The IC then stops switching operation. In the condition where VCC ≤ $V_{CC(P.OFF)}$ of 8.3 V and the control circuit temperature falls below $T_{J(TSD)}$, the TSD circuit is activated again. During the TSD operation, the IC stops its operation. When the causes of the overheating condition are eliminated, the IC automatically returns to normal operation.

9. External Components

9.1. Resonant Transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce influences from eddy current and skin effect, use a bundle of fine litz wires as the wire of the transformer.

9.2. Inductor in PFC Stage

Apply proper design margin to temperature rise or magnetic saturation due to copper loss and iron loss.

9.3. Power MOSFET

Use a power MOSFET with a breakdown voltage, V_{DSS}, providing enough margin to the PFC output voltage, $V_{OUT(PFC)}$. Choose a proper size of heatsink that takes switching and on-resistance losses due to power MOSFETs into account.

9.4. PFC Boost Diode (D1, D2)

Choose a boost diode having a peak reverse voltage, V_{RSM}, which provides enough margin to the PFC output voltage, $V_{OUT(PFC)}$. A fast recovery diode with a short reverse recovery time, t_{rr}, is recommended to reduce noise and loss due to switching. Choose a proper size of heatsink that takes losses caused by forward voltage, V_F, and recovery current into considerations.

9.5. Input Filter

Connect the C8, C9, D9, and D10 in addition to the pi filter (C1, C2, and L1) to the input side. Connect the film capacitors C8 and C9 (about 600 V / 0.1 μF～1.0 μF) to the input side. Connect the general-purpose rectifier diodes D9 and D10 to the input side. C8, C9, D9, and D10 should be selected based on the operation performance checked with an actual board.

9.6. Output Capacitor (C51)

Apply proper design margin to ripple current, ripple voltage, and temperature rise. A low-ESR capacitor is recommended to reduce ripple voltage, in terms of designing switch-mode power supplies.

9.7. Current-resonant Capacitor (C21)

Because large resonant current flows through C21, it should be a capacitor that supports high-current applications with small losses such as a polypropylene film capacitor. High-frequency current flows through C21; therefore, capacitor-specific frequency characteristics must also be taken into account.

10. PCB Pattern Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. High-frequency and high-voltage current loops (see Figure 10-1) should be as small and wide as possible in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

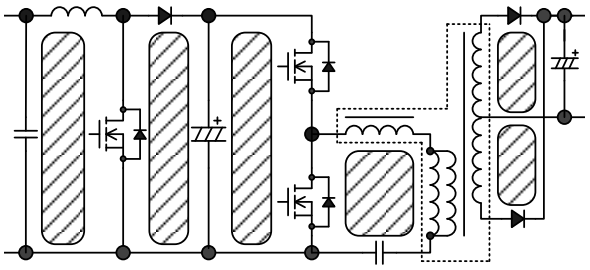

Figure 10-1. High-frequency Current Loop

Figure 10-2 is a peripheral circuit example of the IC.

The following considerations should be taken into account in designing pattern layouts for your application.

1) Main Circuit Trace Layout

Traces of the PFC and LLC circuits, where switching currents pass through, should be as wide and looped small as possible.

2) Logic Ground Trace Layout

If a large current flows through a logic ground, electric potential across the logic ground may vary and thus cause the IC to malfunction. Ground traces should be as wide and short as possible.

Logic ground traces should be designed as close as possible to the GND pin, at a single-point ground (or star ground) that is separated from the main circuit. Do not connect the PGND pin to these traces. Traces of the ground (i.e., the capacitors of the GND, PGND, and VCC pins) should be separately connected at a single-point ground whose connection is configured to the root of the output capacitor C3 in the PFC stage.

3) Peripheral Connections to VCC Pin

Traces connected to the VCC pin should be looped small as possible because the pin supplies power to the IC. Connect the film capacitor C12 (about 0.1 μF to 1.0 μF) between the VCC and GND pins with a minimal length of traces.

4) Peripheral Connections to VB Pin

The components of the bootstrap circuit connected between the VCC and VB pins (D13, R30) should be placed as close as possible to the IC. The capacitor C22 connected between the VB and VS pins should also be placed with a minimal length of traces.

5) Components for Logic Control System

These components should be placed close to the IC, and be connected to the corresponding pin of the IC with a minimal length of traces.

6) Secondary Rectifier Smoothing Circuit

This is the secondary main circuit, in which switching current flows, should be wide and looped small as possible.

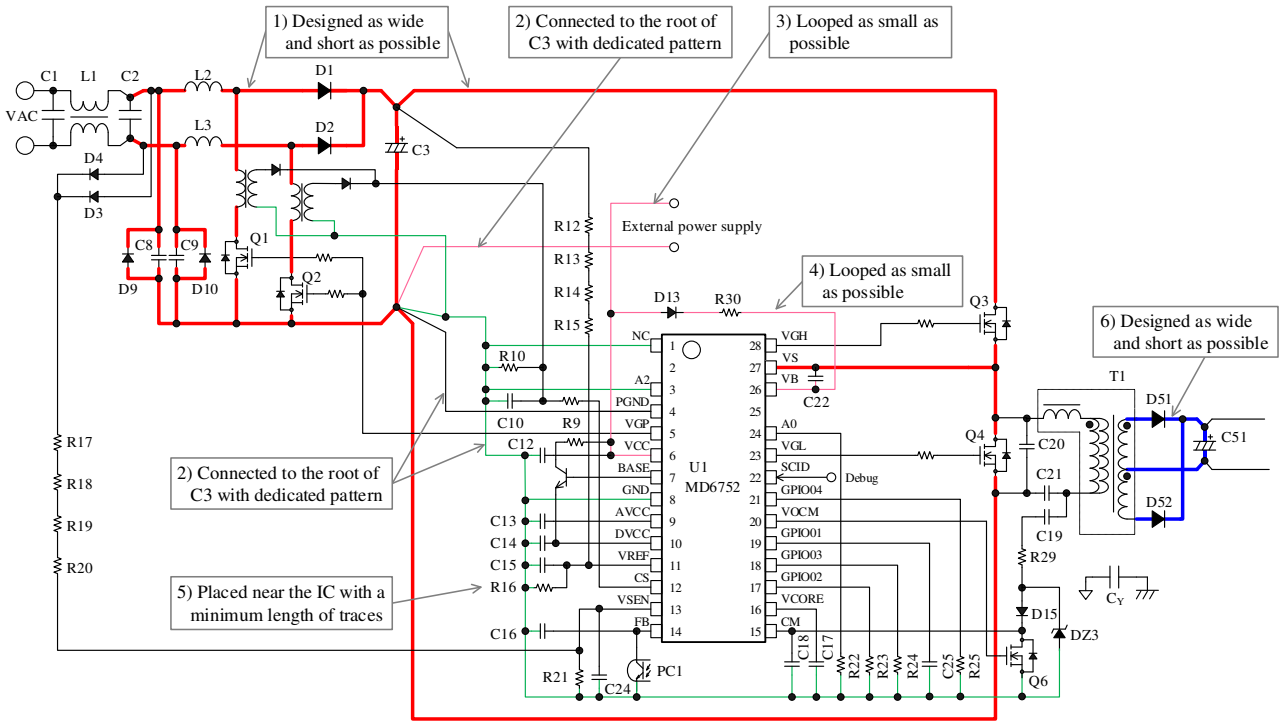

Figure 10-2. Example Connections to IC and Its Peripheral Circuits

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