HIGH-SPEED DIFFERENTIAL RECEIVERS

Check for Samples: SN65LVDS33, SN65LVDT33, SN65LVDS34, SN65LVDT34

FEATURES

- **400-Mbps Signaling Rate[(1)] and 200-Mxfr/s Data Transfer Rate**
- **Operates With a Single 3.3-V Supply**
- **-4 V to 5 V Common-Mode Input Voltage Range**
- **Differential Input Thresholds <±50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range**
- **Integrated 110-Ω Line Termination Resistors On LVDT Products**
- **TSSOP Packaging (33 Only)**
- **Complies With TIA/EIA-644 (LVDS)**
- **Active Failsafe Assures a High-Level Output With No Input**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Input Remains High-Impedance on Power Down**
- **TTL Inputs Are 5 V Tolerant**
- **Pin-Compatible With the AM26LS32, SN65LVDS32B, µA9637, SN65LVDS9637B**

(1) The signalling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

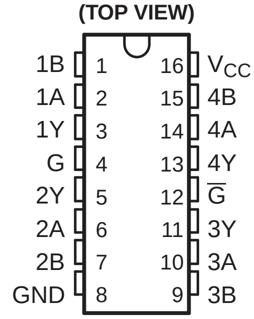
This family of four LVDS data line receivers offers the widest common-mode input voltage range in the industry. These receivers provide an input voltage range specification compatible with a 5-V PECL signal as well as an overall increased ground-noise tolerance. They are in industry standard footprints with integrated termination as an option.

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

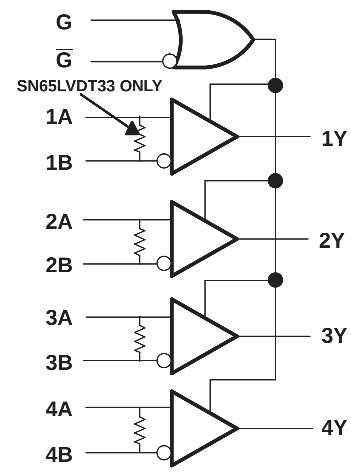
The high-speed switching of LVDS signals usually necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

SN65LVDS33D, SN65LVDT33D
SN65LVDS33PW, SN65LVDT33PW

D OR PW PACKAGE (TOP VIEW)

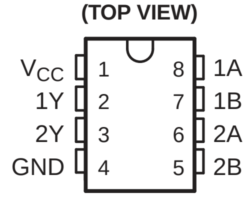


logic diagram (positive logic)

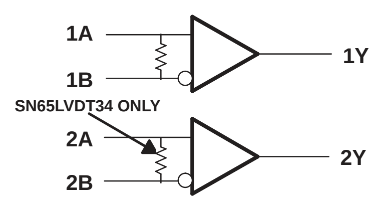


SN65LVDS34D, SN65LVDT34D

D PACKAGE (TOP VIEW)



logic diagram (positive logic)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS(1)

PART NUMBER(2)	NUMBER OF RECEIVERS	TERMINATION RESISTOR	SYMBOLIZATION
SN65LVDS33D	4	No	LVDS33
SN65LVDS33PW	4	No	LVDS33
SN65LVDTS33D	4	Yes	LVDT33
SN65LVDT33PW	4	Yes	LVDT33
SN65LVDS34D	2	No	LVDS34
SN65LVDT34D	2	Yes	LVDT34

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Add the suffix R for taped and reeled carrier.

DESCRIPTION (CONTINUED)

The receivers can withstand ±15 kV human-body model (HBM) and ±600 V machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) failsafe circuit that will provide a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. The failsafe circuit prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling. See *The Active Failsafe Feature of the SN65LVDS32B* application note.

The intended application and signaling technique of these devices is point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS33, SN65LVDT33, SN65LVDS34 and SN65LVDT34 are characterized for operation from –40°C to 85°C.

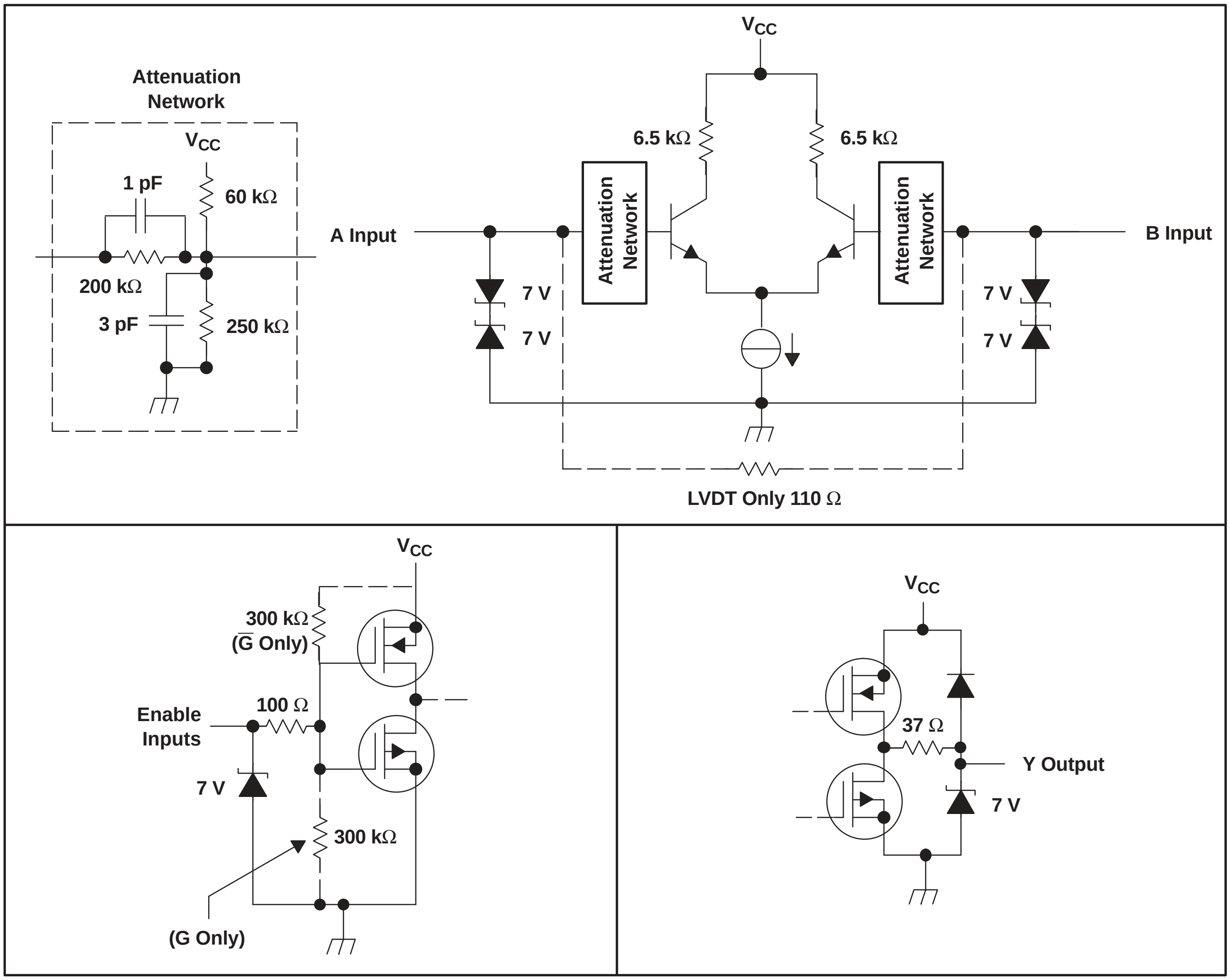
Table 1. Function Tables(1)

SN65LVDS33 and SN65LVDT33			
DIFFERENTIAL INPUT	**ENABLES**		**OUTPUT**
$V_{ID} = V_A - V_B$	**G**	$\overline{G}$	**Y**
$V_{ID} \geq -32$ mV	H	X	H
	X	L	H
-100 mV < $V_{ID} \leq -32$ mV	H	X	?
	X	L	?
$V_{ID} \leq -100$ mV	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

SN65LVDS34 and SN65LVDT34	
DIFFERENTIAL INPUT	**OUTPUT**
$V_{ID} = V_A - V_B$	**Y**
$V_{ID} \geq -32$ mV	H
-100 mV < $V_{ID} \leq -32$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage range, V_{CC} (2)		–0.5 V to 4 V
Voltage range	Enables or Y	–1 V to 6 V
	A or B	–5 V to 6 V
	$\lvert V_A – V_B \rvert$ (LVDT)	1 V
Electrostatic discharge	A, B, and GND (3)	Class 3, A: 15 kV, B: 500 V
Charged-device mode	All pins (4)	±500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D8	725 mW	5.8 mW/°C	377 mW
PW16	774 mW	6.2 mW/°C	402 mW
D16	950 mW	7.6 mW/°C	494 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	Enables	2		5	V
V_{IL}	Low-level input voltage	Enables	0		0.8	V
$\lvert V_{ID} \rvert$	Magnitude of differential input voltage	LVDS	0.1		3	V
		LVDT			0.8	
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)		–4		5	V
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT1}	Positive-going differential input voltage threshold		V_{IB} = –4 V or 5 V, See Figure 1 and Figure 2			50	mV
V_{IT2}	Negative-going differential input voltage threshold			–50			mV
V_{IT3}	Differential input failsafe voltage threshold		See Table 2 and Figure 5	–32		–100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$				50		mV
V_{OH}	High-level output voltage		I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
I_{CC}	Supply current	SN65LVDx33	G at V_{CC}, No load, Steady-state		16	23	mA
			G at GND		1.1	5	
		SN65LVDx34	No load, Steady-state		8	12	
I_I	Input current (A or B inputs)	SN65LVDS	V_I = 0 V, Other input open			±20	µA
			V_I = 2.4 V, Other input open			±20	
			V_I = –4 V, Other input open			±75	
			V_I = 5 V, Other input open			±40	
		SN65LVDT	V_I = 0 V, Other input open			±40	µA
			V_I = 2.4 V, Other input open			±40	
			V_I = –4 V, Other input open			±150	
			V_I = 5 V, Other input open			±80	
I_{ID}	Differential input current ($I_{IA} – I_{IB}$)	SN65LVDS	V_{ID} = 100 mV, V_{IC} = –4 V or 5 V			±3	µA
		SN65LVDT	V_{ID} = 200 mV, V_{IC} = –4 V or 5 V	1.55		2.22	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	SN65LVDS	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V			±20	µA
			V_A or V_B = –4 or 5 V, V_{CC} = 0 V			±50	
		SN65LVDT	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V			±30	
			V_A or V_B = –4 V or 5 V, V_{CC} = 0 V			±100	
I_{IH}	High-level input current (enables)		V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (enables)		V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current			–10		10	µA
C_I	Input capacitance, A or B input to GND		V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{PLH(1)}$	Propagation delay time, low-to-high-level output	See Figure 3	2.5	4	6	ns
$t_{PHL(1)}$	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, failsafe deactivate time	C_L = 10 pF, See Figure 3 and Figure 6			9	ns
t_{d2}	Delay time, failsafe activate time		0.3		1.5	μs
$t_{sk(p)}$	Pulse skew ($\|t_{PHL(1)} - t_{PLH(1)}\|$)	See Figure 3		200		ps
$t_{sk(o)}$	Output skew(2)			150		ps
$t_{sk(pp)}$	Part-to-part skew(3)				1	ns
t_r	Output signal rise time			0.8		ns
t_f	Output signal fall time			0.8		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		5.5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.4	9	ns
t_{PZH}	Propagation delay time, high-impedance -to-high-level output			3.8	9	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	9	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven together.
(3) $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

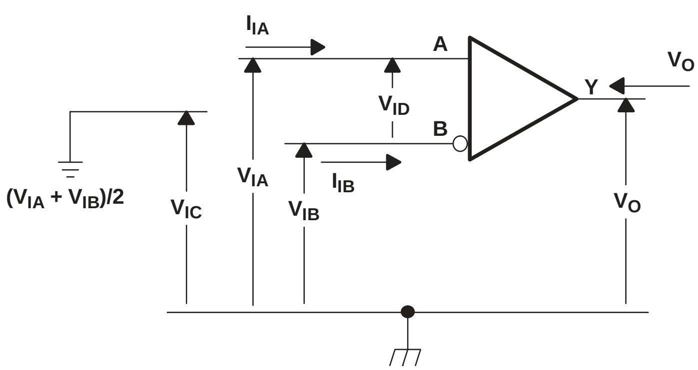
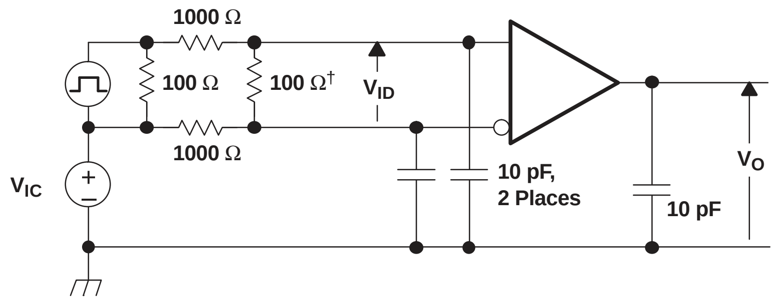
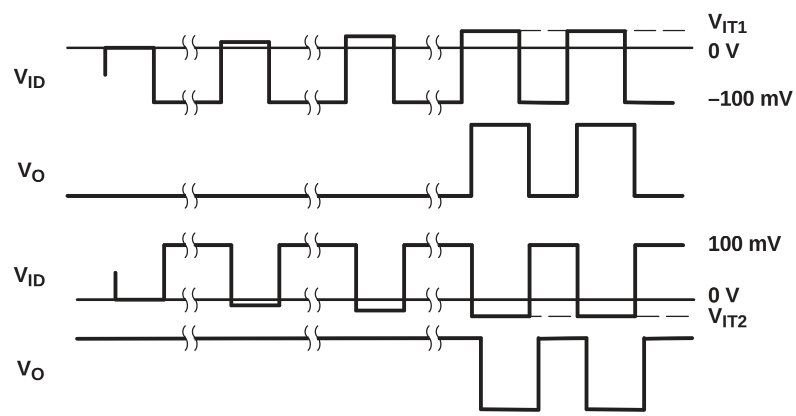


Figure 1. Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



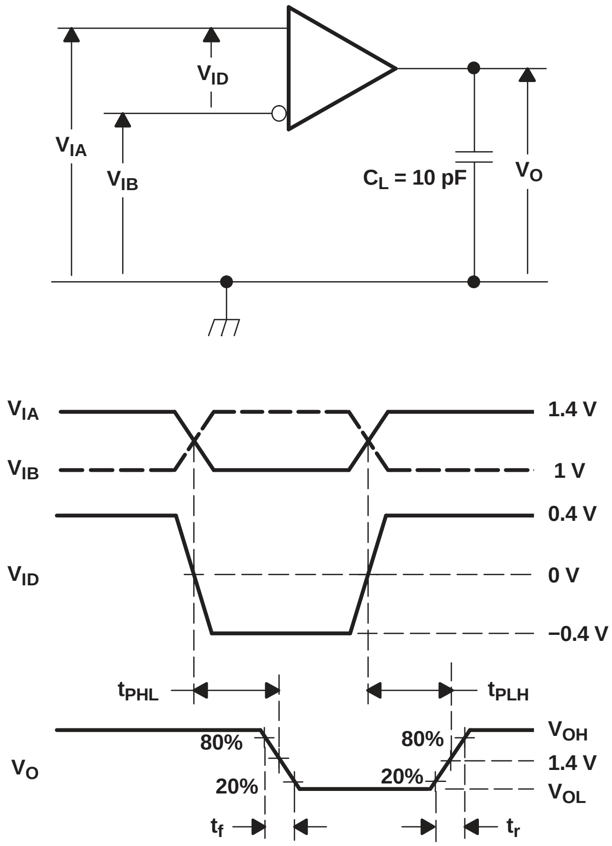
† Remove for testing LVDT device.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions

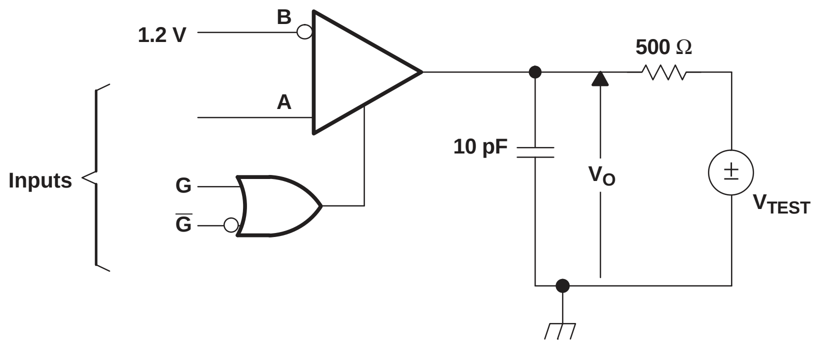
PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ±0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

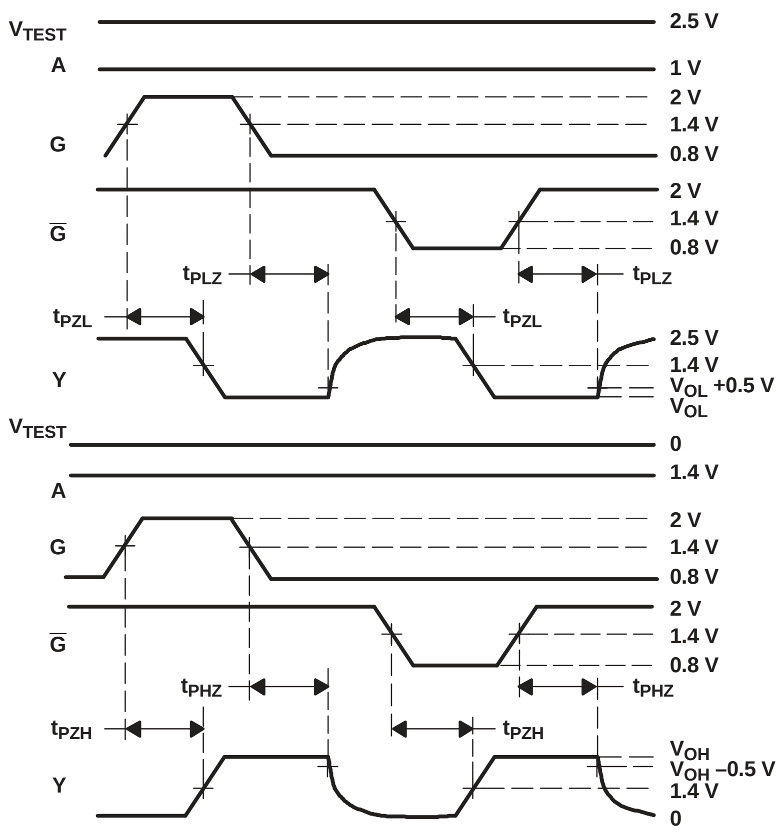
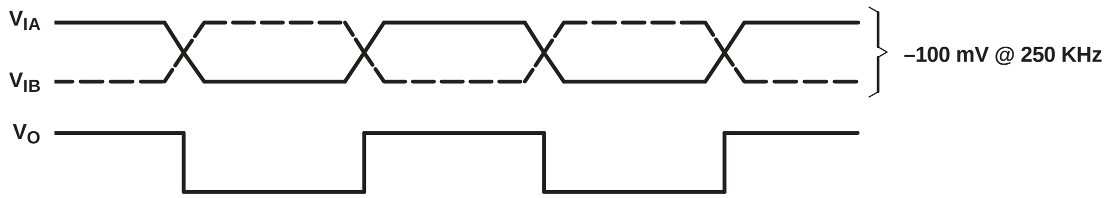


Figure 4. Enable/Disable Time Test Circuit and Waveforms

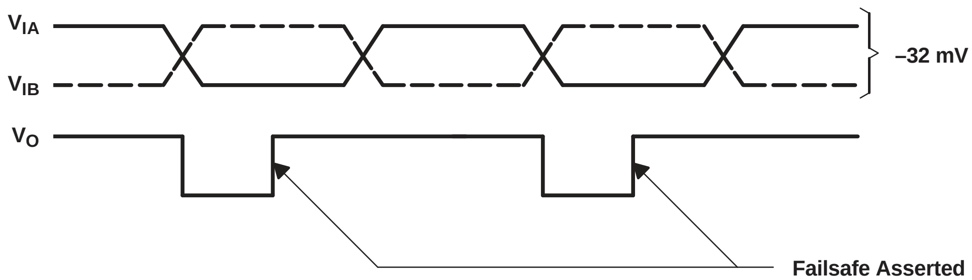
Table 2. Receiver Minimum and Maximum V_{IT3} Input Threshold Test Voltages

APPLIED VOLTAGES[(1)]		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
–4000	–3900	–100	–3950	L
–4000	–3968	–32	–3984	H
4900	5000	–100	4950	L
4968	5000	–32	4984	H

(1) These voltages are applied for a minimum of 1.5 μs.



a) No Failsafe



b) Failsafe Asserted

Figure 5. V_{IT3} Failsafe Threshold Test

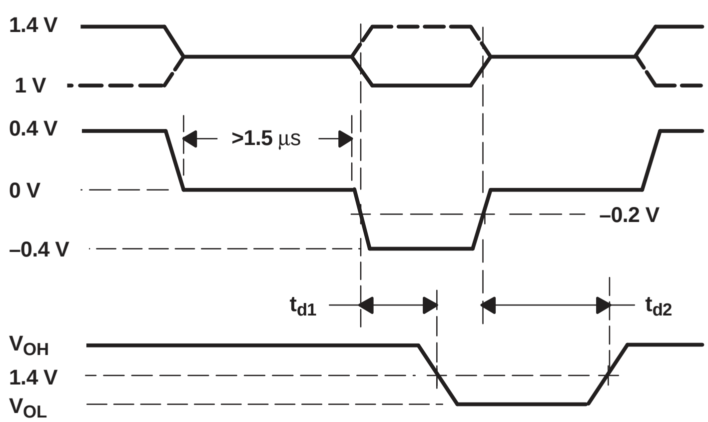


Figure 6. Waveforms for Failsafe Activate and Deactivate

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

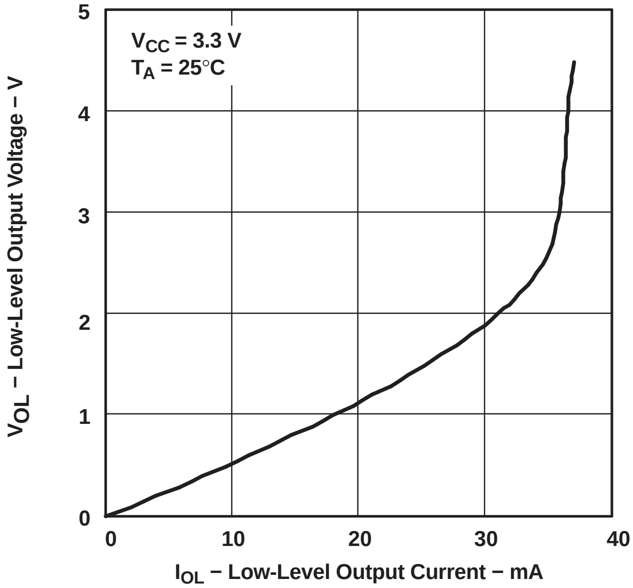


Figure 7.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

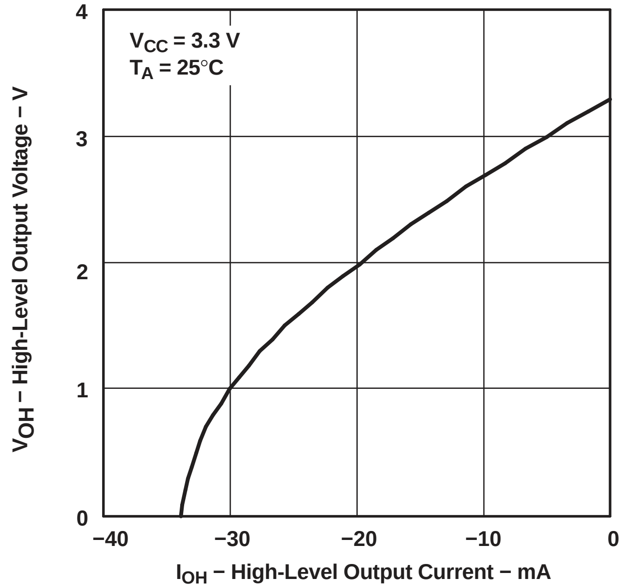


Figure 8.

LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

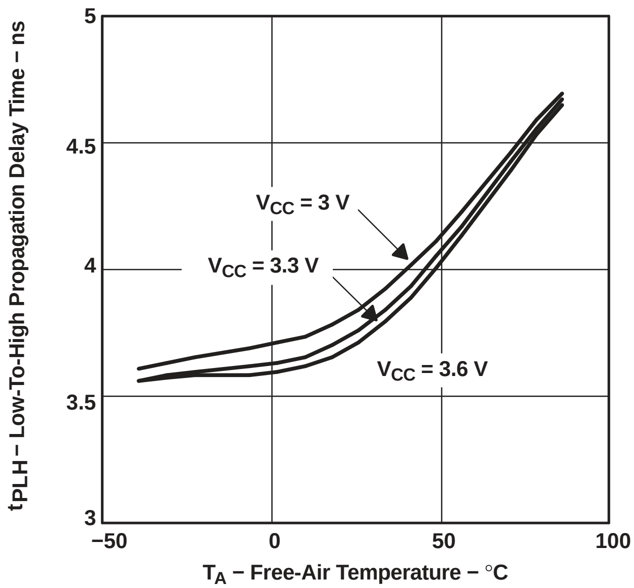


Figure 9.

HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

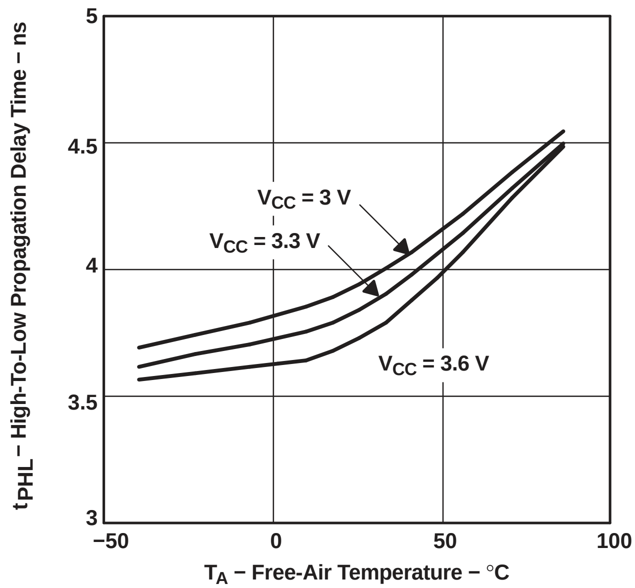


Figure 10.

TYPICAL CHARACTERISTICS (continued)

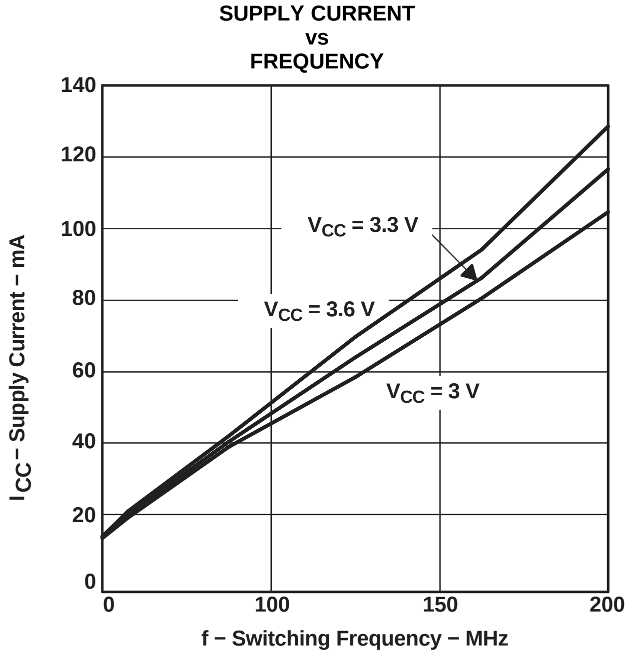
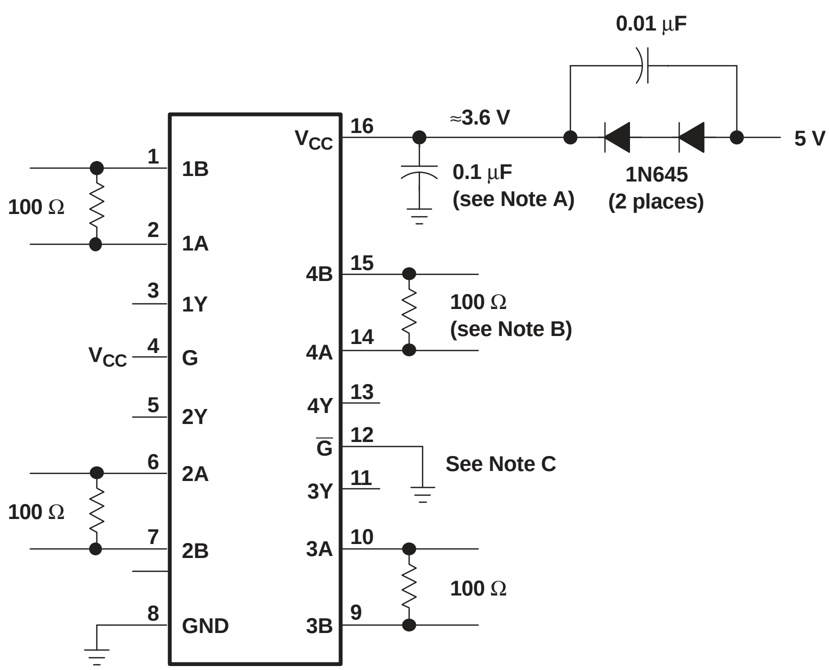


Figure 11.

APPLICATION INFORMATION



A. Place a 0.1-µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 12. Operation With 5-V Supply

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

ACTIVE FAILSAFE FEATURE

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note *The Active Failsafe Feature of the SN65LVDS32B,* (SLLA082A).

The following figure shows one receiver channel with active failsafe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and it detects when the input differential falls below 80 mV. A 600-ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

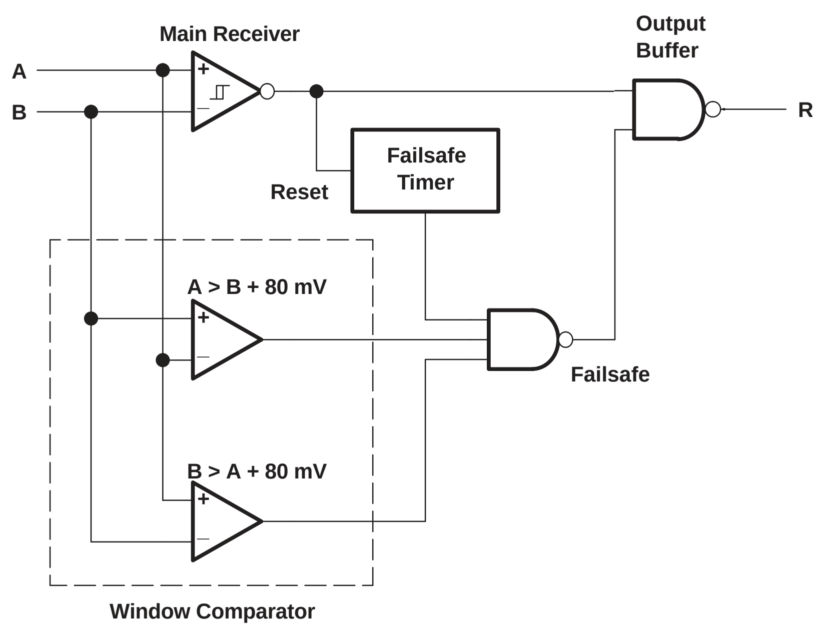


Figure 13. Receiver With Active Failsafe

ECL/PECL-TO-LVTTL CONVERSION WITH TI's LVDS RECEIVER

The various versions of emitter-coupled logic (i.e., ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know of the established technology and that it is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like

LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC}–2 V).

Figure 14 and Figure 15 show the use of an LV/PECL driver driving 5 meters of CAT-5 cable and being received by TI's wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

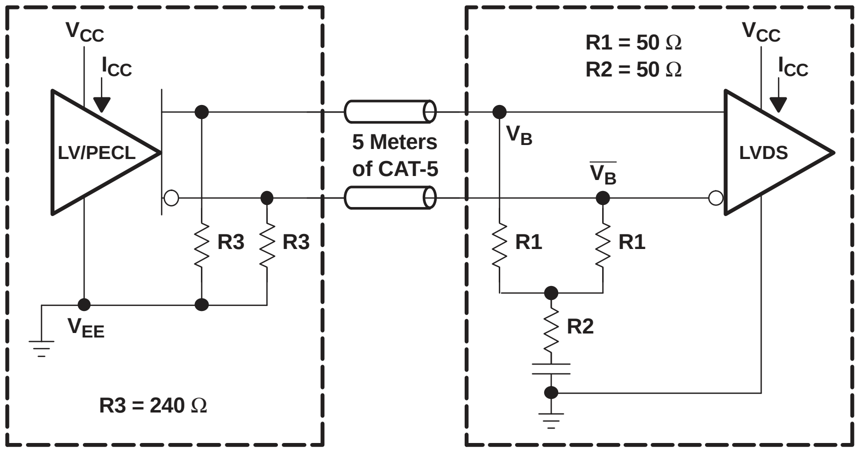


Figure 14. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

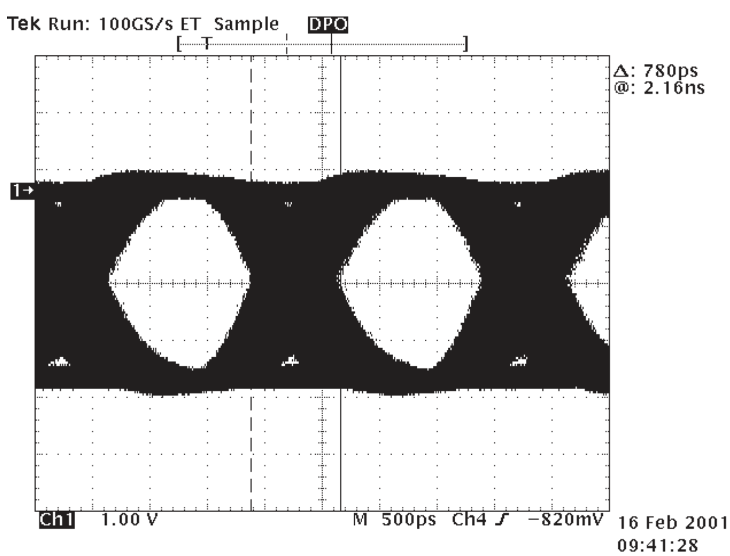


Figure 15. LV/PECL to Remote SN65LVDS33 at 500 Mbps Receiver Output (CH1)

TEST CONDITIONS

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All four channels switching simultaneously with NRZ data. Scope is pulse-triggered simultaneously with NRZ data.

EQUIPMENT

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

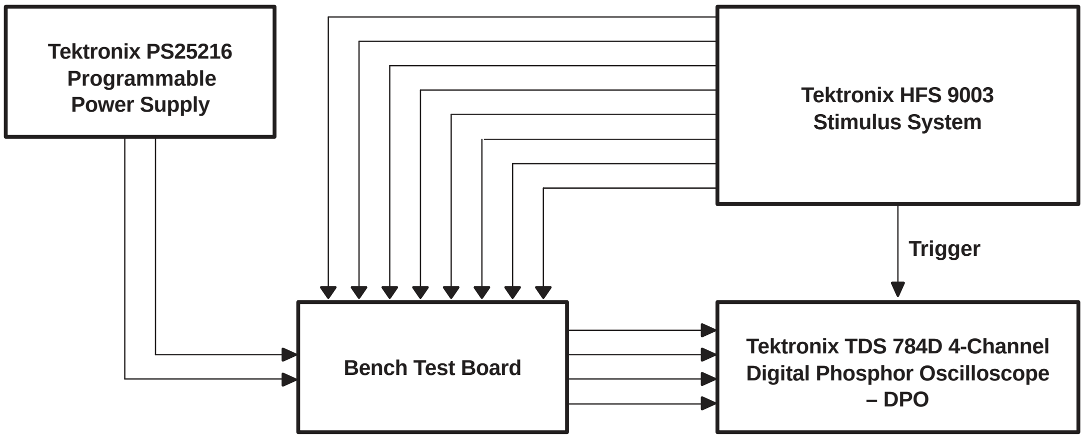


Figure 16. Equipment Setup

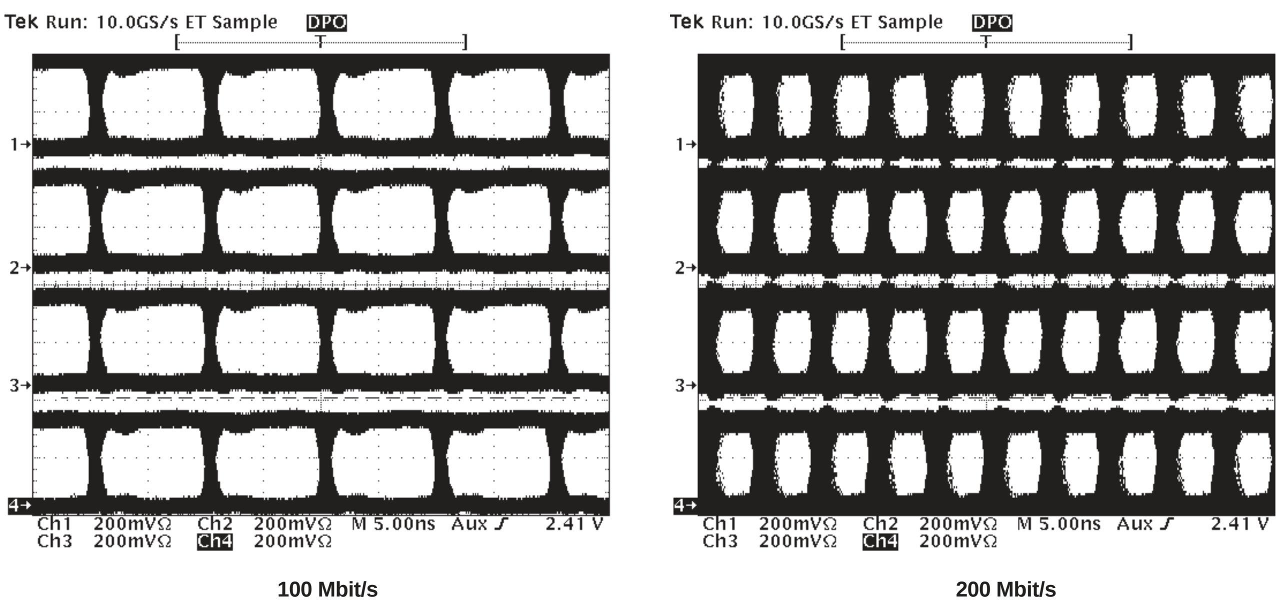


Figure 17. Typical Eye Pattern SN65LVDS33

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS33D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33	Samples
SN65LVDS33DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33	Samples
SN65LVDS33DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33	Samples
SN65LVDS33DRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33	Samples
SN65LVDS33PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33	Samples
SN65LVDS33PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS33	Samples
SN65LVDS34D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS34	Samples
SN65LVDS34DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS34	Samples
SN65LVDS34DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS34	Samples
SN65LVDT33D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33	Samples
SN65LVDT33DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33	Samples
SN65LVDT33PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33	Samples
SN65LVDT33PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33	Samples
SN65LVDT33PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT33	Samples
SN65LVDT34D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT34	Samples
SN65LVDT34DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT34	Samples
SN65LVDT34DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT34	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDS33 :

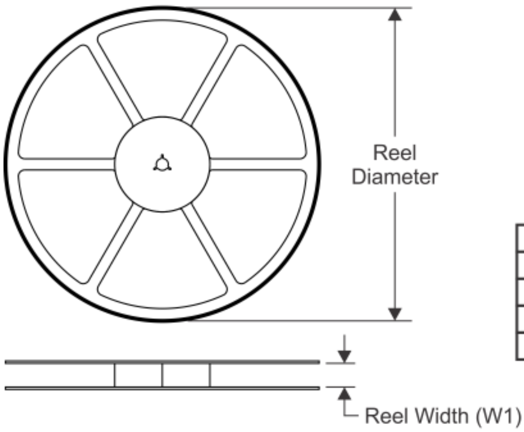
- Enhanced Product: SN65LVDS33-EP

NOTE: Qualified Version Definitions:

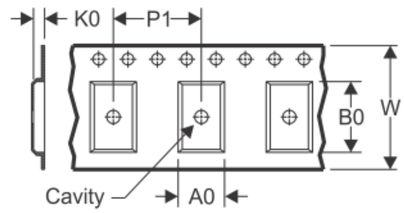
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

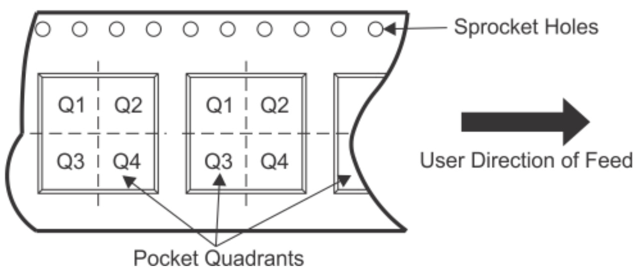


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

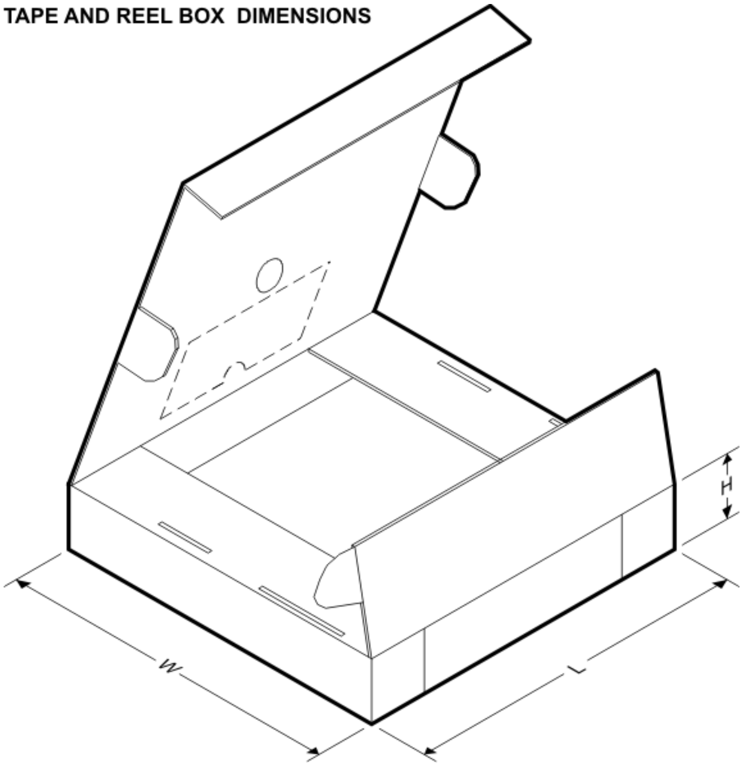
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS33DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS33PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS34DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDT33PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDT34DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

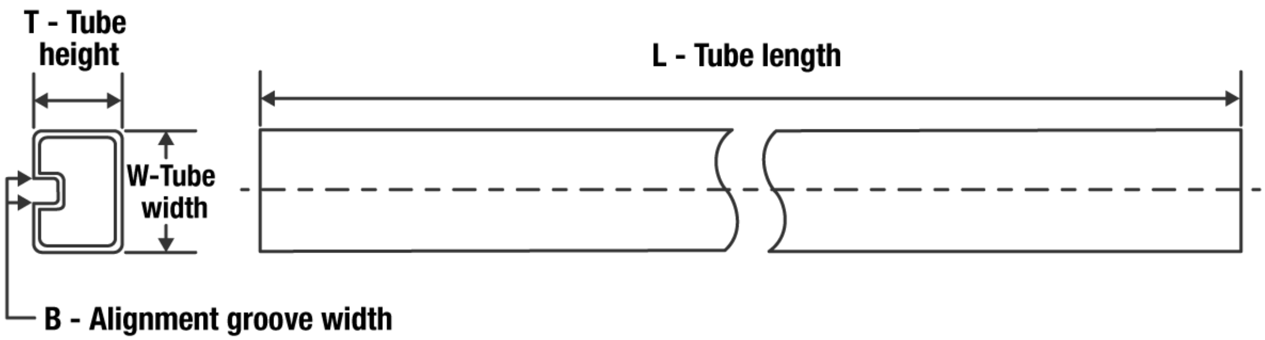
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS33DR	SOIC	D	16	2500	340.5	336.1	32.0
SN65LVDS33PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDS34DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LVDT33PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDT34DR	SOIC	D	8	2500	340.5	336.1	25.0

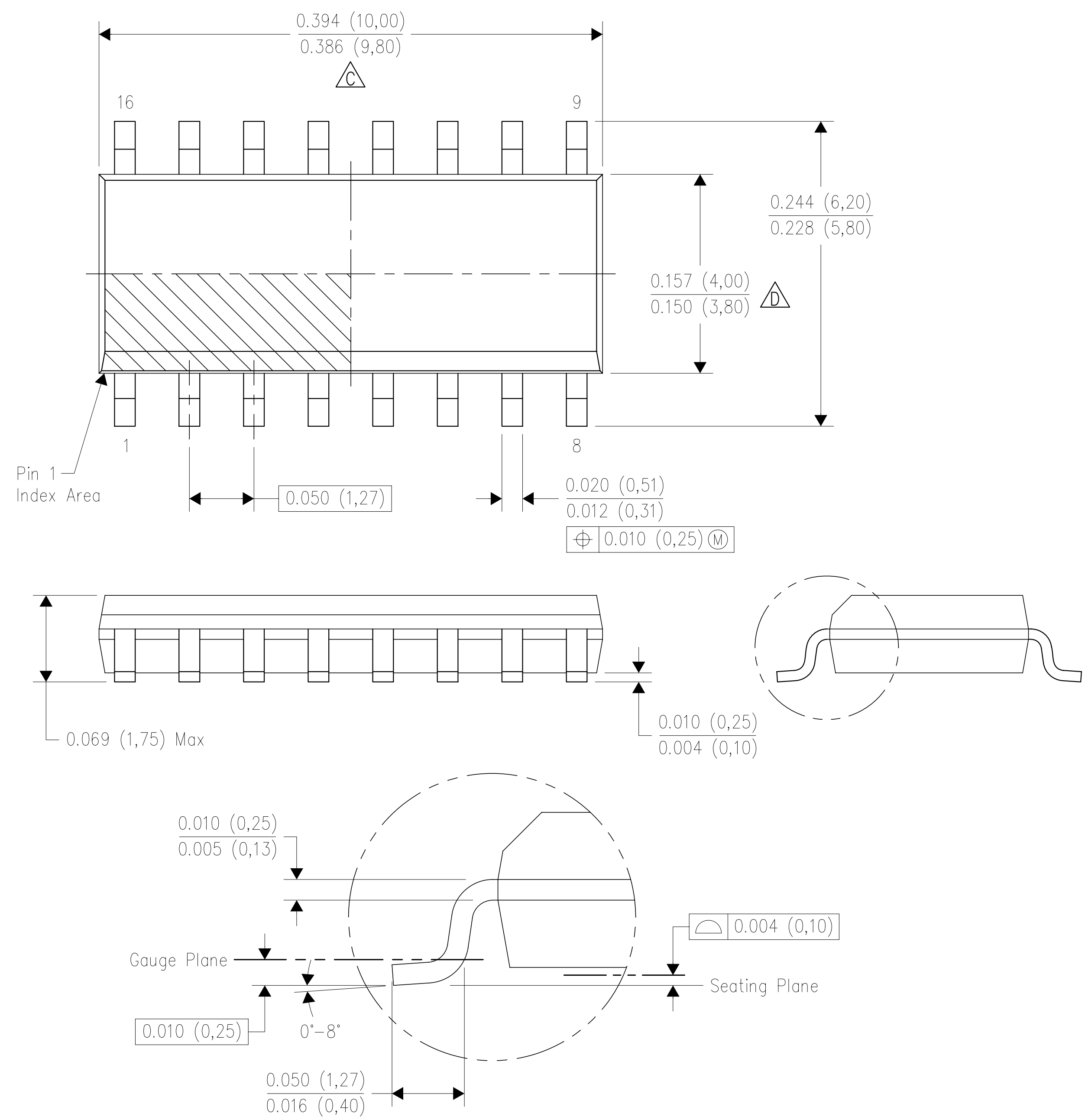
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS33D	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS33DG4	D	SOIC	16	40	507	8	3940	4.32
SN65LVDS33PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS34D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS34D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDT33D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDT33DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDT33PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDT33PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDT34D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDT34D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDT34DG4	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDT34DG4	D	SOIC	8	75	507	8	3940	4.32

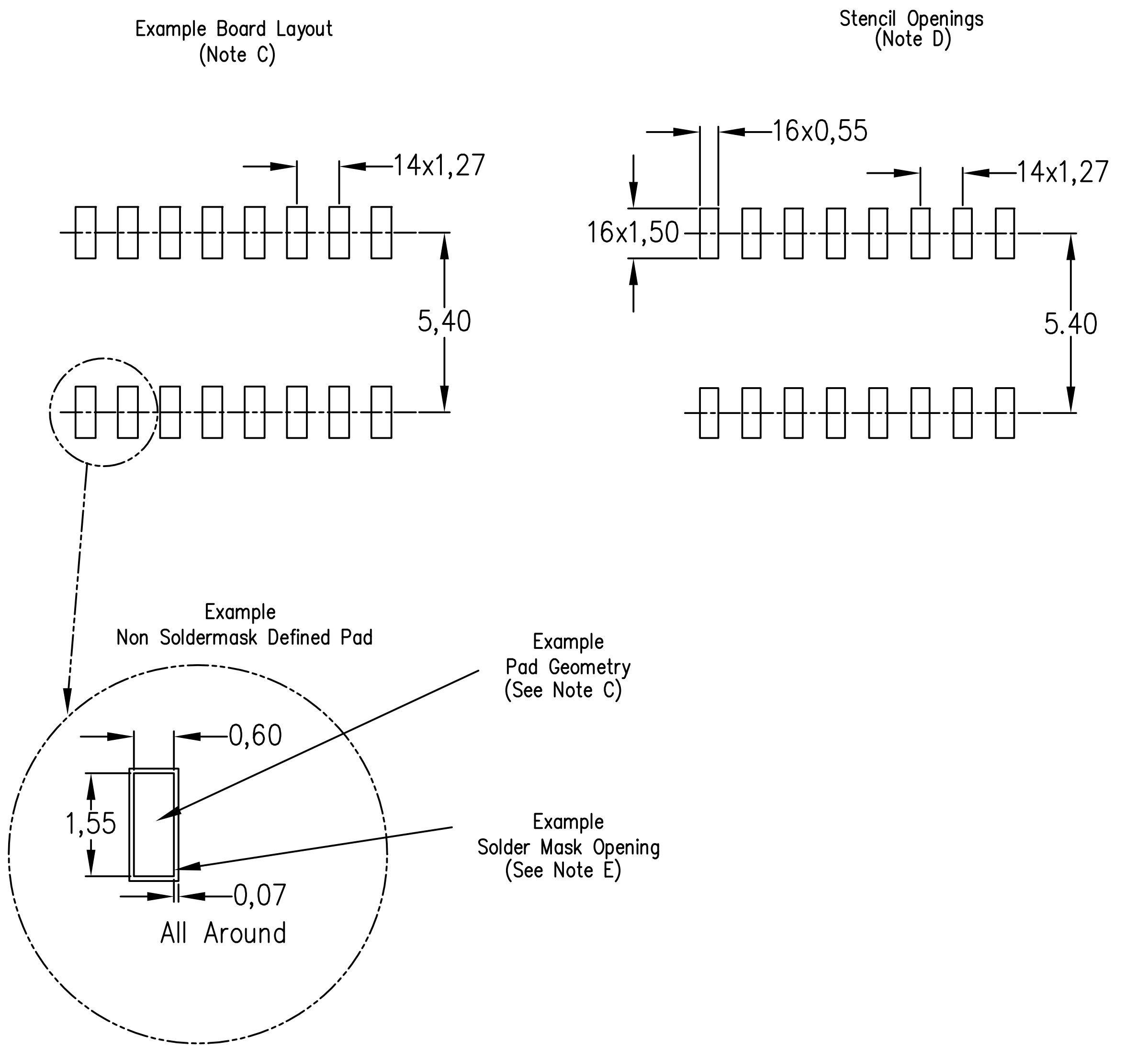
D (R-PDSO-G16) PLASTIC SMALL OUTLINE



4040047-6/M 06/11

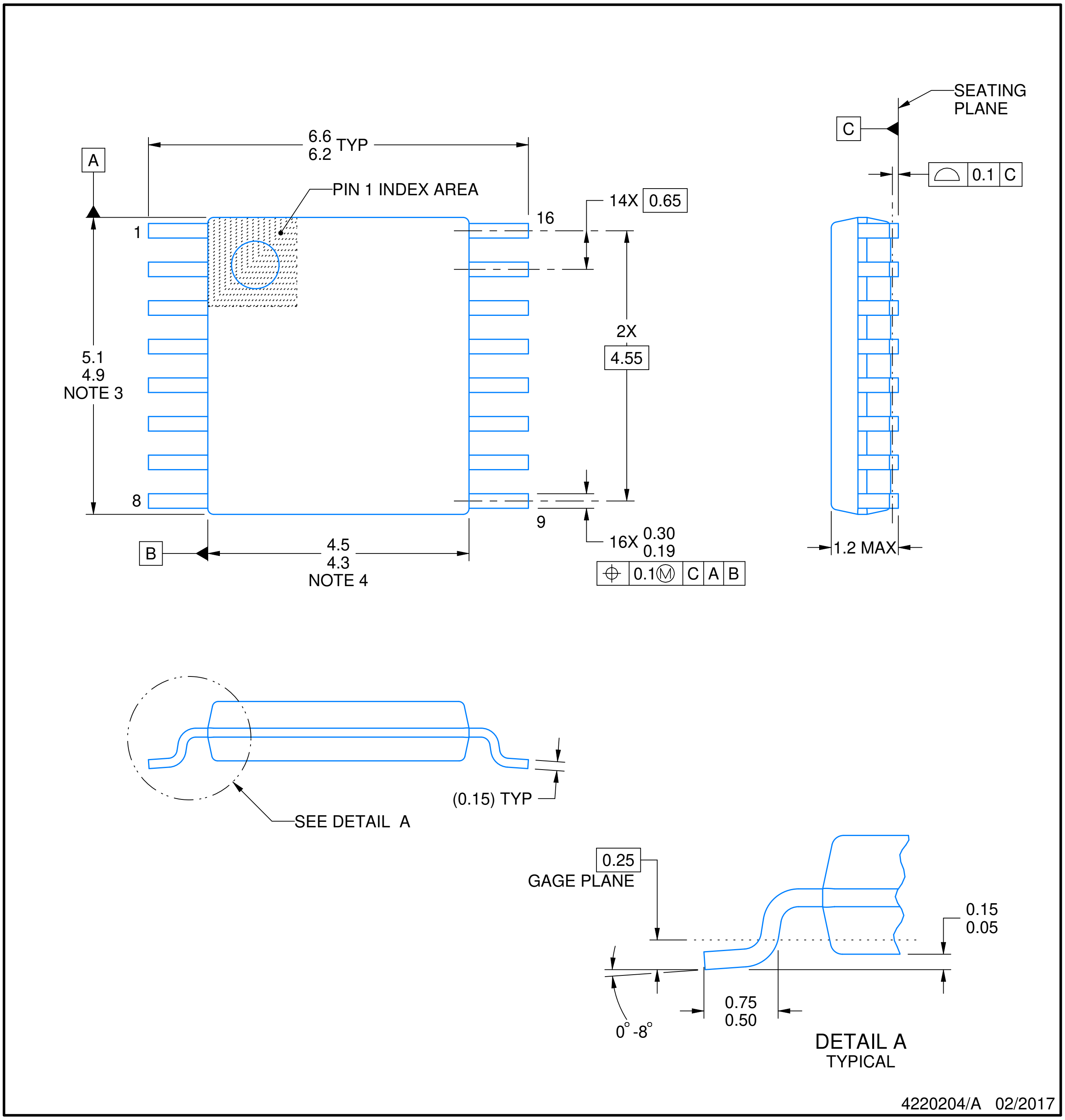
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



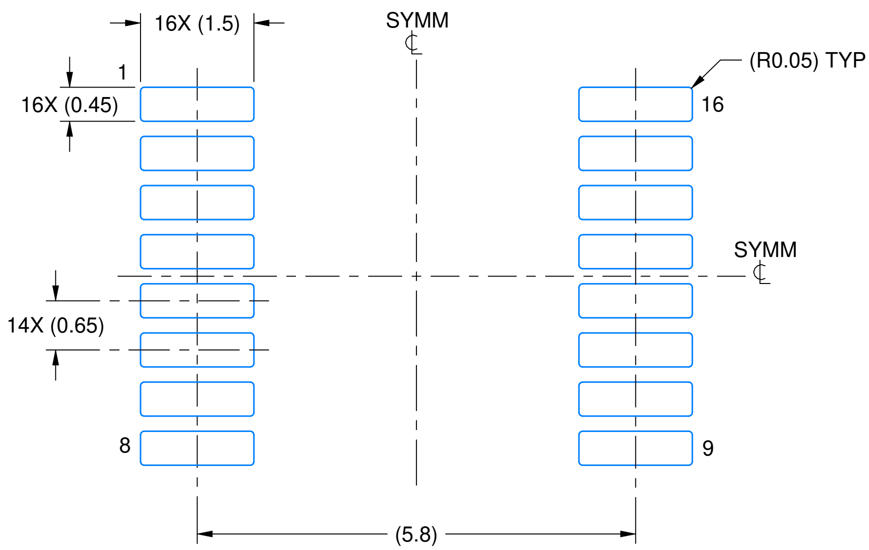
4211283–4/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

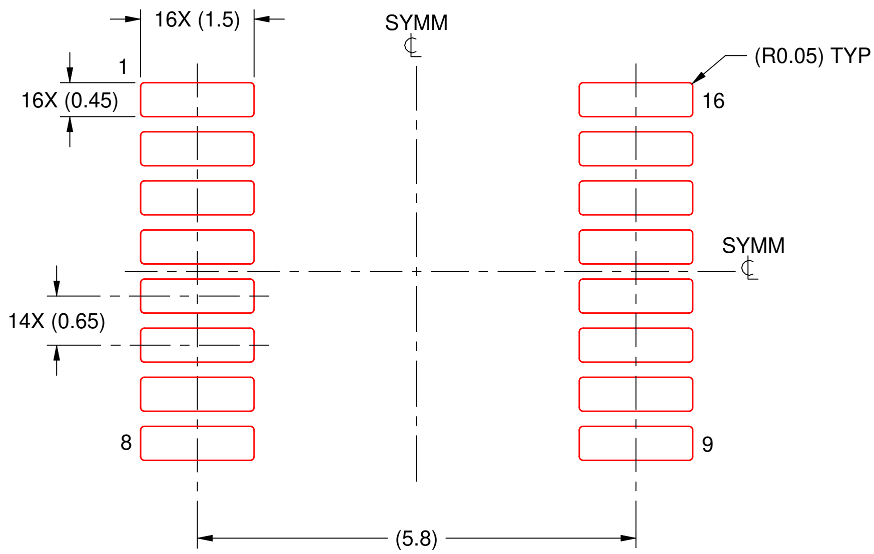
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

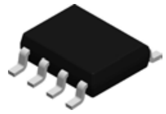


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

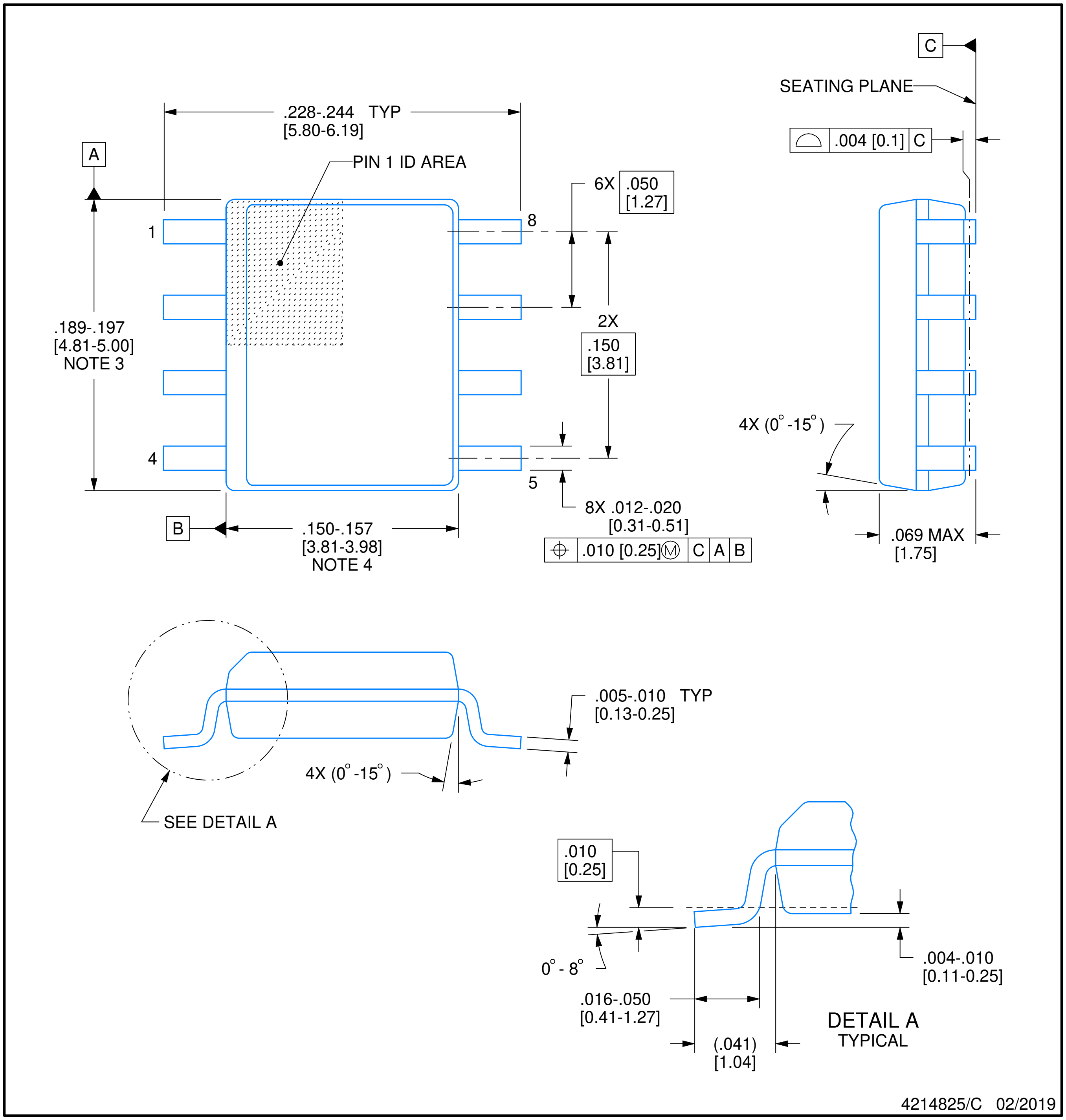


PACKAGE OUTLINE

D0008A

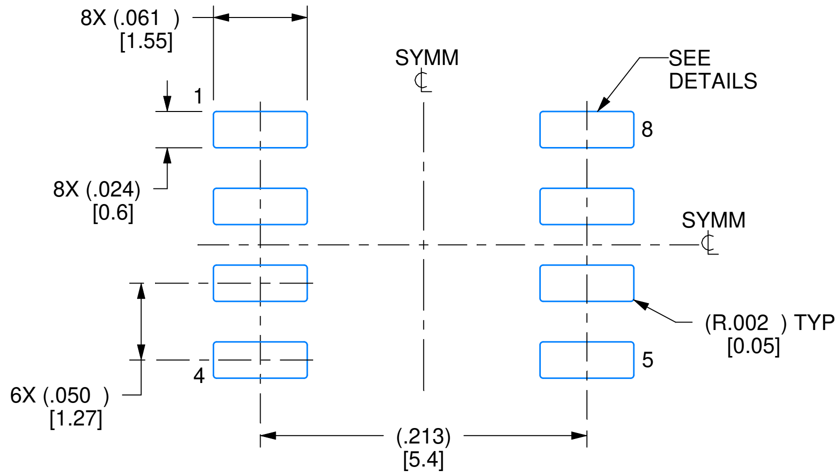
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

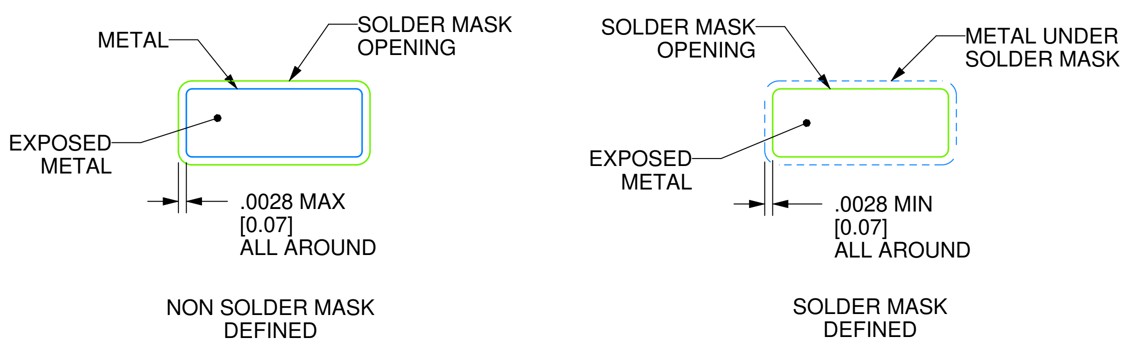


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

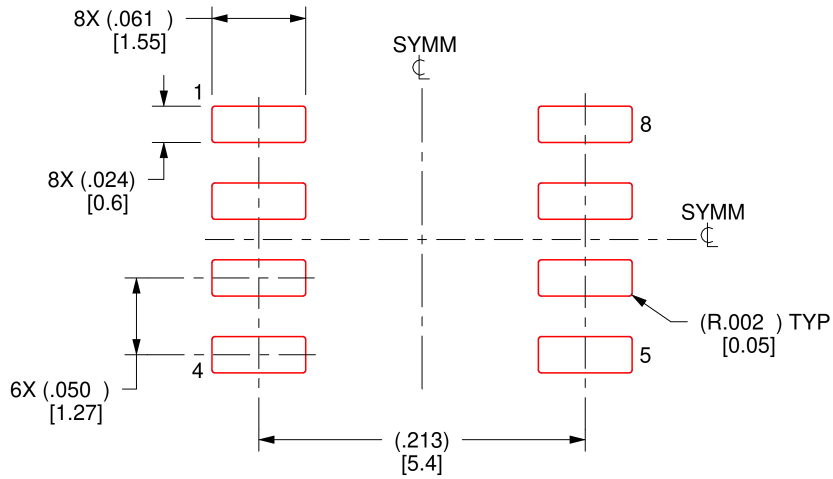
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.