19-0621; Rev 0; 10/06

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

General Description

The MAX13342E/MAX13345E USB-compliant transceivers are designed to minimize the area and external components required to interface low-voltage ASICs to USB. The devices comply with USB 2.0 specification for full-speed-only (12Mbps) operation. The transceivers include an internal 3.3V regulator, an internal 1.5kΩ D+ pullup resistor, and built-in ±15kV ESD protection circuitry to protect the USB I/0 ports (D+,D-). The MAX13345E also has internal series resistors, allowing it to be wired directly to a USB connector.

These devices operate with logic-supply voltages as low as +2.3V, ensuring compatibility with low-voltage ASICs. A low-power mode reduces current consumption to less than 45µA. An enumerate function controls the D+ pullup resistor, allowing devices to logically disconnect while remaining plugged in.

The MAX13342E has controlled output impedance of 2Ω (max) on D+/D-, allowing the use of external switches to multiplex two different USB devices onto a single USB connector. The MAX13345E has 43.5Ω (max) internal resistors on D+/D- for direct connection to the USB connector.

The MAX13342E/MAX13345E are equipped with DAT and SE0 interface signals. These transceivers provide a USB detection function that monitors the presence of USB V_{BUS} and signals the event.

These devices operate over the extended -40°C to +85°C temperature range and are available in UCSP™ 2.0mm x 1.5mm and 14-pin TDFN (3mm x 3mm) packages.

UCSP™ is a trademark of Maxim Integrated Products, Inc.

Applications

PDAs

PC Peripherals

Cellular Telephones

Data Cradles

MP3 Players

Pin Configurations and Selector Guide appear at end of data sheet.

Features

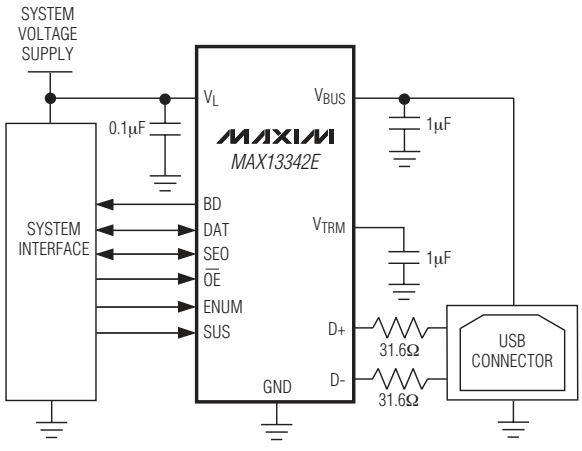
- **USB 2.0 (Full-Speed, 12Mbps)-Compliant Transceiver**
- **Internal Pullup**
- **V_{BUS} Detection**
- **Internal Series Resistors (MAX13345E)**
- **±15kV (HBM) ESD Protection on D+, D-, and V_{BUS}**
- **Enumeration Input Controls D+ Pullup Resistor**
- **Supports 3-Wire DAT/SE0 Interface**
- **+2.3V to +3.6V Interface Voltage (V_L)**
- **No Power-Supply Sequencing Required**
- **Low USB Output Impedance (MAX13342E)**

Ordering Information

PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX13342EETD+	14 TDFN-EP (3mm x 3mm)	ACZ	T1433-2
MAX13342EEBC+*	12 UCSP (2.0mm x 1.5mm)	ACU	B12-3
MAX13345EETD+	14 TDFN-EP (3mm x 3mm)	ADA	T1433-2
MAX13345EEBC+*	12 UCSP (2.0mm x 1.5mm)	ACX	B12-3

**Future product—contact factory for availability.*
+Denotes lead-free package.
EP = Exposed pad.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

ABSOLUTE MAXIMUM RATINGS

(All voltages refer to GND unless otherwise noted.)
Supply Voltage (V_{BUS}) .....-0.3V to +6V
System Supply Voltage (V_L) .....-0.3V to +6V
Output of Internal Regulator (V_{TRM}) .....-0.3V to (V_{BUS} + 0.3V)
Input Voltage (D+, D-) .....-0.3V to +6V
SUS, BD .....-0.3V to (V_L + 0.3V)
ENUM, SE0, DAT .....-0.3V to (V_L + 0.3V)
Short-Circuit Current to V_{BUS} or GND (D+, D-) .....±150mA
Maximum Continuous Current (all other pins) .....±15mA

Continuous Power Dissipation (T_A = +70°C)
14-Pin TDFN (derate 18.5mW/°C above +70°C) 1482mW
4mm x 3mm UCSP
(derate 6.5mW/°C above +70°C).....518mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Bump Soldering .....+235°C
Lead Soldering (10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BUS} = +4.0V to +5.5V, V_L = +2.3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{BUS} = +5.0V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUTS (V_{BUS}, V_{TRM}, V_L)						
V_{BUS} Input Range	V_{BUS}		4.0		5.5	V
V_L Input Range	V_L		2.3		3.6	V
Regulated Supply-Voltage Output	V_{TRM}		3.0	3.3	3.6	V
Operating V_{BUS} Supply Current	I_{VBUS}	Full-speed transmitting/receiving at 12Mbps, C_L = 50pF on D+ and D-			10	mA
Operating V_L Supply Current	I_{VL}	Full-speed transmitting/receiving at 12Mbps, C_L = 15pF receiver outputs, V_L = 2.5V		1.5		mA
Full-Speed Idle and SE0 Supply Current	$I_{VBUS(IDLE)}$	Full-speed idle, V_{D+} >2.7V, V_{D-} <0.3V			500	µA
		SE0: V_{D-} <0.3V, V_{D+} <0.3			500	
Static V_L Supply Current	$I_{VL(STATIC)}$	Full-speed idle, SE0 or suspend mode			10	µA
Suspend Supply Current	$I_{VBUS(SUSP)}$	SE0 = DAT= open; SUS = $\overline{OE}$ = high		30	45	µA
Disable-Mode Supply Current	$I_{VBUS(DIS)}$	V_L = GND or open			25	µA
Sharing-Mode V_L Supply Current	$I_{VL(SHARING)}$	V_{BUS} = GND or open, $\overline{OE}$ = low, SE0 = DAT = low or high, SUS = high			5	µA
D+/D- Supply Current	$I_{D+/D-}$	V_{BUS} = GND or open			20	µA
V_{BUS} Power-Supply Detection Threshold	V_{TH_VBUS}	V_L > 2.3V	0.8		3.6	V
V_{BUS} Power-Supply Detection Hysteresis	$V_{VBUSHYS}$			100		mV
V_L Power-Supply Threshold	V_{TH_VL}			850		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{BUS} = +4.0V to +5.5V, V_L = +2.3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{BUS} = +5.0V, V_L = +2.5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS AND OUTPUTS (DAT, SE0, $\overline{OE}$, ENUM, SUS, BD)						
Input-High Voltage	V_{IH}		0.7 x V_L			V
Input-Low Voltage	V_{IL}				0.3 x V_L	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_L - 0.4			V
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Input Leakage Current	I_{LKG}		-1		+1	µA
Input Capacitance		Measured from input to GND		10		pF
ANALOG INPUTS AND OUTPUTS (D+/D-)						
Differential Input Sensitivity	V_{ID}	$\lvert V_{D+} - V_{D-} \rvert$	200			mV
Differential Common-Mode Voltage Range	V_{CM}	Includes V_{ID} range	0.8		2.5	V
Single-Ended Input Voltage High	V_{IHSE}		2.0			V
Single-Ended Input Voltage Low	V_{ILSE}				0.8	V
Receiver Single-Ended Hysteresis	V_{HYS}			200		mV
Output-Voltage Low	V_{OLD}	R_L = 1.5kΩ from D+ or D- to 3.6V			0.3	V
Output-Voltage High	V_{OHD}	R_L = 15kΩ from D+ or D- to GND	2.8		3.6	V
Off-State Leakage Current		Tri-state driver	-1		+1	µA
Transceiver Capacitance	C_{IND}	Measured from D+ or D- to GND		20		pF
Driver Output Impedance	R_{OUT}	MAX13342E	4		14	Ω
		MAX13345E	28		43	
Internal Pullup Resistor	R_{PU}		1.425	1.500	1.575	kΩ
Input Impedance	Z_{IN}	Drivers off, tri-state driver, ENUM = 0, V_{D+}, V_{D-} = 0 OR +3.6V	1			MΩ
LINEAR REGULATOR						
External Capacitor	C_{OUT}	Compensation of linear regulator	1			µF
ESD PROTECTION (D+, D-)						
Human Body Model				±15		kV
IEC 61000-4-2 Air-Gap Discharge				±8		kV
IEC 61000-4-2 Contact Discharge				±8		kV

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

TIMING CHARACTERISTICS

(V_{BUS} = +4V to +5.5V, V_L = +2.3V to +3.6V, ENUM = V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{BUS} = +5V, V_L = +2.5V, T_A = +25°C.) (Note 1)

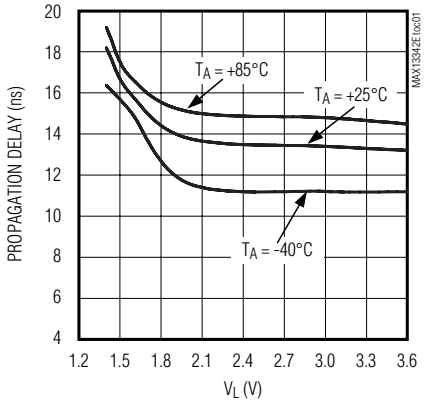
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMITTER (C_L = 50pF)							
Rise Time	t_{FR}	10% to 90% of $\lvert V_{OHD}-V_{OLD}\rvert$ with an external 31.6Ω series resistor (MAX13342E), Figures 3, 8		4		20	ns
Fall Time	t_{FF}	10% to 90% of $\lvert V_{OHD}-V_{OLD}\rvert$ with an external 31.6Ω series resistor (MAX13342E), Figures 3, 8		4		20	ns
Rise-and-Fall Time Matching (Note 1)	t_{LR}/t_{LF}	Figures 3, 8		90		110	%
Output Signal Crossover (Note 2)	V_{CRS_L}, V_{CRS_F}	Figure 4		1.3		2	V
Driver Propagation Delay	t_{PLH_DRV}	Low-to-high transition, Figures 4, 8	V_L > 2.3V			20	ns
	t_{PHL_DRV}	High-to-low transition, Figures 4, 8	V_L > 2.3V			20	
Driver-Enabled Delay Time	t_{PZH_DRV}	Off-to-high transition, Figures 5, 8	V_L > 2.3V			18	ns
	t_{PZL_DRV}	Off-to-low transition, Figures 5, 8	V_L > 2.3V			18	
Driver Disable Delay	t_{PHZ_DRV}	High-to-off transition, Figure 5, 9	V_L > 2.3V			18	ns
	t_{PLZ_DRV}	Low-to-off transition, Figures 5, 9	V_L > 2.3V			18	
RECEIVER (C_L = 15pF)							
Differential Receiver Propagation Delay	t_{PLH_RCV}	Low-to-high transition, Figures 6,10	V_L > 2.3V			20	ns
	t_{PHL_RCV}	High-to-low transition, Figures 6,10	V_L > 2.3V			20	
Single-Ended Receiver Propagation Delay	t_{PLH_SE}	Low-to-high transition, Figures 6,10				18	ns
	t_{PHL_SE}	High-to-low transition, Figures 6,10				18	
Single-Ended Receiver Disable Delay	t_{PHZ_SE}	High-to-off transition, Figure 7	V_L > 2.3V			20	ns
	t_{PLZ_SE}	Low-to-off transition, Figure 7	V_L > 2.3V			20	
Single-Ended Receiver Enable Delay	t_{PZH_SE}	Off-to-high transition, Figure 7	V_L > 2.3V			22	ns
	t_{PZL_SE}	Off-to-low transition, Figure 7	V_L > 2.3V			22	

Note 1: Parameters are 100% production tested at +25°C, unless otherwise noted. Limits over temperature are guaranteed by design.

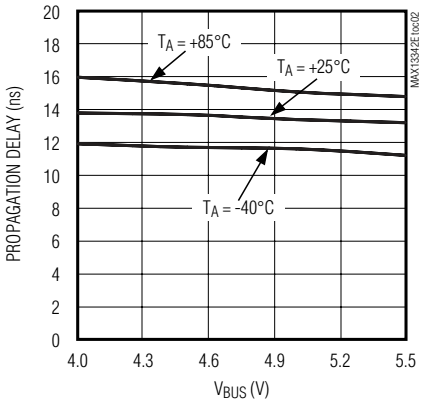
Typical Operating Characteristics

(V_{BUS} = +5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

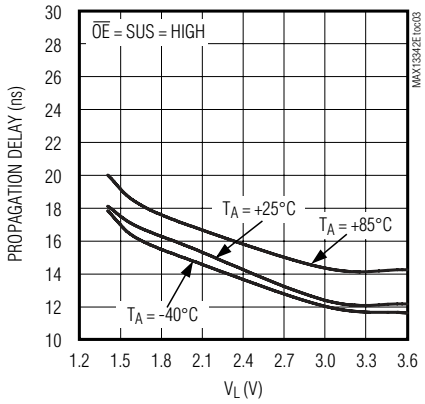
DIFFERENTIAL RECEIVER PROPAGATION DELAY vs. V_L



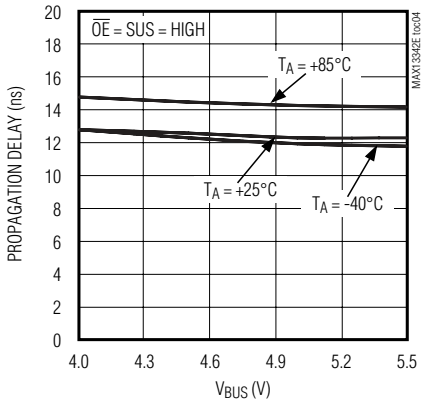
DIFFERENTIAL RECEIVER PROPAGATION DELAY vs. V_{BUS}



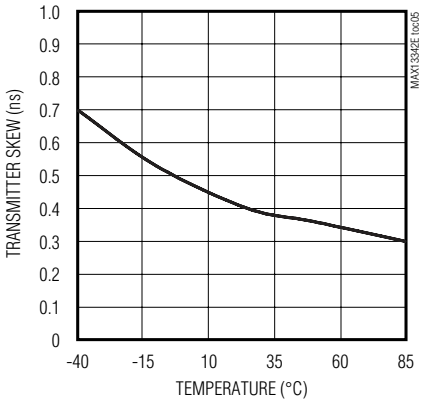
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_L



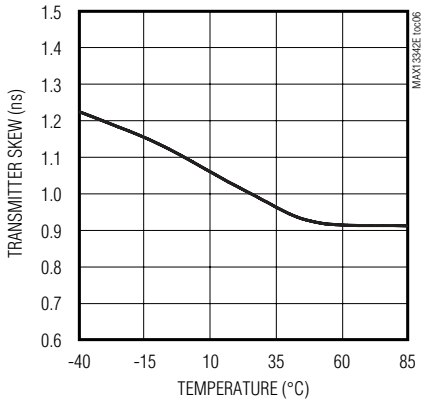
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_{BUS}



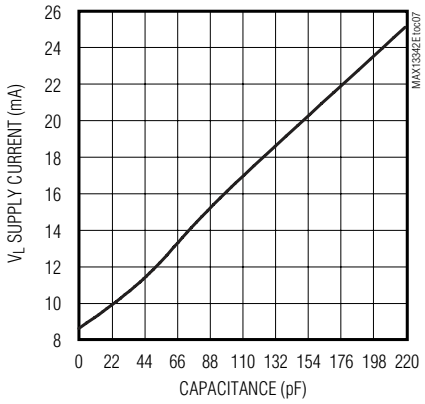
TRANSMITTER SKEW vs. TEMPERATURE



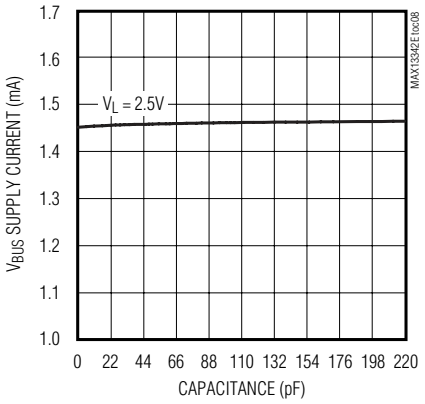
RECEIVER SKEW vs. TEMPERATURE



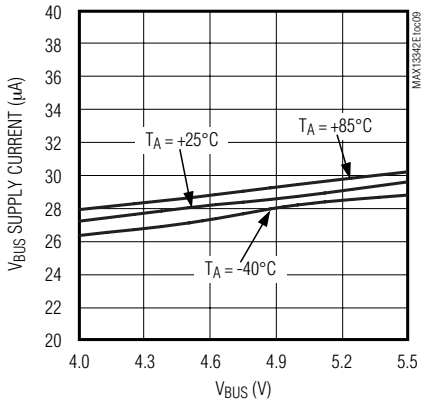
V_L SUPPLY CURRENT vs. D+/D- CAPACITANCE



V_{BUS} SUPPLY CURRENT vs. D+/D- CAPACITANCE



V_{BUS} SUSPEND CURRENT vs. V_{BUS} SUPPLY VOLTAGE

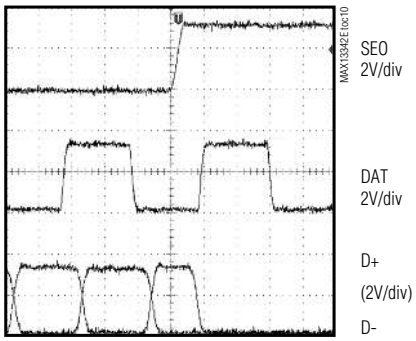


3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

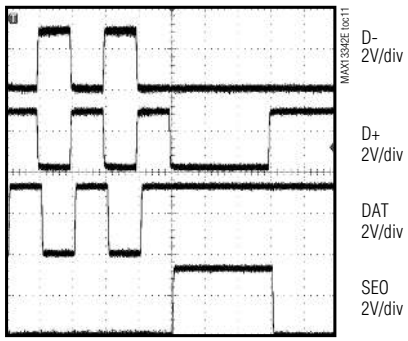
Typical Operating Characteristics (continued)

(V_{BUS} = +5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

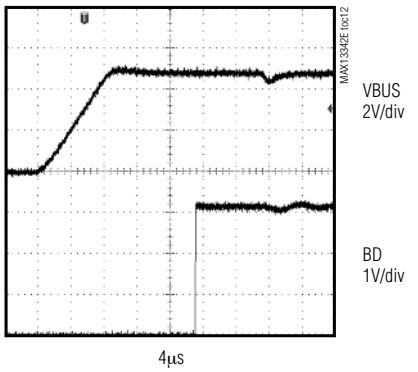
MAX13342E/MAX13345E TRANSMITTING



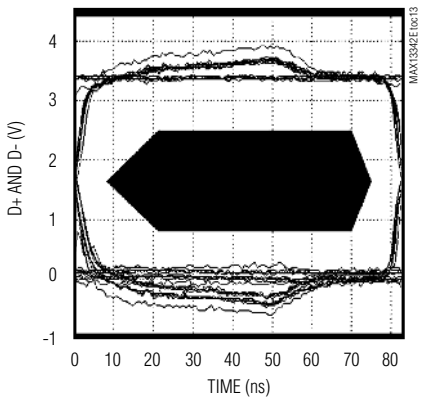
MAX13342E/MAX13345E RECEIVING



MAX13342E/MAX13345E BUS DETECTION



EYE DIAGRAM



Pin Description

PIN		NAME	FUNCTION
TDFN	UCSP		
1	B1	V_{TRM}	Regulated Output Voltage. V_{TRM} provides a 3.3V output derived from V_{BUS}. Bypass V_{TRM} to GND with a 1µF (min) low-ESR capacitor, such as ceramic or plastic film types. V_{TRM} provides power to internal circuitry and the internal D+ pullup resistor. Do not use V_{TRM} to power external circuitry. These USB transceivers can also be powered by an externally regulated 3.3V supply connected to both V_{BUS} and V_{TRM}.
2	A1	V_L	System-Side Power-Supply Input. Connect V_L to the systems logic-level power supply. Bypass V_L to GND with a 0.1µF (min) low-ESR ceramic capacitor.
3	A2	SE0	Logic-Side Data Input/Output. SE0 operates as an input when $\overline{OE}$ is low and as an output when $\overline{OE}$ is high. As an input, when SE0 is active high, D+ and D- are both driven low. As an output, SE0 goes active high when both D+ and D- are low. (See Tables 3 and 4.)
4	A3	DAT	Logic-Side Data Input/Output. DAT operates as an input for data on D+/D- when $\overline{OE}$ is low. DAT operates as the output of the differential receiver on D+/D- when $\overline{OE}$ is high. (See Tables 3 and 4.)
5, 12	—	N.C.	No Connection. Leave N.C. unconnected. N.C. is not internally connected.
6	B3	SUS	Suspend Input. Drive SUS low for normal transceiver operation. Drive SUS high for low-power state.
7	A4	BD	USB Detector Output. A high on BD indicates that V_{BUS} is present.
8	B4	$\overline{OE}$	Output Enable. $\overline{OE}$ controls the USB transmitter outputs (D+/D-) and the interface signals (DAT, SE0) when in USB mode. Drive $\overline{OE}$ high to operate D+/D- as inputs and to operate the logic interface signals as outputs. Drive $\overline{OE}$ low to operate D+/D- as outputs and to operate the logic interface signals as inputs.
9	C4	GND	Ground
10	C3	D-	Negative USB Differential Data Input/Output. D- is wired to the USB connector directly (MAX13345E) or through a series resistor (MAX13342E). D- operates as an input when $\overline{OE}$ is high and as an output when $\overline{OE}$ is low.
11	C2	D+	Positive USB Differential Data Input/Output. D+ is wired to the USB connector directly (MAX13345E) or through a series resistor (MAX13342E). D+ operates as an input when $\overline{OE}$ is high and as an output when $\overline{OE}$ is low.
13	B2	ENUM	Enumerate. Drive ENUM high to connect the internal 1.5kΩ resistor from D+ to V_{TRM}. Drive ENUM low to disconnect the internal 1.5kΩ resistor.
14	C1	V_{BUS}	USB-Side Power-Supply Input. Connect V_{BUS} to the incoming USB power supply. Bypass V_{BUS} to GND with a 1µF ceramic capacitor.
EP	—	EP	Exposed Paddle. Connect EP to GND.

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

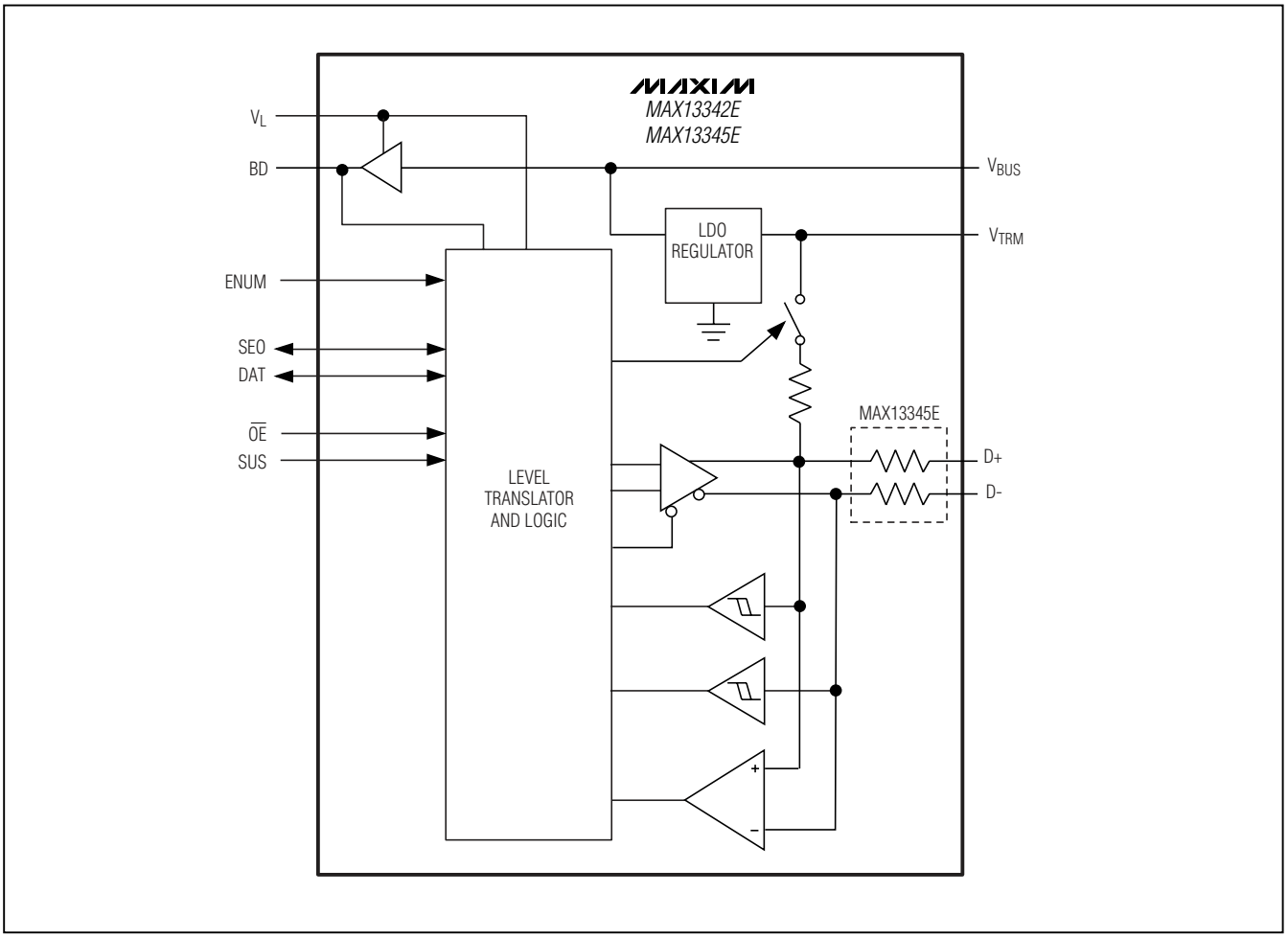


Figure 1. MAX13342E/MAX13345E Functional Diagram

Detailed Description

The MAX13342E/MAX13345E USB-compliant transceivers are designed to minimize the area and external components required to interface low-voltage ASICs to USB. The devices comply with the USB 2.0 specification for full-speed (12Mbps) operation. The transceivers include an internal 3.3V regulator, an internal 1.5kΩ D+ pullup resistor, and built-in ±15kV (HBM) ESD protection circuitry to protect D+, D-. Figure 1 is the MAX13342E/MAX13345E functional diagram.

The MAX13342E has controlled output impedance of 12Ω (max) on D+/D-, allowing the use of external switches to multiplex two different USB devices onto a single USB connector.

The MAX13345E uses internal series resistors on D+/D- to allow direct interface to the USB connector. A low-power mode reduces current consumption to less than 45µA. An enumerate function controls connection of the internal D+ pullup resistor.

The MAX13342E/MAX13345E are equipped with DAT and SE0 interface signals and support the 3-wire USB tranceiver interface. Although the 3-wire interface is commonly associated with USB On-the-Go transceivers, the MAX13342E/MAX13345E support USB peripherals only. These transceivers provide a USB V_{BUS} detection function that monitors the presence of USB V_{BUS} and signals the event.

Interface

The MAX13342E/MAX13345E control signals are used to control the USB D+/D- lines. V_L powers the logic-side interface and sets the input and output thresholds of these signals. The control signals for the MAX13342E and MAX13345E are DAT, SE0, and $\overline{OE}$.

Power-Supply Configuration

Normal Operating Mode

See Table 1 for various power-supply configurations.

V_{BUS} supplies power to the USB transceivers. Connect V_{BUS} to a +4V to +5.5V supply. Connect V_L to a +2.3V to +3.6V supply. V_{BUS} is typically connected directly to the USB connector. An internal regulator provides 3.3V to internal circuitry, and a regulated 3.3V output at V_{TRM}, in addition to powering the internal D+ pullup resistor. The MAX13342E and MAX13345E can be powered by connecting both V_{BUS} and V_{TRM} to a 3.3V external regulator.

Low-Power Mode

Operate the transceivers in low-power mode by asserting SUS high. In low-power mode, the USB differential receiver is turned off and V_{BUS} consumes less than 45µA of supply current. The single-ended D+ and D- receivers are still active when driving SUS high.

Sharing Mode

Connect V_L to a system power supply and leave V_{BUS} (or V_{BUS} and V_{TRM}) unconnected or connected to GND. D+ and D- are tri-stated, allowing other circuitry to share the USB D+ and D- line. V_L consumes less than 5µA of supply current. When operating the transceivers in sharing mode, the SUS input is ignored, and the interface signals (SE0, DAT) are high impedance.

Disable Mode

Connect V_{BUS} to a system power supply and leave V_L unconnected or connect to ground. In disable mode, D+ and D- are tri-stated, and V_{BUS} and/or V_{TRM} (or V_{BUS} and V_{TRM}) consume less than 25µA. When operating the transceivers in disable mode, $\overline{OE}$, SUS, and inputs to the interface control signals are ignored. (See Table 2.)

Table 1. Power-Supply Configuration

V_{BUS} (V)	V_{TRM} (V)	V_L (V)	CONFIGURATION	NOTES
+4.0 to +5.5	+3.0 to +3.6 output	+2.3 to +3.6	Normal mode	—
+4.0 to +5.5	+3.0 to +3.6 output	GND or floating	Disable mode	Table 2
GND or Floating	High Z	+2.3 to +3.6	Sharing mode	Table 2

Table 2. Disable-Mode and Sharing-Mode Connection

INPUTS/OUTPUTS	DISABLE MODE	SHARING MODE
V_{BUS} / V_{TRM}	4V to 5.5V	Floating or connected to GND
V_L	Floating or connected to GND	2.3V to 3.6V input
D+ and D-	High impedance	High impedance
DAT, SE0	High impedance	High impedance
SUS	High impedance	High impedance
BD	Low	Low

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

3-Wire DAT/SE0 Interface

The MAX13342E/MAX13345E use DAT and SE0 to drive data or a single-ended zero onto the D+/D- lines. When $\overline{OE}$ is low, SE0 is an input and functions as a single-ended zero driver. When SE0 is high, both D+ and D- are driven low. When SE0 is driven low, the D+/D- outputs are controlled by DAT.

DAT is used to send data on D+/D- when both $\overline{OE}$ and SE0 are low. When DAT is high, D+ is driven high and D- is driven low. When DAT is low, D+ is driven low and D- is driven high.

In receive mode ($\overline{OE}$ = high), DAT is the output of the differential receiver connected to D+ and D-. SE0 only goes active high when both D+ and D- are low.

Control Signals

USB Detection

The MA13342E/MAX13345E USB detection function indicates that V_{BUS} is present. The MAX13342E/MAX13345E push-pull bus detection output (BD) monitors V_{BUS}, and asserts high when V_{BUS} and V_L are present. BD asserts low if V_{BUS} is less than +3.6V and enters sharing mode.

$\overline{OE}$

$\overline{OE}$ controls the direction of communication when V_L and V_{BUS} are both present. When $\overline{OE}$ is low, DAT and SE0 operate as logic inputs and D+/D - are outputs. When $\overline{OE}$ is high, DAT and SE0 operate as logic outputs and D+/D- are inputs.

SUS

SUS determines whether the MAX13342E/MAX13345E operate in normal mode or in suspend mode. Drive SUS low for normal operation. Drive SUS high to enable suspend mode. In suspend mode, the single-ended receivers (D+/D-) are active to detect a wake-up event. Supply current decreases to less than 45µA in suspend mode.

The MAX13342E/MAX13345E can transmit data on D+ and D- while in suspend mode. This function is used to signal a remote wake-up event.

ENUM

A 1.5kΩ pullup resistor on D+ is used to indicate full-speed (12Mbps) operation. Drive ENUM high to connect the internal pullup resistor from D+ to V_{TRM}. Drive ENUM low to disconnect the internal pullup resistor from D+ to V_{TRM}.

D+ and D-

D+ and D- are bidirectional signals and are ESD protected to ±15kV (HBM). $\overline{OE}$ controls the direction of D+ and D- when in USB normal mode (Tables 3 and 4).

V_{TRM}

An internal linear regulator generates the V_{TRM} voltage (+3.3V typ). V_{TRM} derives power from V_{BUS} (see the *Power-Supply Configuration* section). V_{TRM} powers the internal USB circuitry and provides the pullup voltage for the internal 1.5kΩ resistor. Bypass V_{TRM} to GND with a 1µF ceramic capacitor as close to the device as possible. Do not use V_{TRM} to provide power to external circuitry.

Table 3. Transmit Truth Table

($\overline{OE}$ = 0, SUS = 0)			
INPUTS		OUTPUTS	
DAT	SE0	D+	D-
0	0	0	1
0	1	0	0
1	0	1	0
1	1	0	0

Table 4. Receive Truth Table

($\overline{OE}$ = 1, SUS = 0)			
INPUTS		OUTPUTS	
D+	D-	DAT	SE0
0	0	*DAT	1
0	1	**0	0
1	0	**1	0
1	1	X	0

**Last state*
***D+/D- differential receiver output*
X = Undefined

Applications Information

USB Data Transfer

Transmitting Data

The MAX13342E/MAX13345E transmit USB data to the USB differentially on D+ and D- when $\overline{OE}$ is low. The D+ and D- outputs are determined by SE0 and DAT (see Table 3).

Receiving Data

Drive $\overline{OE}$ high and SUS low to receive data on D+/D-. Differential data received on D+ and D- appear at DAT. SE0 goes high only when both D+ and D- are low (Table 4).

External Resistors (MAX13342E)

The MAX13342E provides low internal resistance on D+/D-. Two external series resistors for impedance matching are required for USB. Place the resistors in between the MAX13342E and the USB connector (see Figure 2).

External Capacitors

Use three external capacitors for proper operation. Bypass V_L to GND with a 0.1µF ceramic capacitor. Bypass V_{BUS} to GND with a 1µF ceramic capacitor. Bypass V_{TRM} to GND with a 1µF (min) ceramic or plastic capacitor. Place all capacitors as close to the device as possible.

UCSP Application Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board (PCB) techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *UCSP—A Wafer-Level Chip-Scale Package* available on Maxim's website at www.maxim-ic.com/ucsp.

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

ESD Protection

The MAX13342E/MAX13345E feature ±15kV (HBM) ESD protection on D+ and D-. The ESD structures withstand high ESD in all states: normal operation, suspend, and powered down. For the ±15kV ESD structures to work correctly, a 1µF or greater capacitor must be connected from V_{TRM} to GND. V_{BUS} and D+/D- are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the IEC 61000-4-2 Contact Discharge Method
- ±8kV using the IEC 61000-4-2 Air-Gap Method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11 shows the Human Body Model, and Figure 12 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX13342E/MAX13345E help the user design equipment that meets level 4 of IEC 61000-4-2, without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 13 shows the IEC 61000-4-2 model. The Air-Gap Discharge Method involves approaching the device with a charged probe. The Contact Discharge Method connects the probe to the device before the probe is energized.

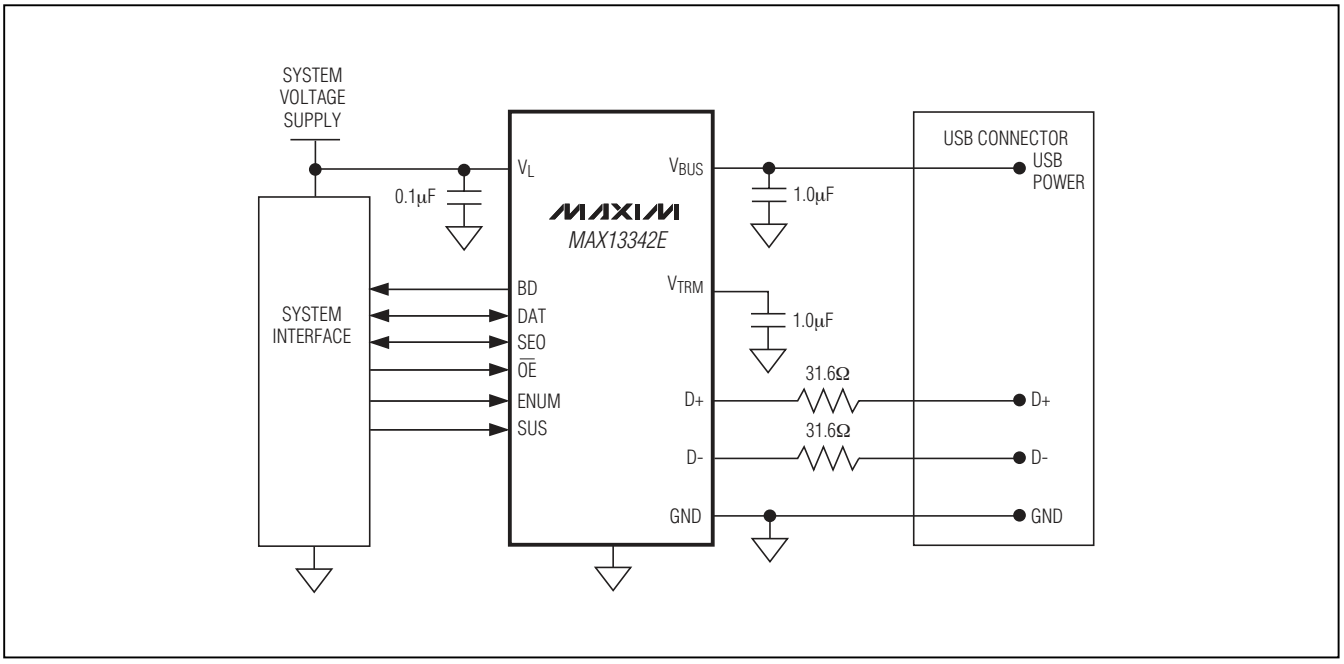


Figure 2. Adding External Resistors to the USB Connector for the MAX13342E

Timing Diagrams/Test Circuits

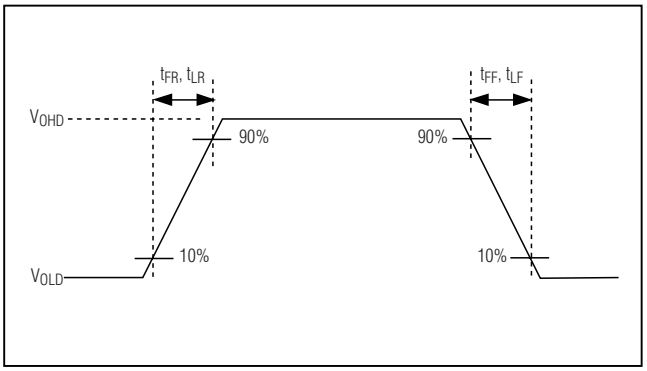


Figure 3. Rise and Fall Times

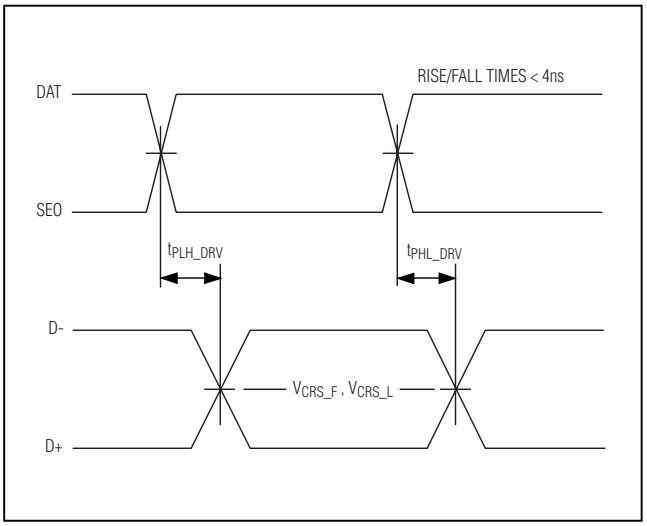


Figure 4. Timing of DAT, SE0 to D+ and D-

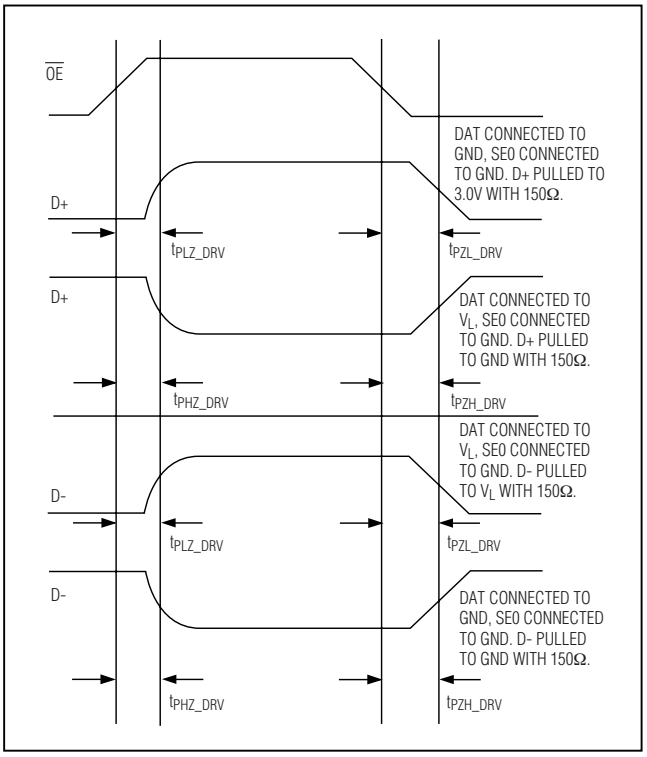


Figure 5. Enable and Disable Timing, Transmitter

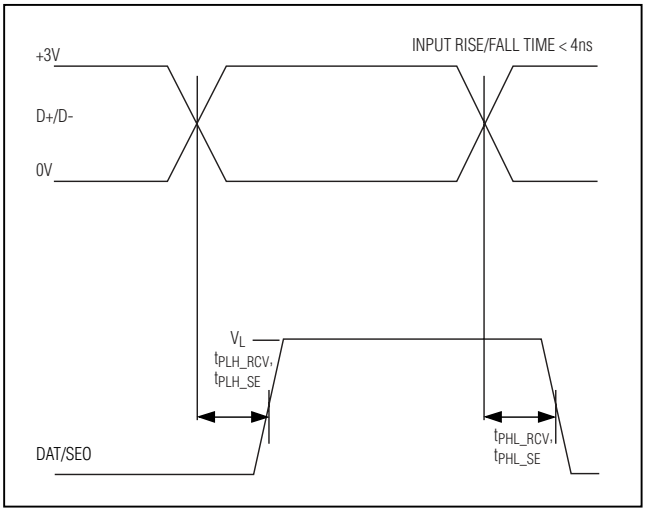


Figure 6. D+/D- to DAT, SE0 Propagation Delays

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

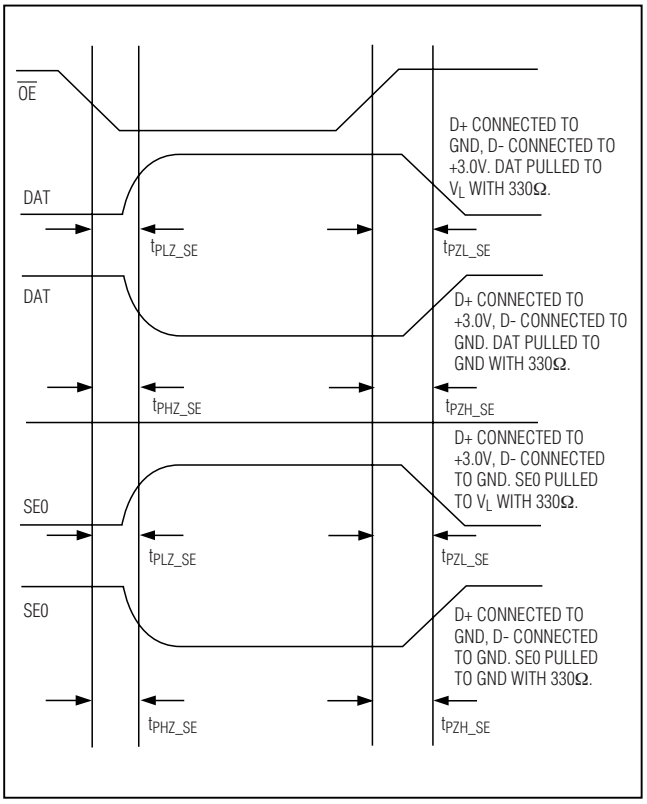


Figure 7. Receiver Enable and Disable Timing

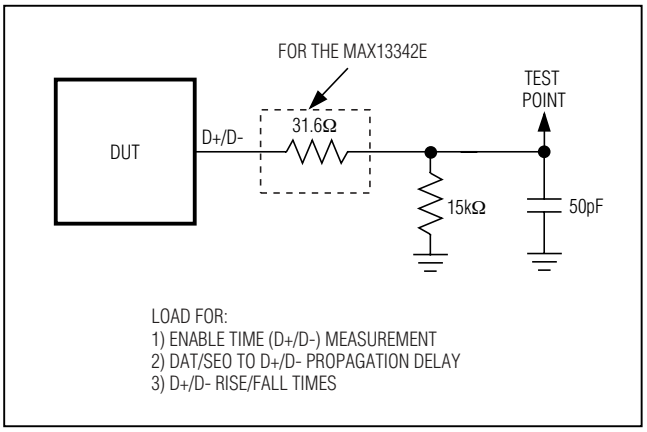


Figure 8. Load for Transmitter Propagation Delay, Enable Time, Transmitter Rise/Fall Times

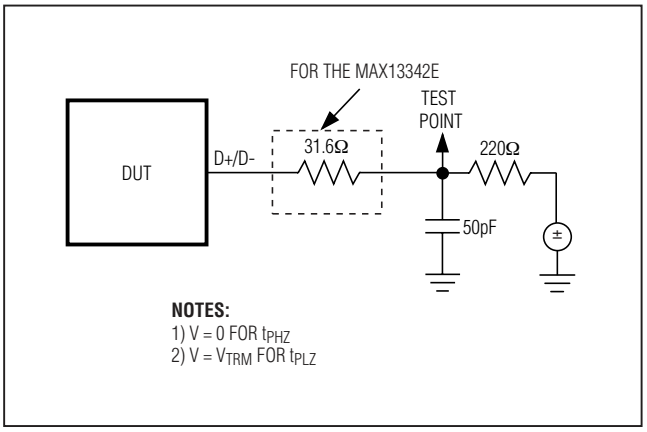


Figure 9. Load for Disable Time Measurements

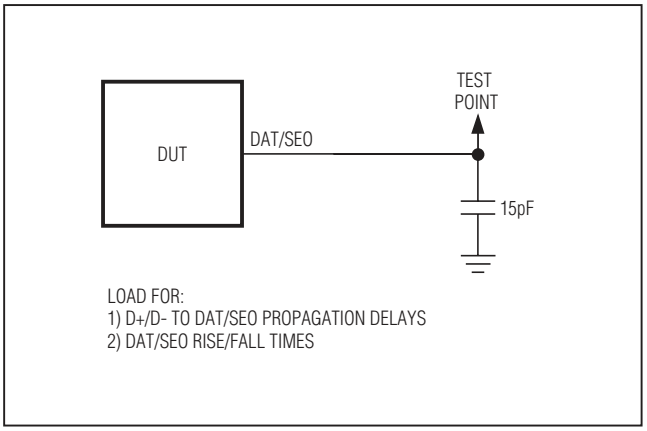


Figure 10. Load for Receiver Propagation Delay and Receiver Rise/Fall Times

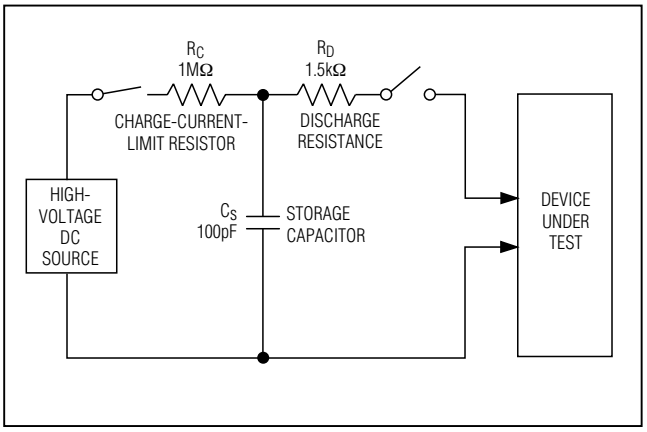


Figure 11. Human Body ESD Test Model

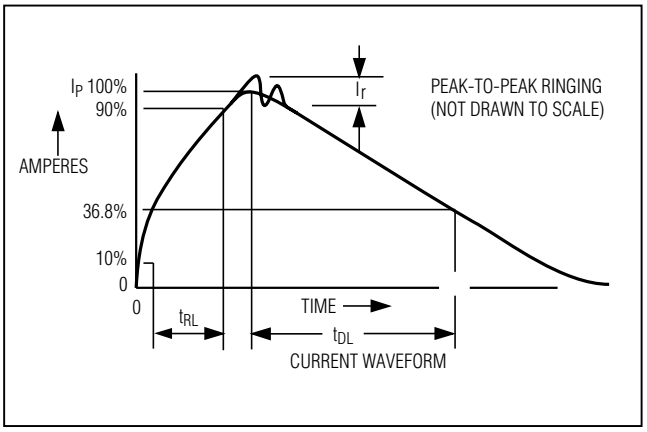


Figure 12. Human Body Model Current Waveform

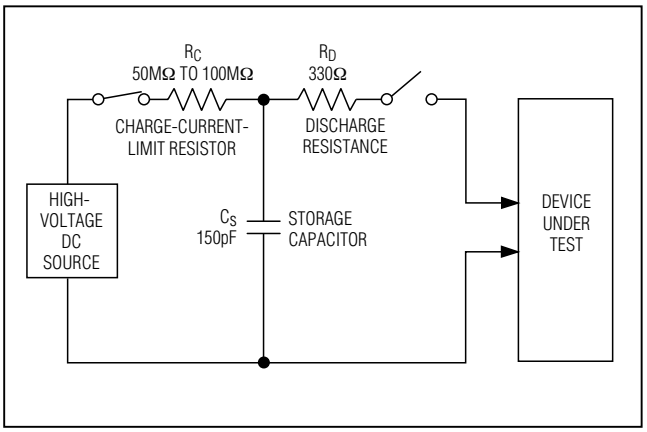
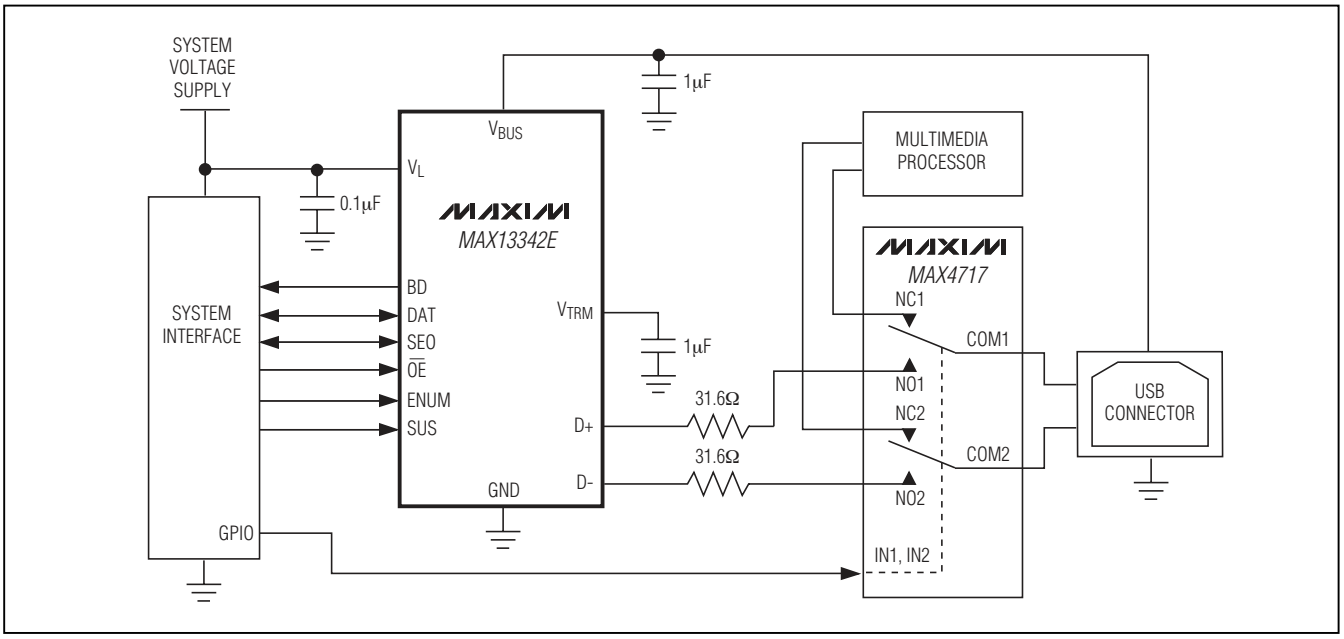


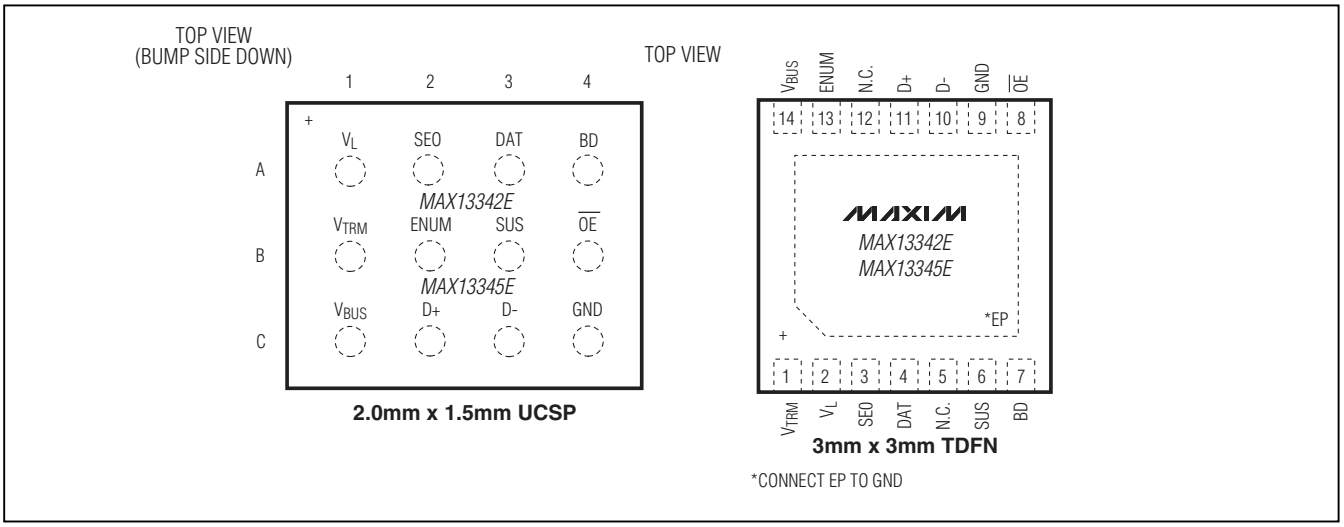
Figure 13. IEC 61000-4-2 ESD Test Model

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

Typical Application Circuit



Pin Configurations



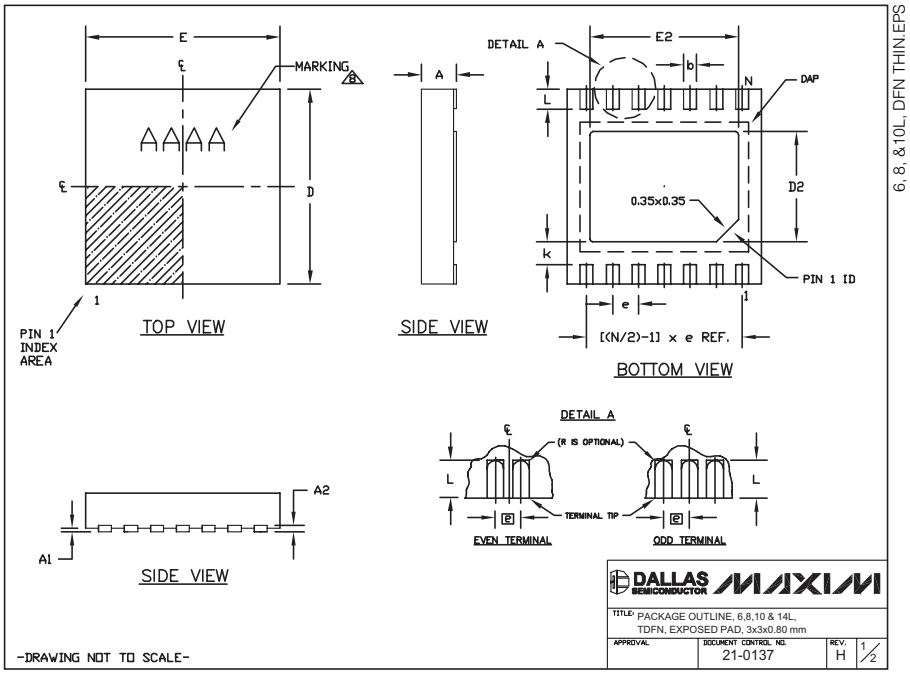
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, &10L, DFN THIN.EPS



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T633-2	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF
T833-1	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-2	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T833-3	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1033-2	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF
T1433-1	14	1.70–0.10	2.30–0.10	0.40 BSC	----	0.20–0.05	2.40 REF
T1433-2	14	1.70–0.10	2.30–0.10	0.40 BSC	----	0.20–0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

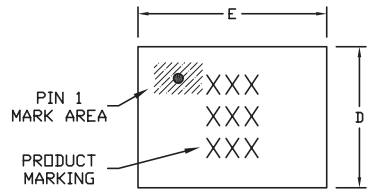
DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. H
2/2
-DRAWING NOT TO SCALE-

3-Wire Interface Full-Speed USB Transceivers With/Without Internal Series Resistors

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

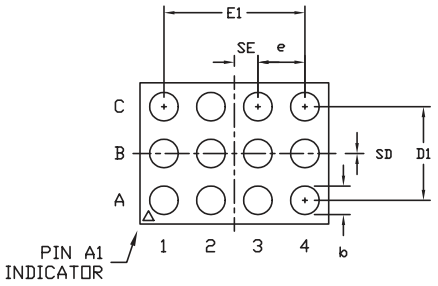
12L, UCSP 4x3.EPS



TOP VIEW

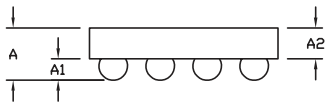
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

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