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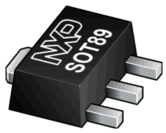


BSS192

240 V, P-channel vertical D-MOS transistor

12 December 2014 Product data sheet

1. General description

P-channel enhancement mode vertical Double-Diffused Field-Effect Transistor (D-MOSFET) in a SOT89 (SC-62) medium power and flat lead Surface Mounted Device (SMD) plastic package.

2. Features and benefits

- Direct interface to Complementary (C-MOS) transitor and Transistor-Transistor Logic (TTL) devices
- Very fast switching
- No secondary breakdown

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

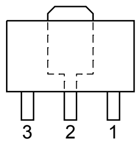
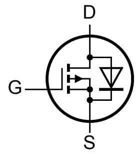
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-240	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	V_{GS} = -10 V; T_{amb} = 25 °C	[1]	-	-	-200	mA
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -200 mA; T_j = 25 °C		-	10	12	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

Scan or click this QR code to view the latest information for this product

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT89	
2	D	drain		
3	G	gate		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BSS192	SOT89	plastic surface-mounted package; die pad for good heat transfer; 3 leads	SOT89

7. Marking

Table 4. Marking codes

Type number	Marking code
BSS192	KB

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-240	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = -10 V; T_{amb} = 25 °C; t ≤ 5 s	[1]	-	-340	mA
		V_{GS} = -10 V; T_{amb} = 25 °C	[1]	-	-200	mA
		V_{GS} = -10 V; T_{amb} = 100 °C	[1]	-	-120	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 μs		-	-800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	560	mW
			[1]	-	1	W
		T_{sp} = 25 °C		-	12.5	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-200	mA

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

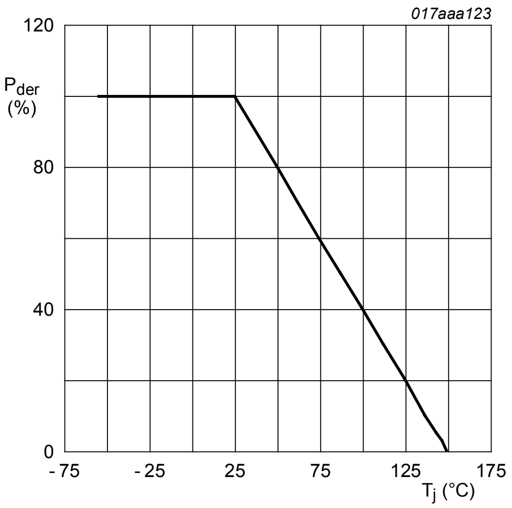


Fig. 1. MOSFET transistor: Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

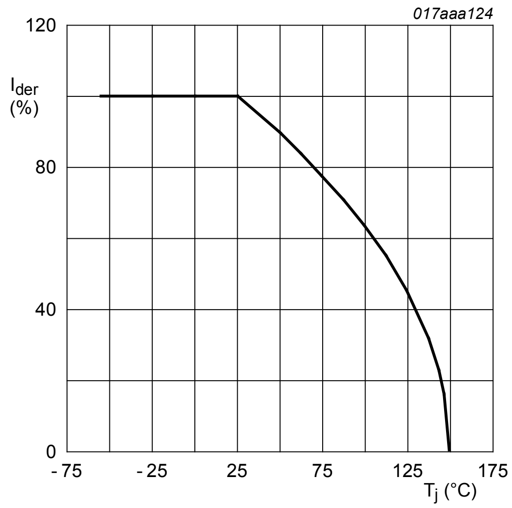
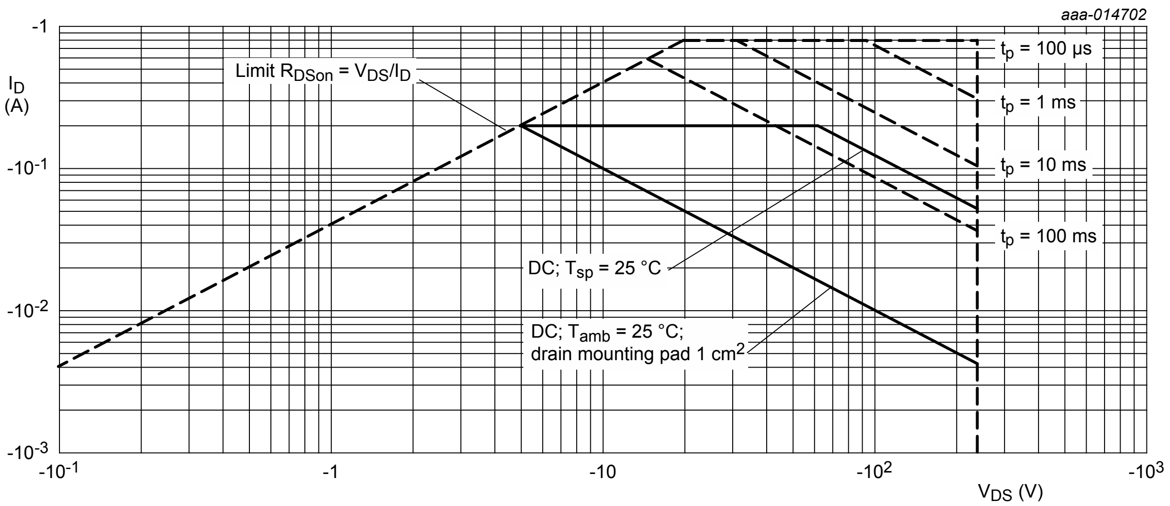


Fig. 2. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$



I_{DM} = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

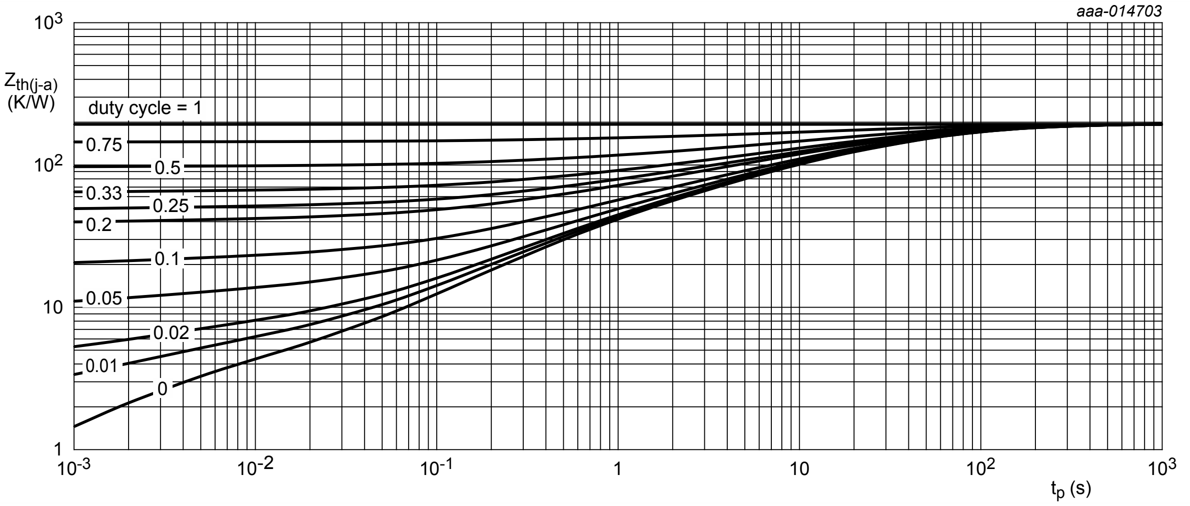
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	194	225	K/W
			[2]	-	108	125	K/W
		t ≤ 5 s	[2]	-	37	42	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	4	10	K/W

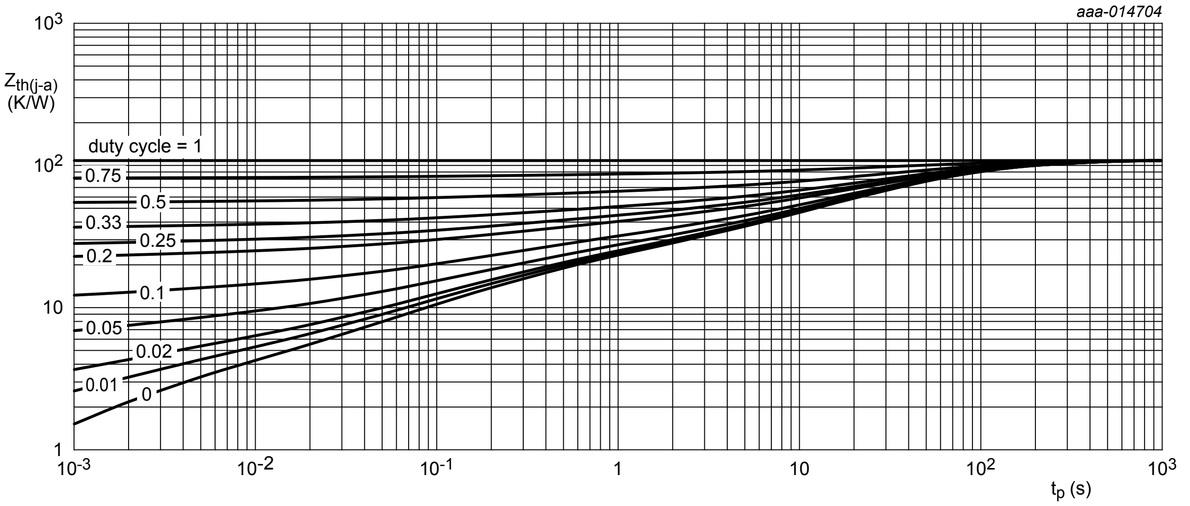
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



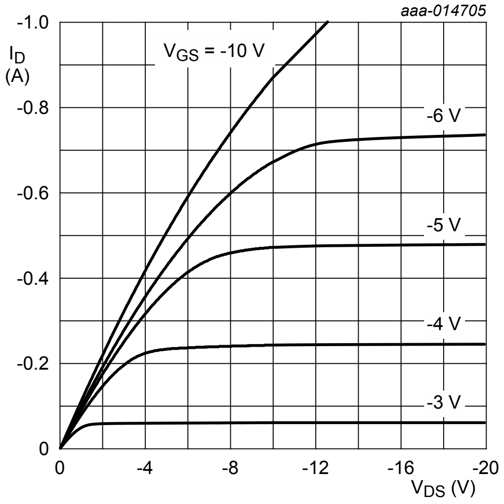
FR4 PCB, mounting pad for drain 1 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

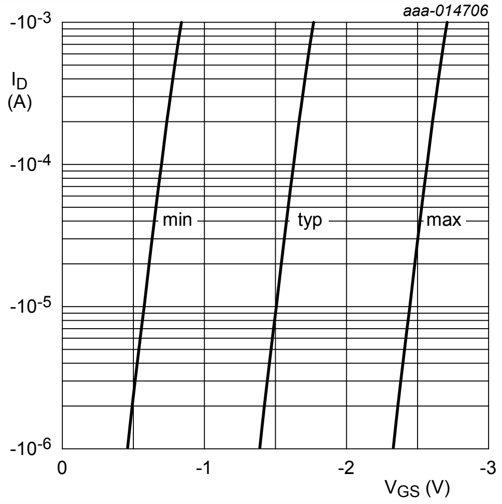
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -10 μA; V_{GS} = 0 V; T_j = 25 °C		-240	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -1 mA; V_{DS} = V_{GS}; T_j = 25 °C		-0.8	-	-2.8	V
I_{DSS}	drain leakage current	V_{DS} = -200 V; V_{GS} = 0.2 V; T_j = 25 °C		-	-0.1	-60	μA
		V_{DS} = -60 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-200	nA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -200 mA; T_j = 25 °C		-	10	12	Ω
		V_{GS} = -10 V; I_D = -200 mA; T_j = 150 °C		-	21	25	Ω
		V_{GS} = -4.5 V; I_D = -100 mA; T_j = 25 °C		-	13	18	Ω
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -200 mA; T_j = 25 °C		-	200	-	mS
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -50 V; I_D = -250 mA; V_{GS} = -10 V; T_j = 25 °C		-	1.9	5	nC
Q_{GS}	gate-source charge			-	0.3	-	nC
Q_{GD}	gate-drain charge			-	0.6	-	nC
C_{iss}	input capacitance	V_{DS} = -25 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	55	90	pF
C_{oss}	output capacitance			-	20	30	pF
C_{rss}	reverse transfer capacitance			-	5	15	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -50 V; I_D = -250 mA; V_{GS} = -10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	3.2	6	ns
t_r	rise time			-	4.6	6	ns
$t_{d(off)}$	turn-off delay time			-	11.7	20	ns
t_f	fall time			-	7	12	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = -200 mA; V_{GS} = 0 V; T_j = 25 °C		-	0.86	1.2	V



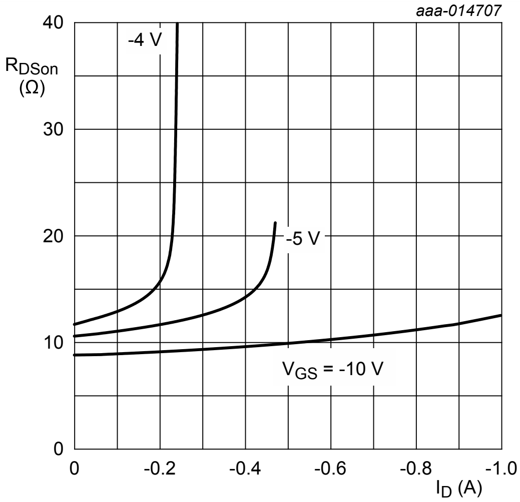
T_j = 25 °C

Fig. 6. **Output characteristics: drain current as a function of drain-source voltage; typical values**



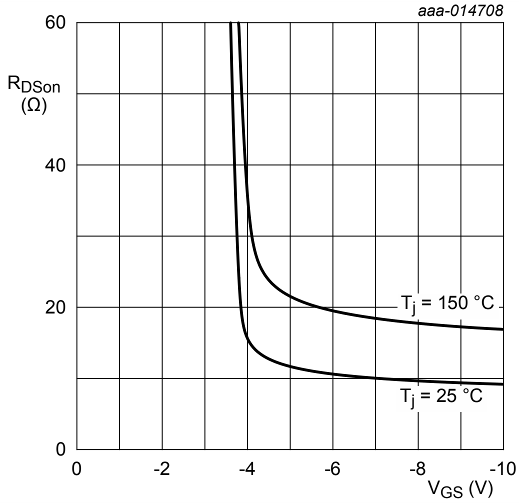
T_j = 25 °C; V_{DS} = -10 V

Fig. 7. **Sub-threshold drain current as a function of gate-source voltage**



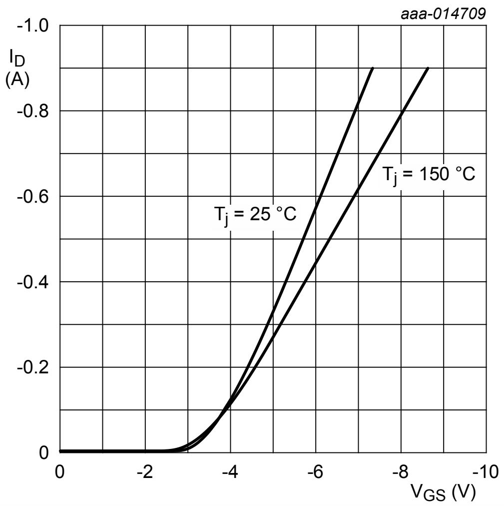
T_j = 25 °C

Fig. 8. **Drain-source on-state resistance as a function of drain current; typical values**



I_D = -200 mA

Fig. 9. **Drain-source on-state resistance as a function of gate-source voltage; typical values**



$V_{DS} > I_D \times R_{DSon}$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

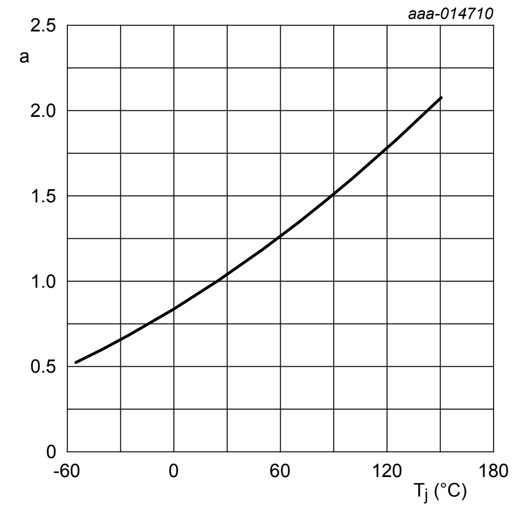
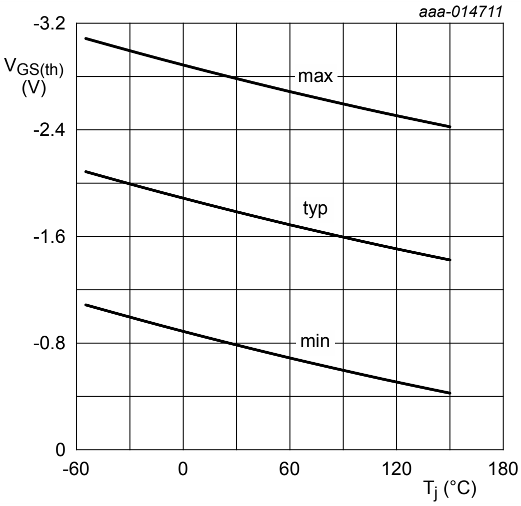


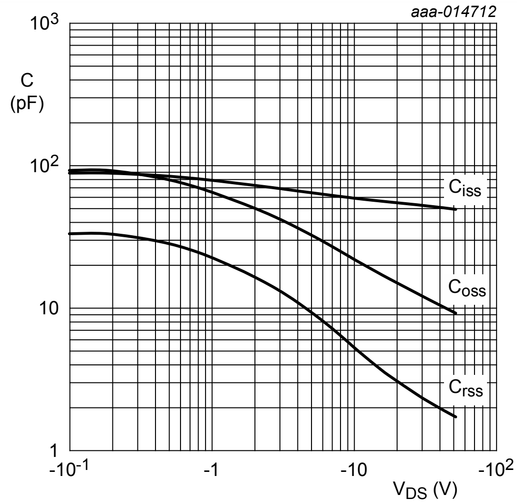
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$



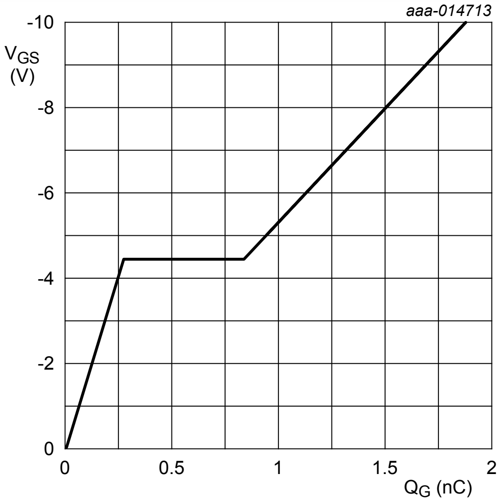
I_D = -1 mA; $V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -0.25 A; V_{DS} = -50 V; T_{amb} = 25 °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

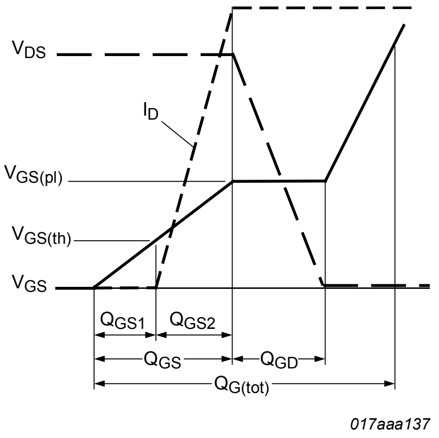
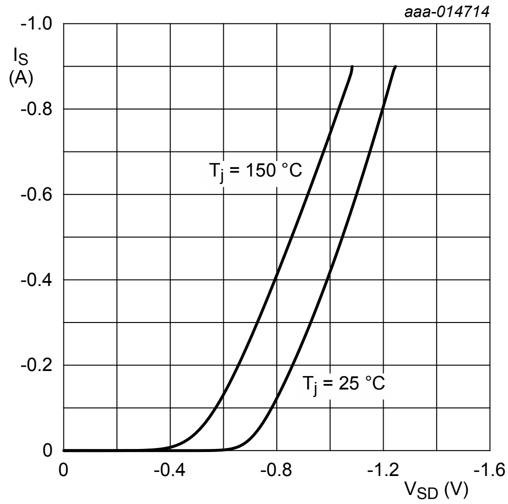


Fig. 15. MOSFET transistor: Gate charge waveform definitions



V_{GS} = 0 V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

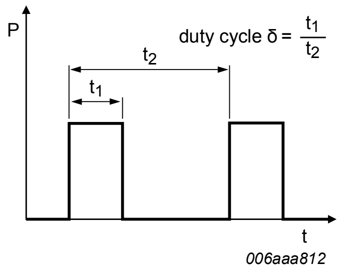
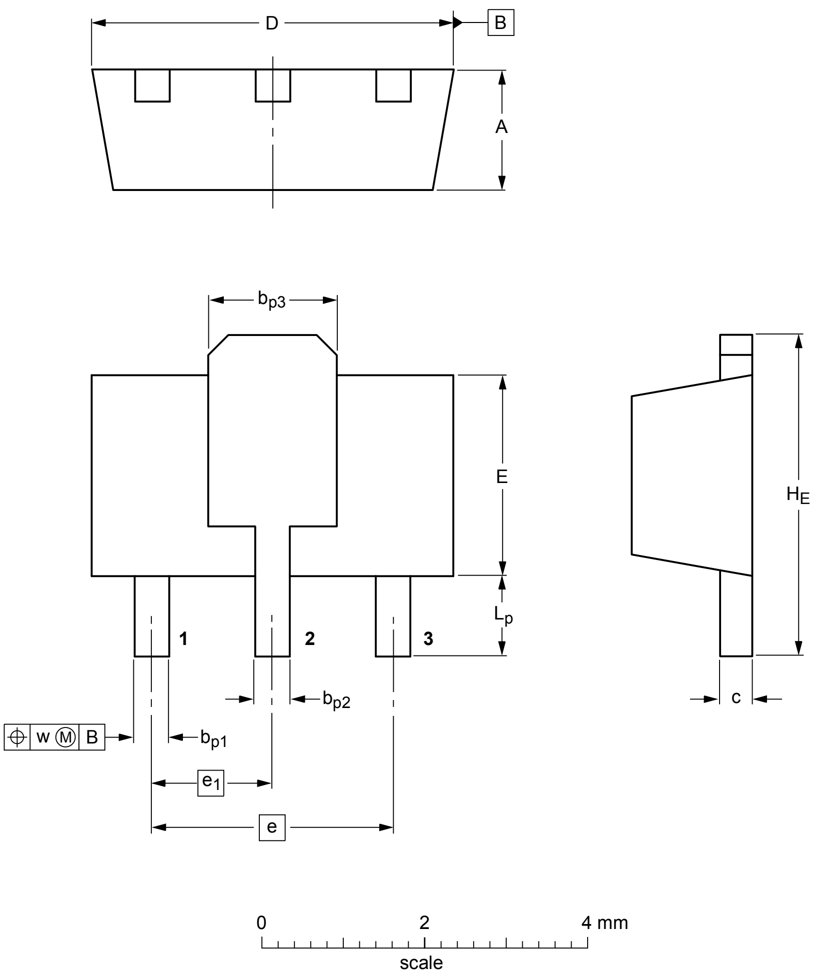


Fig. 17. Duty cycle definition

12. Package outline

Plastic surface-mounted package; exposed die pad for good heat transfer; 3 leads **SOT89**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_{p1}	b_{p2}	b_{p3}	c	D	E	e	e_1	H_E	L_p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			~~06-03-16~~ 06-08-29

Fig. 18. Package outline SOT89

13. Soldering

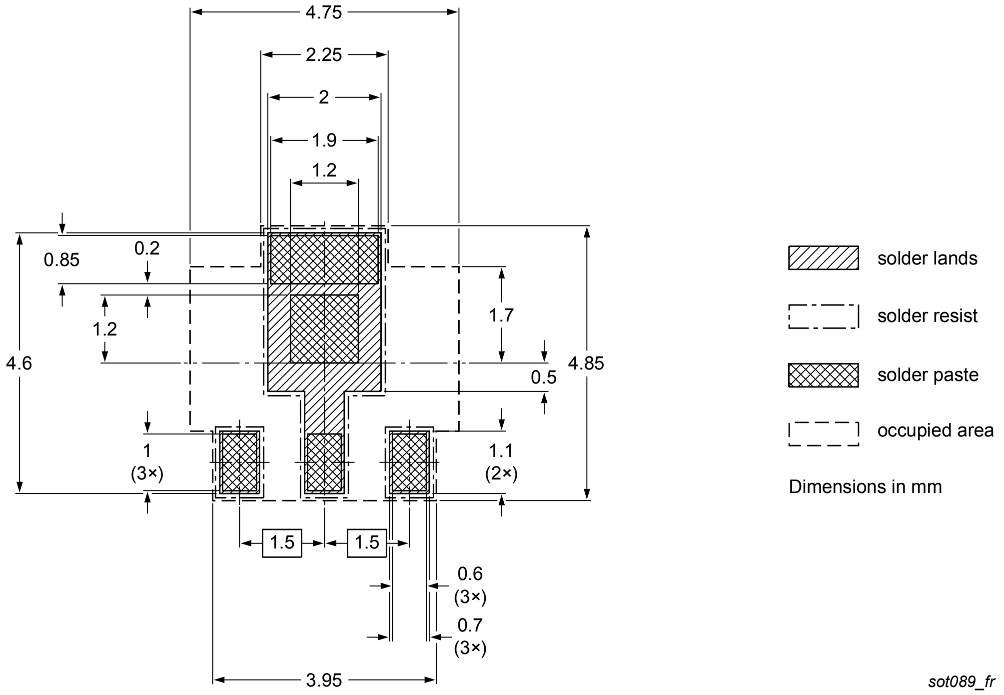


Fig. 19. Reflow soldering footprint for SOT89

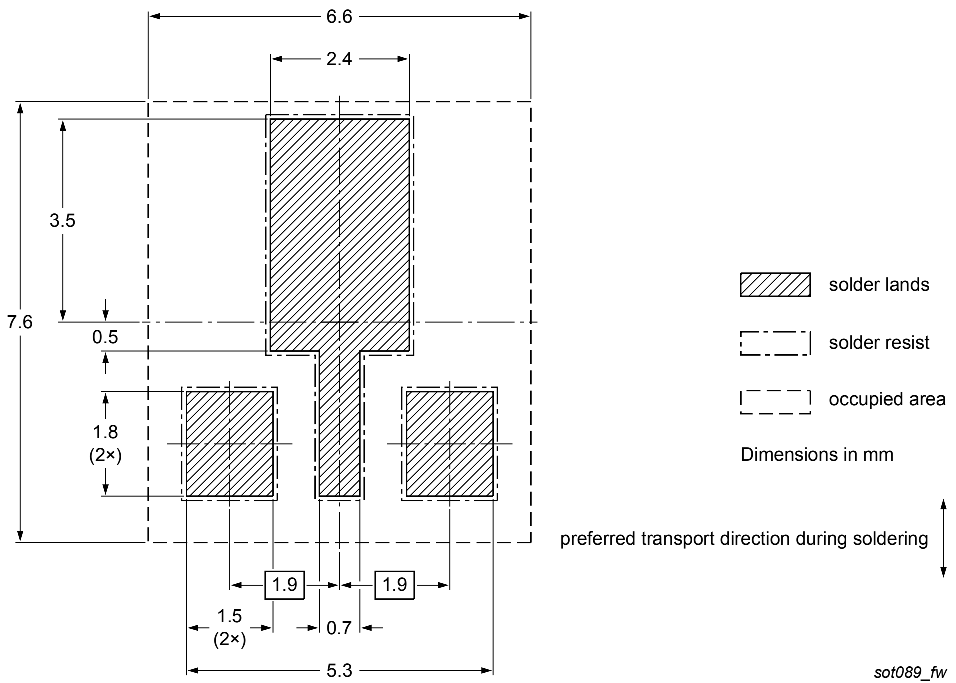


Fig. 20. Wave soldering footprint for SOT89

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BSS192 v.4	20141212	Product data sheet	-	BSS192 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors • Legal texts have been adapted to the new company name where appropriate			
BSS192 v.3	20021120		-	BSS192 v.2
BSS192 v.2	20020522		-	BSS192 v.1
BSS192 v.1	19970620			-

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15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 12 December 2014