

TPS659118 User's Guide for 66AK2G02 Processor

This user's guide is a reference for integrating the TPS659118 power-management integrated circuit (PMIC) into a system using the 66AK2G02 processor from Texas Instruments.

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1 Introduction

This user's guide is a reference for connectivity between the TPS659118 PMIC and the 66AK2G02 processor from Texas Instruments.

The TPS659118 EEPROM bit configuration and power-up sequence is also described. This user's guide does not provide details about the power resources or the functionality of the device. For such information, refer to the full specification document, [TPS65911x Integrated Power Management Unit Top Specification](#).

2 Platform Connection

Figure 1 shows a high-level view of an example system-power solution proposal using the TPS659118 device for the processor.

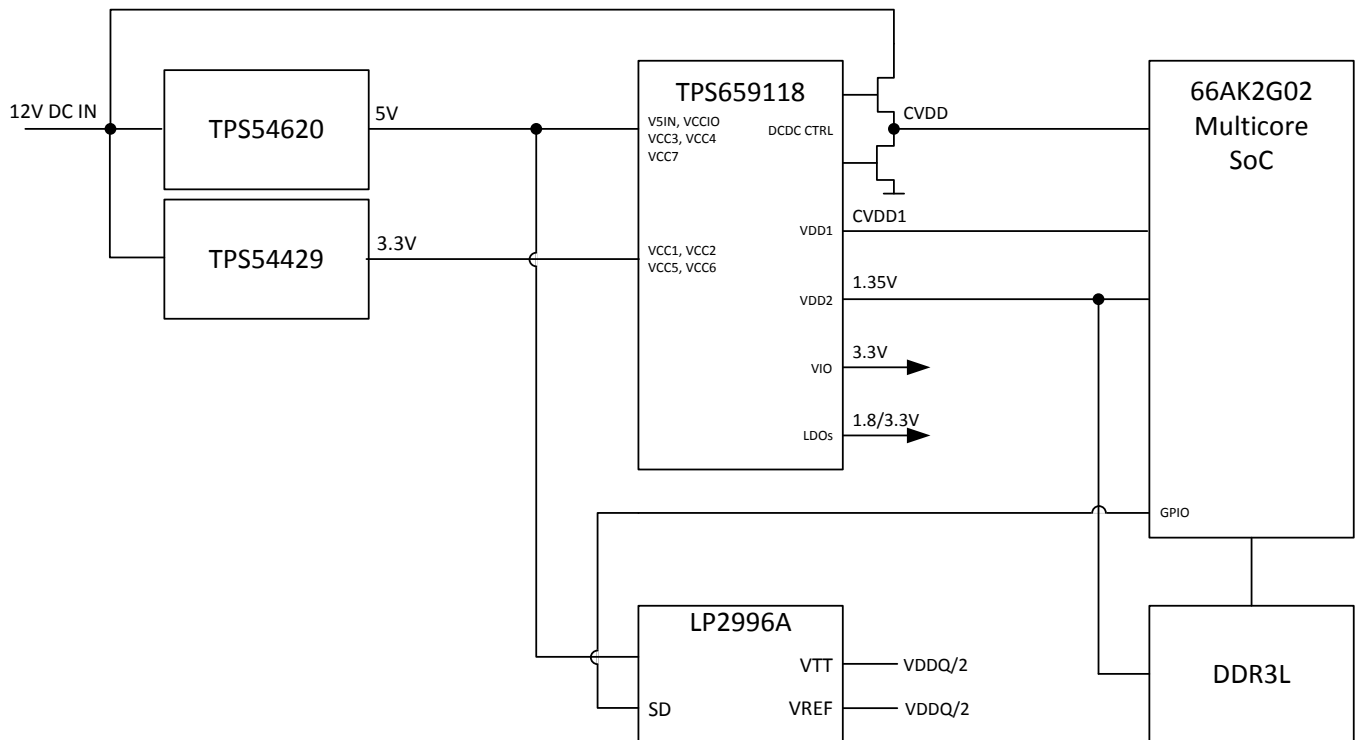
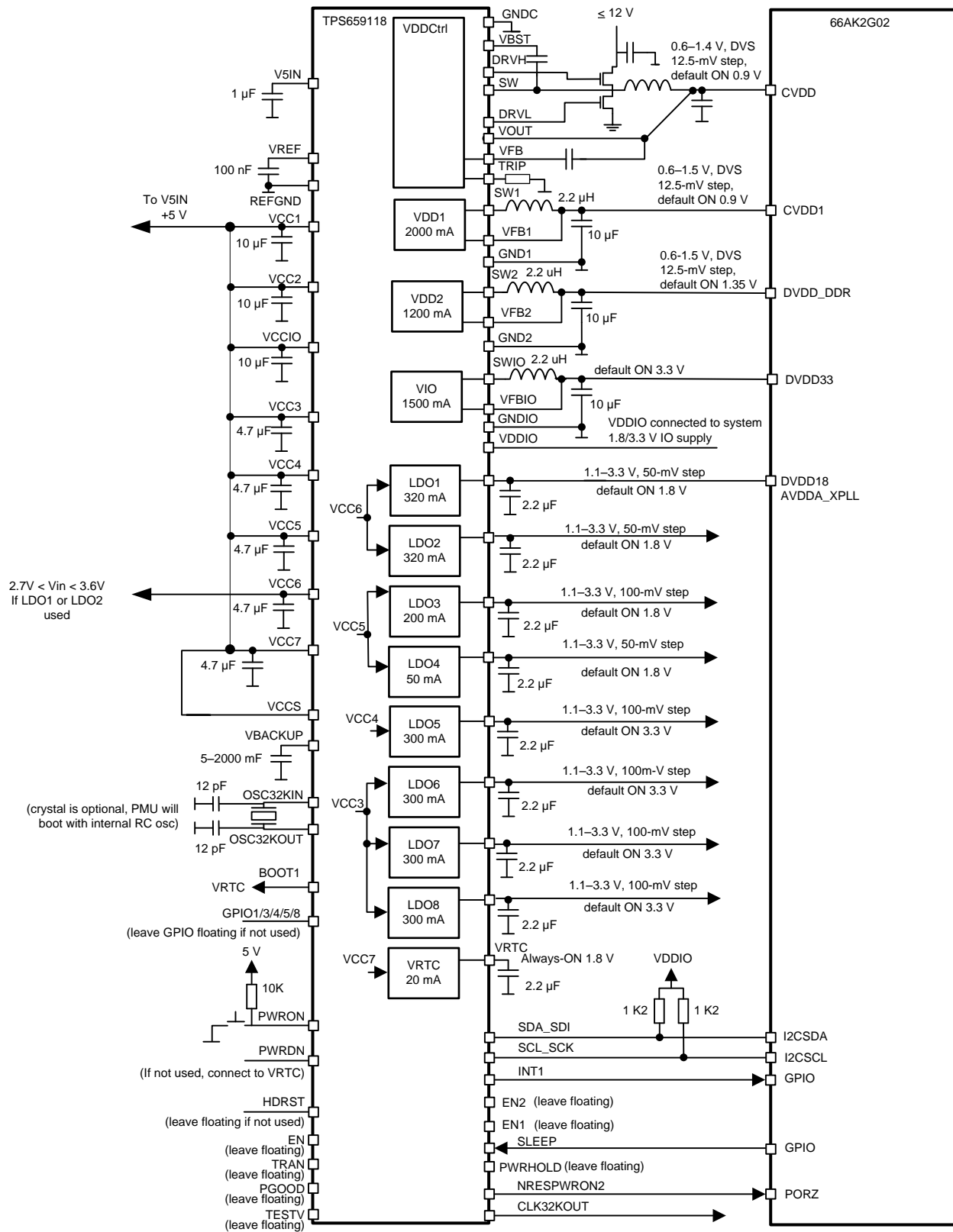


Figure 1. Example Power Solution With TPS659118

Figure 2 shows the detailed connections between the processor and the TPS659118 device.



SWCU181-001

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Figure 2. Processor Connection With TPS659118

Notes for the connection diagram and operation defined by the EEPROM:

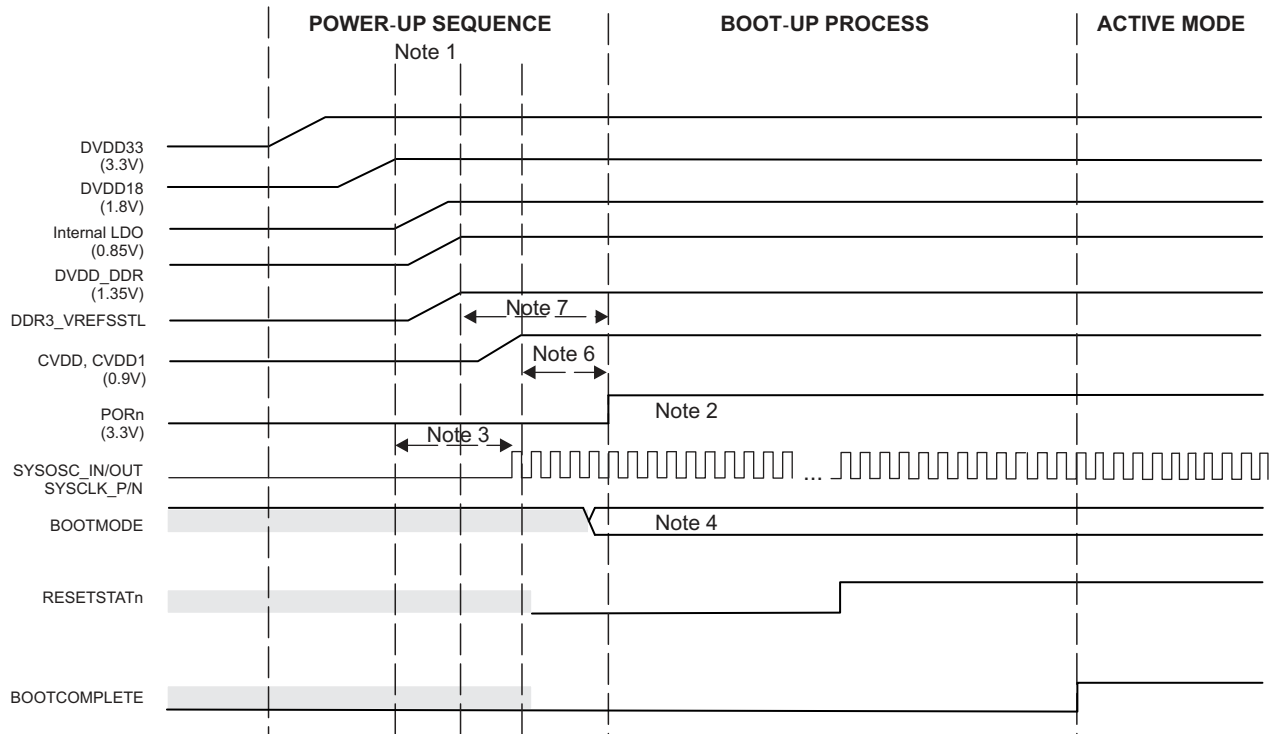
- The TPS659118 transitions from NO SUPPLY to OFF to ACTIVE states when a supply is inserted into VCC7 (VMBHI_IT_MSK = 0 in EEPROM).
- The VMBCH threshold of the TPS659118 is programmed as 3.1 V so VCCS must be greater than 3.1 V for an OFF-to-ACTIVE transition.
- The voltage level of the main control signals (I2C, INT2, NRESPWRON, EN1, and EN2) is defined by the VDDIO connection.
- The PWRHOLD pin is programmed as a GPI; therefore, the DEV_ON control bit is set to 1 after a power-on event, and the PWRHOLD signal is not required to keep the PMIC active.
- To keep the PMIC in OFF mode, clear the DEV_ON bit before sending shutdown instructions; otherwise, the PMIC turns back on.
- The internal RC oscillator is used for boot. After boot, software can switch to using a crystal oscillator if it has been connected.
- If backup battery is not used, VBACKUP should be connected to VCC7.
- GPIO0 is a push-pull output at the VCC7 level.
- GPIO2, GPIO6, and GPIO7 are open drain-outputs and require an external pullup. These GPIOs can actively pull down after 4 ms from the time the VCC7 supply is valid.

3 Power-Up Sequencing

3.1 Power-Up Sequence for Processor

The typical power-up sequence for the 66AK2G02 is:

3.3 V → 1.8 V → Memory (1.35 V) → Core (0.9 V)



- (1) Power up begins by powering up DVDD33 first.
- (2) PORn is asserted until all supplies are within operating range.
- (3) Oscillator power-up time (approximately 1 to 2 ms).
- (4) BOOTMODE pins are latched at rising edge of PORn (synchronously using SYSOSC_IN / OUT or SYSCLK_P / N).
- (5) RESETSTATn and BOOTCOMPLETE are outputs for informational purposes.
- (6) Oscillator stabilization time (approximately 2 ms).
- (7) If externally sourced, must be present prior to POR.

Figure 3. Power-Up Sequence for 66AK2G02 Processor

3.2 TPS659118 EEPROM Power-Up Sequence

When the BOOT pin is set high, the TPS659118 powers up with the sequence required by the processor, see [Table 1](#). The correct power-up sequence is configured in the EEPROM (factory programmable only).

Apart from the main power rails required for the processor, several LDO rails are also powered up at initial power up to support system peripherals.

[Table 1](#) lists the power-up sequence for the TPS659118 device.

Table 1. EEPROM Power-Up Sequence of TPS659118

TPS659118 Power Rail	TPS659118 Sequence Number
Supply insertion to VCC7, VCCS ⁽¹⁾	–
VIO, LDO5, LDO6, LDO7, LDO8, GPIO2	2
	3
LDO1, LDO2, LDO3, LDO4, GPIO7	4
VDD2, GPIO0	5
VDDCTRL, GPIO6	6
VDD1, CLK32KOUT	7
	8
	9
NRESPWRON	10
	11
	12
	14

⁽¹⁾ Supply insertion is the start-on event.

[Figure 4](#) shows the power-up sequence timing.

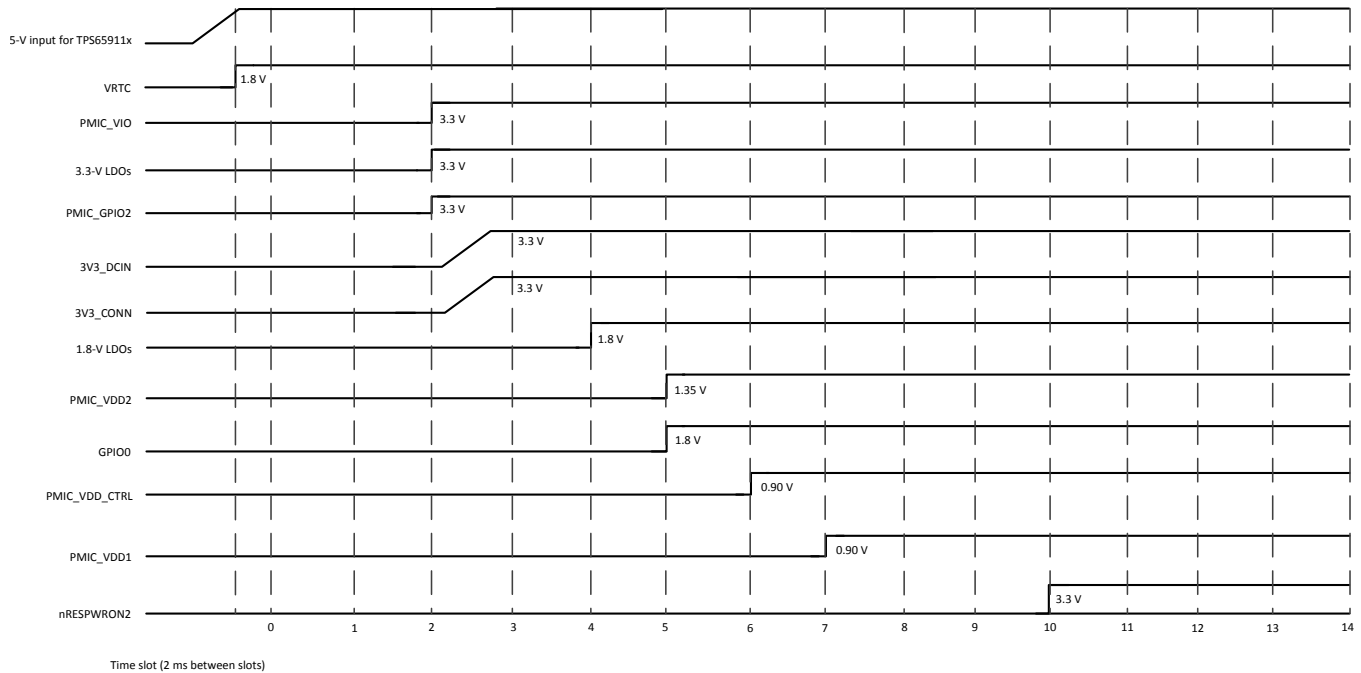


Figure 4. Power Sequencing

Table 2 lists the EEPROM values for the TPS659118 device.

Table 2. EEPROM Configuration for TPS659118

Register	Bit	Description	Option Selected
VDD1_OP_REG/ VDD1_SR_REG	SEL	VDD1 voltage level selection for boot	0.9 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection, ×1 or ×2	×1
EEPROM		VDD1 time slot selection	7
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Enable Skip
VDD2_OP_REG/ VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.35 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection, ×1 or ×3	×1
EEPROM		VDD2 time slot selection	5
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Enable Skip
VIO_REG	SEL[3:9]	VIO voltage selection	3.3 V
EEPROM		VIO time slot selection	2
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Enable Skip
VDDCtrl_OP_REG/ VDDCtrl_SR_REG	SEL	VDDCtrl voltage level selection for boot	0.9 V
EEPROM		VDDCtrl time slot	6
LDO1_REG	SEL[7:2]	LDO1 voltage selection	1.8 V
EEPROM		LDO1 time slot	4
LDO2_REG	SEL[7:2]	LDO2 voltage selection	1.8 V
EEPROM		LDO2 time slot	4
LDO3_REG	SEL[6:2]	LDO3 voltage selection	1.8 V
EEPROM		LDO3 time slot	4
LDO4_REG	SEL[7:2]	LDO4 voltage selection	1.8 V
EEPROM		LDO4 time slot	4
LDO5_REG	SEL[6:2]	LDO5 voltage selection	3.3 V
EEPROM		LDO5 time slot	2
LDO6_REG	SEL[6:2]	LDO6 voltage selection	3.3 V
EEPROM		LDO6 time slot	2
LDO7_REG	SEL[6:2]	LDO7 voltage selection	3.3 V
EEPROM		LDO7 time slot	2
LDO8_REG	SEL[6:2]	LDO8 voltage selection	3.3 V
EEPROM		LDO8 time slot	2
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON, NRESPWRON2 pin		NRESPWRON time slot	10
GPIO0 pin		GPIO0 time slot	5
GPIO2 pin		GPIO2 time slot	2
GPIO6 pin		GPIO6 time slot	6
GPIO7 pin		GPIO7 time slot	4
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during OFF state. 1 = VRC LDO will be in full-power mode during OFF state.	0
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal or external clock. 1 = Clock source is internal RC oscillator.	1
DEVCTRL_REG	DEV_ON	0 = No impact 1 = Will maintain device on, in ACTIVE or SLEEP state	1

Table 2. EEPROM Configuration for TPS659118 (continued)

Register	Bit	Description	Option Selected
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	PWON_LP_OFF	0 = Turnoff after PWRON long press not allowed. 1 = Turnoff after PWRON long press.	1
DEVCTRL2_REG	PWON_LP_RST	0 = No impact 1 = Reset digital core when device is OFF.	0
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	0
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up is reason required before switch-on.	0
INT_MSK3_REG	GPIO5_F_IT_MSK	0 = GPIO5 falling edge detection interrupt not masked. 1 = GPIO5 falling edge detection interrupt masked.	1
INT_MSK3_REG	GPIO5_R_IT_MSK	0 = GPIO5 rising edge detection interrupt not masked. 1 = GPIO5 rising edge detection interrupt masked.	1
INT_MSK3_REG	GPIO4_F_IT_MSK	0 = GPIO4 falling edge detection interrupt not masked. 1 = GPIO4 falling edge detection interrupt masked.	1
INT_MSK3_REG	GPIO4_R_IT_MSK	0 = GPIO4 rising edge detection interrupt not masked. 1 = GPIO4 rising edge detection interrupt masked.	1
GPIO0_REG	GPIO_ODEN	0 = GPIO0 configured as push-pull output. 1 = GPIO0 configured as open-drain output.	0
WATCHDOG_REG	WATCHDOG_EN	0 = Watchdog disabled 1 = Watchdog enabled, periodic operation with 100 s	0
VMBCH_REG	VMBBUF_BYPASS	0 = Enable input buffer for external resistive divider. 1 = In single-cell system, disable buffer for lower power consumption.	1
VMBCH_REG	VMBCH_SEL[5:1]	Select threshold for boot gating comparator COMP1, 2.5–3.5 V.	3.1 V
EEPROM	AUTODEV_ON	0 = PWRHOLD pin is used as PWRHOLD feature. 1 = PWRHOLD pin is GPI. After power-on, DEV_ON is set high internally, no processor action required to maintain supplies.	1
EEPROM	PWRDN_POL	0 = PWRDN signal is active low. 1 = PWRDN signal is active high.	1

4 Getting Started With the TPS659118 Device

4.1 First Initialization

4.1.1 Power-Down Sequence Configuration

To meet processor power-down sequence requirements, select the reverse sequence by setting the PWR_OFF_SEQ bit to 1 in the DEVCTRL_REG register.

4.1.2 I/O Polarity/Muxing Configuration

Voltage scaling for VDD1, VDD2, and VDDCtrl can be done through the main I²C interface. EN1/EN2 interface is not supported by the 66AK2G02 Processor.

SLEEP mode is not supported by 66AK2G02 Processor.

Update the GPIOx configuration (GPIOx_REG) based on application requirements.

4.1.3 Define Wake Up/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG, INT_MSK2_REG, and INT_MSK3_REG registers to enable an interrupt to the processor on the INT1 line.

4.1.4 Backup Battery Configuration

If the system has a backup battery, set the BBCHEN bit to 1 in the BBCH_REG register to enable backup battery charging. The maximum voltage can be set based on backup battery specifications by using the BBSEL bits in the BBCH_REG register.

4.1.5 DC-DC Maximum Current Capability

In VIO_REG, VDD1_REG, and VDD2_REG registers, set ILMAX according to required maximum current.

4.1.6 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used. By default in sleep mode, all resources maintain their output voltage and load capability but response to transients (load change) is reduced.

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG and SLEEP_KEEP_RES_ON_REG registers.

Resources that can be set off in the SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG and SLEEP_SET_RES_OFF_REG registers.

4.2 Event Management Through Interrupts

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that a supply has been connected (PMIC leaving the BACKUP or NO SUPPLY state) and the system must be initialized (see [Section 4.1, First Initialization](#)).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in the OFF or SLEEP state, then this acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 4 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged in the next 1 second, the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of the die is reaching the limit. The software must take action to decrease the power consumption before automatic shutdown.

4.2.5 INT_STS_REG.PWRHOLD_R/F_IT

INT_STS_REG.PWRHOLD_R/F_IT indicates a GPI interrupt event.

4.2.6 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

4.2.7 INT_STS2(3)_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT indicates a GPIO interrupt event. It can be used to wake up the device from the SLEEP state. This can be an interrupt coming from any peripheral device or alike.

4.2.8 INT_STS_REG3.PWRDN_IT

INT_STS_REG.PWRDN_IT is triggered when PWRDN reset is detected.

4.2.9 INT_STS_REG3.VMBCH2_H/L_IT

INT_STS_REG.VMBCH2_H/L_IT is triggered when comparator2 input (VCCS) is above or below the threshold.

4.2.10 INT_STS_REG3.WATCHDG_IT

INT_STS_REG.WATCHDOG_IT is triggered from the watchdog (periodic or interrupt mode).

Revision History

Version	Literature Number	Date	Notes
*	SWCU176	May 2016	Initial release

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