



Features

- 128K x 36 or 256K x 18 Organizations
- CMOS Technology
- Synchronous Flow-Thru Mode Of Operation with Self-Timed Late Write
- Dual Differential Input and Output Clocks
- +3.3V Power Supply, V_{DDQ} , V_{REF} & Ground
- HSTL Input and Output levels
- Registered Addresses, Write Enables, Sync Select and Data Ins
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 X 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers

Description

The IBM041840QLAA and IBM043640QLAA 4Mb SRAMs are Synchronous Flow-Thru Mode, high performance CMOS Static Random Access Memories that are versatile, wide I/O, and achieve 4.5 nsec cycle times. Dual differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K Clock, all Addresses, Write-Enables, Sync Select

and Data Ins are registered internally. Differential clocks C and \bar{C} are used to control the Output Data hold time by allowing output data to change after the rising edge of the C clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with HSTL I/O interfaces.

X36 BGA Bump Layout (Top View)

	1	2	3	4	5	6	7
A	V _{DDQ}	SA5	SA7	NC	SA16	SA14	V _{DDQ}
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V _{DD}	SA10	SA15	NC
D	DQc18	DQc19	V _{SS}	ZQ	V _{SS}	DQb10	DQb9
E	DQc20	DQc21	V _{SS}	\overline{SS}	V _{SS}	DQb12	DQb11
F	V _{DDQ}	DQc22	V _{SS}	\overline{G}	V _{SS}	DQb13	V _{DDQ}
G	DQc23	DQc24	\overline{SBWc}	\overline{C}	\overline{SBWb}	DQb15	DQb14
H	DQc25	DQc26	V _{SS}	C	V _{SS}	DQb17	DQb16
J	V _{DDQ}	V _{DD}	V _{REF}	V _{DD}	V _{REF}	V _{DD}	V _{DDQ}
K	DQd34	DQd35	V _{SS}	K	V _{SS}	DQa8	DQa7
L	DQd32	DQd33	\overline{SBWd}	\overline{K}	\overline{SBWa}	DQa6	DQa5
M	V _{DDQ}	DQd31	V _{SS}	\overline{SW}	V _{SS}	DQa4	V _{DDQ}
N	DQd29	DQd30	V _{SS}	SA0	V _{SS}	DQa3	DQa2
P	DQd27	DQd28	V _{SS}	SA1	V _{SS}	DQa1	DQa0
R	NC	SA4	M1*	V _{DD}	M2*	SA12	NC
T	NC	NC	SA3	SA2	SA13	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD} and V_{DD}, respectively.

X18 BGA Bump Layout (Top View)

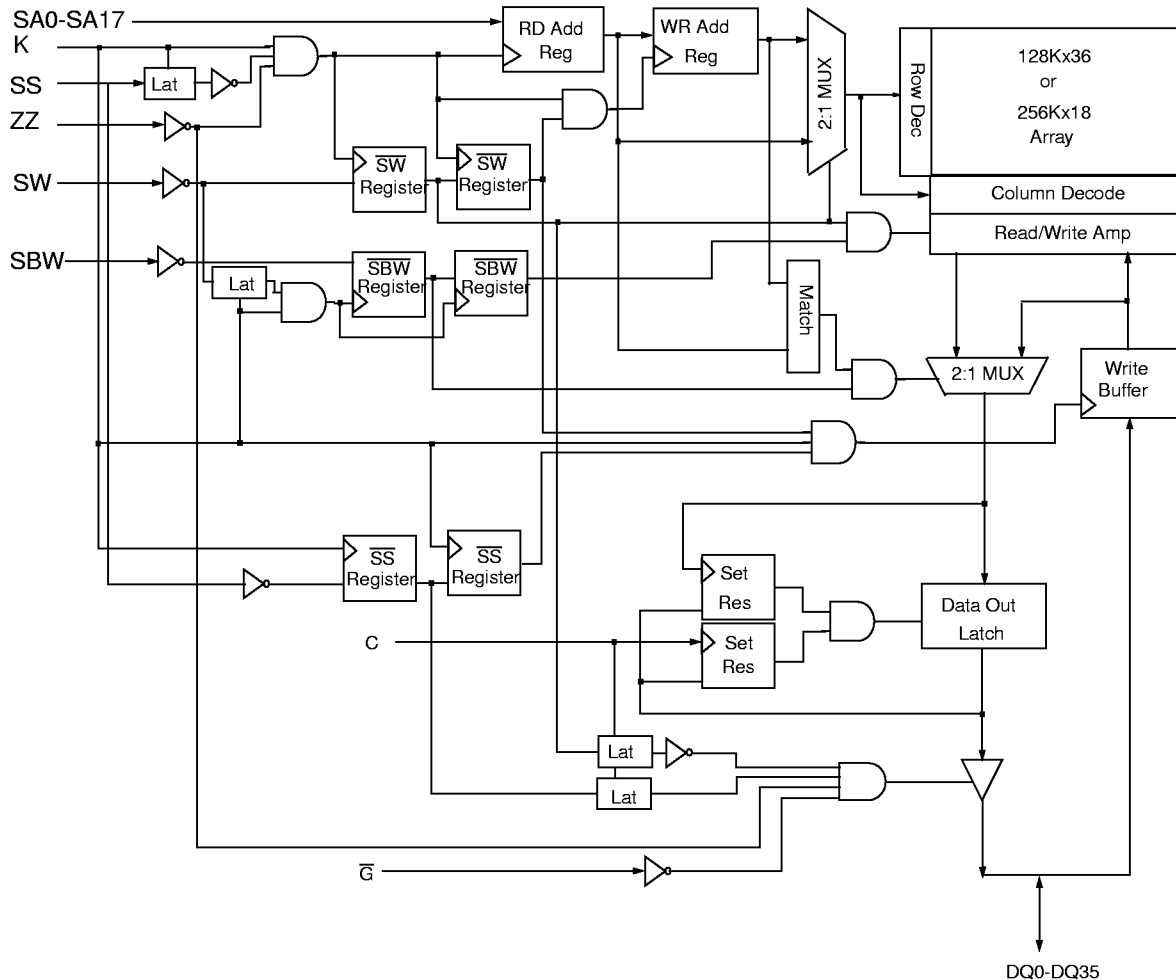
	1	2	3	4	5	6	7
A	V _{DDQ}	SA5	SA7	NC	SA16	SA14	V _{DDQ}
B	NC	NC	SA8	NC	SA11	NC	NC
C	NC	SA6	SA9	V _{DD}	SA10	SA15	NC
D	DQb9	NC	V _{SS}	ZQ	V _{SS}	DQa1	NC
E	NC	DQb12	V _{SS}	\overline{SS}	V _{SS}	NC	DQa2
F	V _{DDQ}	NC	V _{SS}	\overline{G}	V _{SS}	DQa4	V _{DDQ}
G	NC	DQb15	\overline{SBWb}	\overline{C}	V _{SS}	NC	DQa5
H	DQb16	NC	V _{SS}	C	V _{SS}	DQa8	NC
J	V _{DDQ}	V _{DD}	V _{REF}	V _{DD}	V _{REF}	V _{DD}	V _{DDQ}
K	NC	DQb17	V _{SS}	K	V _{SS}	NC	DQa7
L	DQb14	NC	V _{SS}	\overline{K}	\overline{SBWa}	DQa6	NC
M	V _{DDQ}	DQb13	V _{SS}	\overline{SW}	V _{SS}	NC	V _{DDQ}
N	DQb11	NC	V _{SS}	SA0	V _{SS}	DQa3	NC
P	NC	DQb10	V _{SS}	SA1	V _{SS}	NC	DQa0
R	NC	SA4	M1	V _{DD}	M2	SA13	NC
T	NC	SA2	SA3	NC	SA17	SA12	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD} and V_{DD} respectively.

Pin Description

SA0-SA15	Address Input	\bar{G}	Asynchronous Output Enable
DQ0-DQ35	Data I/O	\bar{SS}	Synchronous Select
K, \bar{K}	Differential Input Register Clocks	M1, M2	Clock Mode Inputs - Selects Single or Dual Clock Operation.
C, \bar{C}	Differential Output Data Hold Control Clocks	$V_{REF(2)}$	GTL/HSTL Input Reference Voltage
\bar{SW}	Write Enable, Global	V_{DD}	Power Supply (+3.3V)
\bar{SBW}_a	Write Enable, Byte a (DQ0-DQ8)	V_{SS}	Ground
\bar{SBW}_b	Write Enable, Byte b (DQ9-DQ17)	V_{DDQ}	Output Power Supply
\bar{SBW}_c	Write Enable, Byte c (DQ18-DQ26)	ZZ	Asynchronous Sleep Mode
\bar{SBW}_d	Write Enable, Byte d (DQ27-DQ35)	ZQ	Output Driver Impedance Control
TMS,TDI,TCK	IEEE 1149.1 Test Inputs (LVTTTL levels)	NC	No Connect
TDO	IEEE 1149.1 Test Output (LVTTTL level)		

Block Diagram



SRAM FEATURES

Late Write

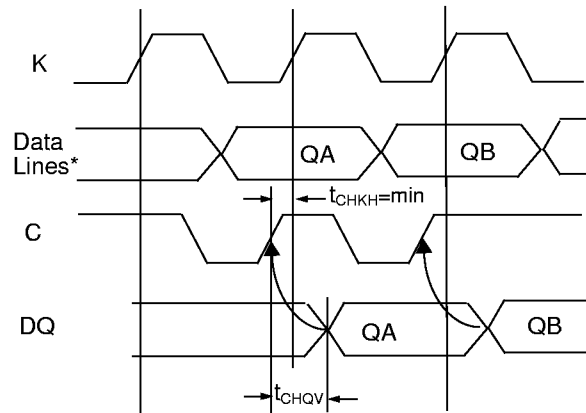
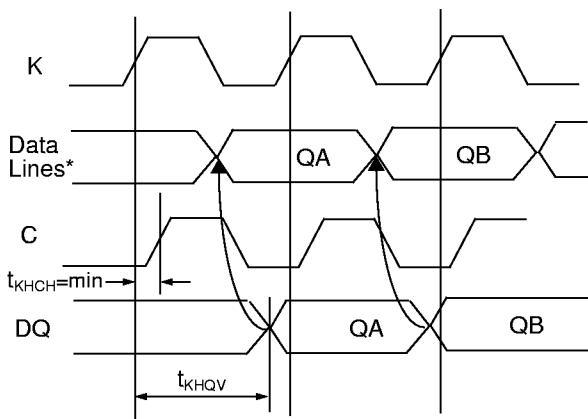
Late Write function allows for write data to be registered one cycle after addresses and controls. This feature will alleviate SRAM data bus contention going from a Read to Write cycle by eliminating one dead cycle. Late Write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. In the case a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with address and data in the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array occurs on a byte by byte basis. When one byte is written during a write cycle, read data from the last written address will have new byte data from the write buffer and remaining bytes from the SRAM array.

Dual Clock Operation

In Dual Clock Operation, the K Clocks are used to register all synchronous inputs and start the SRAM operation. The C Clocks are used to control the output data timings. During Write ($\overline{SW}=L$) or Deselect ($\overline{SS}=H$) operations, the rising edge of C Clock triggers the time to High-Z. During Read operations the location of the rising edge of the C Clock will determine the output data valid placement by allowing SRAM output data to flow through after the rising edge. When the rising edge of the C Clock occurs early in a Read cycle (e.g. $t_{KHCH} = \text{Min.}$), data from the SRAM will become available at a t_{KHQV} time, as it would in a Flow-Through Read implementation (see Dual Clock Diagram #1 below). As the C Clock rising edge moves away from $t_{KHCH} = \text{Min.}$, towards a $t_{CHKH} = \text{Min.}$, of the next K Clock rising edge, the output data may become "gated" by the C Clock (see Dual Clock Diagram #2 below). The SRAM access time will then become referenced to the C Clock (i.e. t_{CHQV}). This feature allows SRAM users to fully control the output data hold time over voltage, temperature and process variations, and provide minimum output data latency.

Dual Clock Diagram #1: Output data becomes available as a result of internal data lines flowing through the output latch unrestrained by the C clock.

Dual Clock Diagram #2: Internal data lines await at the output latch for the rising edge of C clock. The C clock enables the output latch and allows output data to become available.



*Data Lines refer to internal data lines connecting to Data Output Latch See Block Diagram on page 3.

Mode Control

Mode control pins: M1 and M2 are used to select four different JEDEC standard read protocols. This SRAM supports both the Single Clock, Flow-Through ($M1 = V_{SS}$, $M2 = V_{SS}$) and Dual Clock Flow-Through protocols ($M1 = V_{DD}$, $M2 = V_{DD}$). This data sheet only describes Dual Clock Flow-Through functionality. Mode control



inputs must be set with power up and must not change during SRAM operation.

Power Down Mode

Power Down Mode or “Sleep” Mode is enabled by switching asynchronous signal ZZ High. When the SRAM is in Sleep mode, the outputs will go to a High-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes to normal operation.

Programmable Impedance/Power Up Requirements

An external resistor, R_Q , must be connected between the ZQ pin on the SRAM and V_{SS} to allow for the SRAM to adjust its output driver impedance. The value of R_Q must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of R_Q to guarantee impedance matching with a tolerance of 7.5% is between 175Ω and 350Ω . Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. One evaluation occurs every 64 clock cycles and each evaluation may move the output driver impedance level only one step at a time towards the optimum level. The output driver has 32 discrete binary weighted steps. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, therefore, triggering an update. The user may choose to invoke asynchronous \bar{G} updates by providing a \bar{G} setup and hold about the K Clock to guarantee the proper update. There are no power up requirements for the SRAM; however, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 clock cycles followed by a Low-Z to High-Z transition.

Ordering Information

Part Number	Organization	Speed	Leads
IBM041840QLAA-4	256K x 18	6.5ns Access / 4.5 ns Cycle	7 X 17 BGA
IBM041840QLAA-5	256K x 18	7.0ns Access / 5ns Cycle	7 X 17 BGA
IBM041840QLAA-6	256K x 18	7.5ns Access / 6ns Cycle	7 X 17 BGA
IBM043640QLAA-4	128K x 36	6.5ns Access / 4.5 ns Cycle	7 X 17 BGA
IBM043640QLAA-5	128K x 36	7.0ns Access / 5ns Cycle	7 X 17 BGA
IBM043640QLAA-6	128K x 36	7.5ns Access / 6ns Cycle	7 X 17 BGA

Output Enable Truth Table

Operation	\bar{G}	DQ
Read	L	$D_{OUT} 0-35$
Read	H	High-Z
Sleep (ZZ=H)	X	High-Z
Write ($\bar{SW}=L$)	X	High-Z
Deselect ($\bar{SS}=H$)	X	High-Z



Clock Truth Table

K, C CLK	ZZ	\overline{SS}	\overline{SW}	\overline{SBWA}	\overline{SBWB}	\overline{SBWC}	\overline{SBWD}	DQ (n)	DQ (n+1)	Mode
L→H	L	L	H	X	X	X	X	D _{OUT} 0-35	X	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	High-Z	D _{IN} 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	High-Z	D _{IN} 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	High-Z	D _{IN} 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	High-Z	D _{IN} 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	High-Z	D _{IN} 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	High-Z	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	High-Z	X	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V _{DD}	-0.5 to 3.9	V	1
Input Voltage	V _{IN}	-0.5 to V _{DD} +0.5	V	1
Output Voltage	V _{OUT}	-0.5 to V _{DD} +0.5	V	1
Operating Temperature	T _J	0 to +110	°C	1
Storage Temperature	T _{STG}	-55 to +125	°C	1
Short Circuit Output Current	I _{OUT}	25	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



Preliminary

PBGA Thermal Characteristics

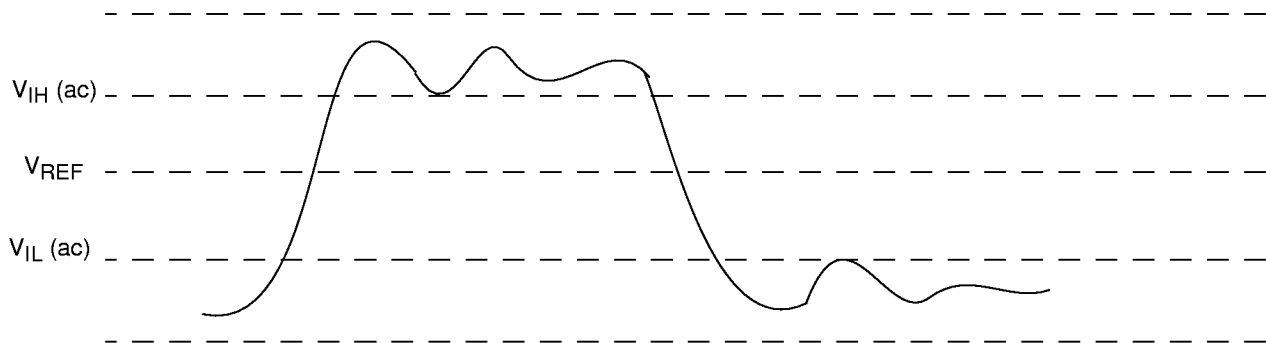
Item	Symbol	Rating	Units
Thermal Resistance Junction to Case	R _{QJC}	1	°C/W

AC Input Characteristics

Item	Symbol	Min	Max	Notes
AC Input Logic High	V _{IH} (ac)	TBD		3
AC Input Logic Low	V _{IL} (ac)		TBD	3
Clock Input Differential Voltage	V _{DIF} (ac)	TBD		2
V _{REF} Peak to Peak ac Voltage	V _{REF} (ac)		5% V _{REF} (dc)	1

1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. Performance is a function on V_{IH} and V_{IL} levels to clock inputs.
3. See AC Input Definition figure on page 7.

AC Input Definition



Recommended DC Operating Conditions ($T_J=0$ to 110°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.15	3.3	3.47	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.5	1.6	V	1
Input High Voltage	V_{IH}	$V_{REF} + 0.1$	—	$V_{DDQ} + 0.3$	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	$V_{REF} - 0.1$	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	0.90	V	1
Clocks Signal Voltage	V_{IN-CLK}	-0.3	—	$V_{DDQ} + 0.3$	V	1, 4
Differential Clocks Signal Voltage	$V_{DIF-CLK}$	0.1	—	$V_{DDQ} + 0.6$	V	1, 5
Clocks Common Mode Voltage	V_{CM-CLK}	0.55	—	0.90	V	1
Output Current	I_{OUT}	—	5	8	mA	

1. All voltages referenced to V_{SS} . All V_{DD} , V_{DDQ} and V_{SS} pins must be connected.
 2. $V_{IH}(\text{Max})\text{DC} = V_{DDQ} + 0.3$ V, $V_{IH}(\text{Max})\text{AC} = V_{DD} + 1.5$ V (pulse width $\leq 4.0\text{ns}$).
 3. $V_{IL}(\text{Min})\text{DC} = -0.3$ V, $V_{IL}(\text{Min})\text{AC} = -1.5$ V (pulse width $\leq 4.0\text{ns}$).
 4. V_{IN-CLK} specifies the maximum allowable DC excursions of each differential clock (K, \bar{K} , C, \bar{C}).
 5. $V_{DIF-CLK}$ specifies the minimum Clock differential voltage required for switching.

Capacitance ($T_J=0$ to 110°C , $V_{DD}=3.3 -5\% + 5\%$ V, $f=1\text{MHz}$)

Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	C_{IN}	$V_{IN} = 0\text{V}$	3	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	$V_{OUT} = 0\text{V}$	4	pF



Preliminary

DC Electrical Characteristics ($T_J = 0$ to $+110^\circ\text{C}$, $V_{DD} = 3.3 \pm 5\% \text{ V}$)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current - X36 ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL} , \overline{ZZ} & $\overline{SS} = V_{IL}$)	I_{DD5} I_{DD6}	— —	650 575	mA	1
Average Power Supply Operating Current - X18 ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL} , \overline{ZZ} & $\overline{SS} = V_{IL}$)	I_{DD5} I_{DD6}	— —	600 525	mA	1
Power Supply Standby Current ($\overline{ZZ} = V_{IH}$, All other inputs = V_{IH} or V_{IL} , $I_{OUT} = 0$)	I_{SBZZ}	—	150	mA	1
($\overline{SS} = V_{IH}$, $\overline{ZZ} = V_{IL}$, All other inputs = V_{IH} or V_{IL} , $I_{OUT} = 0$)	I_{SBSS}	—	200	mA	1
Input Leakage Current, any input ($V_{IN} = V_{SS}$ or V_{DD})	I_{LI}	—	+1	μA	
Output Leakage Current ($V_{OUT} = V_{SS}$ or V_{DD} , DQ in High-Z)	I_{LO}	—	+1	μA	
Output "High" Level Voltage ($I_{OH} = -6\text{mA}$ @ $V_{DDQ} / 2 + 0.3$)	V_{OH}	$V_{DDQ} - .4$	V_{DDQ}	V	2
Output "Low" Level Voltage ($I_{OL} = +6\text{mA}$ @ $V_{DDQ} / 2 - 0.3$)	V_{OL}	V_{SS}	$V_{SS} + .4$	V	2

- I_{OUT} = Chip Output Current.
- Minimum Impedance Output Driver.

Programmable Impedance Output Driver DC Electrical Characteristics

($T_J = 0$ to $+110^\circ\text{C}$, $V_{DD} = 3.3 - 5\% + 5\% \text{ V}$)

Parameter	Symbol	Min.	Max.	Units	Notes
Output "High" Level Voltage	V_{OH}	$V_{DDQ} / 2$	V_{DDQ}	V	1
Output "Low" Level Voltage	V_{OL}	V_{SS}	$V_{DDQ} / 2$	V	2

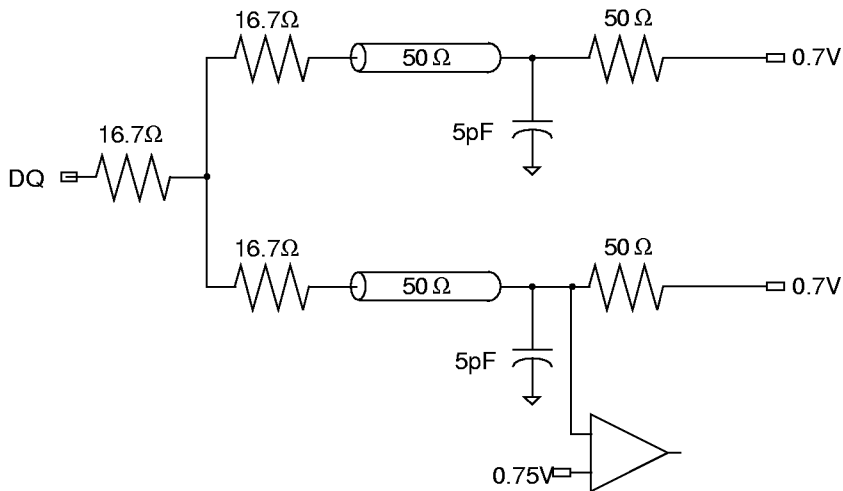
- $I_{OH} = (V_{DDQ} / 2) / (RQ / 5)$ 7.5% @ $V_{OH} = V_{DDQ} / 2$ For: $150\Omega \leq RQ \leq 350\Omega$.
- $I_{OL} = (V_{DDQ} / 2) / (RQ / 5)$ 7.5% @ $V_{OL} = V_{DDQ} / 2$ For: $150\Omega \leq RQ \leq 350\Omega$.

AC Test Conditions ($T_J=0$ to 110°C , $V_{DD}=3.3 - 5\% + 5\% V$, $V_{DDQ}+ 1.5V$)

Parameter	Symbol	Conditions	Units	Notes
Input High Level	V_{IH}	1.25	V	
Input Low Level	V_{IL}	0.25	V	
Input Reference Voltage	V_{REF}	0.75	V	
Differential Clocks Voltage	$V_{DIF-CLK}$	0.75	V	
Clocks Common Mode Voltage	V_{CM-CLK}	0.75	V	
Input Rise Time	T_R	0.5	ns	
Input Fall Time	T_F	0.5	ns	
I/O Signals Reference Level (except K, C Clocks)		0.75	V	
Clocks Reference Level		Differential Cross Point	V	
Output Load Conditions				1

1. See AC Test Loading figure on page 10.

AC Test Loading





Preliminary

AC Characteristics ($T_J=0$ to 110°C , $V_{DD}=3.3 - 5\% + 5\% V$)

Parameter	Symbol	-4		-5		-6		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
K Clock Cycle Time	t_{KHKH}	4.5	—	5.0	—	6.0	—	ns	
K Clock High Pulse Width	t_{KHKL}	1.5	—	1.5	—	1.5	—	ns	
K Clock Low Pulse Width	t_{KLKH}	1.5	—	1.5	—	1.5	—	ns	
C Clock Cycle Time	t_{CHCH}	t_{KHKH}	—	t_{KHKH}	—	t_{KHKH}	—	ns	
C Clock High Pulse Width	t_{CHCL}	1.5	—	1.5	—	1.5	—	ns	
C Clock Low Pulse Width	t_{CLCH}	1.5	—	1.5	—	1.5	—	ns	
K to C Clock Delay	t_{KHCH}	1.5	—	1.5	—	1.5	—	ns	
C to K Clock Delay	t_{CHKH}	0.8	—	1.0	—	1.0	—	ns	
K Clock to Output Valid	t_{KHQV}	—	6.5	—	7.0	—	7.5	ns	1
Data Out Hold Time from K Clock	t_{KHQX}	2.0	—	2.5	—	3.0	—	ns	1, 2, 4
K Clock High to Output Active	t_{KHQX4}	2.5	—	3.0	—	3.5	—	ns	1, 2, 4
C Clock to Output Valid	t_{CHQV}	—	2.5	—	3.0	—	3.0	ns	1, 5
Data Out Hold Time from C clock	t_{CHQX}	0.5	—	0.5	—	0.5	—	ns	1, 2, 5
C Clock High to Output High-Z	t_{CHQZ}	—	2.5	—	3.0	—	3.0	ns	1, 2
C Clock High to Output Active	t_{CHQX2}	0.5	—	0.5	—	0.5	—	ns	1, 2, 5
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	0.5	—	ns	6
Address Hold Time	t_{KHAX}	1.0	—	1.0	—	1.0	—	ns	6
Synchronous Select Setup Time	t_{SVKH}	0.5	—	0.5	—	0.5	—	ns	6
Synchronous Select Hold Time	t_{KHSX}	1.0	—	1.0	—	1.0	—	ns	6
Write Enables Setup Time	t_{WVKH}	0.5	—	0.5	—	0.5	—	ns	6
Write Enables Hold Time	$t_{KH WX}$	1.0	—	1.0	—	1.0	—	ns	6
Data In Setup Time	t_{DVKH}	0.5	—	0.5	—	0.5	—	ns	6
Data In Hold Time	t_{KHDX}	1.0	—	1.0	—	1.0	—	ns	6
Output Enable to Output Valid	t_{GLQV}	—	2.4	—	2.5	—	3.0	ns	1
Output Enable to Low-Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	ns	1, 2
Output Enable to High-Z	t_{GHQZ}	—	2.4	—	2.5	—	3.0	ns	1, 2
Output Enable Set-up Time	t_{GHKH}	0.5	—	0.5	—	0.5	—	ns	1, 3
Output Enable Hold Time	t_{KHGX}	1.5	—	1.5	—	1.5	—	ns	1, 3

1. See AC Test Loading figure on page 10.
2. Transitions are measured $\pm t_{bd}$ mV from steady state voltage.
3. Output Driver Impedance update specifications for \bar{G} induced updates. Write and Deselect cycles will also induce Output Driver updates during High-Z.
4. t_{KHQX} and t_{KHQX4} are used in instances where $t_{KHCH} = \text{Min.}$ and, therefore, the C Clock may not gate the output data.
5. t_{CHQV} , t_{CHQX} and t_{CHQX2} are used in instances where the output data is gated by the C Clock.
6. In use conditions V_{IH} , V_{IL} , T_{rise} , T_{fall} of inputs must be within 20% of V_{IH} , V_{IL} , T_{rise} , T_{fall} of Clocks.

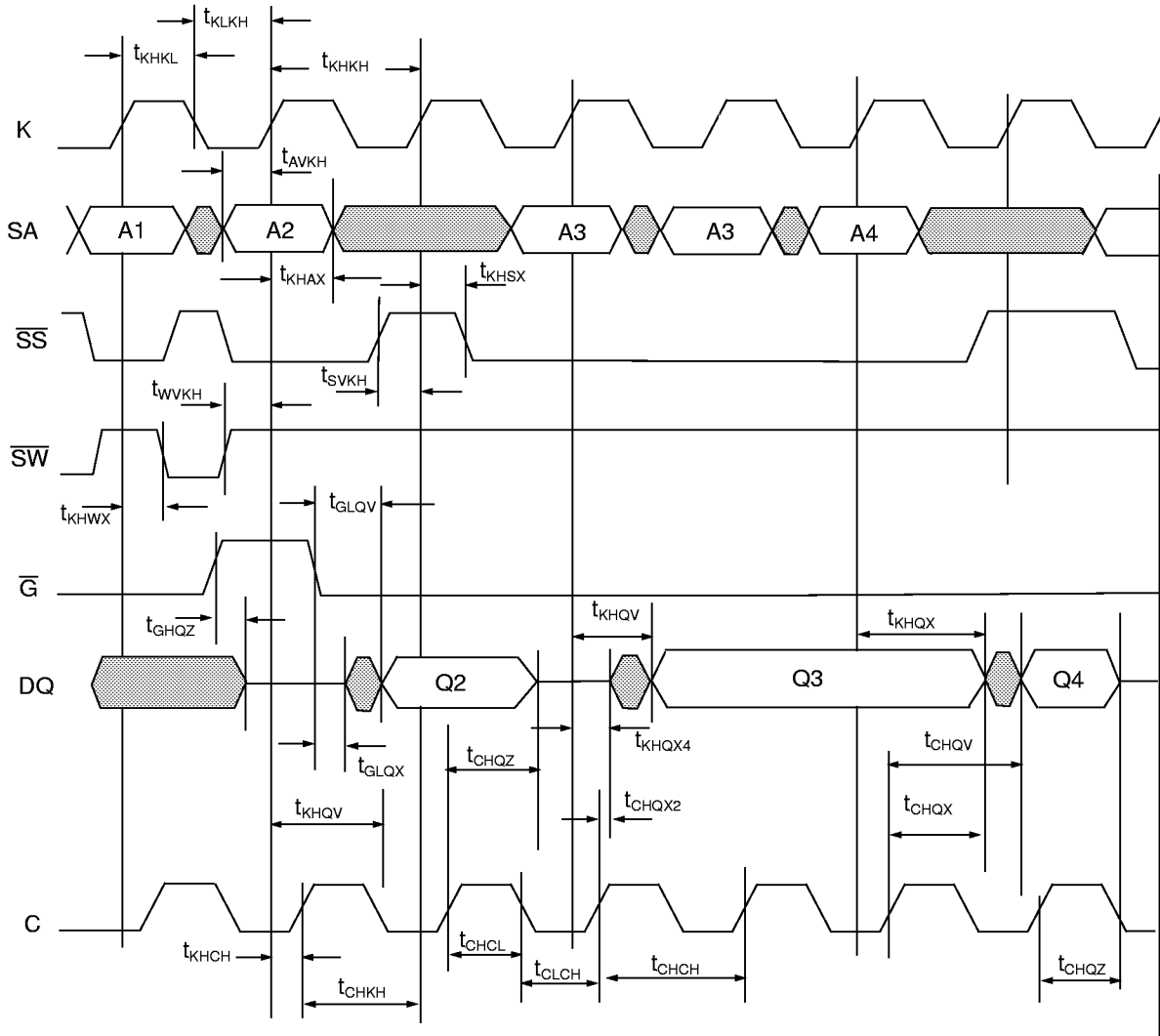


AC Characteristics ($T_J=0$ to 110°C , $V_{DD}=3.3 - 5\% + 5\% V$)

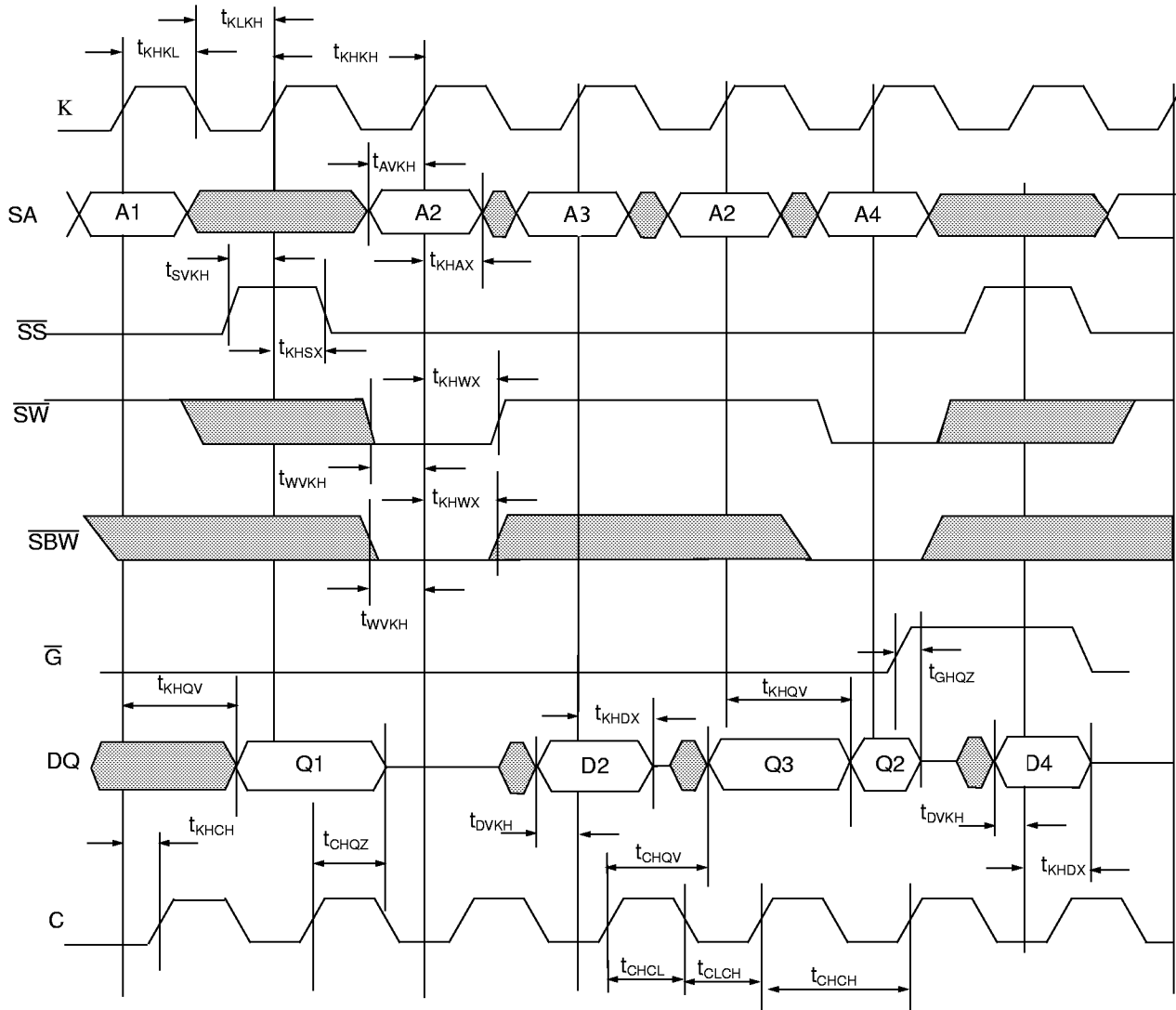
Parameter	Symbol	-4		-5		-6		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Sleep Mode Recovery Time	t_{ZZR}	4.5	—	5	—	6	—	ns	
Sleep Mode Enable Time	t_{ZZE}	—	4.5	—	5	—	6	ns	

1. See AC Test Loading figure on page 10.
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4. t_{KHQX} and t_{KHQX4} are used in instances where $t_{KHCH} = \text{Min.}$ and, therefore, the C Clock may not gate the output data.
5. t_{CHQV} , t_{CHQX} and t_{CHQX2} are used in instances where the output data is gated by the C Clock.
6. In use conditions V_{IH} , V_{IL} , T_{rise} , T_{fall} of inputs must be within 20% of V_{IH} , V_{IL} , T_{rise} , T_{fall} of Clocks.

Timing Diagram (Read and Deselect Cycles)



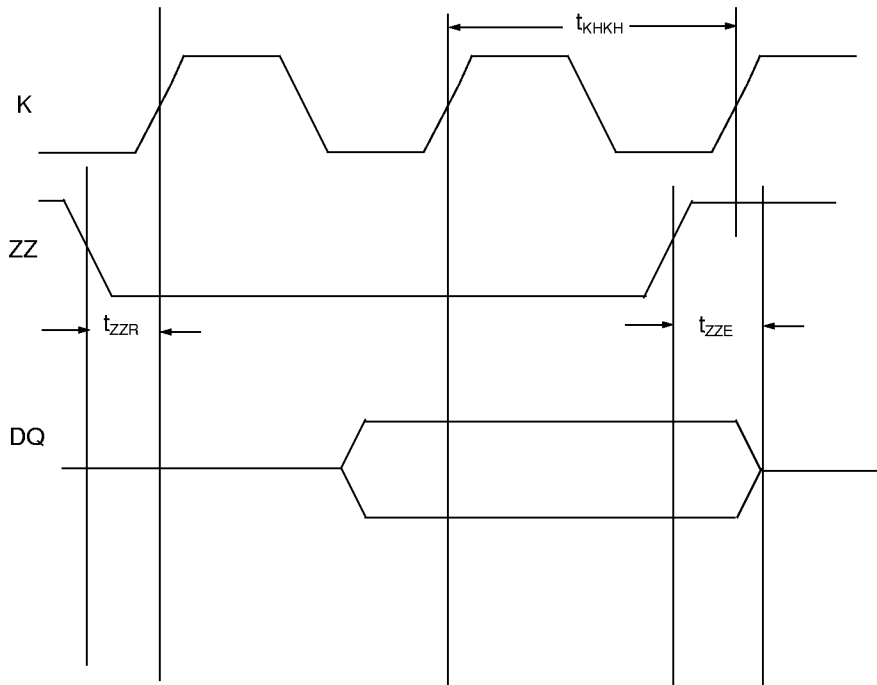
Timing Diagram (Read Followed by Write)



Notes:

1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Timing Diagram (Sleep Mode)



IEEE 1149.1 Tap And Boundary Scan

The SRAM provides a limited set of JTAG functions intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE std. 1149.1, the SRAMs contain a TAP controller, Instruction register, Boundary Scan register, Bypass register and ID register.

The TAP controller has a standard 16-state state machine that resets internally upon power-up, therefore, TRST signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

Caution: TCK, TMS, TDI inputs must be biased down, even if JTAG is not used.

JTAG Recommended DC Operating Conditions (T_J=0 to 110°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V _{IH1}	2.2	—	V _{DD} +0.3	V	1
JTAG Input Low Voltage	V _{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V _{OH1}	2.4	—	—	V	1, 2
JTAG Output Low Level	V _{OL1}	—	—	0.4	V	1, 3

1. All JTAG Inputs/Outputs are LVTTTL Compatible only.
2. I_{OH1} = -8mA at 2.4V.
3. I_{OL1} = +8mA at 0.4V.

JTAG AC Test Conditions (T_J=0 to 110°C, V_{DD}=3.3 -5% + 5% V)

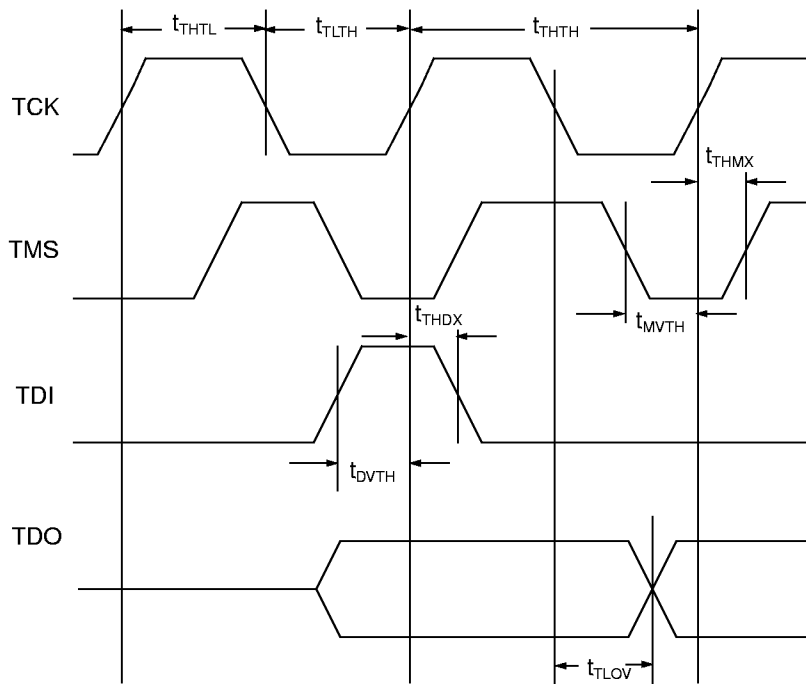
Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V _{IH1}	3.0	V	
Input Pulse Low Level	V _{IL1}	0.0	V	
Input Rise Time	T _{R1}	2.0	ns	
Input Fall Time	T _{F1}	2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

1. See AC Test Loading figure on page 10.

JTAG AC Characteristics ($T_J=0$ to 110°C , $V_{DD}=3.3$ -5% + 5% V)

Parameter	Symbol	Min.	Max.	Units	Notes
TCK Cycle Time	t_{THTH}	20	—	ns	
TCK High Pulse Width	t_{THTL}	7	—	ns	
TCK Low Pulse Width	t_{TLTH}	7	—	ns	
TMS Setup	t_{MVTH}	4	—	ns	
TMS Hold	t_{THMX}	4	—	ns	
TDI Setup	t_{DVTH}	4	—	ns	
TDI Hold	t_{THDX}	4	—	ns	
TCK Low to Valid Data	t_{TLOV}	—	7	ns	1

1. See AC Test Loading figure on page 10.

JTAG Timing Diagram


Scan Register Definition

Register Name	Bit Size X18	Bit Size X36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

- * The Boundary Scan chain consists of the following bits:
- 36 or 18 bits for Data Inputs Depending on X18 or X36 Configuration
 - 15 bits for SA0 - SA14 for X36, 16 bits for SA0 - SA15 for X18
 - 4 bits for SBW_a - SBW_d in X36, 2 bits for SBW_a and SBW_b in X18
 - 11 bits for K, \bar{K} , C, \bar{C} , ZQ, \bar{SS} , \bar{G} , \bar{SW} , ZZ, M1 and M2
 - 4 bits for Place Holders

* K, \bar{K} , C, \bar{C} clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacture JEDEC Code (11:1)	Start Bit (0)
256K X18	0001	011 100 1011	001000	000 101 001 00	1
128K X36	0001	011 010 1100	001000	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1, 5
001	IDCODE	2
010	SAMPLE-Z	1, 5
011	PRIVATE	
100	SAMPLE	4, 5
101	PRIVATE	
110	PRIVATE	
111	BYPASS	3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to VSS when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. SRAM must not be in Sleep mode (ZZ = H) when SAMPLE-Z or SAMPLE instructions are invoked.

List of IEEE 1149.1 standard violations:

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d



Preliminary

Boundary Scan Order (X36)

(PH =Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ13	6F	49	DQ26	2H
2	SA1	4P	26	DQ11	7E	50	DQ25	1H
3	SA2	4T	27	DQ12	6E	51	\overline{SBWc}	3G
4	SA12	6R	28	DQ9	7D	52	ZQ	4D
5	SA13	5T	29	DQ10	6D	53	\overline{SS}	4E
6	ZZ	7T	30	SA14	6A	54	\overline{C}	4G
7	DQ1	6P	31	SA15	6C	55	C	4H
8	DQ0	7P	32	SA10	5C	56	\overline{SW}	4M
9	DQ3	6N	33	SA16	5A	57	\overline{SBWd}	3L
10	DQ2	7N	34	PH*	6B	58	DQ34	1K
11	DQ4	6M	35	SA11	5B	59	DQ35	2K
12	DQ6	6L	36	SA8	3B	60	DQ32	1L
13	DQ5	7L	37	PH*	2B	61	DQ33	2L
14	DQ8	6K	38	SA7	3A	62	DQ31	2M
15	DQ7	7K	39	SA9	3C	63	DQ29	1N
16	\overline{SBWa}	5L	40	SA6	2C	64	DQ30	2N
17	\overline{K}	4L	41	SA5	2A	65	DQ27	1P
18	K	4K	42	DQ19	2D	66	DQ28	2P
19	\overline{G}	4F	43	DQ18	1D	67	SA3	3T
20	\overline{SBWb}	5G	44	DQ21	2E	68	SA4	2R
21	DQ16	7H	45	DQ20	1E	69	SA0	4N
22	DQ17	6H	46	DQ22	2F	70	M1	3R
23	DQ14	7G	47	DQ24	2G			
24	DQ15	6G	48	DQ23	1G			

1. * Input of PH register connected to V_{SS} .



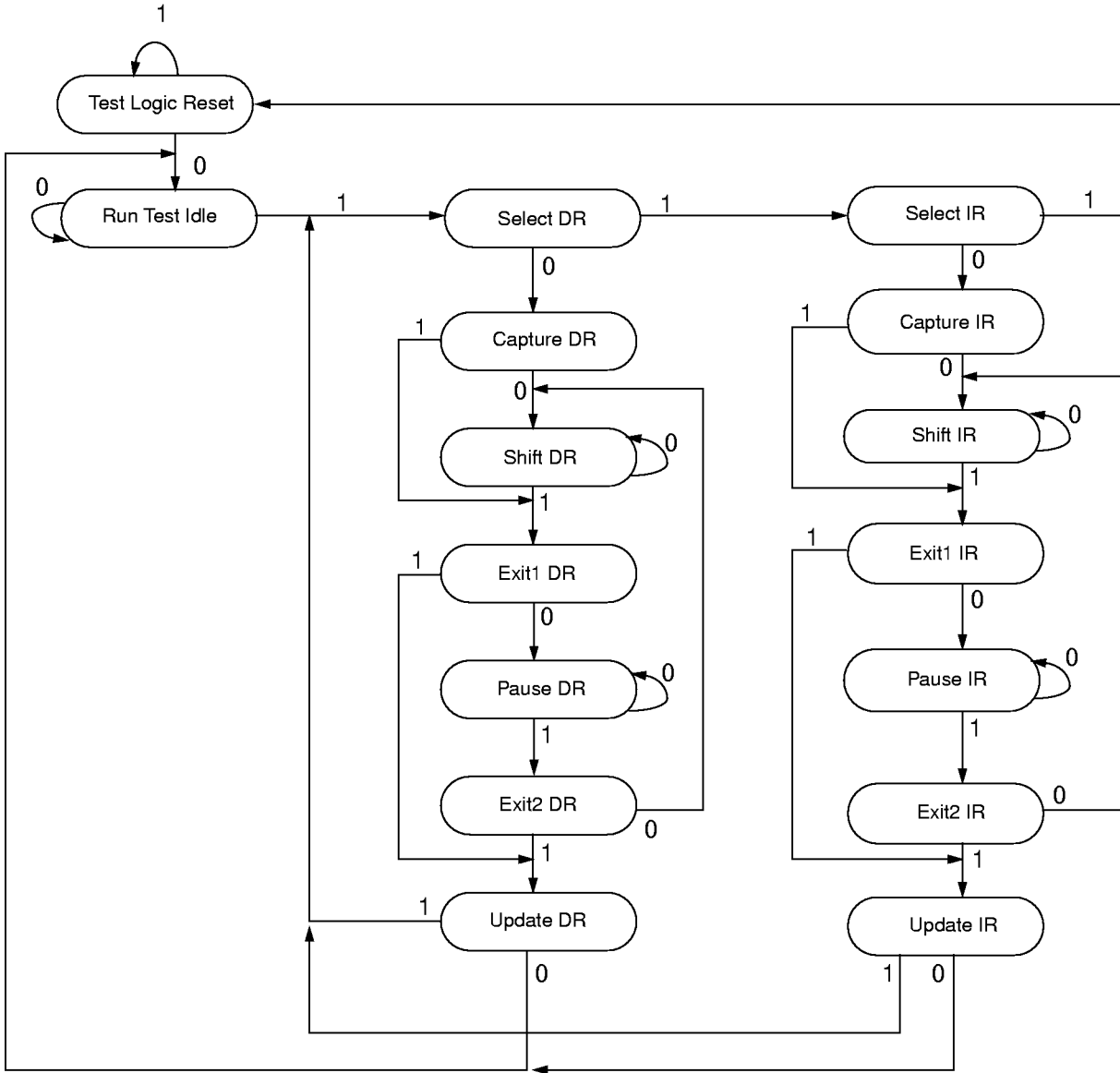
Boundary Scan Order (X18)

(PH =Place Holder)

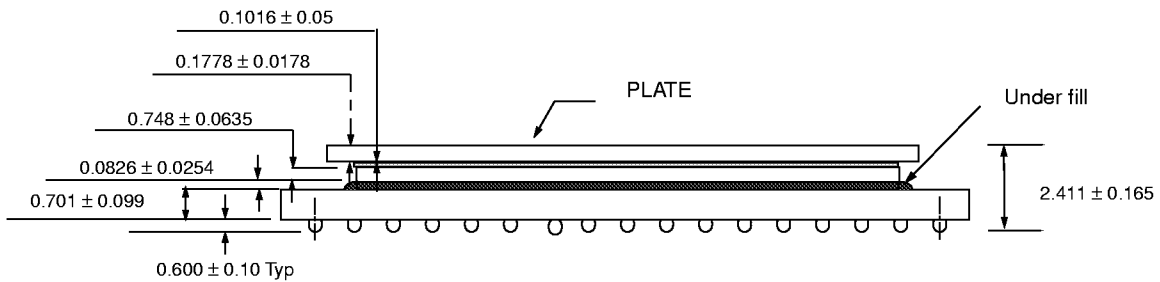
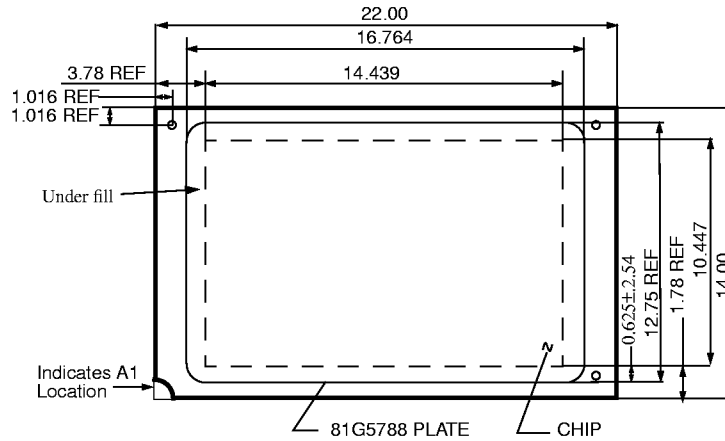
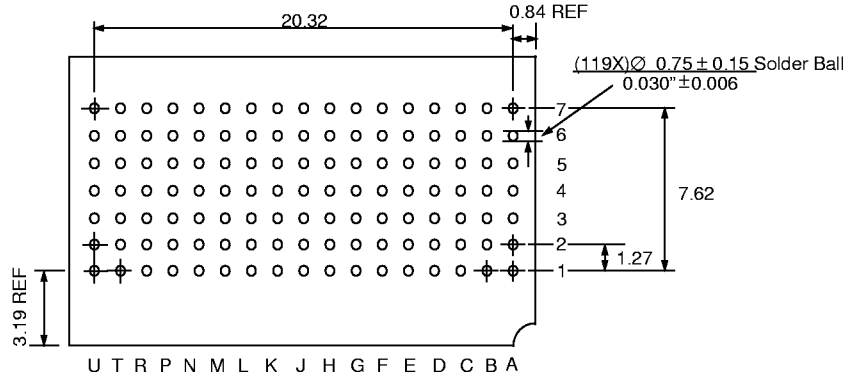
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	27	PH*	2B
2	SA12	6T	28	SA7	3A
3	SA1	4P	29	SA9	3C
4	SA13	6R	30	SA6	2C
5	SA17	5T	31	SA5	2A
6	ZZ	7T	32	DQ9	1D
7	DQ0	7P	33	DQ12	2E
8	DQ3	6N	34	DQ15	2G
9	DQ6	6L	35	DQ16	1H
10	DQ7	7K	36	SBWb	3G
11	SBWa	5L	37	ZQ	4D
12	K	4L	38	SS	4E
13	K	4K	39	C	4G
14	G	4F	40	C	4H
15	DQ8	6H	41	SW	4M
16	DQ5	7G	42	DQ17	2K
17	DQ4	6F	43	DQ14	1L
18	DQ2	7E	44	DQ13	2M
19	DQ1	6D	45	DQ11	1N
20	SA14	6A	46	DQ10	2P
21	SA15	6C	47	SA3	3T
22	SA10	5C	48	SA4	2R
23	SA16	5A	49	SA0	4N
24	PH*	6B	50	SA2	2T
25	SA11	5B	51	M1	3R
26	SA8	3B			

1. * Input of PH register connected to V_{SS}.

TAP Controller State Machine



7 x 17 BGA Dimensions



Note: All dimensions in Millimeters