

## Description

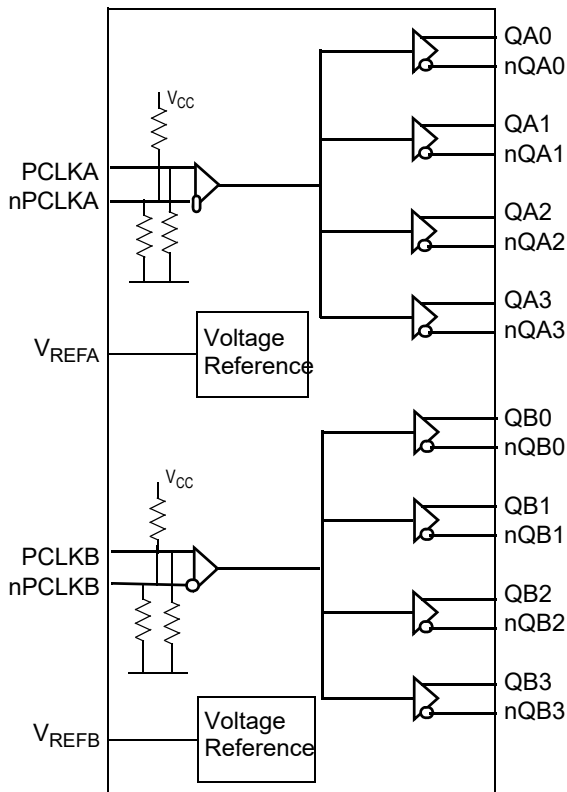
The 8SLVP2104I is a high-performance differential dual LVPECL fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals.

The 8SLVP2104I is characterized to operate from a 3.3V or 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8SLVP2104I ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and four low skew outputs are available. The integrated bias voltage reference enable easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

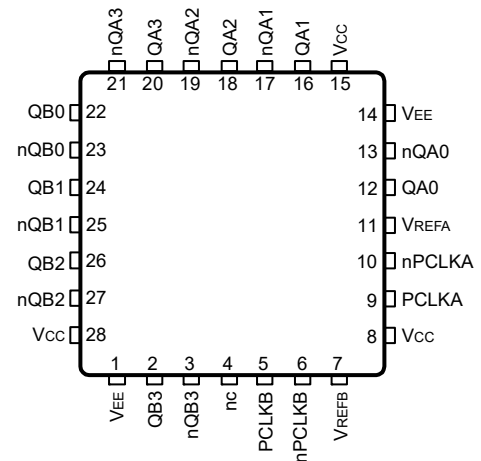
## Features

- Two 1:4, low skew, low additive jitter LVPECL output pairs
- Two differential clock input pairs
- Differential pairs can accept the following differential input levels: LVDS, LVPECL, CML
- Maximum input clock frequency: 2GHz
- Output skew: 8ps (typical)
- Propagation delay: 270ps (maximum)
- Low additive phase jitter, RMS: 47fs (maximum)
- Full 3.3V and 2.5V supply voltage
- Maximum device current consumption ( $I_{EE}$ ): 93mA (maximum)
- Available in lead-free (RoHS 6), 28-Lead VFQFN package
- -40°C to 85°C ambient operating temperature
- Supports case temperature  $\leq 105^\circ\text{C}$  operations
- Differential PCLKA, nPCLKA and PCLKB, nPCLKB pairs can also accept single-ended LVCMOS levels. See Applications section Wiring the Differential Input Levels to Accept Single-ended Levels (Figure 1A and Figure 1B).

## Block Diagram



## Pin Assignments



**8SLVP2104I**  
**28-VFQFN**  
**5mm x 5mm x 0.75mm package body**  
**NB Package**  
**Top View**

## Pin Descriptions and Characteristics

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 14	V <sub>EE</sub>	Power		Negative supply pins.
2, 3	QB3, nQB3	Output		Differential output pair B3. LVPECL interface levels.
4	nc	Unused		Do not connect.
5	PCLKB	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
6	nPCLKB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock/data input. V <sub>CC</sub> /2 default when left floating.
7	V <sub>REFB</sub>	Output		Bias voltage reference for the PCLKB, nPCLKB input pair.
8, 15, 28	V <sub>CC</sub>	Power		Power supply pins.
9	PCLKA	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
10	nPCLKA	Input	Pullup/ Pulldown	Inverting differential LVPECL clock/data input. V <sub>CC</sub> /2 default when left floating.
11	V <sub>REFA</sub>	Output		Bias voltage reference for the PCLKA, nPCLKA input pair.
12, 13	QA0, nQA0	Output		Differential output pair A0. LVPECL interface levels.
16, 17	QA1, nQA1	Output		Differential output pair A1. LVPECL interface levels.
18, 19	QA2, nQA2	Output		Differential output pair A2. LVPECL interface levels.
20, 21	QA3, nQA3	Output		Differential output pair A3. LVPECL interface levels.
22, 23	QB0, nQB0	Output		Differential output pair B0. LVPECL interface levels.
24, 25	QB1, nQB1	Output		Differential output pair B1. LVPECL interface levels.
26, 27	QB2, nQB2	Output		Differential output pair B2. LVPECL interface levels.

NOTE: *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			2		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Maximum Junction Temperature, $T_{J,MAX}$	150°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Input Sink/Source, $I_{REF}$	±2mA
ESD - Human Body Model, NOTE 1	2000V
ESD - Charged Device Model, NOTE 1	1500V

NOTE 1: According to JEDEC/JESD 22-A114/22-C101. ESD ratings are target specifications.

## Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
$T_A$	Ambient air temperature	-40		85	°C
$T_J$	Junction temperature			125	°C

NOTE 1: It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.

NOTE 2: All conditions in the table must be met to guarantee device functionality.

NOTE 3: The device is verified to the maximum operating junction temperature through simulation.

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3V	3.465	V
$I_{EE}$	Power Supply Current				93	mA
$I_{CC}$	Power Supply Current	QA[0:3] and QB[0:3] terminated 50Ω to $V_{CC} - 2V$			384	mA

**Table 3B. Power Supply DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	2.5V	2.625	V
$I_{EE}$	Power Supply Current				83	mA
$I_{CC}$	Power Supply Current	QA[0:3] and QB[0:3] terminated $50\Omega$ to $V_{CC} - 2V$			379	mA

**Table 3C. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  
 $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current PCLKA, nPCLKA; PCLKB, nPCLKB	$V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current PCLKA, PCLKB nPCLKA, nPCLKB	$V_{CC} = 3.465V, V_{IN} = 0V$	-10			$\mu A$
		$V_{CC} = 3.465V, V_{IN} = 0V$	-150			$\mu A$
$V_{REFA},$ $V_{REFB}$	Reference Voltage for Input Bias	$I_{REF} = 2mA$	$V_{CC} - 1.6$	$V_{CC} - 1.3$	$V_{CC} - 1.1$	V
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.1$	$V_{CC} - 0.9$	$V_{CC} - 0.8$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$	$V_{CC} - 1.5$	$V_{CC} - 1.4$	V

NOTE: Input and output parameters vary 1:1 with  $V_{CC}$ .

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 3D. LVPECL DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current PCLKA, nPCLKA; PCLKB, nPCLKB	$V_{CC} = V_{IN} = 2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current PCLKA, PCLKB nPCLKA, nPCLKB	$V_{CC} = 2.625V, V_{IN} = 0V$	-10			$\mu A$
		$V_{CC} = 2.625V, V_{IN} = 0V$	-150			$\mu A$
$V_{REFA},$ $V_{REFB}$	Reference Voltage for Input Bias	$I_{REF} = 2mA$	$V_{CC} - 1.6$	$V_{CC} - 1.3$	$V_{CC} - 1.1$	V
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.1$	$V_{CC} - 0.9$	$V_{CC} - 0.8$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$	$V_{CC} - 1.5$	$V_{CC} - 1.4$	V

NOTE: Input and output parameters vary 1:1 with  $V_{CC}$ .

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Electrical Characteristics

**Table 4A. AC Electrical Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{REF}$	Input Frequency PCLKA, nPCLKA; PCLKB, nPCLKB				2	GHz
$\Delta V/\Delta t$	Input Edge Rate PCLKA, nPCLKA; PCLKB, nPCLKB		1.5			V/ns
$t_{PD}$	Propagation Delay; NOTE 1	PCLKA, nPCLKA to any QAx, nQAx or PCLKB, nPCLKB to any QBx, nQBx for $V_{PP} = 0.1V$ or $0.3V$	50	165	270	ps
Channel_ISOL	Channel Isolation	$f_{REF} = 122.88MHz$		78		dB
$t_{sk(o)}$	Output Skew; NOTE 2, 3	Any Output		8	25	ps
$t_{sk(b)}$	Bank Skew; NOTE 3, 4	Within QAx, QBx		7	20	ps
$t_{sk(p)}$	Pulse Skew	$f_{REF} = 100MHz$		7	27	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5			100	200	ps
$t_{JIT, SP}$	Spurious Suppression, Coupling from QA3 to QB0	$f_{QB0} = 500MHz$ , $V_{PP(PCLKB)} = 0.15V$ , $V_{CMR(PCLKB)} = 1V$ and $f_{QA3} = 62.5MHz$ , $V_{PP(PCLKA)} = 1V$ , $V_{CMR(PCLKA)} = 1V$		-66		dB
		$f_{QB0} = 500MHz$ , $V_{PP(PCLKB)} = 0.15V$ , $V_{CMR(PCLKB)} = 1V$ and $f_{QA3} = 15.625MHz$ , $V_{PP(PCLKA)} = 1V$ , $V_{CMR(PCLKA)} = 1V$		-77		dB
$t_R / t_F$	Output Rise/ Fall Time	20% to 80%	40	100	150	ps
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 6, 8	$f_{REF} < 1.5 GHz$	0.1		1.5	V
		$f_{REF} > 1.5 GHz$	0.2		1.5	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 6, 7, 8		1.0		$V_{CC} - 0.6$	V
$V_{O(pp)}$	Output Voltage Swing, Peak-to-Peak	$V_{CC} = 3.3V$ , $f_{REF} \leq 2GHz$	0.4	0.6	1.0	V
		$V_{CC} = 2.5V$ , $f_{REF} \leq 2GHz$	0.35	0.55	1.0	V
$V_{DIFF\_OUT}$	Differential Output Voltage Swing, (Peak-to-Peak)	$V_{CC} = 3.3V$ , $f_{REF} \leq 2GHz$	0.8	1.2	2.0	V
		$V_{CC} = 2.5V$ , $f_{REF} \leq 2GHz$	0.7	1.1	2.0	V

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crosspoint.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew within a bank with equal load conditions. Measured at the differential crosspoints.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE 6:  $V_{IL}$  should not be less than  $-0.3V$ .  $V_{IH}$  should not be higher than  $V_{CC}$ .

NOTE 7: Common mode input voltage is defined as the crosspoint.

NOTE 8: For single-ended LVCMOS input applications, please refer to the Applications Information, Wiring the Differential Input to accept single-ended levels, Figures 1A and 1B.

**Table 4B. AC Additive Phase Jitter Electrical Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$t_{JIT}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	$f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 1kHz – 40MHz		100	120	fs
		$f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 10kHz – 20MHz		65	80	fs
		$f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 12kHz – 20MHz		65	80	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 1kHz – 40MHz		58	65	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 10kHz – 20MHz		43	47	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 12kHz – 20MHz		43	47	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$ , Integration Range: 1kHz – 40MHz		59	68	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$ , Integration Range: 10kHz – 20MHz		43	48	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$ , Integration Range: 12kHz – 20MHz		43	47	fs

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 4C. AC Additive Phase Jitter Electrical Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

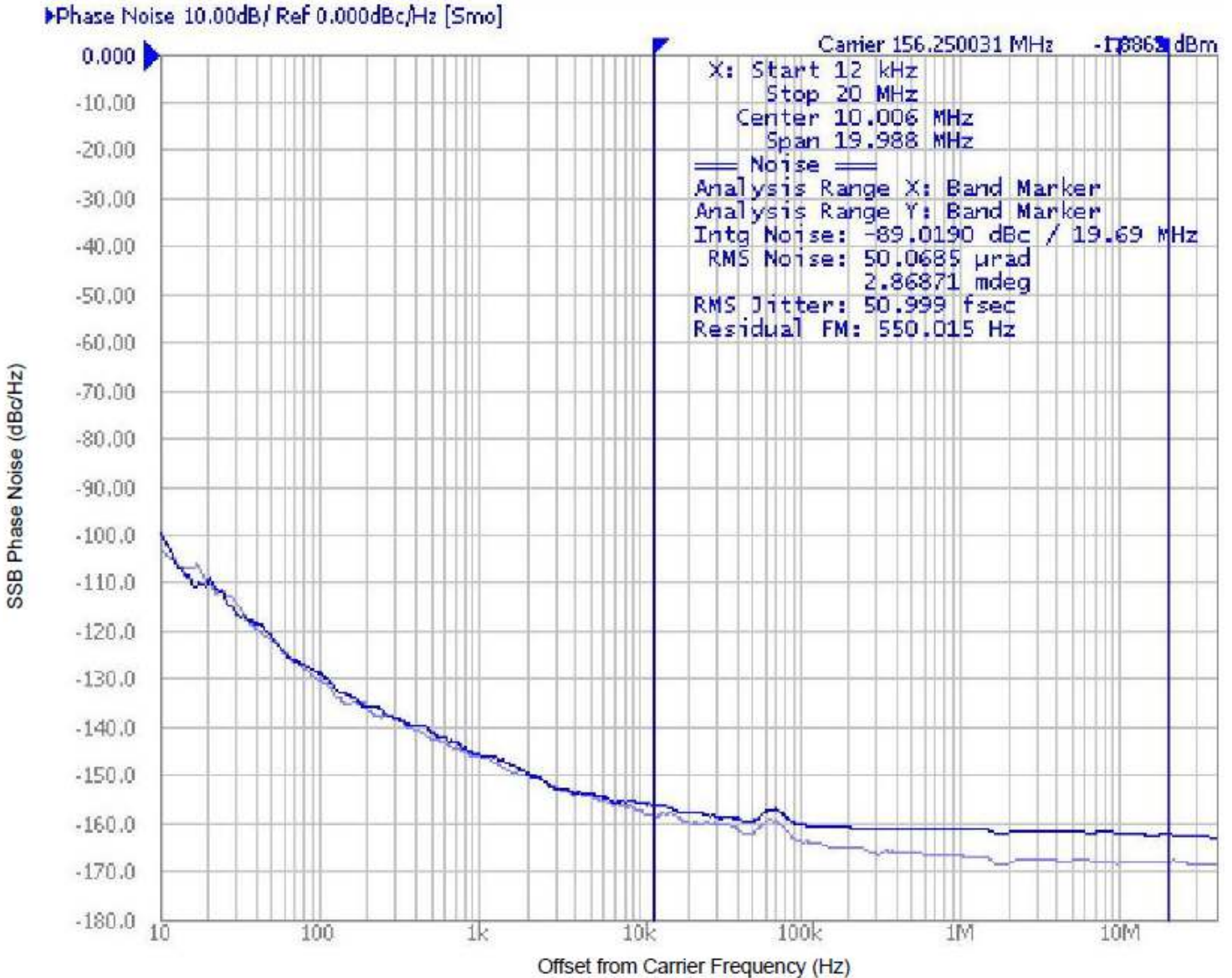
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$t_{JIT}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	$f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 1kHz – 40MHz		108	125	fs
		$f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 10kHz – 20MHz		71	86	fs
		$f_{REF} = 122.88\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 12kHz – 20MHz		71	86	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 1kHz – 40MHz		62	69	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 10kHz – 20MHz		45	50	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 1V$ , Integration Range: 12kHz – 20MHz		45	50	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$ , Integration Range: 1kHz – 40MHz		64	72	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$ , Integration Range: 10kHz – 20MHz		46	52	fs
		$f_{REF} = 156.25\text{MHz}$ Square Wave, $V_{PP} = 0.5V$ , Integration Range: 12kHz – 20MHz		46	52	fs

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

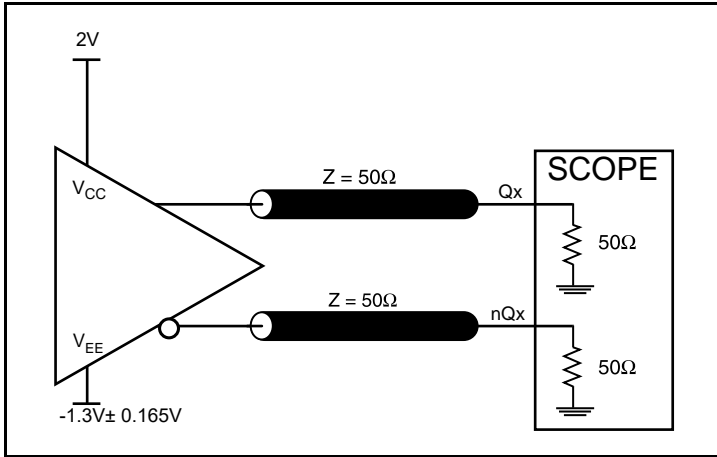
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



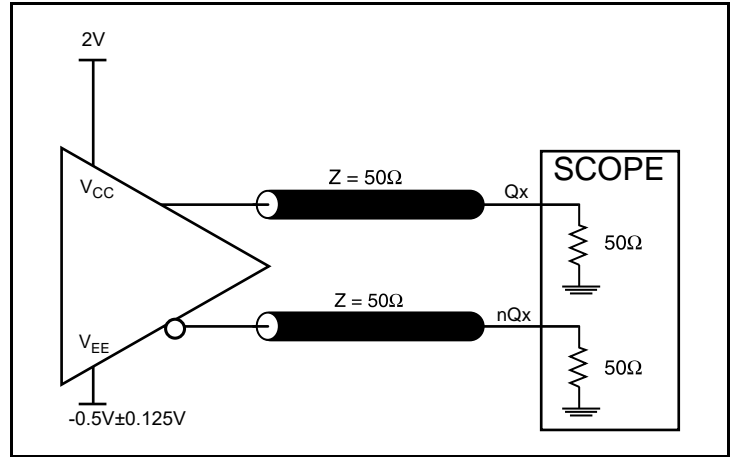
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

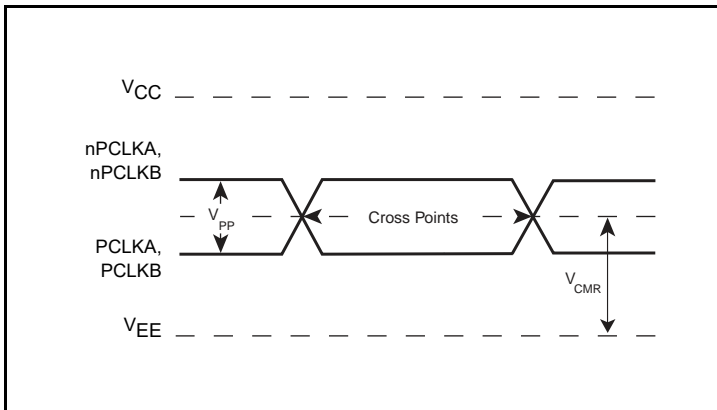
## Parameter Measurement Information



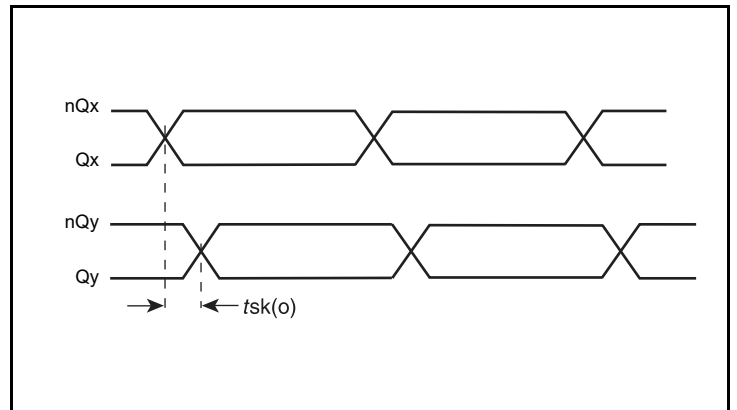
3.3V LVPECL Output Load AC Test Circuit



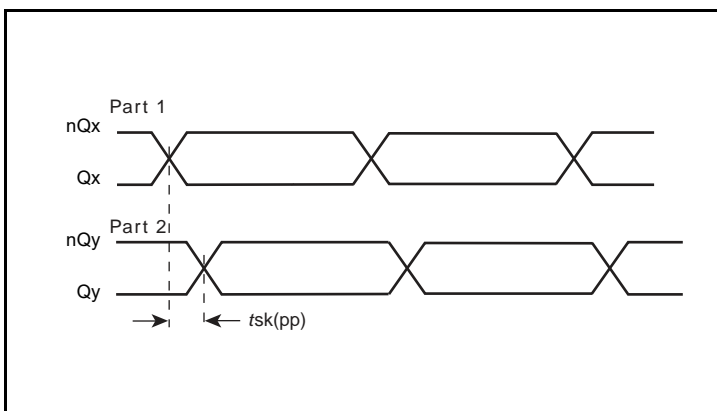
2.5V LVPECL Output Load AC Test Circuit



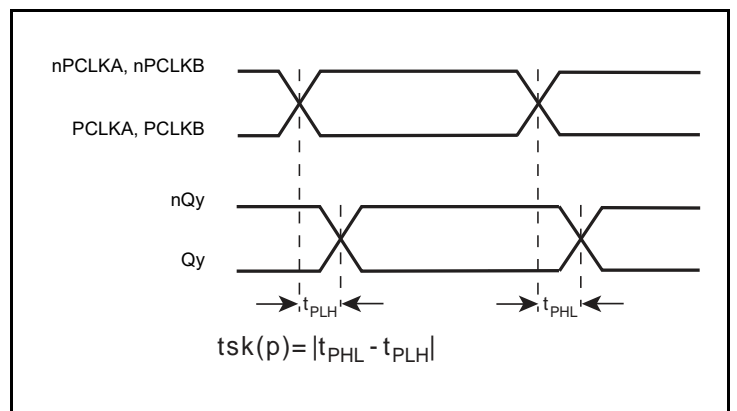
Differential Input Level



Output Skew



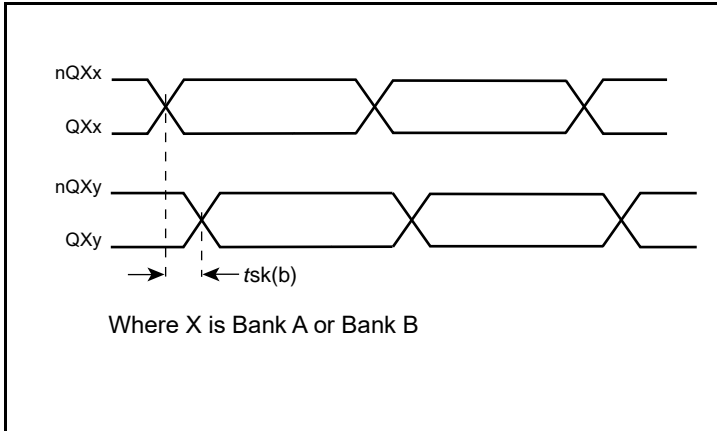
Part-to-Part Skew



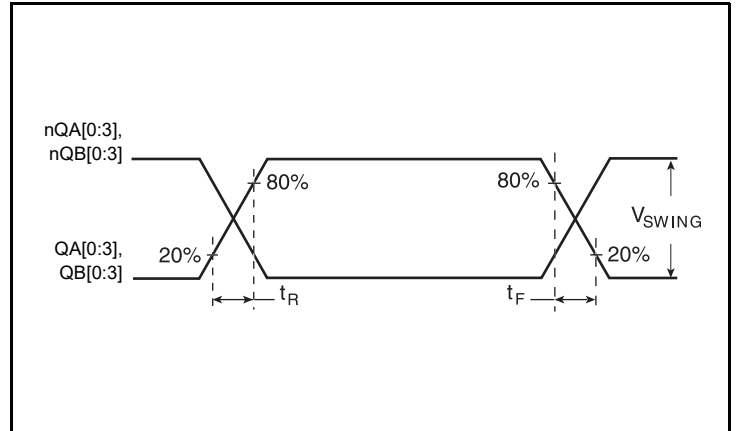
Pulse Skew



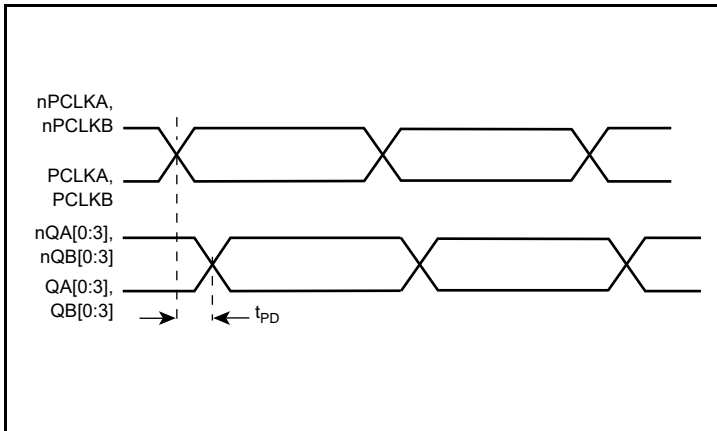
Parameter Measurement Information, continued



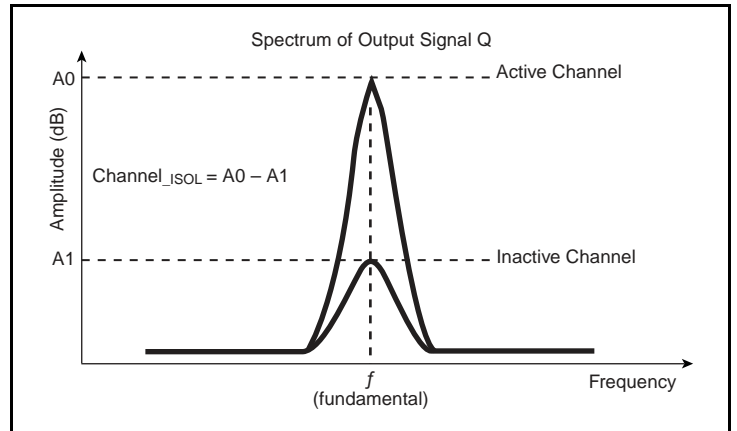
Bank Skew



Output Rise/Fall Time



Propagation Delay



Channel Isolation

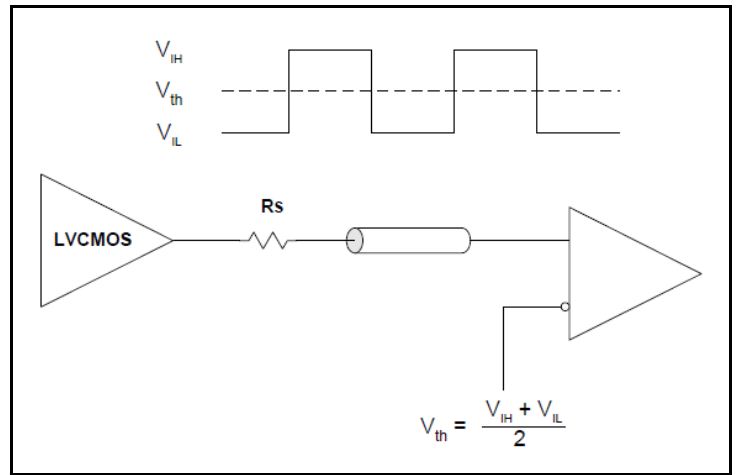
## Applications Information

### Wiring the Differential Input to Accept Single-Ended Levels

The IDT8SLVP2104I inputs can be interfaced to LVPECL, LVDS, CML or LVCMOS drivers. *Figure 1A* illustrates how to DC couple a single LVCMOS input to the IDT8SLVP2104I. The value of the series resistance  $R_S$  is calculated as the difference between the transmission line impedance and the driver output impedance. This resistor should be placed close to the LVCMOS driver. To avoid cross-coupling of single-ended LVCMOS signals, apply the LVCMOS signals to no more than one PCLK input.

A practical method to implement  $V_{th}$  is shown in *Figure 1B* below. The reference voltage  $V_{th} = V_1 = V_{CC}/2$ , is generated by the bias resistors  $R_1$  and  $R_2$ . The bypass capacitor ( $C_1$ ) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible.

The ratio of  $R_1$  and  $R_2$  might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ ,  $R_1$  and  $R_2$  value should be adjusted to set  $V_1$  at 1.25V. The values below apply when both the single-ended swing and  $V_{CC}$  are at the same voltage.



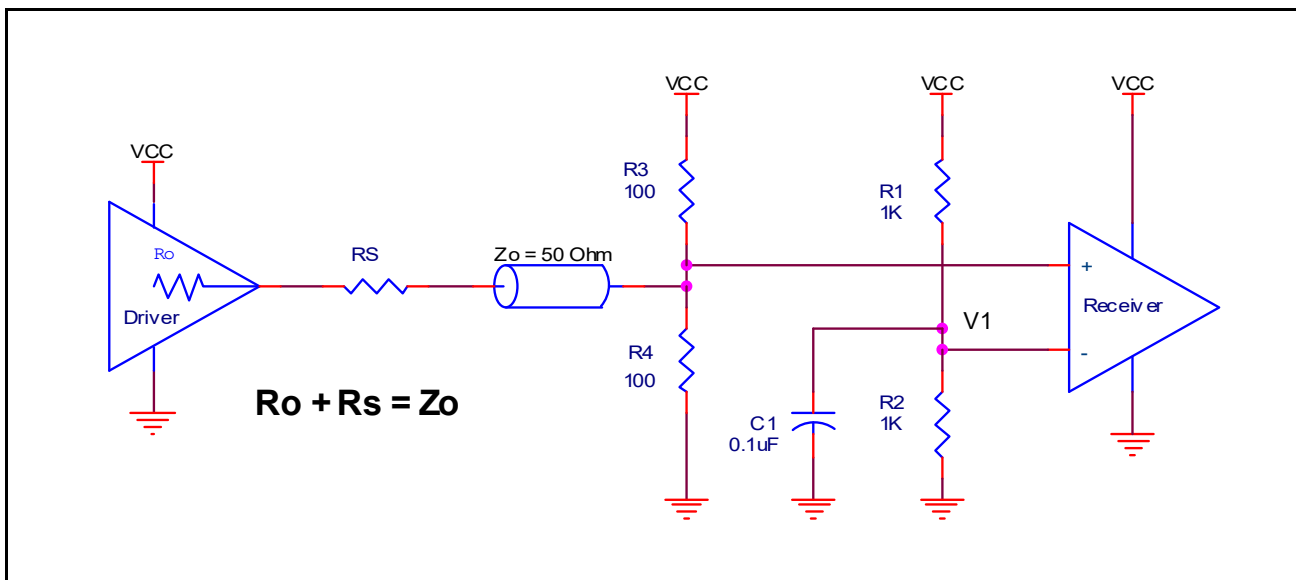
**Figure 1A. DC-Coupling a Single LVCMOS Input to the IDT8SLVP2104I**

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced, particularly if both input references are LVCMOS to minimize cross talk. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3V$  and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ .

*Figure 1B* shows a way to attenuate the PCLK input level by a factor of two as well as matching the transmission line between the LVCMOS driver and the IDT8SLVP2104I at both the source and the

load. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance.  $R_3$  and  $R_4$  in parallel should equal the transmission line impedance; for most  $50\Omega$  applications,  $R_3$  and  $R_4$  will be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Though some of the recommended components of *Figure 1B* might not be used, the pads should be placed in the layout so that they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.



**Figure 1B. Alternative DC Coupling a Single LVCMOS Input to the IDT8SLVP2104I**

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## Recommendations for Unused Input and Output Pins

### Inputs:

#### PCLKx/nPCLKx Inputs

For applications requiring only one differential input, the unused PCLKx and nPCLKx pins can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the unused PCLKx input to ground.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### V<sub>REFX</sub>

Unused V<sub>REFA</sub> and V<sub>REFB</sub> pins can be left floating. We recommend that there is no trace attached.

### 3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the PCLK /nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

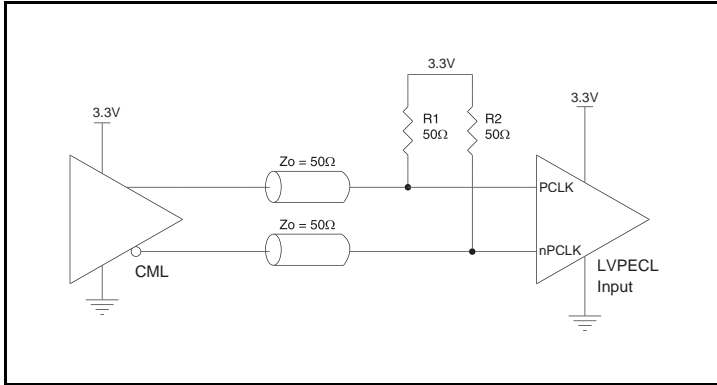


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

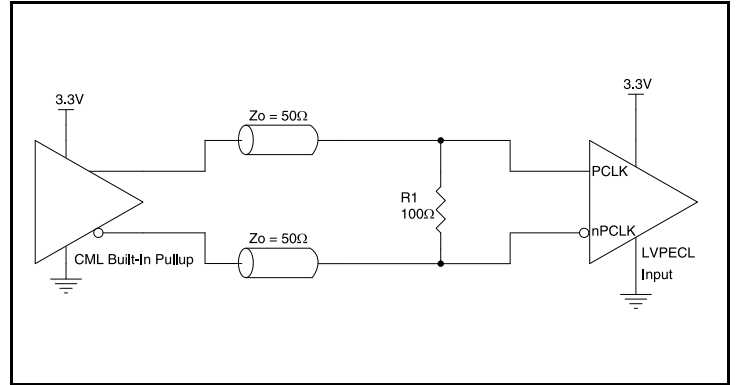


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

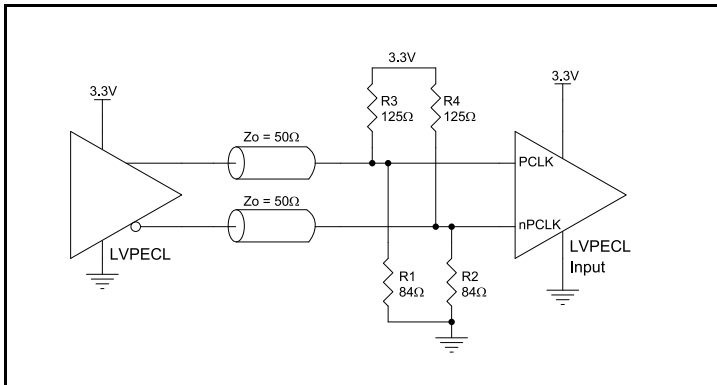


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

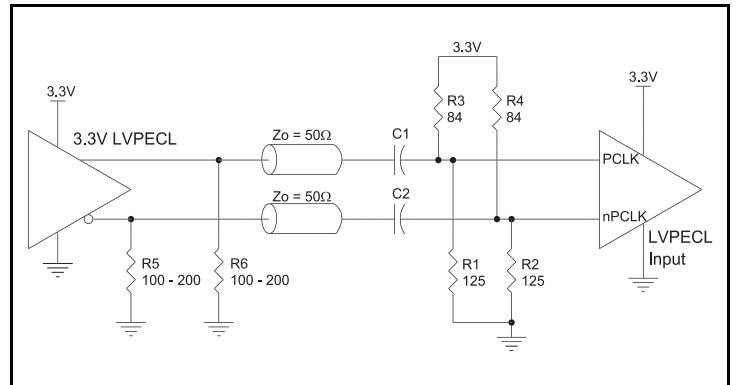


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

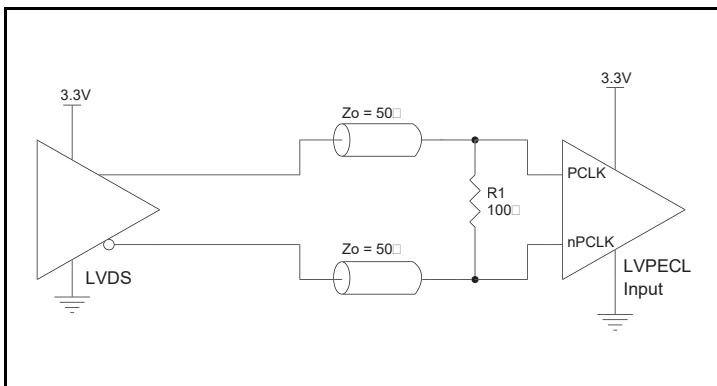


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

## 2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 3A to 3E* show interface examples for the PCLK /nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

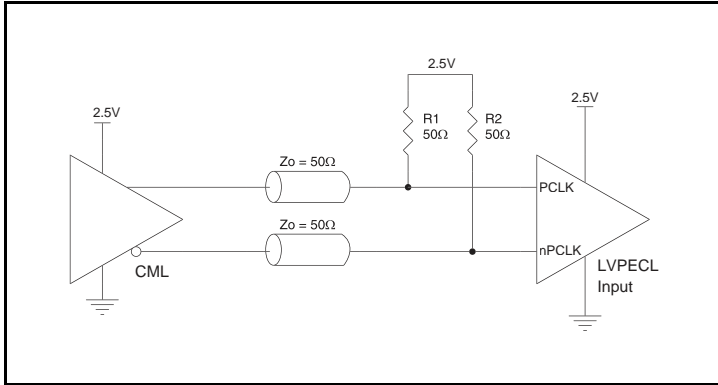


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

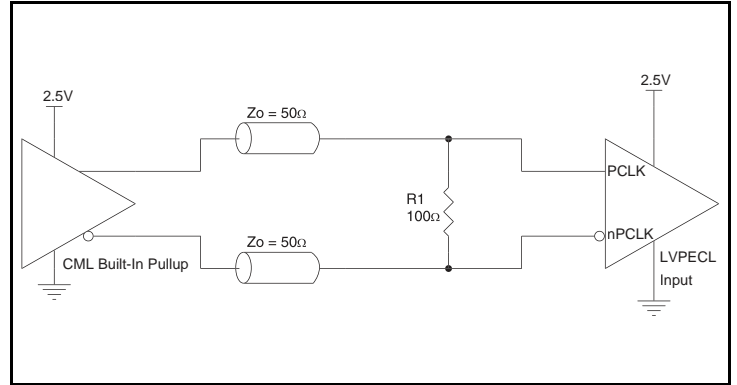


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

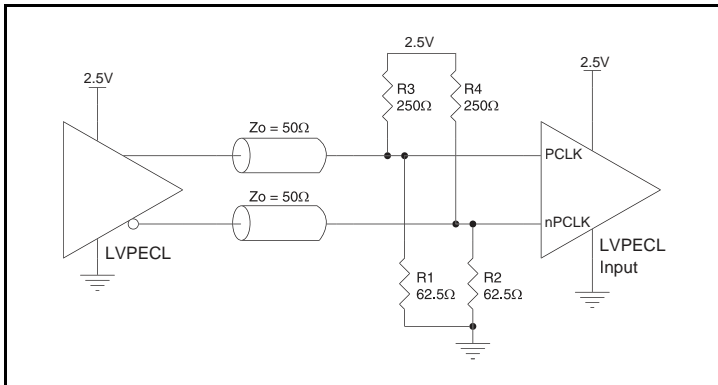


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

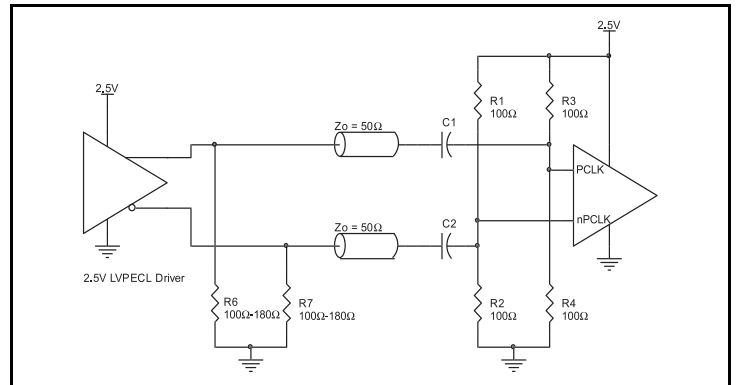


Figure 3D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

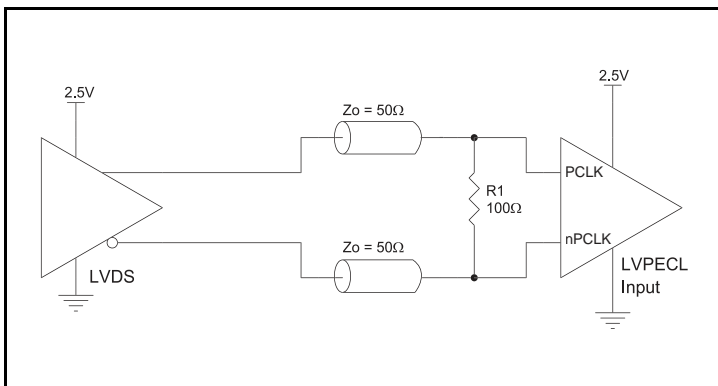


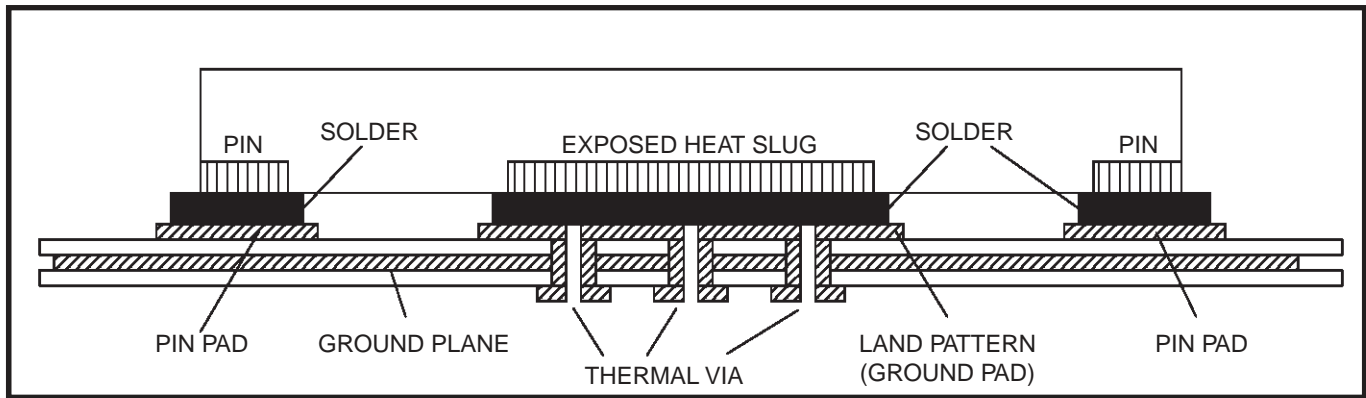
Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

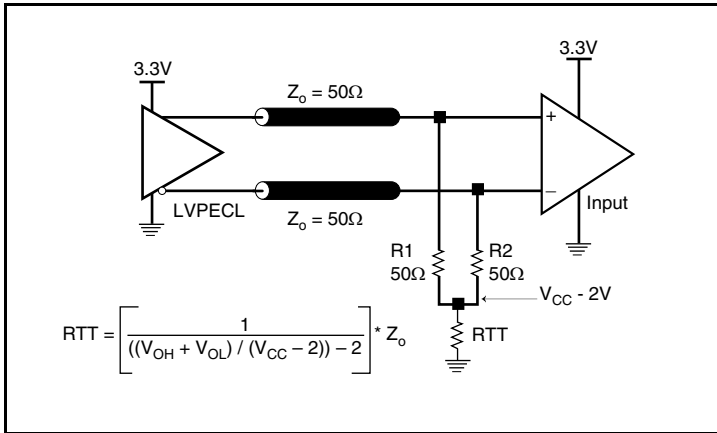


Figure 5A. 3.3V LVPECL Output Termination

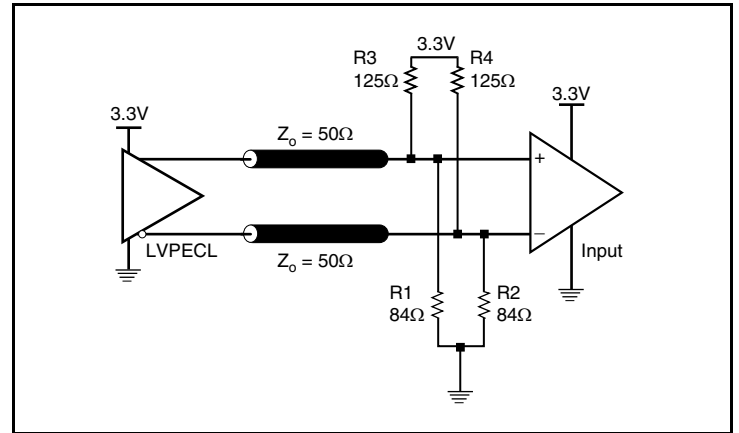


Figure 5B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 6A and Figure 6B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 6B can be eliminated and the termination is shown in Figure 6C.

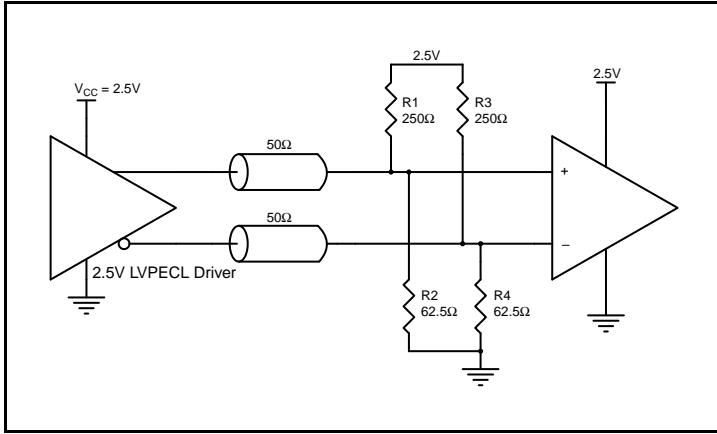


Figure 6A. 2.5V LVPECL Driver Termination Example

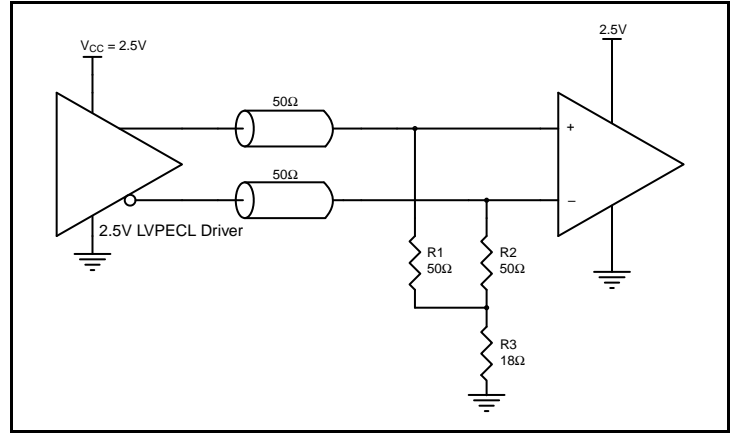


Figure 6B. 2.5V LVPECL Driver Termination Example

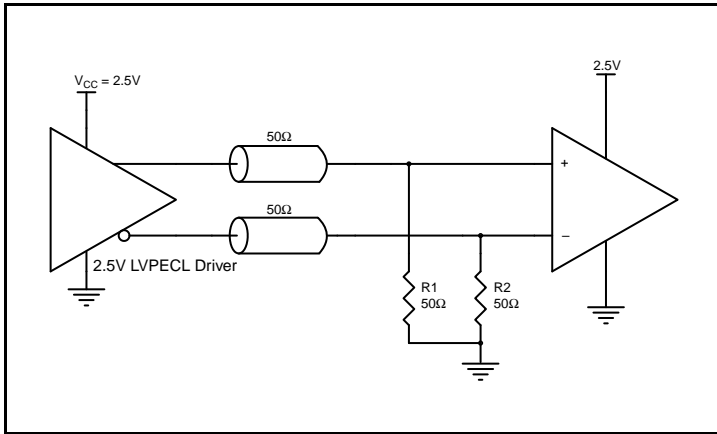


Figure 6C. 2.5V LVPECL Driver Termination Example



## Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8SLVP2104I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8SLVP2104I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 93mA = 322.25mW$
- Power (outputs)<sub>MAX</sub> = **36mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $8 * 36mW = 288mW$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $322.25mW + 288mW = 610.25mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 46.2°C/W per Table 5 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.610W * 46.2^\circ C/W = 113.2^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

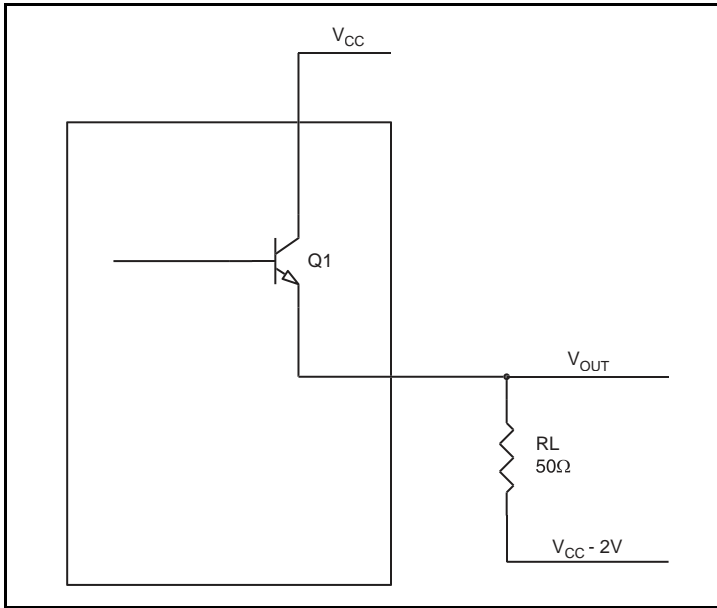
**Table 5. Thermal Resistance  $\theta_{JA}$  for 28-Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.4°C/W	37.1°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ . These are typical calculations.

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.8V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.8V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.4V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.4V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.8V)/50\Omega] * 0.8V = \mathbf{19.2mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.4V)/50\Omega] * 1.4V = \mathbf{16.8mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{36mW}$

## Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter  $\Psi_{JB}$  (Psi-JB) to calculate the junction temperature ( $T_J$ ) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter,  $\Psi_{JB}$ , is calculated using the following equation:

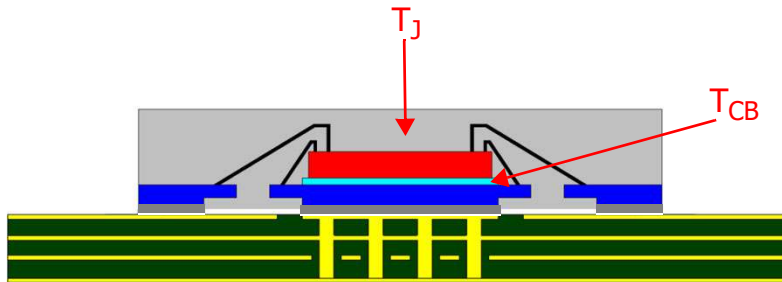
$T_J = T_{CB} + \Psi_{JB} \times P_d$ , Where

$T_J$  = Junction temperature at steady state condition in ( $^{\circ}\text{C}$ ).

$T_{CB}$  = Case temperature (Bottom) at steady state condition in ( $^{\circ}\text{C}$ ).

$\Psi_{JB}$  = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

$P_d$  = power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature ( $T_{CB}$ ). A good connection ensures that temperature at the exposed pad ( $T_{CB}$ ) and the board temperature ( $T_B$ ) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature ( $T_J$ ):  $T_J = T_{CB} + \Psi_{JB} \times P_d$

Package type:	28-Lead VFQFN
Body size:	5mm x 5mm x 0.75mm
ePad size:	3.25mm x 3.25mm
Thermal Via:	4 x 4 matrix
$\Psi_{JB}$	2.4 C/W
$T_{CB}$	105 $^{\circ}\text{C}$
$P_d$	0.610 W

For the variables above, the junction temperature is equal to 106.5 $^{\circ}\text{C}$ . Since this is below the maximum junction temperature of 125 $^{\circ}\text{C}$ , there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 113.2 $^{\circ}\text{C}$ , this device can function without the degradation of the specified AC or DC parameters.

## Reliability Information

**Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 28-Lead VFQFN**

$\theta_{JA}$ at 0 Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.4°C/W	37.1°C/W

## Transistor Count

The transistor count for the 8SLVP2104I is: 309

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

[www.idt.com/document/psc/nbnbg28-package-outline-50-x-50-mm-body-050-mm-pitch-qfn](http://www.idt.com/document/psc/nbnbg28-package-outline-50-x-50-mm-body-050-mm-pitch-qfn)

## Ordering Information

**Table 7. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVP2104ANBGI	LVP2104ANBGI	“Lead-Free” 28-Lead VFQFN	Tray	-40°C to 85°C
8SLVP2104ANBGI8	LVP2104ANBGI	“Lead-Free” 28-Lead VFQFN	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40°C to 85°C
8SLVP2104ANBGI/W	LVP2104ANBGI	“Lead-Free” 28-Lead VFQFN	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40°C to 85°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

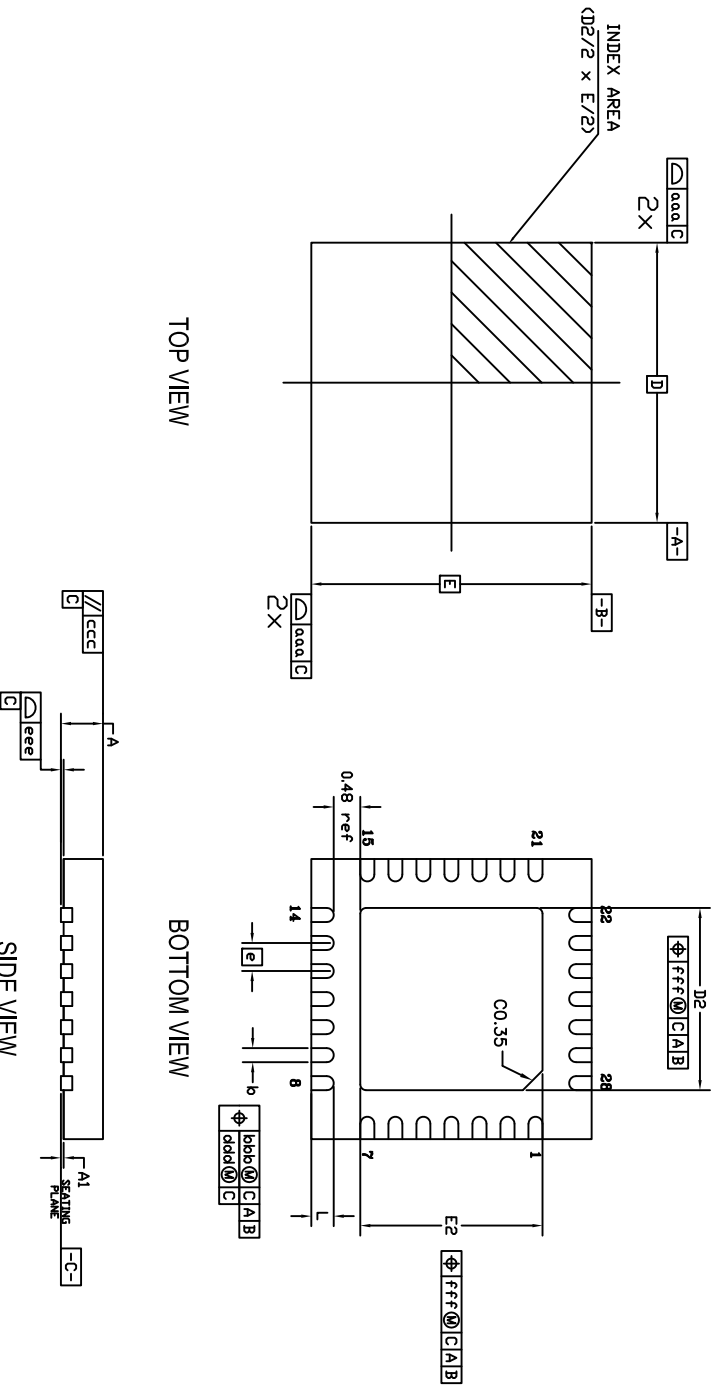
**Table 8. Pin 1 Orientation in Tape and Reel Packaging**

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

## Revision History


Revision Date	Description of Change
January 15, 2019	<ul style="list-style-type: none"> <li>• Updated the description of <a href="#">Absolute Maximum Ratings</a></li> <li>• Added <a href="#">Recommended Operating Conditions</a></li> <li>• Updated the <a href="#">Package Outline Drawings</a>; however, no technical changes</li> <li>• Completed other minor improvements</li> </ul>
June 8, 2015	Features Section - added case temperature bullet. Added case temperature consideration section.
November 19, 2014	Per PCN# 1406-01, Effective Date 11/19/2014 Changed maximum IEE to 93mA in the Features Section on page 1, Table 3A on page 3 and Power Considerations and calculations on page 17. Updated the datasheet format.
January 28, 2014	Changed Note 6 to read “V <sub>IL</sub> should not be less than -0.3V. V <sub>IH</sub> should not be higher than V <sub>CC</sub> .”
February 19, 2013	Fixed Ohm symbol and Zo font issues in drawings.
January 30, 2013	Added Features Bullet: Differential PCLKA, nPCLKA and PCLKB, nPCLKB pairs can also accept single-ended LVCMOS levels. Added NOTE 8 to V <sub>PP</sub> , V <sub>CMR</sub> . Updated the “Wiring the Differential Input to Accept Single-Ended Levels” note.
August 2, 2012	Ordering Information Table - added additional row. Added Orientation Packaging Table.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	06/04/10	KS
01	CORRECTION ON L	09/22/10	DP
02	COMBINE POD & LAND PATTERN	1/22/14	JH

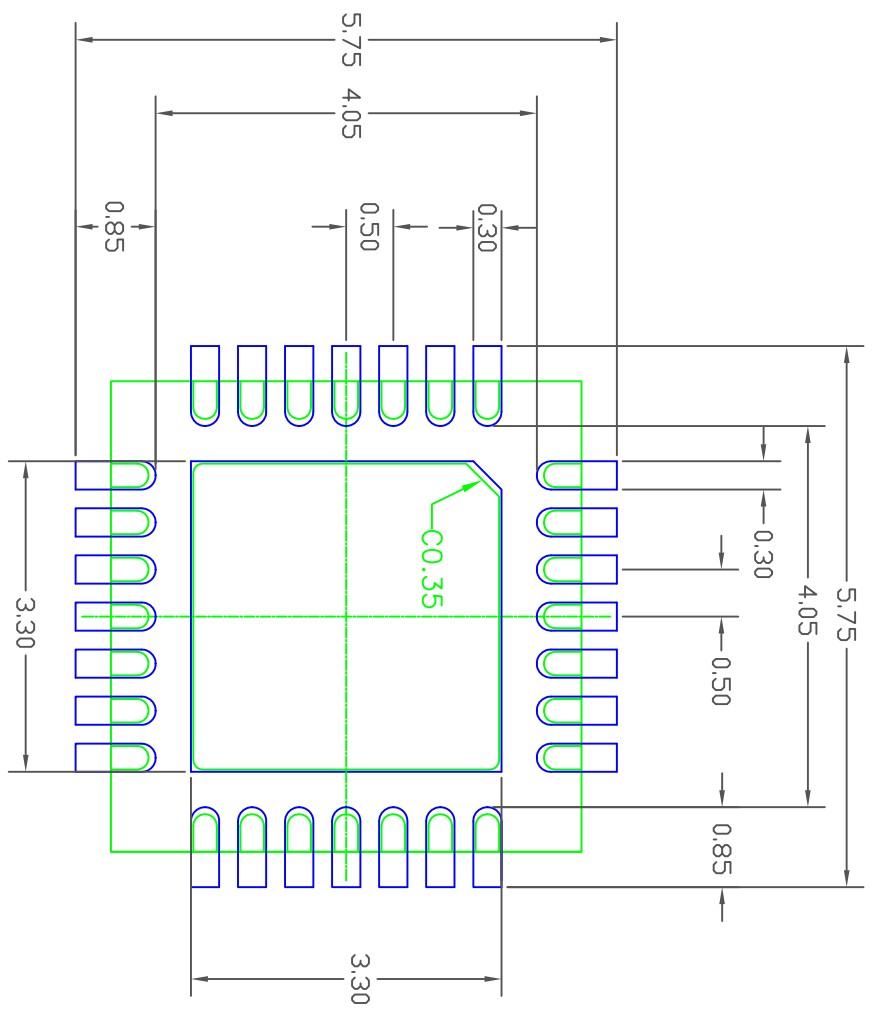


SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	3.15	3.25	3.35
E2	3.15	3.25	3.35
L	0.30	0.40	0.50
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
ccc	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
  2. ALL DIMENSIONS ARE IN MILLIMETERS.


<b>TOLERANCES</b> UNLESS SPECIFIED DECIMAL ±.1 ANGULAR ±1° XXX±.05 XXX±.030		 <b>IDT</b> www.idt.com	6024 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
<b>APPROVALS</b> DRAWN: XJS CHECKED:	DATE: 06/02/10 <b>TITLE</b> NB/NBG28 PACKAGE OUTLINE 5.0 x 5.0 mm BODY 0.50 mm PITCH QFN		
SIZE: C DRAWING No.: PSC-4312	DO NOT SCALE DRAWING		

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	06/04/10	KS
01	CORRECTION ON L	09/22/10	DP
02	COMBINE POD & LAND PATTERN	1/22/14	JH



- NOTES:
1. ALL DIMENSION ARE IN mm, ANGLES IN DEGREES.
  2. TOP DOWN VIEW, AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOW FOR REFERENCE IN PCB.
  4. LAND PATTERN IN BLUE, NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		ANGULAR ±1°	
DECIMAL	XXX± .05		
XX± .1	XXX± .030		
APPROVALS	DATE	TITLE	NB/NBG28 PACKAGE OUTLINE
DRAWN <i>JKS</i>	06/02/10	SIZE	5.0 x 5.0 mm BODY
CHECKED		DRAWING No.	0.50 mm PITCH QFN
		SIZE	C
		DRAWING No.	PSC-4312
		REV	02
DO NOT SCALE DRAWING		SHEET 2 OF 2	


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