IS62WV12816DALL/DBLL
IS65WV12816DALL/DBLL

128K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

JUNE 2013

FEATURES

- High-speed access time: 35ns, 45ns, 55ns
- CMOS low power operation
  – 36 mW (typical) operating
  – 9 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  – 1.8V ± 10% V_{DD} (IS62/65WV12816DALL)
  – 2.5V--3.6V V_{DD} (IS62/65WV12816DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and Autotmovie temperature support
- 2CS Option Available
- Lead-free available

DESCRIPTION

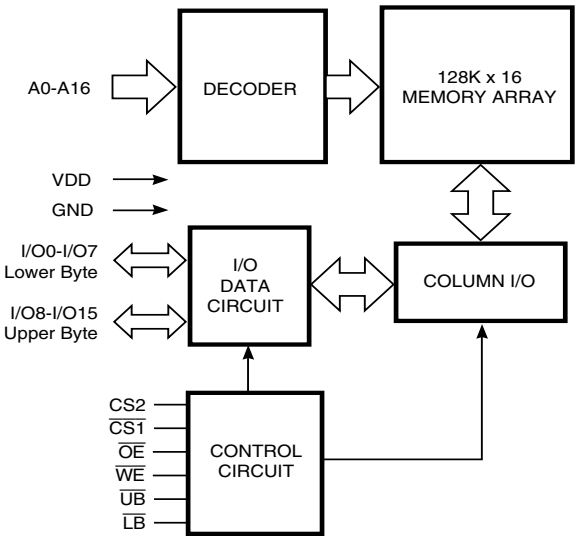
The *ISSI* IS62/65WV12816DALL/DBLL are high-speed, 2M bit static RAMs organized as 128K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) or when $\overline{CS1}$ is LOW, CS2 is HIGH and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS62/65WV12816DALL/DBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II).

FUNCTIONAL BLOCK DIAGRAM



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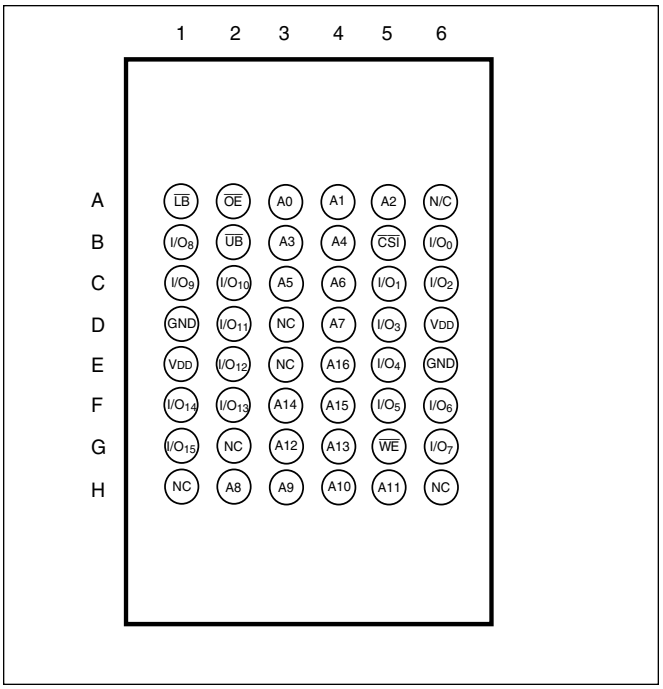
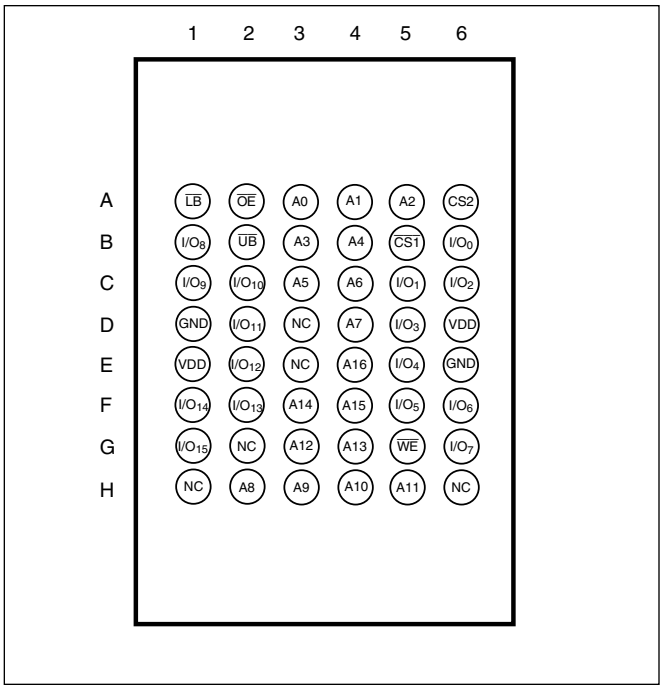
a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATIONS

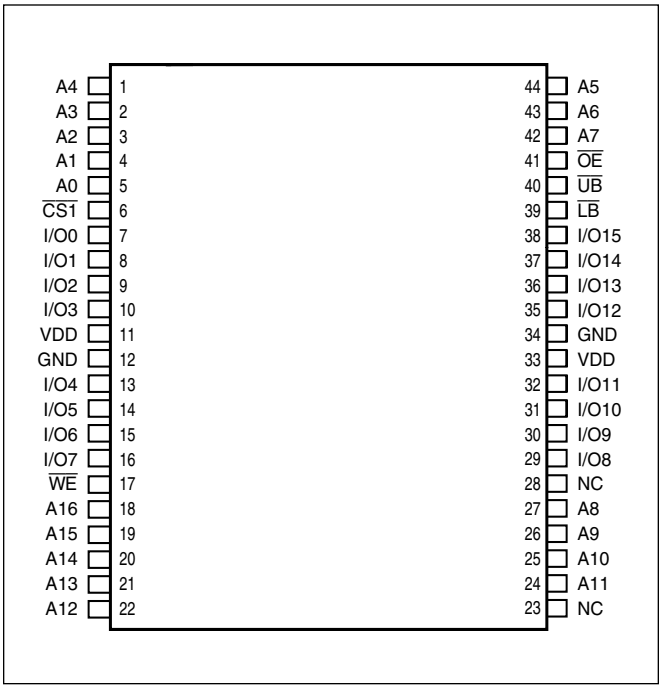
48-Pin mini BGA (6mm x 8mm) (Package Code B)



48-Pin mini BGA (6mm x 8mm) 2 CS Option (Package Code B2)



44-Pin mini TSOP (Type II) (Package Code T)



PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	H	L	H	L	High-Z	D_{OUT}	
	H	L	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	H	X	H	L	High-Z	D_{IN}	
	L	L	H	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS62WV12816DALL	IS62WV12816DBLL
Commercial	0°C to +70°C	1.8V ± 10%	2.5V - 3.6V
Industrial	–40°C to +85°C	1.8V ± 10%	2.5V - 3.6V
		IS65WV12816DALL	**IS65WV12816DBLL**
Automotive	-40°C to +125°C	1.8V ± 10%	2.5V - 3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.8V ± 10%	1.4	—	V
		I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.8V ± 10%	—	0.2	V
		I_{OL} = 1.0 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.8V ± 10%	1.4	V_{DD} + 0.2	V
			2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		1.8V ± 10%	–0.2	0.4	V
			2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
For IS62/65WV12816DALL:
V_{IL} (min.) = -1.0V AC (pluse width < 10ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 1.0V AC; (pluse width < 10ns). Not 100% tested.

For IS62/65WV12816DBLL:
V_{IL} (min.) = -2.0V AC (pluse width < 10ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 2.0V AC; (pluse width < 10ns). Not 100% tested.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

IS62/65WV12816DALL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind. Auto.	15 20 25	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com. Ind. Auto.	3 3 4	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	$\overline{CS2}$ = VIL f = 0Hz	Com. Ind. Auto.	0.3 0.3 0.5	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	(1) 0V ≤ CS2 ≤ 0.2V OR (2) $\overline{CS1}$ ≥ VDD - 0.2V, CS2 ≥ VDD - 0.2V OR (3) $\overline{LB}$ and $\overline{UB}$ ≥ VDD- 0.2V $\overline{CS1}$ ≤ 0.2V, CS2 ≥ VDD - 0.2V, f= 0Hz	Com. Ind. Auto.	4 6 15	µA

IS62/65WV12816DBLL, POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max 35	Max. 45	Max. 55	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	22	20	18	mA
			Ind.	23	21	19	
			Auto.	35	30	25	
			typ.[2]	15	12	10	
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com.	3	3	3	mA
			Ind.	3	3	3	
			Auto.	4	4	4	
I_{SB1}	TTL Standby Current (TTL Inputs)	CS2 = VIL f = 0Hz	Com.	0.2	0.2	0.2	mA
			Ind.	0.2	0.2	0.2	
			Auto.	0.3	0.3	0.3	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	(1) 0V ≤ CS2 ≤ 0.2V OR (2) $\overline{CS1}$ ≥ VDD - 0.2V, CS2 ≥ VDD - 0.2V OR (3) $\overline{LB}$ and $\overline{UB}$ > VDD- 0.2V $\overline{CS1}$ ≤ 0.2V, CS2 ≥ VDD - 0.2V f= 0Hz	Com.	5	5	5	µA
			Ind.	7	7	7	
			Auto.	25	25	25	
			typ.[2]	2	2	2	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

AC TEST CONDITIONS

Parameter	IS62/65WV12816DALL (Unit)	IS62/65WV12816DBLL (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2V	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	1V/1ns	1V/1ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.8V ± 10%	2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

AC TEST LOADS

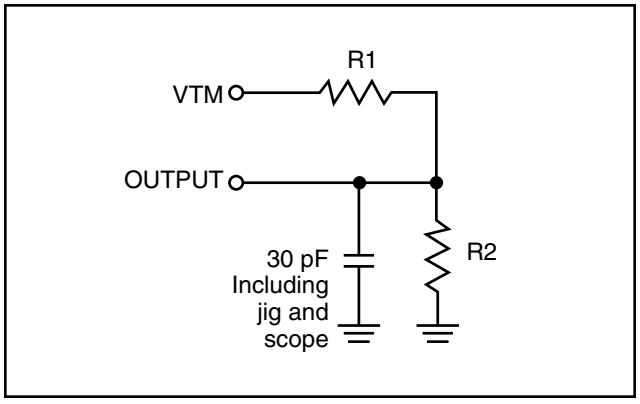


Figure 1

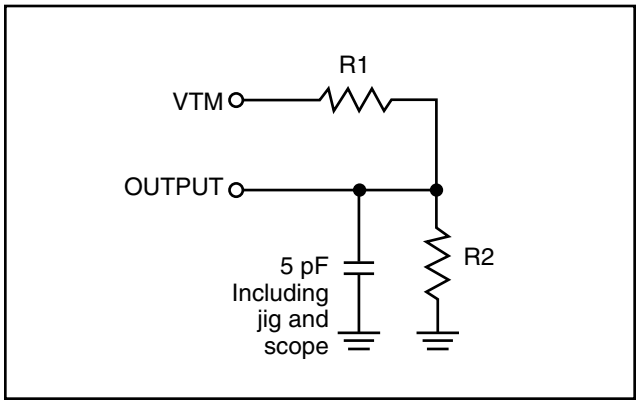


Figure 2

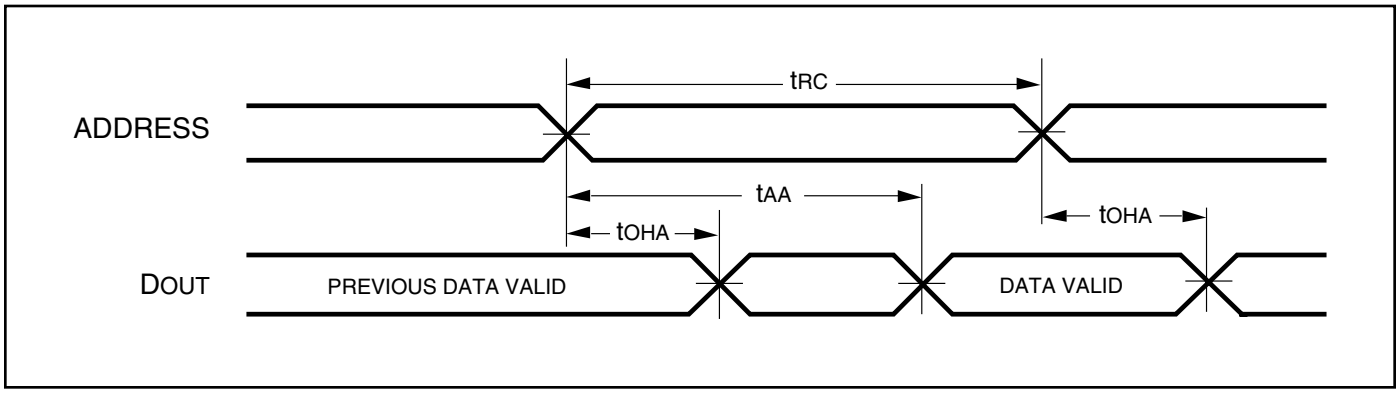
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	35 ns		45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	ns
t_{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	35	—	45	—	55	ns
t_{DOE}	$\overline{OE}$ Access Time	—	15	—	20	—	25	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	10	—	15	—	20	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	10	0	15	0	20	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	35	—	45	—	55	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	10	0	15	0	20	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns

Notes:
1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

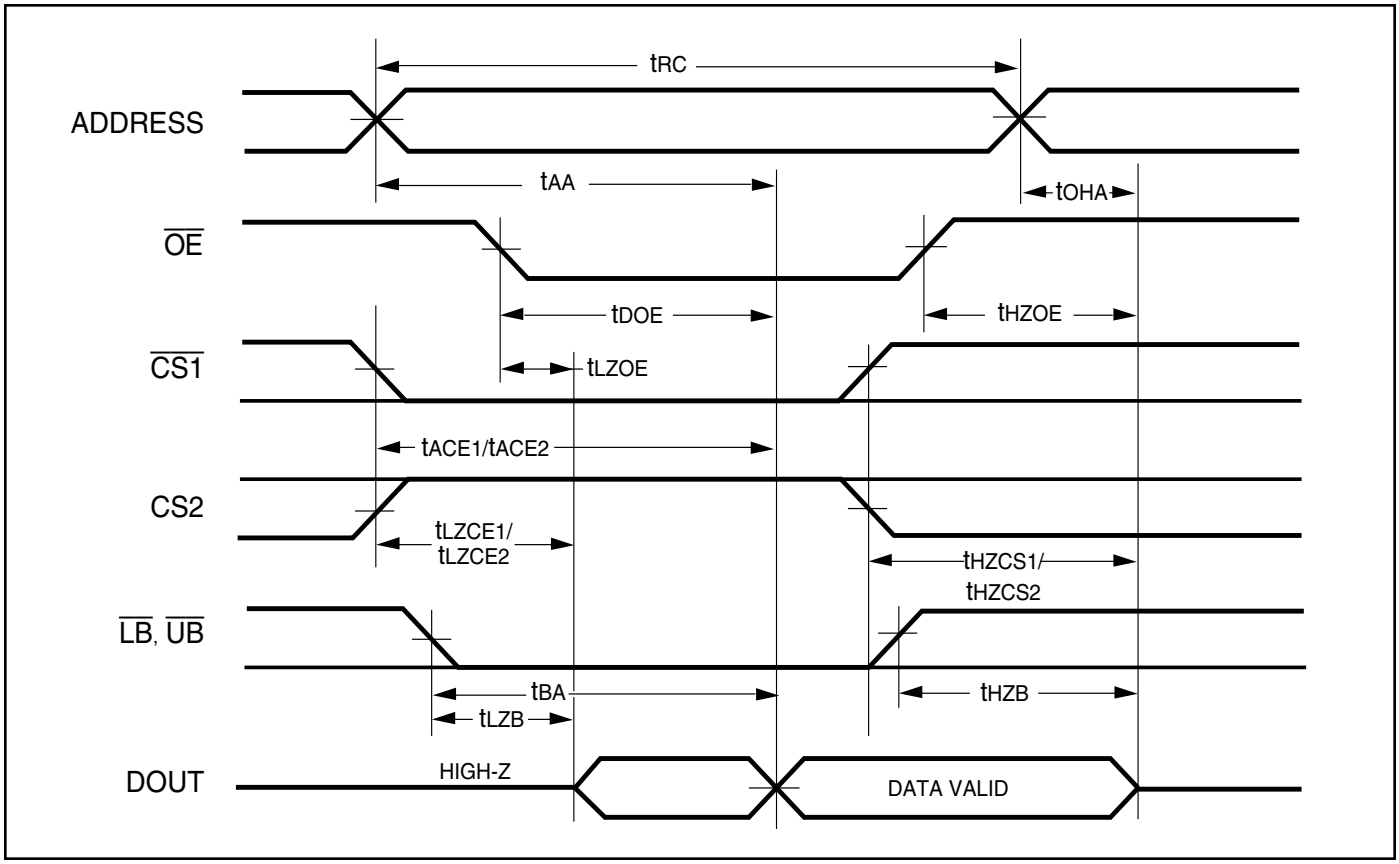
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

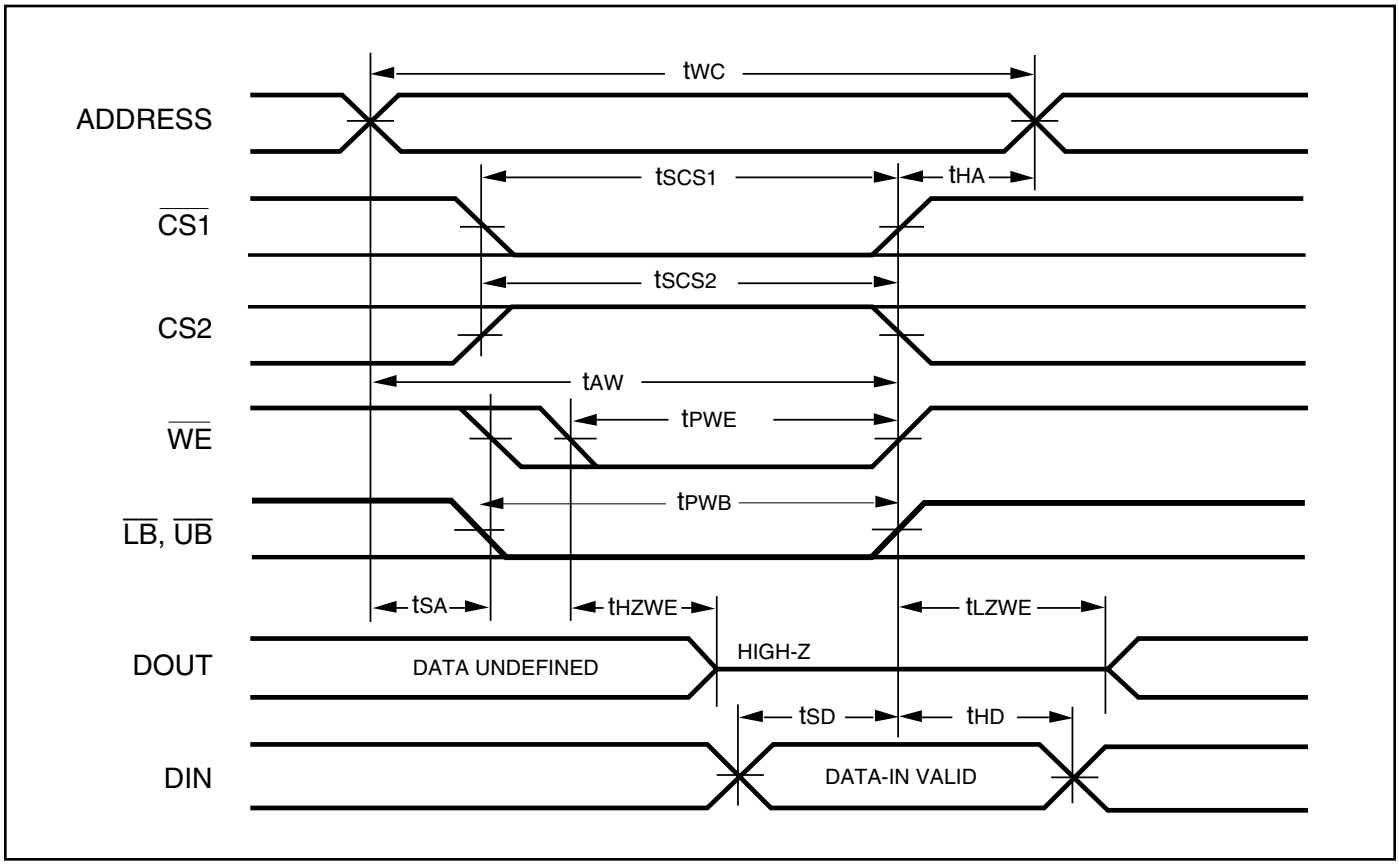
Symbol	Parameter	35 ns Min.	35 ns Max.	45 ns Min.	45 ns Max.	55 ns Min.	55 ns Max.	Unit
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	25	—	35	—	45	—	ns
t_{AW}	Address Setup Time to Write End	25	—	35	—	45	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	30	—	35	—	45	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	30	—	35	—	40	—	ns
t_{SD}	Data Setup to Write End	15	—	20	—	25	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	20	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

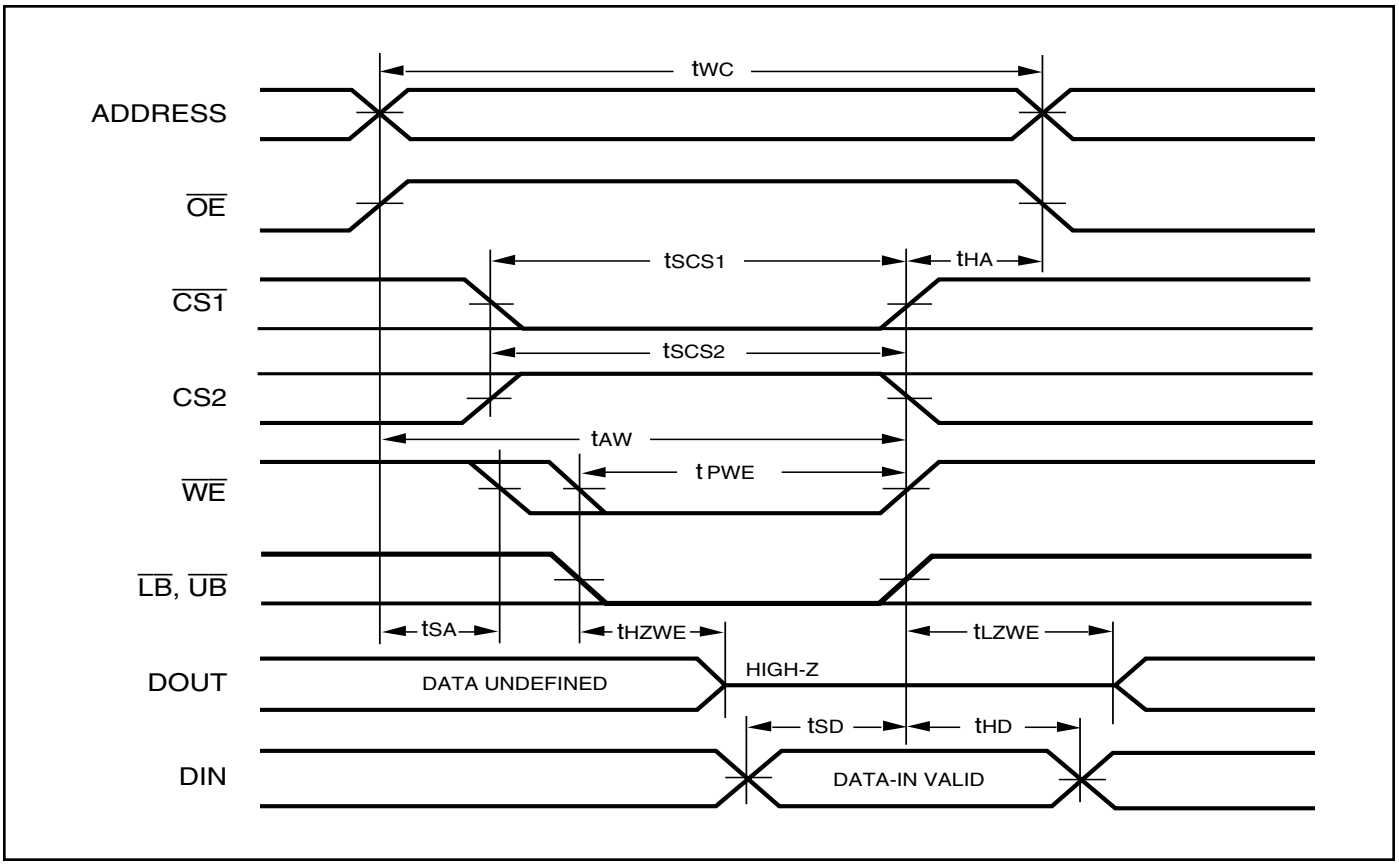
WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS1}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

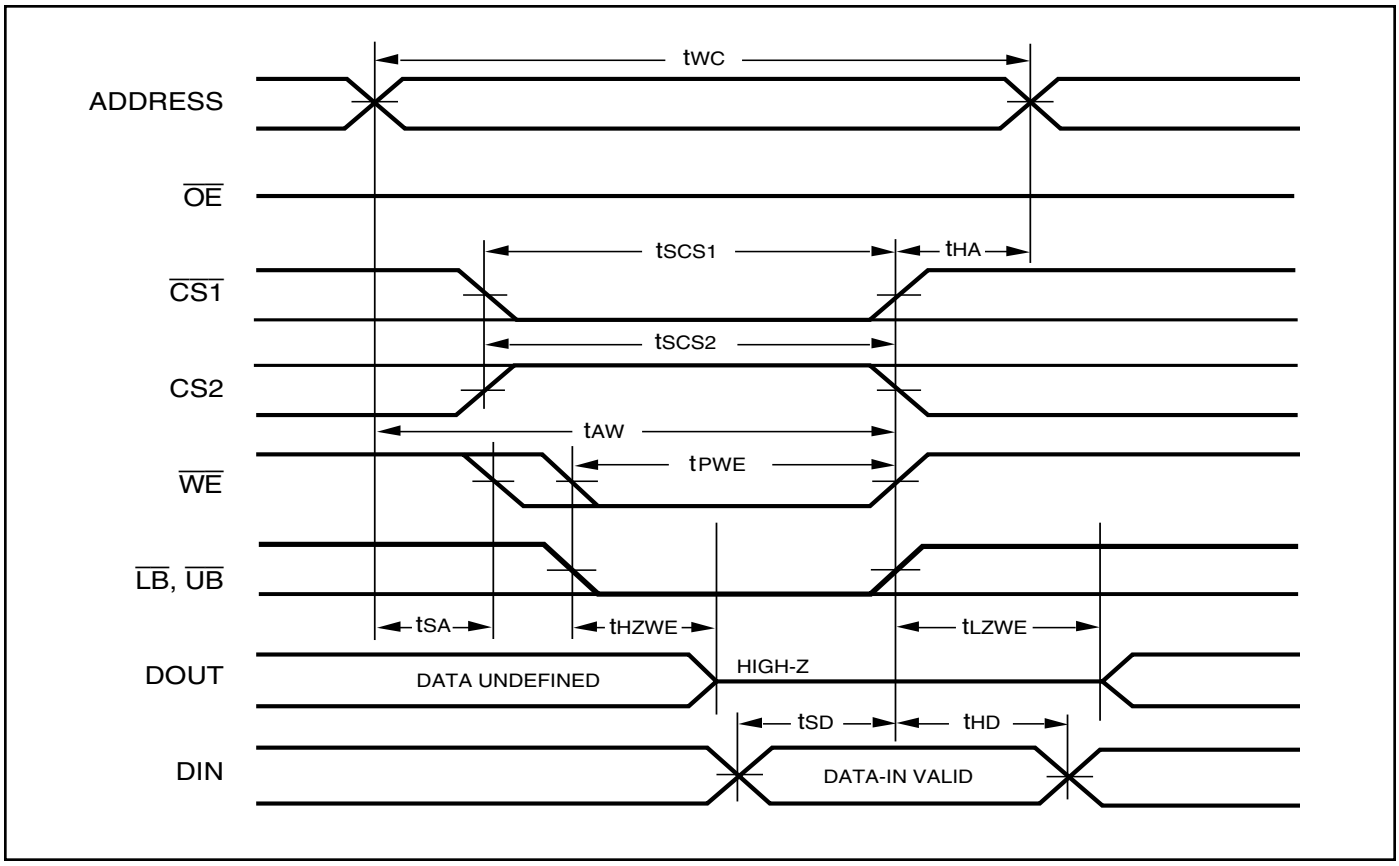
AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



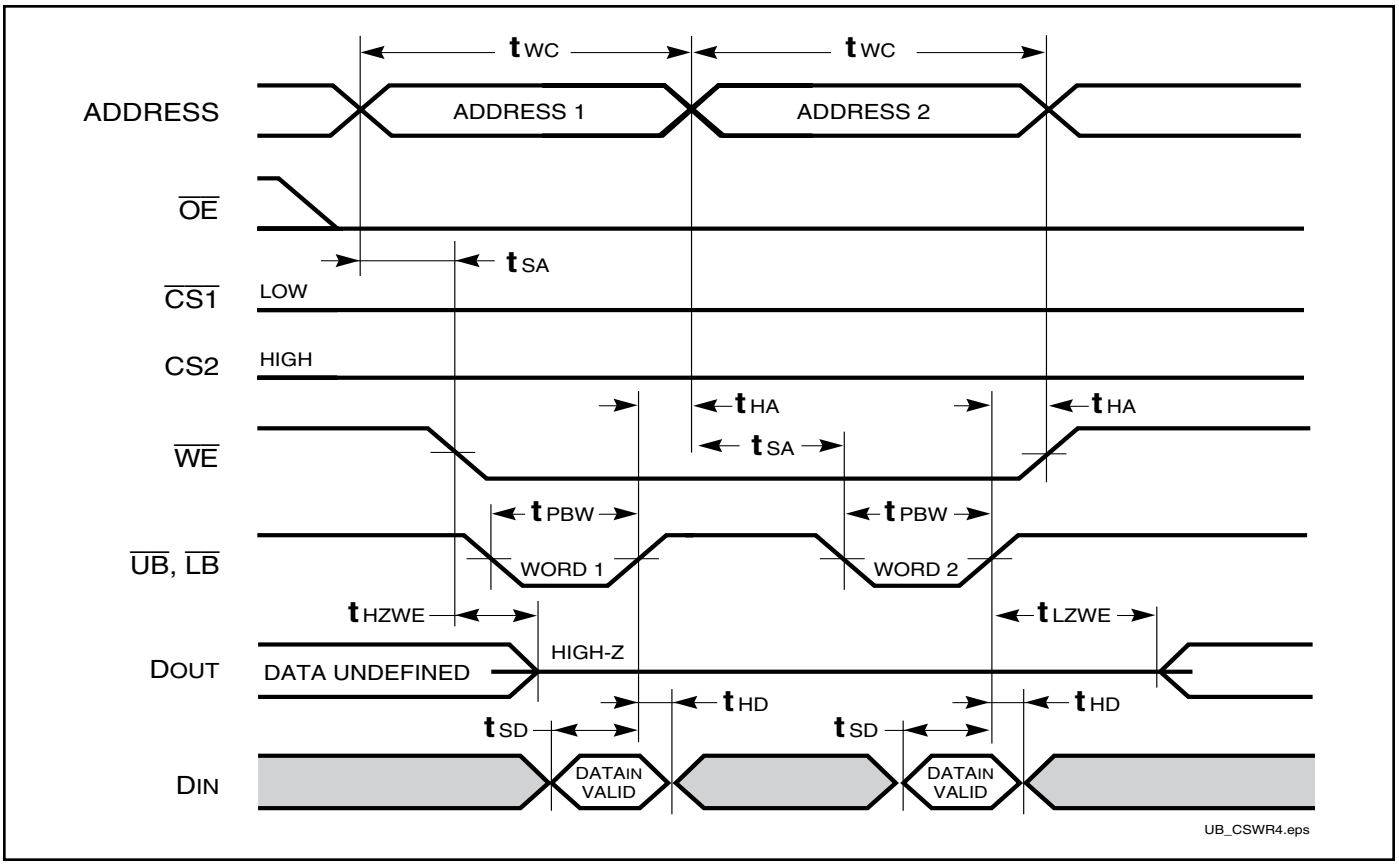
AC WAVEFORMS

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)

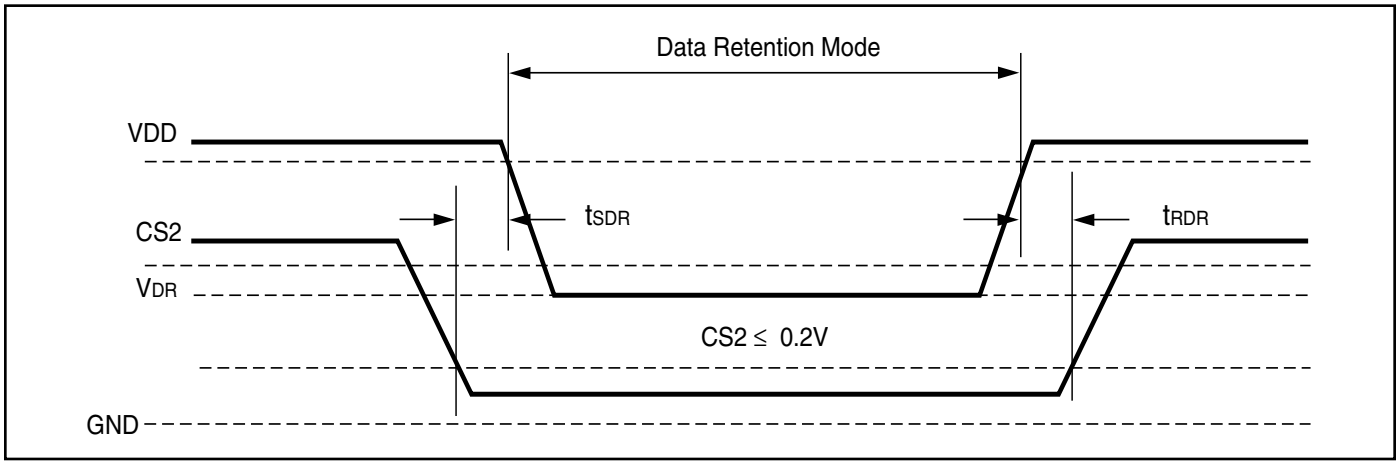


DATA RETENTION SWITCHING CHARACTERISTICS

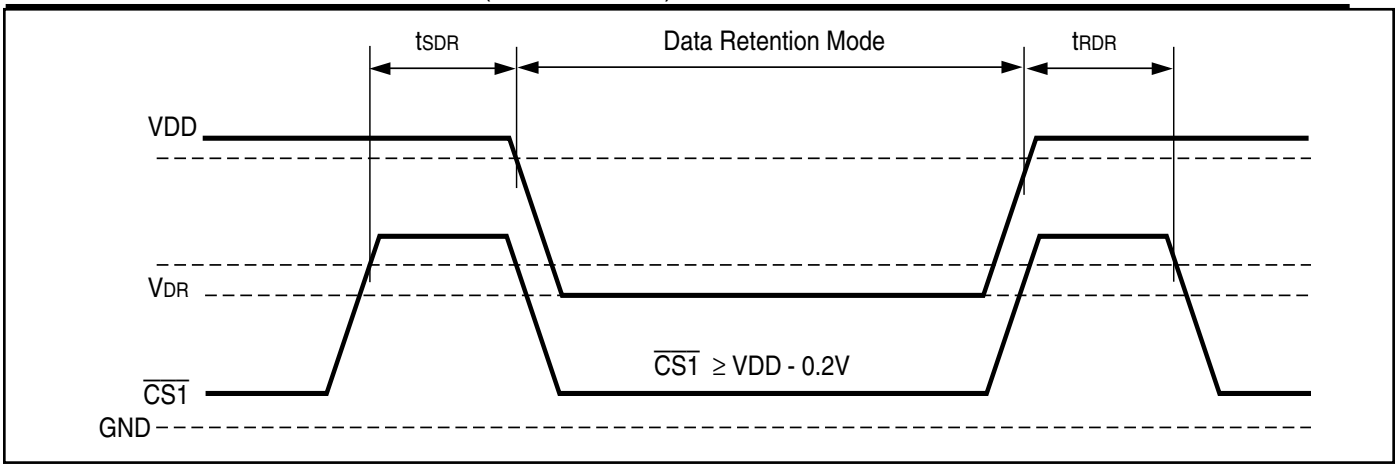
Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.5	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = V_{DR}$(min),	Com.	—	4	µA
		(1) 0V ≤ CS2 ≤ 0.2V, or	Ind.	—	6	µA
		(2) $\overline{CS1} \geq V_{DD} - 0.2V$, CS2 ≥ V_{DD} - 0.2V or	Auto.	—	20	µA
		(3) $\overline{LB}$ and $\overline{UB} \geq V_{DD}$ -0.2V, $\overline{CS1} \leq 0.2V$, CS2 ≥ V_{DD} - 0.2V	typ.[2]	2		µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns	
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns	

Note:
1. Typical values are measured at $V_{DD} = V_{DR}$(min), T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (CS2 Controlled)

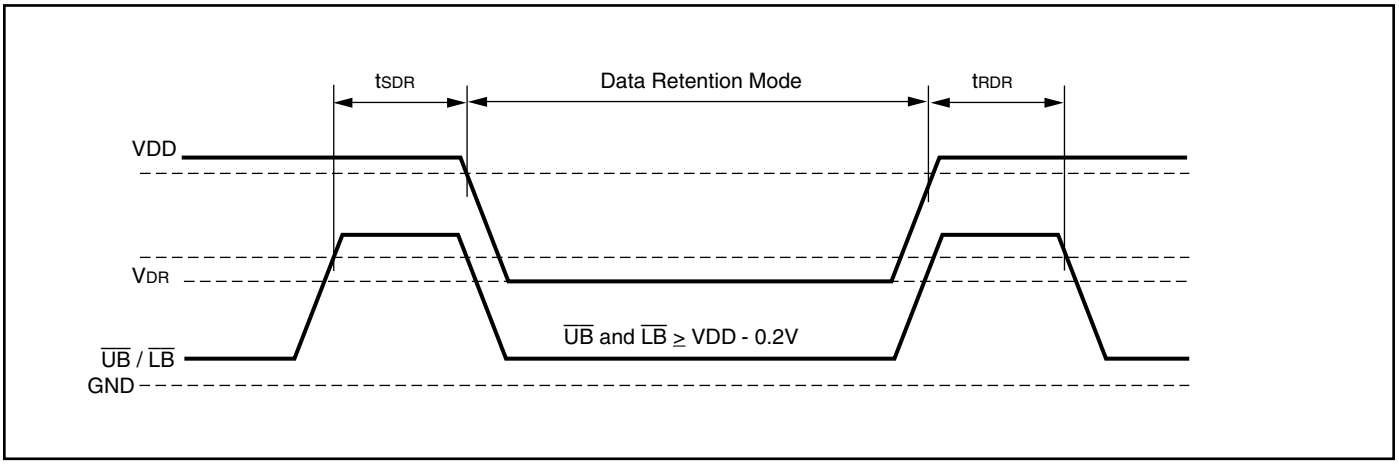


DATA RETENTION WAVEFORM (CS1Controlled)



Note:
1. CS2 must satisfy either CS2 ≥ Vcc -0.2V or CS2 ≤ 0.2V

DATA RETENTION WAVEFORM ($\overline{UB}$and $\overline{LB}$ Controlled)



Note:
1. CS2 must satisfy either CS2 ≥ Vcc -0.2V or CS2 ≤ 0.2V
2. $\overline{CS1}$ must satisfy either CS1 ≥ Vcc -0.2V or CS1 ≤ 0.2V

ORDERING INFORMATION: IS62WV12816DALL (1.65V - 2.2V)
Industrial Range: –40°C to +85°C

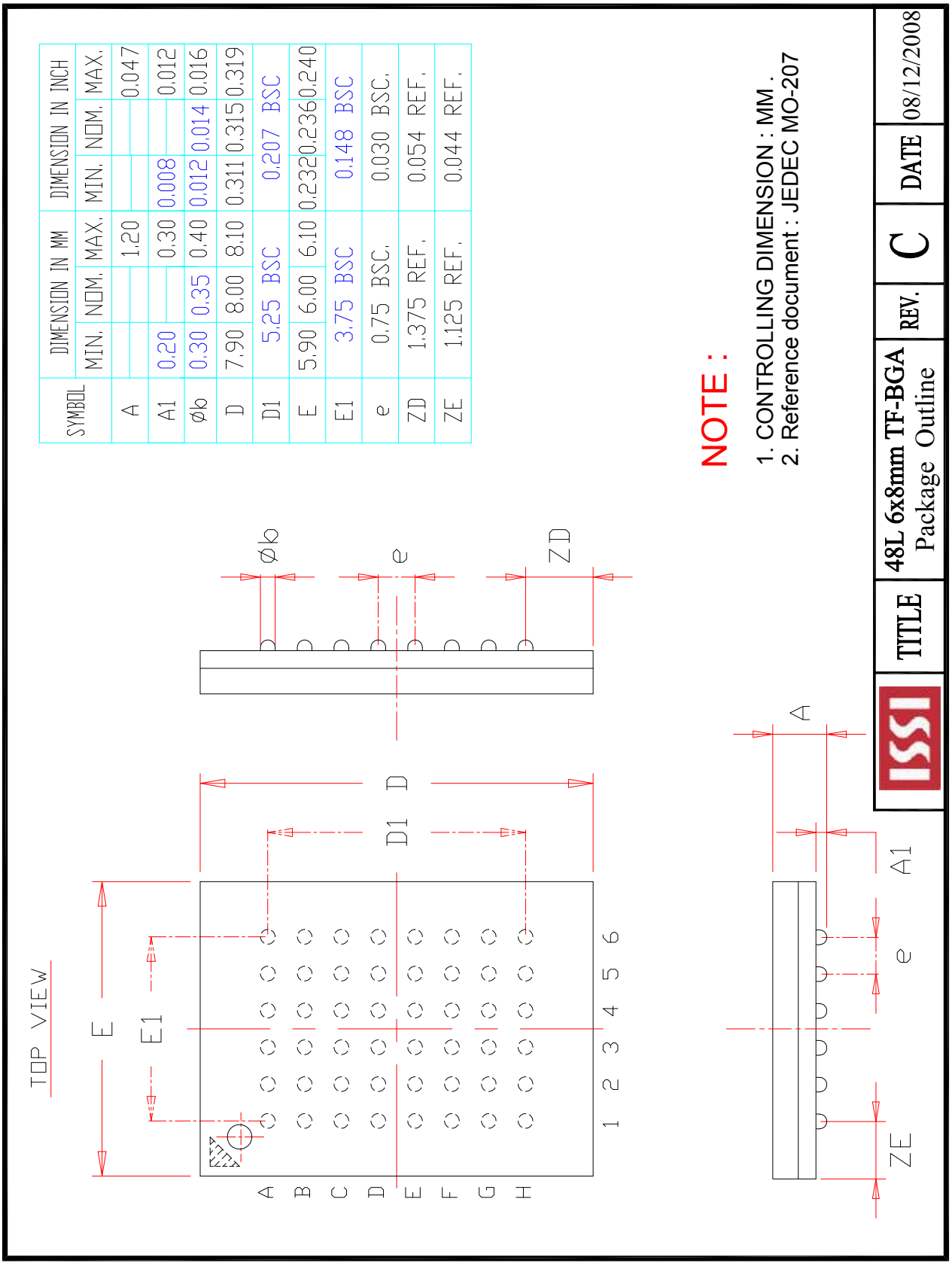
Speed (ns)	Order Part No.	Package
55	IS62WV12816DALL-55TI	TSOP (Type II)
	IS62WV12816DALL-55BI	mini BGA (6mm x 8mm)
	IS62WV12816DALL-55BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DALL-55B2I	mini BGA (6mm x 8mm), 2 CS Option

ORDERING INFORMATION: IS62WV12816DBLL (2.5V - 3.6V)
Industrial Range: –40°C to +85°C

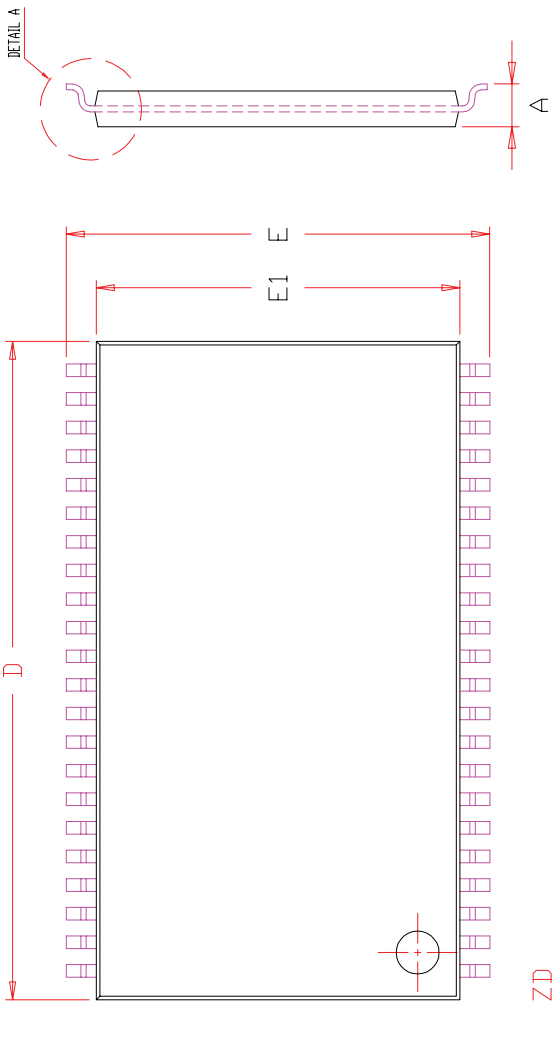
Speed (ns)	Order Part No.	Package
35	IS62WV12816DBLL-35TLI	TSOP (Type II), Lead-free
	IS62WV12816DBLL-35BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DBLL-35B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free
45	IS62WV12816DBLL-45TLI	TSOP (Type II), Lead-free
	IS62WV12816DBLL-45BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DBLL-45B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free
55	IS62WV12816DBLL-55TI	TSOP (Type II)
	IS62WV12816DBLL-55TLI	TSOP (Type II), Lead-free
	IS62WV12816DBLL-55BI	mini BGA (6mm x 8mm)
	IS62WV12816DBLL-55BLI	mini BGA (6mm x 8mm), Lead-free
	IS62WV12816DBLL-55B2I	mini BGA (6mm x 8mm), 2 CS Option
	IS62WV12816DBLL-55B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

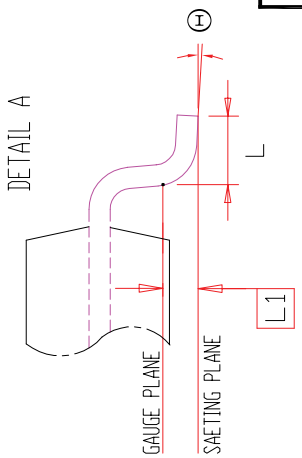
ORDERING INFORMATION: IS65WV12816DBLL (2.5V - 3.6V)
Automotive Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
45	IS65WV12816DBLL-45CTLA3	TSOP (Type II), Lead-free, Copper Leadframe
	IS65WV12816DBLL-45BLA3	mini BGA (6mm x 8mm), Lead-free


SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
øb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207
TOP VIEW
E
E1
D
D1
øb
e
ZD
A
A1
ZE
1 2 3 4 5 6
A B C D E F G H
TITLE
48L 6x8mm TF-BGA Package Outline
REV.
C
DATE
08/12/2008

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
θ	0	—	8°	0	—	8°





NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	REV.	DATE
ISSI	44L 400mil TSOP-2 Package Outline	F	06/04/2008