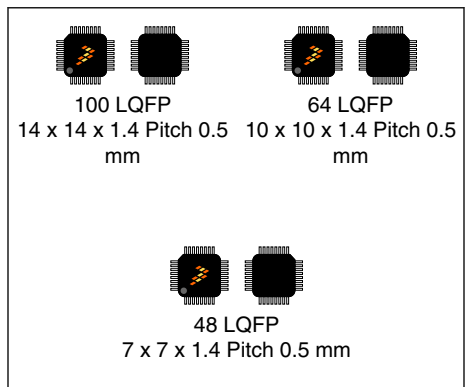


KV4X Data Sheet

150 MHz ARM Cortex-M4 core based Microcontroller with FPU

The Kinetis KV4x MCU family is a member of the Kinetis V series and provides a high-performance solution for 3-phase BLDC, PMSM and ACIM motor control as well as Digital Power Conversion. Built upon the ARM® Cortex®-M4 core operating at 150 MHz with DSP and floating point unit, features include; dual 12-bit analog-to-digital converters with 240ns conversion time, up to 30 PWM channels for support of multi-motor systems, eFlexPWM module with 260ps resolution for digital power conversion applications, programmable delay block, memory protection unit, dual FlexCAN modules and 64 to 256 KB of flash memory. KV4x MCUs are offered in 48LQFP, 64LQFP, and 100LQFP packages. All Kinetis V series MCUs are supported by a comprehensive enablement suite from Freescale and third-party resources including reference designs, software libraries and motor configuration tools.

MKV46FxxxVLY15
MKV45FxxxVLY15
MKV44FxxxVLY15
MKV43FxxxVLY15
MKV41FxxxVLY15
MKV40FxxxVLY15



Core

- ARM® Cortex®-M4 core up to 150 MHz with single precision Floating Point Unit (FPU)

Memories

- Up to 256 KB of program flash memory
- Up to 32 KB of RAM

System peripherals

- 16-channel DMA controller
- Low-leakage wakeup unit
- SWD interface and Micro Trace buffer
- Advanced independent clocked watchdog

Clocks

- 32 to 40 kHz or 3 to 32 MHz crystal oscillator
- Multipurpose clock generator (MCG) with frequency-locked loop and phase-locked loop referencing either internal or external reference clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Temperature range: -40 to 105 °C

Human-machine interface

- General-purpose input/output

Communication interfaces

- Two Universal Asynchronous Receiver/Transmitter (UART) / FlexSCI modules with programmable 8- or 9-bit data format
- One 16-bit SPI module
- One I2C module
- Two FlexCAN modules

Analog Modules

- Two 12-bit cyclic ADCs
- Four analog comparator (CMP) containing a 6-bit DAC and programmable reference input
- One 12-bit DAC

Timers

- One eFlexPWM with 4 sub-modules, providing 12 PWM outputs
- Two 8-channel FlexTimers (FTM0 and FTM3)
- One 2-channel FlexTimers (FTM1)
- Four Periodic interrupt timers (PIT)
- Two Programmable Delay Blocks (PDB)
- Quadrature Encoder/Decoder (ENC)

Security and integrity modules

- Hardware CRC module to support fast cyclic redundancy checks
- External Watchdog Monitor (EWM)

This document contains information on a new product. Specifications and information herein are subject to change without notice. © 2014 Freescale Semiconductor, Inc. All rights reserved.

Preliminary



NOTE

The 48-pin LQFP package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

Ordering Information

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MKV46F256VLL15	256	32	74
MKV46F256VLH15	256	32	48
MKV46F128VLL15	128	24	74
MKV46F128VLH15	128	24	48
MKV45F256VLL15	256	32	74
MKV45F256VLH15	256	32	48
MKV45F128VLL15	128	24	74
MKV45F128VLH15	128	24	48
MKV44F128VLL15	128	24	74
MKV44F128VLH15	128	24	48
MKV44F128VLF15	128	24	38
MKV44F64VLH15	64	16	48
MKV44F64VLF15 ¹	64	16	38
MKV43F128VLL15	128	24	74
MKV43F128VLH15	128	24	48
MKV43F128VLF15 ¹	128	24	38
MKV43F64VLH15	64	16	48
MKV43F64VLF15 ¹	64	16	38
MKV41F128VLF15 ¹	128	24	38
MKV41F64VLF15 ¹	64	16	38
MKV40F256VLL15	256	32	74
MKV40F256VLH15	256	32	48
MKV40F128VLL15	128	24	74
MKV40F128VLH15	128	24	48
MKV40F128VLF15 ¹	128	24	38
MKV40F64VLH15	64	16	48
MKV40F64VLF15 ¹	64	16	38

1. Package Your Way

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KV4XPB ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KV4XP100M150RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KV4XP100M150 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_V_0N72K ¹
Package drawing	Package dimensions are provided in package drawings.	<ul style="list-style-type: none"> LQFP 100-pin: 98ASS23308W¹ LQFP 64-pin: 98ASS23234W¹ LQFP 48-pin: 98ASH00962A¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

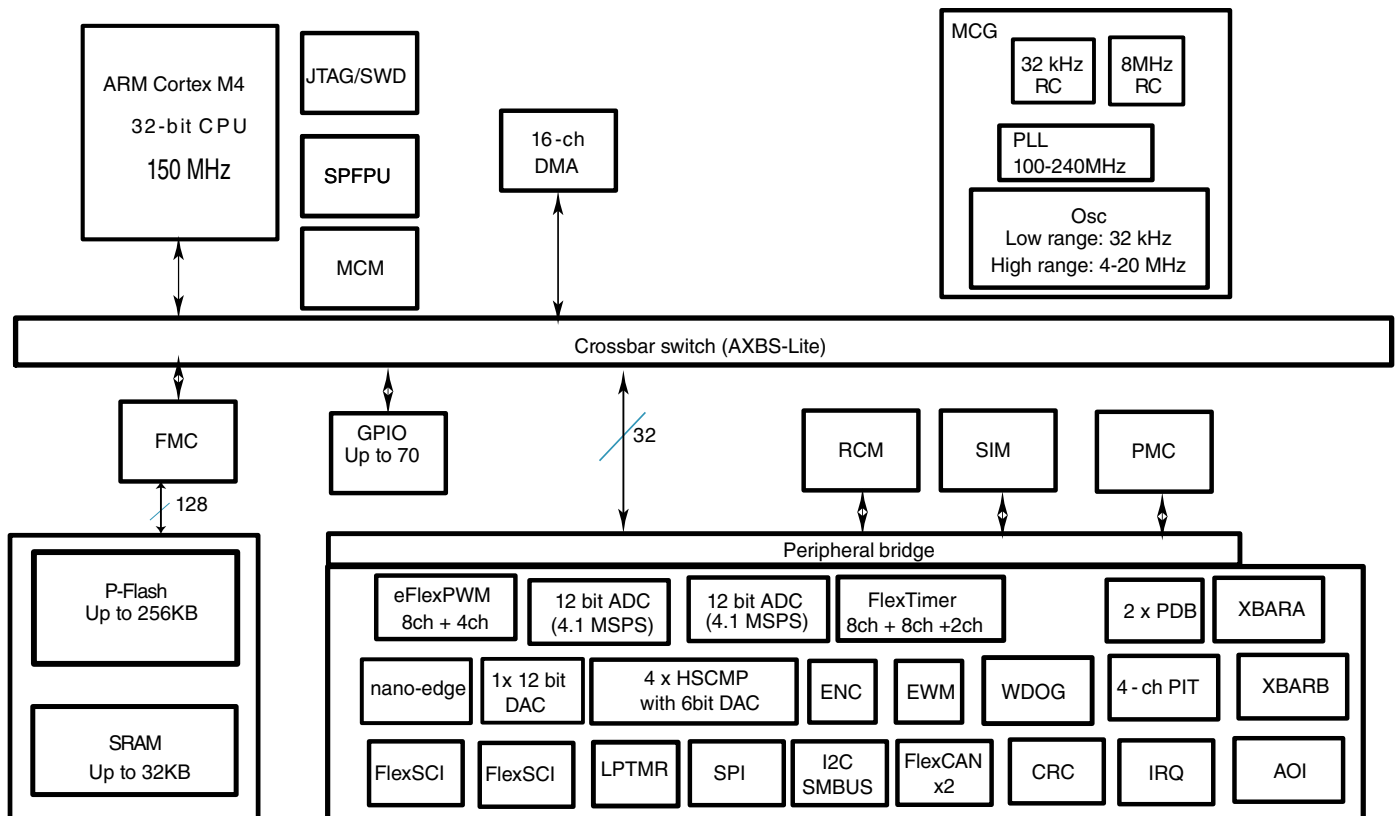


Figure 1. KV4x block diagram



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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human-body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-up Test*.

1.4 Voltage and current operating ratings

Ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	Digital pin input voltage (except open drain pins)	-0.3	$V_{DD} + 0.3^1$	V
	Open drain pins (PTC6 and PTC7)	-0.3	5.5	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Maximum value of V_{IO} (except open drain pins) must be 3.8 V.

1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 1](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 1. Absolute Maximum Ratings ($V_{SS} = 0$ V, $V_{SSA} = 0$ V)

Symbol	Description	Notes ¹	Min	Max	Unit
V_{DD}	Supply Voltage Range		-0.3	4.0	V
V_{DDA}	Analog Supply Voltage Range		-0.3	4.0	V
V_{REFHx}	ADC High Voltage Reference		-0.3	4.0	V
V_{REFLx}	ADC Low Voltage Reference		-0.3	0.3	V
ΔV_{DD}	Voltage difference V_{DD} to V_{DDA}		-0.3	0.3	V
ΔV_{SS}	Voltage difference V_{SS} to V_{SSA}		-0.3	0.3	V
V_{IN}	Digital Input Voltage Range	Pin Groups 1, 2	-0.3	4.0	V
V_{OSC}	Oscillator Input Voltage Range	Pin Group 4	-0.4	4.0	V
V_{INA}	Analog Input Voltage Range	Pin Group 3	-0.3	4.0	V
I_{IC}	Input clamp current, per pin ($V_{IN} < 0$)		—	-20.0	mA
I_{OC}	Output clamp current, per pin ($V_O < 0$) ²		—	-20.0	mA
V_{OUT}	Output Voltage Range (Normal Push-Pull mode)	Pin Group 1	-0.3	4.0	V
V_{OUTOD}	Output Voltage Range (Open Drain mode)	Pin Group 2	-0.3	5.5	V
V_{OUT_DAC}	DAC Output Voltage Range	Pin Group 5	-0.3	4.0	V
T_A	Ambient Temperature Industrial		-40	105	°C
T_{STG}	Storage Temperature Range (Extended Industrial)		-55	150	°C

1. Default Mode

- Pin Group 1: GPIO, TDI, TDO, TMS, TCK
- Pin Group 2: RESET, PORTC6, and PORTC7
- Pin Group 3: ADC and Comparator Analog Inputs

- Pin Group 4: XTAL, EXTAL
 - Pin Group 5: DAC analog output
2. Continuous clamp current per pin is -2.0 mA

2 General

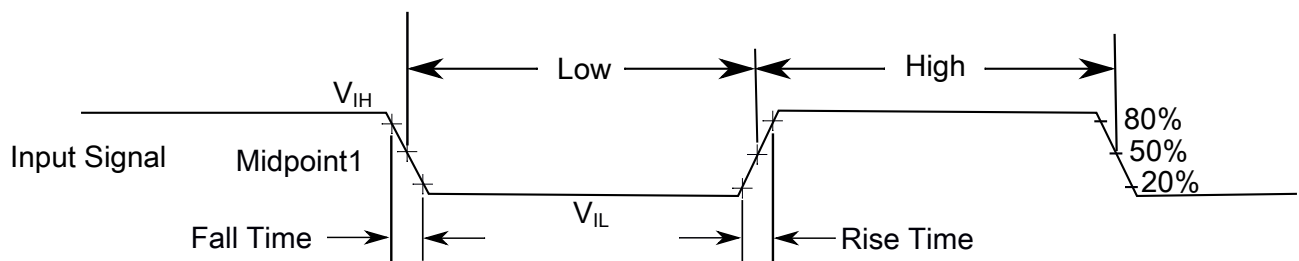
Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on freescale.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



$$\text{The midpoint is } V_{IL} + (V_{IH} - V_{IL}) / 2$$

Figure 2. Input signal measurement reference



General

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are slew rate disabled, and
 - are normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Recommended Operating Conditions

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 2. Recommended Operating Conditions ($V_{REFLX}=0V$, $V_{SSA}=0V$, $V_{SS}=0V$)

Symbol	Description	Notes ¹	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Digital		1.8		3.6	V
V_{DDA}	Supply voltage (analog)		2.7	3.0	3.6	V
V_{REFHx}	ADC (Cyclic) Reference Voltage High		2.7		V_{DDA}	V
ΔV_{DD}	Voltage difference V_{DD} to V_{DDA}		-0.1	0	0.1	V
ΔV_{SS}	Voltage difference V_{SS} to V_{SSA}		-0.1	0	0.1	V
F_{MCGOUT}	Device Clock Frequency		0.04		150	MHz
T	<ul style="list-style-type: none"> • using internal RC oscillator • using external clock source 		0		150	
V_{IH}	Input Voltage High (digital inputs)	Pin Groups 1, 2	$0.7 \times V_{DD}$		3.6	V
V_{IL}	Input Voltage Low (digital inputs)	Pin Groups 1, 2			$0.35 \times V_{DD}$	V
V_{IHOSC}	Oscillator Input Voltage High XTAL driven by an external clock source	Pin Group 4	2.0		$V_{DD} + 0.3$	V
V_{ILOSC}	Oscillator Input Voltage Low	Pin Group 4	-0.3		0.8	V
C_{out}	DAC Output Current Drive Strength	Pin Group 5			1	mA
I_{OH}	Output Source Current High (at V_{OH} min.)	Pin Group 1	—		-2	mA
	<ul style="list-style-type: none"> • Programmed for low drive strength • Programmed for high drive strength 	Pin Group 6, 7	—		-18	
I_{OL}	Output Source Current Low (at V_{OL} max.) ²	Pin Groups 1, 2	—		2	mA
	<ul style="list-style-type: none"> • Programmed for low drive strength • Programmed for high drive strength 	Pin Groups 6	—		18	
T_A	Ambient Operating Temperature		-40		105	°C

Table continues on the next page...

Table 2. Recommended Operating Conditions ($V_{REFLX}=0V$, $V_{SSA}=0V$, $V_{SS}=0V$) (continued)

Symbol	Description	Notes ¹	Min	Typ	Max	Unit
N_F	Flash Endurance (Program Erase Cycles)	$T_A = -40^{\circ}C$ to $105^{\circ}C$	10K		—	cycles
T_R	Flash Data Retention	$T_J \leq 85^{\circ}C$ avg	15		—	years
t_{FLRET}	Flash Data Retention with < 100 Program/ Erase Cycles	$T_J \leq 85^{\circ}C$ avg	25	—	—	years

1. Default Mode

- Pin Group 1: GPIO, TDI, TDO, TMS, TCK
- Pin Group 2: \overline{RESET}
- Pin Group 3: ADC and Comparator Analog Inputs
- Pin Group 4: XTAL, EXTAL
- Pin Group 5: DAC analog output
- Pin Group 6: PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4. have high output current capability
- Pin Group 7: PTC6 and PTC7 are true open drain pins and have no P-chanl transistor. A external pull-up resistor is required when these pins are outputs.

2. Total chip source or sink current cannot exceed 75 mA.

2.2.2 LVD and POR operating requirements

Table 3. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	± 80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	± 60	—	mV	

Table continues on the next page...

Table 3. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 PORT Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Notes ¹	Min	Typ	Max	Unit	Test Conditions
V _{OH} ²	Output Voltage High	Pin Group 1	V _{DD} - 0.5	—	—	V	I _{OH} = I _{OHmax}
V _{OL}	Output Voltage Low	Pin Groups 1, 2	—	—	0.5	V	I _{OL} = I _{OLmax}
I _{IH}	Digital Input Current High pull-up enabled or disabled	Pin Groups 1, 2	—	0	+/- 2.5	μA	V _{IN} = 2.4V to 5.5V
I _{IHC}	Comparator Input Current High	Pin Group 3	—	0	+/- 2	μA	V _{IN} = V _{DDA}
I _{IHOSC}	Oscillator Input Current High	Pin Group 3	—	0	+/- 2	μA	V _{IN} = V _{DDA}
I _{IL}	Digital Input Current Low • pull-up enabled • pull-up disabled	Pin Groups 1, 2	TBD TBD	TBD TBD	TBD TBD	μA	V _{IN} = 0V
R _{Pull-Up}	Internal Pull-Up Resistance		20	—	50	kΩ	—
I _{ILC}	Comparator Input Current Low	Pin Group 3	—	0	+/- 2	μA	V _{IN} = 0V
I _{ILOSC}	Oscillator Input Current Low	Pin Group 3	—	0	+/- 2	μA	V _{IN} = 0V
V _{DAC}	DAC Output Voltage Range	Pin Group 5	Typically V _{SSA} + 40mV	—	Typically V _{DDA} - 40mV	V	R _{LD} = 3 kΩ C _{LD} = 400 pf
I _{OZ}	Output Current ¹ High Impedance State	Pin Groups 1, 2	—	0	+/- 2.5	μA	—
V _{HYS}	Schmitt Trigger Input Hysteresis	Pin Groups 1, 2	—	0.06 x V _{DD}	—	V	—
C _{IN}	Input Capacitance		—	10	—	pF	—
C _{OUT}	Output Capacitance		—	10	—	pF	—

1. Default Mode

- Pin Group 1: GPIO, TDI, TDO, TMS, TCK

- Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
 - Pin Group 3: ADC and Comparator Analog Inputs
 - Pin Group 4: XTAL, EXTAL
 - Pin Group 5: DAC
2. PTC6 and PTC7 are true open drain so have no high drive output transistor so there is no V_{OH} spec for them. These pins must be terminated with a pull-up resistor to V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	
	• $VLLS0 \rightarrow \text{RUN}$	—	—	139	μs	
	• $VLLS1 \rightarrow \text{RUN}$	—	—	139	μs	
	• $VLLS3 \rightarrow \text{RUN}$	—	—	76	μs	
	• $VLPS \rightarrow \text{RUN}$	—	—	5.3	μs	
	• $\text{STOP} \rightarrow \text{RUN}$	—	—	5.3	μs	

2.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors (All I_{DDs} are Target values)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	16.7	50	mA	ADC/DAC powered on

Table continues on the next page...

Table 6. Power consumption operating behaviors (All IDD's are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
						and clocked at 5 MHz.
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA <ul style="list-style-type: none"> @ 1.8V @ 3.0V 	—	6.5	14	mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 25 MHz
		—	6.6	15	mA	
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA <ul style="list-style-type: none"> @ 1.8V @ 3.0V 	—	9.6	18	mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 50 MHz
		—	9.8	20	mA	
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA <ul style="list-style-type: none"> @ 1.8V @ 3.0V 	—	16.1	18	mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 100 MHz.
		—	16.2	20	mA	
I _{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA <ul style="list-style-type: none"> @ 1.8V @ 3.0V 	—	25.3	50	mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 150 MHz.
		—	25.7	60	mA	
I _{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from flash,excludes ADC IDDA <ul style="list-style-type: none"> @ 1.8V @ ambient @ 3.0V <ul style="list-style-type: none"> @ 25°C @ 105°C 	—	33.7	90	mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 150 MHz. Nanoedge module at 75 MHz.
		—	33.1	100	mA	
		—	39.6	120	mA	
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	8.6	—	mA	
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.574	—	mA	CPU freq 4Mhz
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.836	—	mA	CPU freq 4Mhz
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.285	—	mA	2Mhz bus frequency
I _{DD_STOP}	Stop mode current at 3.0 V	—	0.366	2		

Table continues on the next page...

Table 6. Power consumption operating behaviors (All IDD's are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.868	TBD	mA	
		—	3.5	TBD	mA	
		—			mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.059	TBD	μA	
		—	—	TBD	μA	
		—	0.717	TBD	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.124	TBD	mA	
		—	3.8	TBD	mA	
		—	—	TBD	mA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	0.122	TBD	mA	
		—	3.7	TBD	mA	
		—	4.1	TBD	mA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	749	TBD	nA	
		—	2.2	TBD	μA	
		—	9.9	TBD	μA	
I _{DD_VLLS0B}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	470	TBD	nA	
		—	1.9	TBD	μA	
		—	9.5	TBD	μA	
I _{DD_VLLS0A}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> • @ -40 to 25°C • @ 70°C • @ 105°C 	—	180	TBD	nA	
		—	1.6	TBD	μA	
		—	9.1	TBD	μA	

Table 7. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IREFSTEN4MHZ}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I _{IREFSTEN32KHZ}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I _{EREFSTEN4MHZ}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	μA
I _{EREFSTEN32KHZ}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1							
	VLLS3	440	490	540	560	570	580	
	LLS	440	490	540	560	570	580	
	VLPS	490	490	540	560	570	680	
	STOP	510	560	560	560	610	680	
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							μA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled

- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

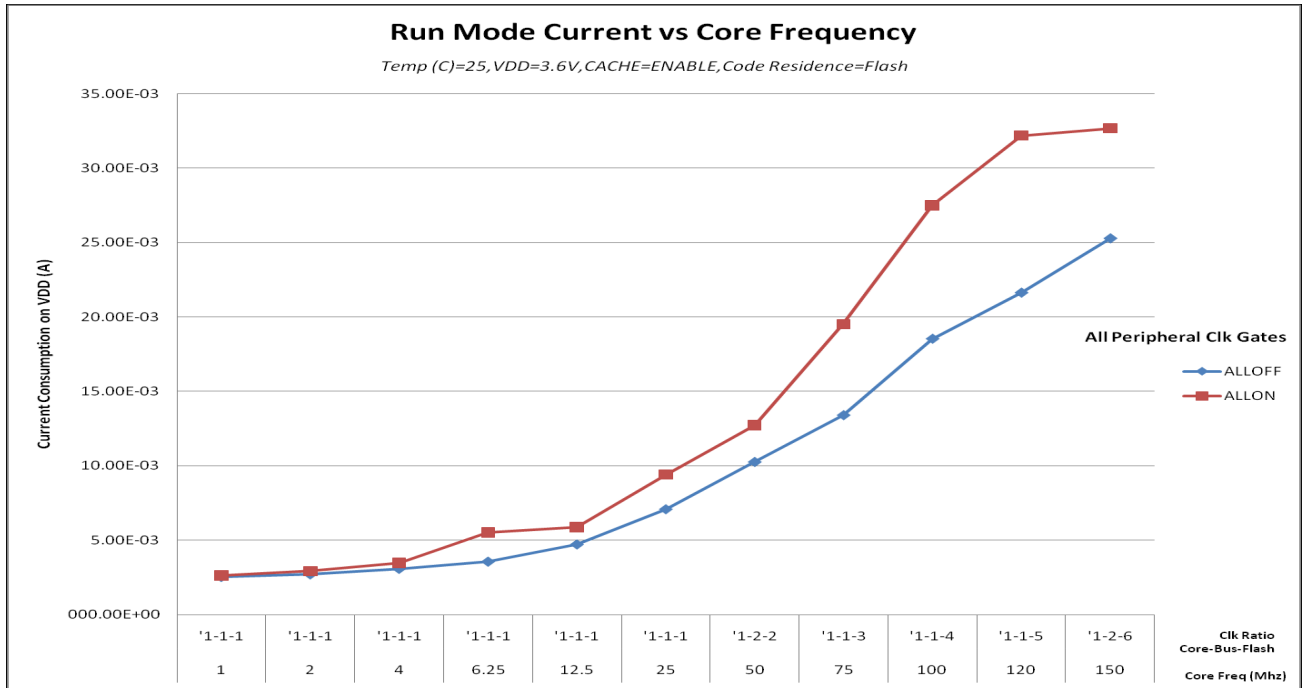


Figure 3. Run mode supply current vs. core frequency

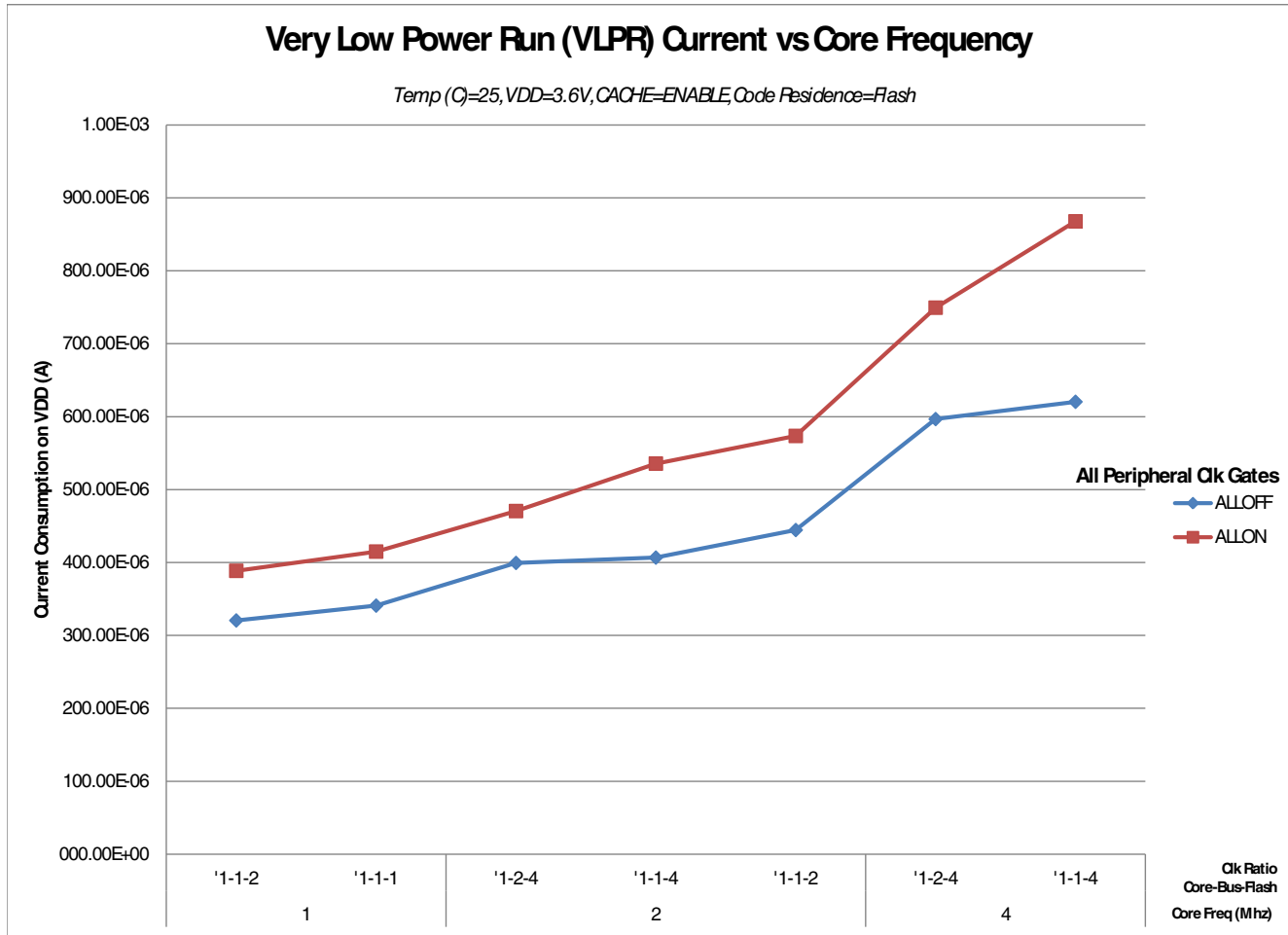


Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	15	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	17	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	12	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	4	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code.

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, $f_{OSC} = 10\text{ MHz}$ (crystal), $f_{SYS} = 75\text{ MHz}$, $f_{BUS} = 25\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Typical device clock specifications

Table 10. Typical device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	72	MHz	
f_{BUS}	Bus and Flash clock	—	24	MHz	
f_{FPCK}	Fast peripheral clock	—	72	MHz	
f_{NANO}	Nano-edge clock	—	144	MHz	
Low Speed RUN mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{BUS}	Bus and Flash clock	—	25	MHz	
f_{FPCK}	Fast peripheral clock	—	100	MHz	
f_{NANO}	Nano-edge clock	—	200	MHz	

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I²C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time				3
	Fast slew rate				
	1.71 ≤ VDD ≤ 2.7 V	—	8	ns	
	2.7 ≤ VDD ≤ 3.6 V	—	7	ns	
	Port rise and fall time				
	Slow slew rate				
	1.71 ≤ VDD ≤ 2.7 V	—	25	ns	
	2.7 ≤ VDD ≤ 3.6 V	—	15	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T _J	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C

2.4.2 Thermal attributes

Table 13. Thermal attributes

Board type	Symbol	Description	100 LQFP	64 LQFP	48 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	62	64	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	49	46	57	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	52	68	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	43	39	51	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	28	35	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	17	15	25	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	2	7	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 14. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation			

Table continues on the next page...

Table 14. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

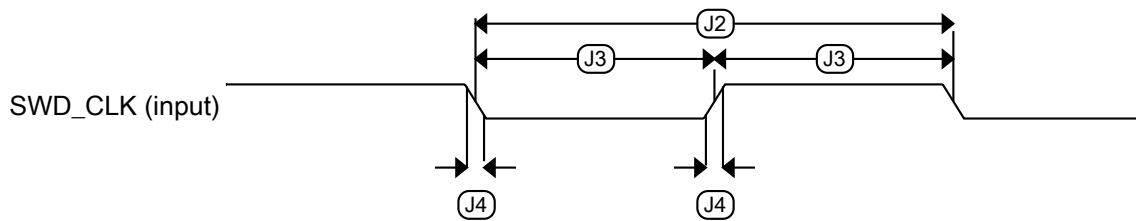


Figure 5. Serial wire clock input timing

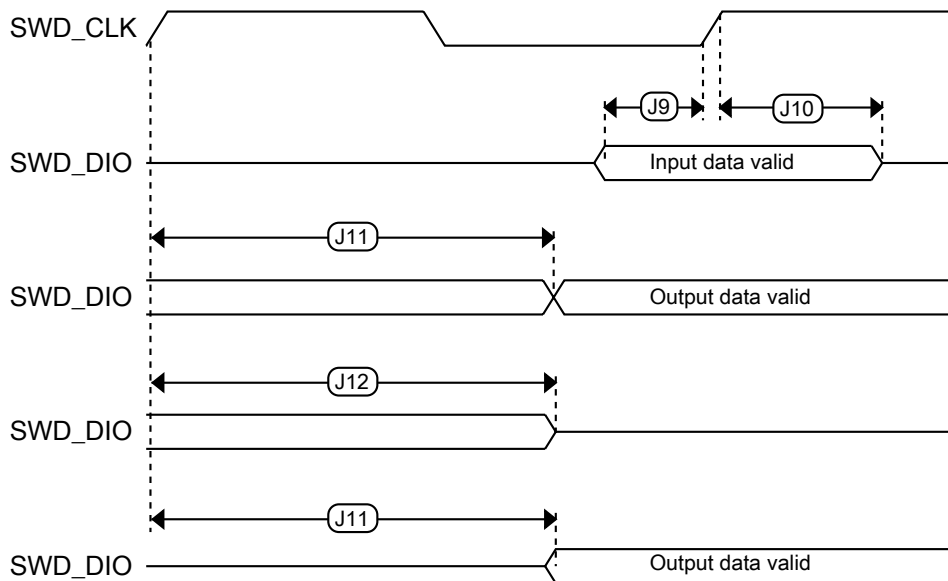


Figure 6. Serial wire data timing

3.1.2 Debug trace timing specifications

Table 15. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	1.5	ns
T_h	Data hold	2	1.0	ns

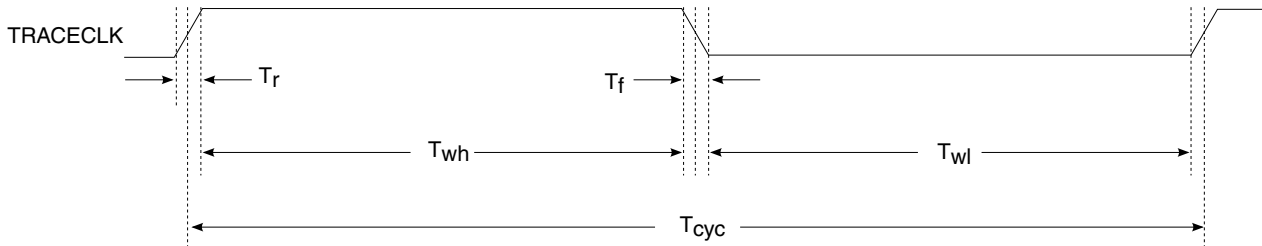


Figure 7. TRACE_CLKOUT specifications

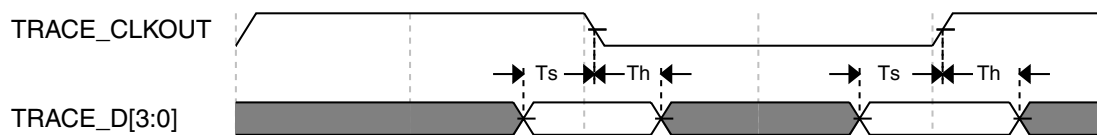


Figure 8. Trace data specifications

3.1.3 JTAG electricals

Table 16. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
		0	25	

Table continues on the next page...

Table 16. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	<ul style="list-style-type: none"> JTAG and CJTAG Serial Wire Debug 	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	<ul style="list-style-type: none"> Boundary Scan 	50	—	ns
	<ul style="list-style-type: none"> JTAG and CJTAG 	20	—	ns
	<ul style="list-style-type: none"> Serial Wire Debug 	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 17. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	<ul style="list-style-type: none"> Boundary Scan 	0	10	
	<ul style="list-style-type: none"> JTAG and CJTAG 	0	20	
	<ul style="list-style-type: none"> Serial Wire Debug 	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	<ul style="list-style-type: none"> Boundary Scan 	50	—	ns
	<ul style="list-style-type: none"> JTAG and CJTAG 	25	—	ns
	<ul style="list-style-type: none"> Serial Wire Debug 	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns

Table continues on the next page...

Table 17. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

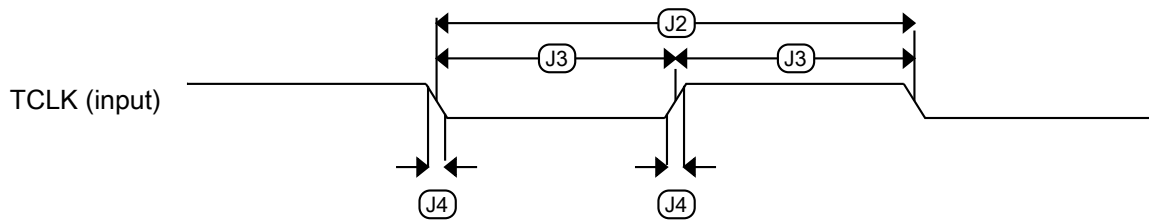


Figure 9. Test clock input timing

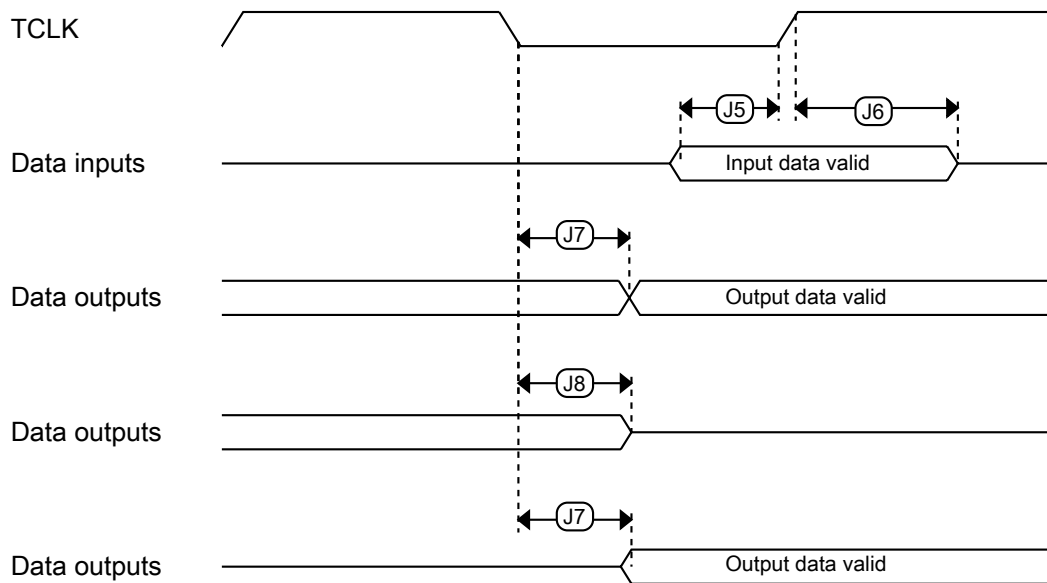


Figure 10. Boundary scan (JTAG) timing

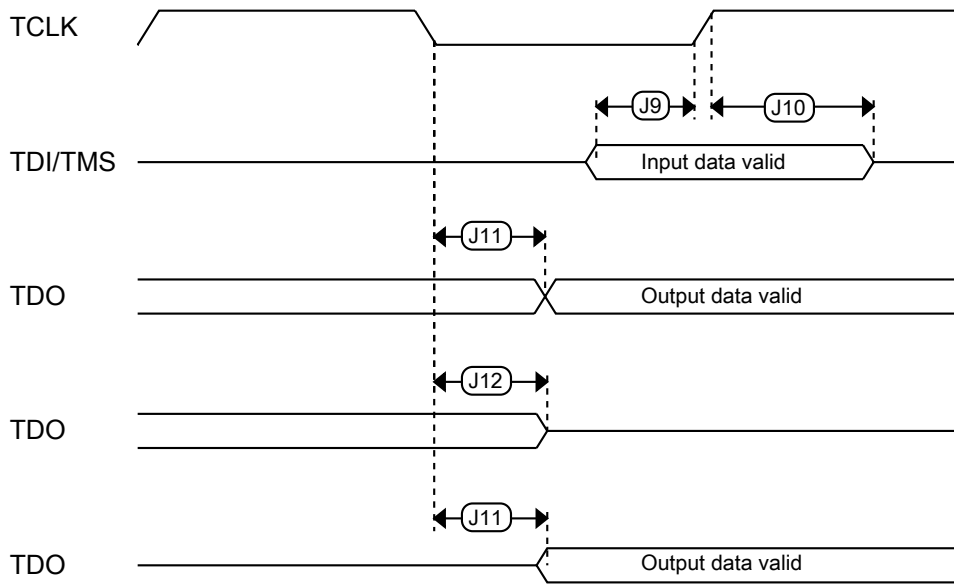


Figure 11. Test Access Port timing

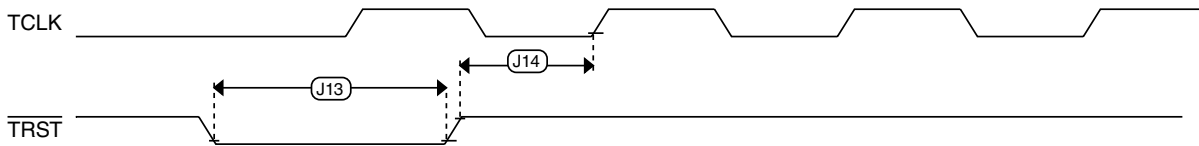


Figure 12. TRST timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz		
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1	
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	$\%f_{dco}$	1	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	—	± 1	$\%f_{dco}$	1	
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz		
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz		
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints_t}$	—	—	kHz		
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints_t}$	—	—	kHz		
FLL							
f_{fil_ref}	FLL reference frequency range	31.25	—	39.0625	kHz		
f_{dco}	DCO output frequency range	Low range (DRS=00) $640 \times f_{fil_ref}$	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) $1280 \times f_{fil_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fil_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fil_ref}$	80	83.89	100	MHz	
$f_{dco_t_DMX3}$ 2	DCO output frequency	Low range (DRS=00) $732 \times f_{fil_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fil_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fil_ref}$	—	71.99	—	MHz	
		High range (DRS=11)	—	95.98	—	MHz	

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	$2929 \times f_{\text{fill_ref}}$					
$J_{\text{cyc_fll}}$	FLL period jitter <ul style="list-style-type: none"> $f_{\text{DCO}} = 48 \text{ MHz}$ $f_{\text{DCO}} = 98 \text{ MHz}$ 	—	180	—	ps	
$t_{\text{fill_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL						
$f_{\text{pll_ref}}$	PLL reference frequency range	8	—	16	MHz	
$f_{\text{vcoclk_2x}}$	VCO output frequency	180	—	360	MHz	
f_{vcoclk}	PLL output frequency	90	—	180	MHz	
$f_{\text{vcoclk_90}}$	PLL quadrature output frequency	90	—	180	MHz	
I_{pll}	PLL operating current <ul style="list-style-type: none"> VCO @ 176 MHz ($f_{\text{osc_hi_1}} = 32 \text{ MHz}$, $f_{\text{pll_ref}} = 8 \text{ MHz}$, VDIV multiplier = 22) 	—	2.8	—	mA	7
I_{pll}	PLL operating current <ul style="list-style-type: none"> VCO @ 360 MHz ($f_{\text{osc_hi_1}} = 32 \text{ MHz}$, $f_{\text{pll_ref}} = 8 \text{ MHz}$, VDIV multiplier = 45) 	—	4.7	—	mA	7
$J_{\text{cyc_pll}}$	PLL period jitter (RMS) <ul style="list-style-type: none"> $f_{\text{vco}} = 48 \text{ MHz}$ $f_{\text{vco}} = 120 \text{ MHz}$ 	—	120	—	ps	8
$J_{\text{acc_pll}}$	PLL accumulated jitter over 1 μs (RMS) <ul style="list-style-type: none"> $f_{\text{vco}} = 48 \text{ MHz}$ $f_{\text{vco}} = 120 \text{ MHz}$ 	—	1350	—	ps	8
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
$t_{\text{pll_lock}}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{\text{pll_ref}})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{\text{dco_t}}$) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz • 16 MHz • 24 MHz • 32 MHz 	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I _{DDOSC}	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> • 4 MHz • 8 MHz • 16 MHz • 24 MHz • 32 MHz 	—	400	—	μA	1
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}^5	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	μ s	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec4k}$	Read 1s Section execution time (flash sector)	—	—	60	μ s	1
t_{pgmchk}	Program Check execution time	—	—	45	μ s	1
t_{rdsrc}	Read Resource execution time	—	—	30	μ s	1
t_{pgm4}	Program Longword execution time	—	65	145	μ s	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	—
t_{rdonce}	Read Once execution time	—	—	25	μ s	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μ s	—
t_{ersall}	Erase All Blocks execution time	—	500	3000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μ s	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmpretp10k}	Data retention after up to 10 K cycles	5	50	—	years	—
t _{nvmpretp1k}	Data retention after up to 1 K cycles	20	100	—	years	—
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 12-bit cyclic Analog-to-Digital Converter (ADC) parameters

Table 25. 12-bit ADC electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage	V _{DDA}	2.7	3.3	3.6	V
V _{refh} Supply Voltage	V _{refhx}	2.7		V _{DDA}	V
ADC Conversion Clock	f _{ADCCLK}	0.6		25	MHz
Conversion Range	R _{AD}	V _{REFL}		V _{REFH}	V

Table continues on the next page...

Table 25. 12-bit ADC electrical specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V_{ADIN}	V_{REFL}		V_{REFH}	V
External Reference		V_{SSA}		V_{DDA}	
Internal Reference					
Timing and Power					
Conversion Time	t_{ADC}		6		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block)	I_{ADRUN}		1		mA
<ul style="list-style-type: none"> at 600 kHz ADC Clock, LP mode ≤ 8.33 MHz ADC Clock, 00 mode ≤ 12.5 MHz ADC Clock, 01 mode ≤ 16.67 MHz ADC Clock, 10 mode ≤ 20 MHz ADC Clock, 11 mode ≤ 25 MHz ADC Clock 			5.7		
			10.5		
			17.7		
			22.6		
			TBD		
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.02		μA
V_{REFH} Current	I_{VREFH}		0.001		μA
Accuracy (DC or Absolute)					
Integral non-Linearity	I_{NL}		+/- 3	+/- 5	LSB
Differential non-Linearity ¹	DNL		+/- 0.6	+/- 0.9	LSB ²
Monotonicity					
Offset	V_{OFFSET}			+/- 17	mV
<ul style="list-style-type: none"> 1x gain mode 2x gain mode 4x gain mode 				+/- 20	
				+/- 25	
Gain Error	E_{GAIN}		0.801 to 0.809	0.798 to 0.814	
AC Specifications					
Signal to Noise Ratio	SNR		59		dB
Total Harmonic Distortion	THD		64		dB
Spurious Free Dynamic Range	SFDR		65		dB
Signal to Noise plus Distortion	SINAD		59		dB
Effective Number of Bits	ENOB		9.5		bits
ADC Inputs					
Input Leakage Current	I_{IN}		0	+/-2	μA
Input Injection Current	I_{INJ}			+/-3	mA
Input Capacitance	C_{ADI}		4.8		pF
Sampling Capacitor					

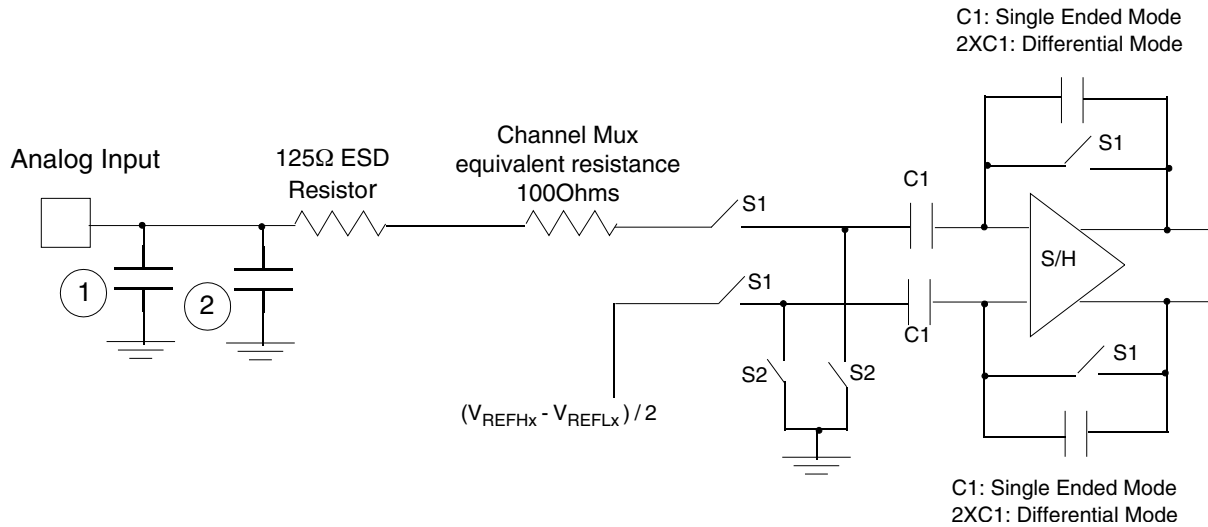
 1. I_{NL} measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

2. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting

3.6.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100\text{ohm} + 125\text{ohm}$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. Sampling capacitor at the sample and hold circuit. Capacitor C1 (4.8pF) is normally disconnected from the input, and is only connected to the input at sampling time.
4. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

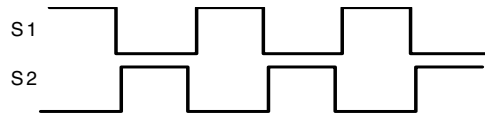


Figure 13. Equivalent circuit for A/D loading

3.6.2 CMP and 6-bit DAC electrical specifications

Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	μ A
I_{DDL5}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	μ A
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to $V_{DD} - 0.7$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

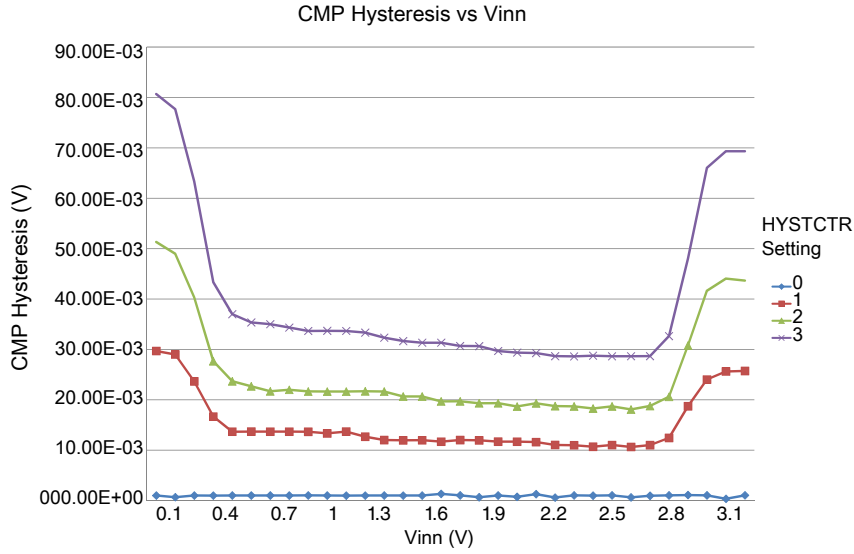


Figure 14. Typical hysteresis vs. Vin level ($V_{DD} = 3.3\text{ V}$, $P_{MODE} = 0$)

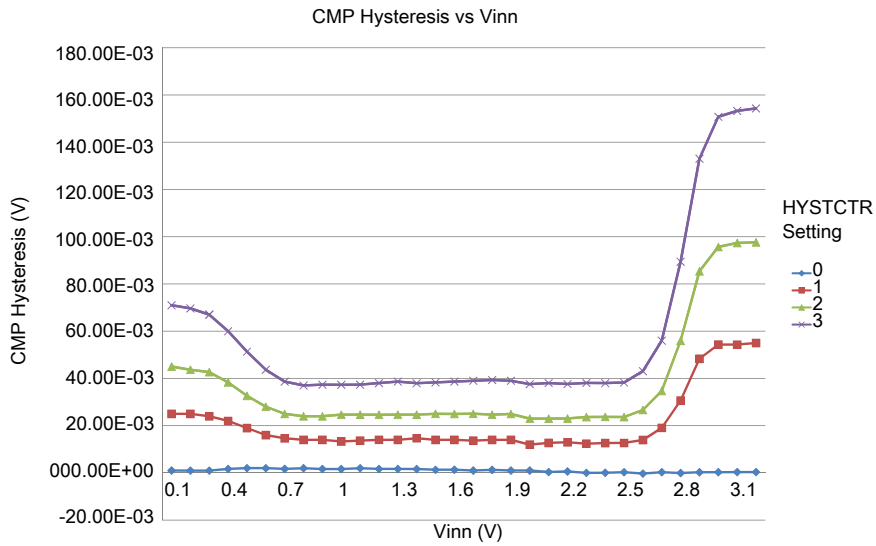


Figure 15. Typical hysteresis vs. Vin level ($V_{DD} = 3.3\text{ V}$, $P_{MODE} = 1$)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 27. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 28. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μ A	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μ A	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μ s	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μ s	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) <ul style="list-style-type: none"> • High-speed mode • Low speed mode 	—	1	5	μ s	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4$ V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μ V/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 k Ω)	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h	—	—	—	V/ μ s	

Table continues on the next page...

Table 28. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	1.2	1.7	—		
		0.05	0.12	—		
BW	3dB bandwidth				kHz	
	<ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	550	—	—		
		40	—	—		

1. Settling within ± 1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4$ V
5. Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
6. $V_{DDA} = 3.0$ V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

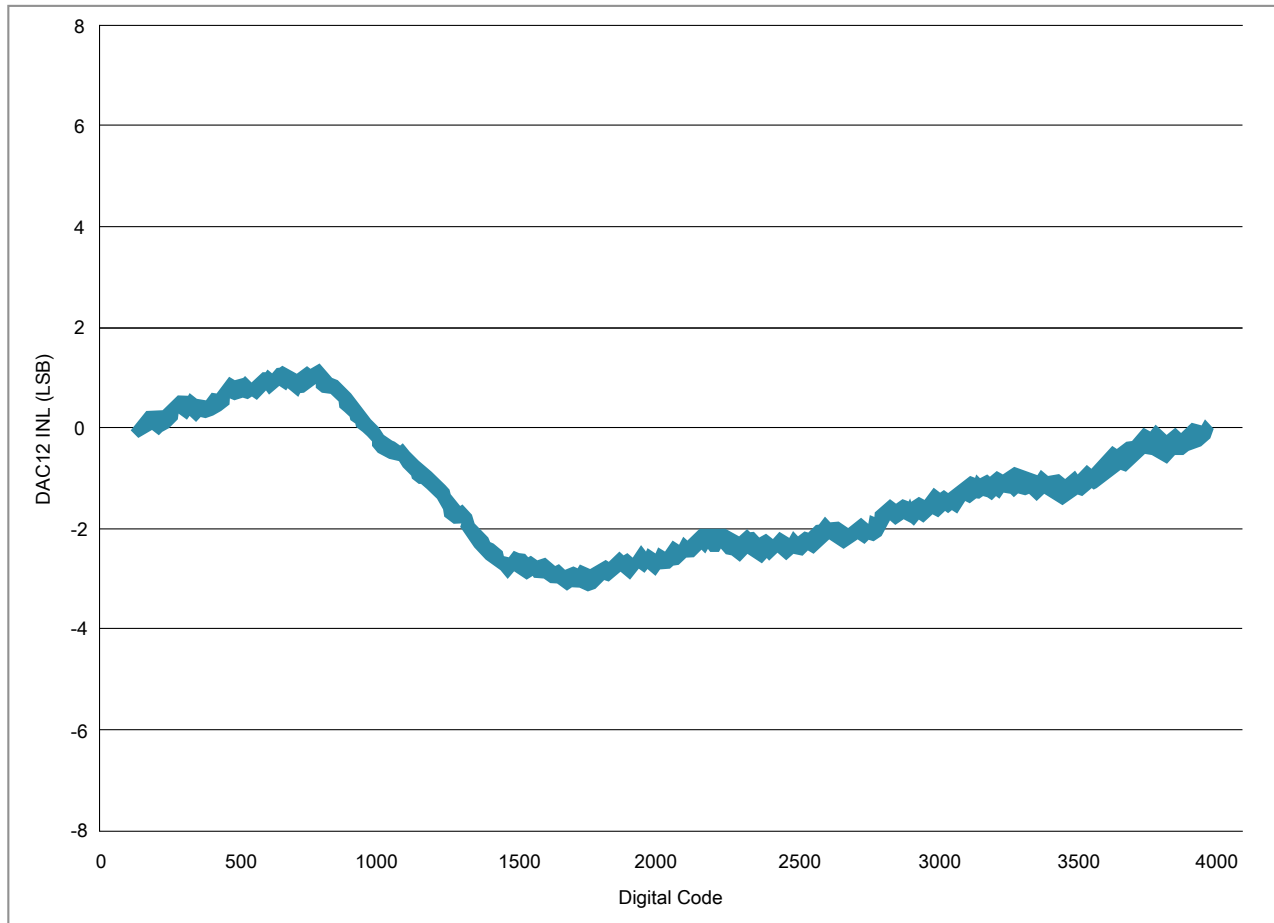


Figure 16. Typical INL error vs. digital code

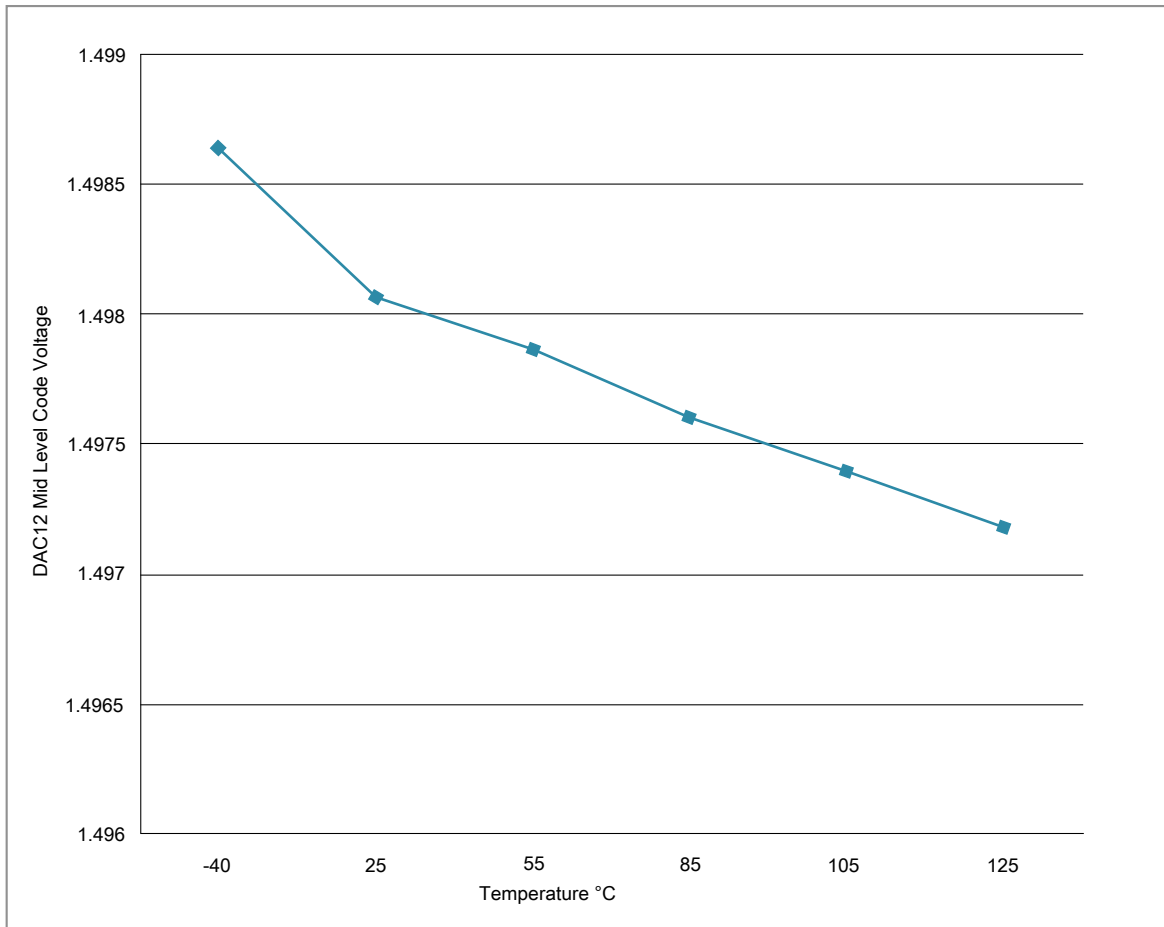


Figure 17. Offset at half scale vs. temperature

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces



3.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

NOTE

Fast pads:

- SIN: PTE19
- SOUT: PTE18
- SCK: PTE17
- PCS: PTE16

Open drain pads:

- SIN: PTC7
- SOUT: PTC6

Table 29. Master mode DSPI timing for normal pads (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCS _n to DSPI_SCK output valid	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS _n output hold	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 30. Master mode DSPI timing for fast pads (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	37.5	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	

Table continues on the next page...

Table 30. Master mode DSPI timing for fast pads (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCS n to DSPI_SCK output valid	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS n output hold	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	13	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPI x _CTAR n [PSSCK] and SPI x _CTAR n [CSSCK].
2. The delay is programmable in SPI x _CTAR n [PASC] and SPI x _CTAR n [ASC].

Table 31. Master mode DSPI timing for open drain pads (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCS n to DSPI_SCK output valid	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS n output hold	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	15.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-3	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPI x _CTAR n [PSSCK] and SPI x _CTAR n [CSSCK].
2. The delay is programmable in SPI x _CTAR n [PASC] and SPI x _CTAR n [ASC].

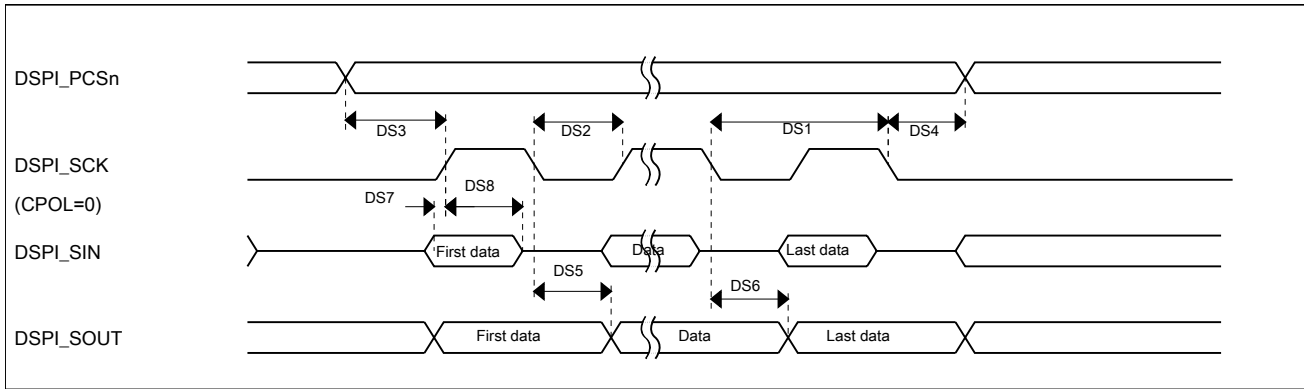


Figure 18. DSPI classic SPI timing — master mode

Table 32. Slave mode DSPI timing for normal pads (limited voltage range)

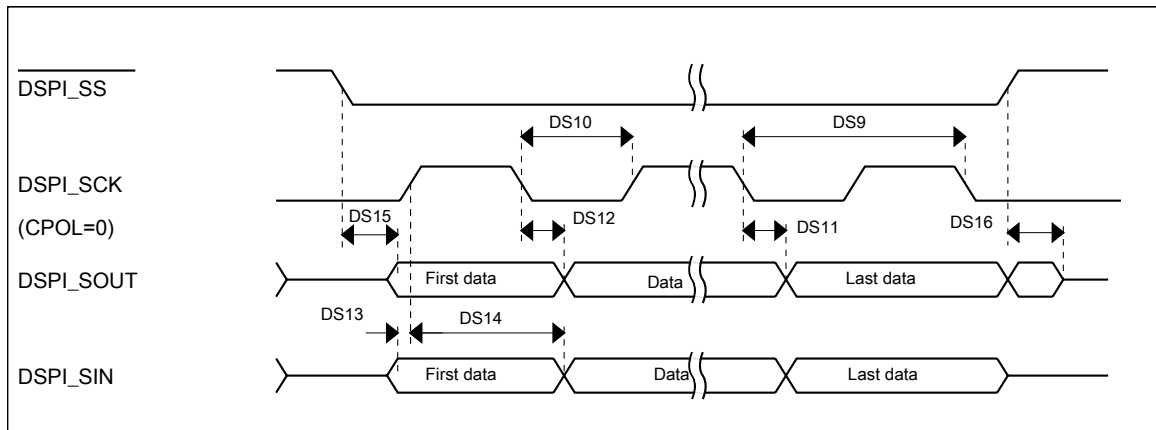
Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	15	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	15	ns

Table 33. Slave mode DSPI timing for fast pads (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		25	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	17	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	11	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	11	ns

Table 34. Slave mode DSPI timing for open drain pads (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	28	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI_SS}$ active to DSPI_SOUT driven	—	22	ns
DS16	$\overline{DSPI_SS}$ inactive to DSPI_SOUT not driven	—	22	ns


Figure 19. DSPI classic SPI timing — slave mode

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

NOTE

Fast pads:

- SIN: PTE19
- SOUT: PTE18



Peripheral operating requirements and behaviors

- SCK: PTE17
- PCS: PTE16

Open drain pads:

- SIN: PTC7
- SOUT: PTC6

Table 35. Master mode DSPI timing for normal pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	18.75	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCS _n valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCS _n invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 36. Master mode DSPI timing fast pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCS _n valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCS _n invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

- The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 37. Master mode DSPI timing open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	18.75	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	26	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

- The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
- The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
- The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

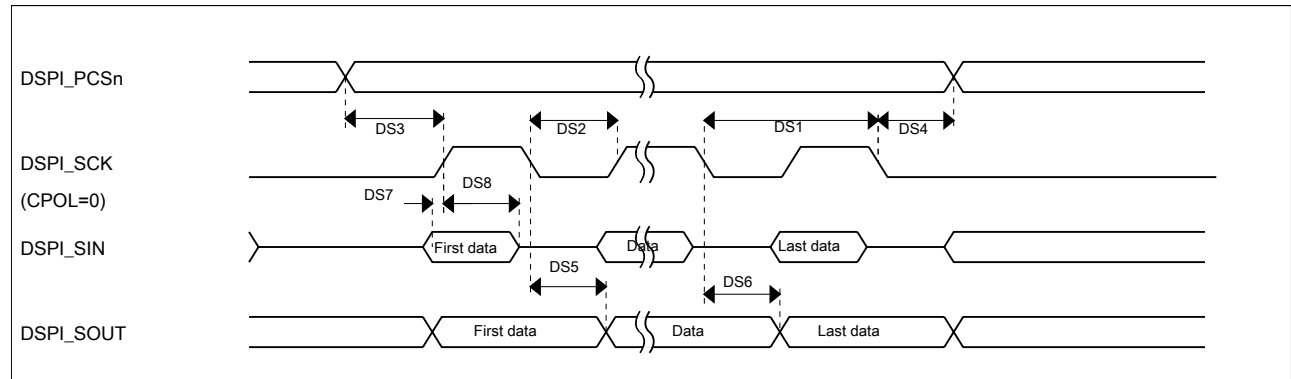


Figure 20. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing for normal pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	12.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	27.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns

Table continues on the next page...

Table 38. Slave mode DSPI timing for normal pads (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	22	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	22	ns

Table 39. Slave mode DSPI timing for fast pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	18.75	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}/2}) - 4$	$(t_{\text{SCK}/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	15	ns

Table 40. Slave mode DSPI timing for open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	9.375	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}/2}) - 4$	$(t_{\text{SCK}/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	43.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	38	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	38	ns

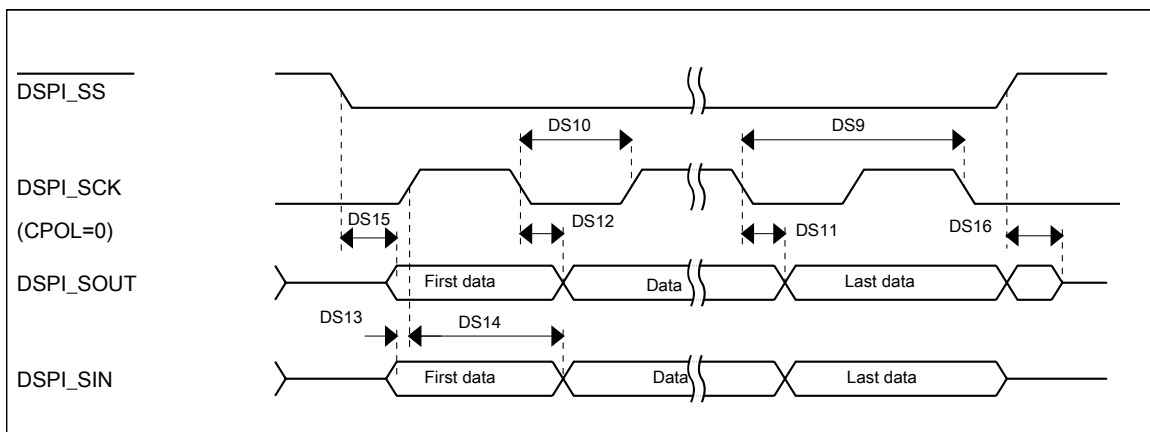


Figure 21. DSPI classic SPI timing — slave mode

3.8.3 I²C

See [General switching specifications](#).

3.8.4 UART

See [General switching specifications](#).

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W

5 Pinout

5.1 KV4x Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 48-pin LQFP package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	126	B5	PTC19	DISABLED		PTC19		UART3_CTS_b	ENET0_1588_TMR3	FLEXPWMB_B3		
—	134	M10	VSS	DISABLED	VSS							
—	135	F8	VDD	DISABLED	VDD							
—	137	C9	PTD8/LLWU_P24	DISABLED		PTD8/LLWU_P24	I2C1_SCL	UART5_RX			FLEXPWMA_A3	
—	138	B9	PTD9	DISABLED		PTD9	I2C1_SDA	UART5_TX			FLEXPWMA_B3	
—	139	B3	PTD10	DISABLED		PTD10		UART5_RTS_b			FLEXPWMA_A2	
—	140	B2	PTD11/LLWU_P25	DISABLED		PTD11/LLWU_P25	SPI2_PCS0	UART5_CTS_b			FLEXPWMA_B2	
—	141	B1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	XBAR0_IN5	XBAR0_OUT5	FLEXPWMA_A1	
—	142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		XBAR0_IN7	XBAR0_OUT7	FLEXPWMA_B1	
—	143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		XBAR0_IN11	XBAR0_OUT11	FLEXPWMA_A0	
—	144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1				FLEXPWMA_B0	
1	1	—	PTE0/CLKOUT32K	ADCB_CH6f	ADCB_CH6f	PTE0/CLKOUT32K		UART1_TX	XBAR0_OUT10	XBAR0_IN11		
2	2	—	PTE1/LLWU_P0	ADCB_CH7f	ADCB_CH7f	PTE1/LLWU_P0		UART1_RX	XBAR0_OUT11	XBAR0_IN7		
3	—	—	PTE2/LLWU_P1	ADCB_CH6g	ADCB_CH6g	PTE2/LLWU_P1		UART1_CTS_b				



100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
4	—	—	PTE3	ADCB_CH7g	ADCB_CH7g	PTE3		UART1_RTS_b				
5	—	—	PTE4/LLWU_P2	DISABLED		PTE4/LLWU_P2						
6	—	—	PTE5	DISABLED		PTE5					FTM3_CH0	
7	—	—	PTE6/LLWU_P16	DISABLED		PTE6/LLWU_P16					FTM3_CH1	
8	3	1	VDD	VDD	VDD							
9	4	2	VSS	VSS	VSS							
10	5	3	PTE16	ADCA_CH0	ADCA_CH0	PTE16	SPI0_PCS0	UART1_TX	FTM_CLKIN0		FTM0_FLT3	
11	6	4	PTE17/LLWU_P19	ADCA_CH1	ADCA_CH1	PTE17/LLWU_P19	SPI0_SCK	UART1_RX	FTM_CLKIN1		LPTMR0_ALT3	
12	7	5	PTE18/LLWU_P20	ADCB_CH0	ADCB_CH0	PTE18/LLWU_P20	SPI0_SOUT	UART1_CTS_b	I2C0_SDA			
13	8	6	PTE19	ADCB_CH1	ADCB_CH1	PTE19	SPI0_SIN	UART1_RTS_b	I2C0_SCL		CMP3_OUT	
14	—	—	ADCA_CH6a	ADCA_CH6a	ADCA_CH6a							
15	—	—	ADCA_CH7a	ADCA_CH7a	ADCA_CH7a							
16	—	7	PTE20	ADCA_CH6b	ADCA_CH6b	PTE20		FTM1_CH0	UART0_TX			
17	—	8	PTE21	ADCA_CH7b	ADCA_CH7b	PTE21		FTM1_CH1	UART0_RX			
18	9	—	ADCA_CH2	ADCA_CH2	ADCA_CH2							
19	10	—	ADCA_CH3	ADCA_CH3	ADCA_CH3							
20	11	—	ADCA_CH6c	ADCA_CH6c	ADCA_CH6c							
21	12	—	ADCA_CH7c	ADCA_CH7c	ADCA_CH7c							
22	13	9	VDDA	VDDA	VDDA							
23	14	10	VREFH	VREFH	VREFH							
24	15	11	VREFL	VREFL	VREFL							
25	16	12	VSSA	VSSA	VSSA							
26	17	13	PTE29	ADCA_CH4/ CMP1_IN5/ CMP0_IN5	ADCA_CH4/ CMP1_IN5/ CMP0_IN5	PTE29		FTM0_CH2		FTM_CLKIN0		
27	18	14	PTE30	DAC0_OUT/ CMP1_IN3/ ADCA_CH5	DAC0_OUT/ CMP1_IN3/ ADCA_CH5	PTE30		FTM0_CH3		FTM_CLKIN1		
28	19	—	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3							
29	—	—	VSS	VSS	VSS							
30	—	—	VDD	VDD	VDD							
31	20	15	PTE24	ADCB_CH4	ADCB_CH4	PTE24	CAN1_TX	FTM0_CH0	XBAR0_IN2	I2C0_SCL	EWM_OUT_b	XBAR0_OUT4
32	21	16	PTE25/LLWU_P21	ADCB_CH5	ADCB_CH5	PTE25/LLWU_P21	CAN1_RX	FTM0_CH1	XBAR0_IN3	I2C0_SDA	EWM_IN	XBAR0_OUT5
33	—	—	PTE26	DISABLED		PTE26						



Pinout

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
34	22	17	PTA0	JTAG_TCLK/ SWD_CLK		PTA0	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5	XBAR0_IN4	EWM_IN		JTAG_TCLK/ SWD_CLK
35	23	18	PTA1	JTAG_TDI		PTA1	UART0_RX	FTM0_CH6	CMP0_OUT		FTM1_CH1	JTAG_TDI
36	24	19	PTA2	JTAG_TDO/ TRACE_SWO		PTA2	UART0_TX	FTM0_CH7	CMP1_OUT		FTM1_CH0	JTAG_TDO/ TRACE_SWO
37	25	20	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_ b	FTM0_CH0	XBAR0_IN9	EWM_OUT_b	FLEXPWMA_ A0	JTAG_TMS/ SWD_DIO
38	26	21	PTA4/ LLWU_P3	NMI_b		PTA4/ LLWU_P3		FTM0_CH1	XBAR0_IN10	FTM0_FLT3	FLEXPWMA_ B0	NMI_b
39	27	—	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT		JTAG_TRST_ b
40	—	22	VDD	VDD	VDD							
41	—	23	VSS	VSS	VSS							
42	28	—	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0				FTM1_QD_ PHA
43	29	—	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1				FTM1_QD_ PHB
44	—	—	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX				
45	—	—	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX				
46	—	—	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_ b/ UART0_COL_ b				
47	—	—	PTA17	ADCA_CH7e	ADCA_CH7e	PTA17	SPI0_SIN	UART0_RTS_ b				
48	30	—	VDD	VDD	VDD							
49	31	—	VSS	VSS	VSS							
50	32	24	PTA18	EXTAL0	EXTAL0	PTA18	XBAR0_IN7	FTM0_FLT2	FTM_CLKIN0	XBAR0_ OUT8	FTM3_CH2	
51	33	25	PTA19	XTAL0	XTAL0	PTA19	XBAR0_IN8	FTM1_FLT0	FTM_CLKIN1	XBAR0_ OUT9	LPTMR0_ ALT1	
52	34	26	RESET_b	RESET_b	RESET_b							
53	35	27	PTB0/ LLWU_P5	ADCB_CH2	ADCB_CH2	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	UART0_RX
54	36	28	PTB1	ADCB_CH3	ADCB_CH3	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_ PHB	UART0_TX
55	37	29	PTB2	ADCA_CH6e/ CMP2_IN2	ADCA_CH6e/ CMP2_IN2	PTB2	I2C0_SCL	UART0_RTS_ b	FTM0_FLT1		FTM0_FLT3	
56	38	30	PTB3	ADCB_CH7e/ CMP3_IN5	ADCB_CH7e/ CMP3_IN5	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_ b			FTM0_FLT0	
57	—	—	PTB9	DISABLED		PTB9						
58	—	—	PTB10	ADCB_CH6a	ADCB_CH6a	PTB10					FTM0_FLT1	



100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
59	—	—	PTB11	ADCB_CH7a	ADCB_CH7a	PTB11					FTM0_FLT2	
60	—	—	VSS	VSS	VSS							
61	—	—	VDD	VDD	VDD							
62	39	31	PTB16	DISABLED		PTB16		UART0_RX	FTM_CLKIN2	CAN0_TX	EWM_IN	XBAR0_IN5
63	40	32	PTB17	DISABLED		PTB17		UART0_TX	FTM_CLKIN1	CAN0_RX	EWM_OUT_b	
64	41	—	PTB18	DISABLED		PTB18	CAN0_TX		FTM3_CH2			
65	42	—	PTB19	DISABLED		PTB19	CAN0_RX		FTM3_CH3			
66	—	—	PTB20	DISABLED		PTB20				FLEXPWMA_X0	CMP0_OUT	
67	—	—	PTB21	DISABLED		PTB21				FLEXPWMA_X1	CMP1_OUT	
67	100	D9	PTB21	DISABLED		PTB21	SPI2_SCK			FLEXPWMA_X1	CMP1_OUT	
68	—	—	PTB22	DISABLED		PTB22				FLEXPWMA_X2	CMP2_OUT	
68	101	C12	PTB22	DISABLED		PTB22	SPI2_SOUT			FLEXPWMA_X2	CMP2_OUT	
69	—	—	PTB23	DISABLED		PTB23		SPI0_PCS5		FLEXPWMA_X3	CMP3_OUT	
69	102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FLEXPWMA_X3	CMP3_OUT	
70	43	33	PTC0	ADCB_CH6b	ADCB_CH6b	PTC0	SPI0_PCS4	PDB0_EXTRG			FTM0_FLT1	SPI0_PCS0
70	103	B12	PTC0	ADCB_CH6b	ADCB_CH6b	PTC0	SPI0_PCS4	PDB0_EXTRG			FTM0_FLT1	SPI0_PCS0
71	44	34	PTC1/LLWU_P6	ADCB_CH7b	ADCB_CH7b	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FLEXPWMA_A3	XBAR0_IN11	
71	104	B11	PTC1/LLWU_P6	ADCB_CH7b	ADCB_CH7b	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FLEXPWMA_A3	XBAR0_IN11	
72	45	35	PTC2	ADCB_CH6c/CMP1_IN0	ADCB_CH6c/CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FLEXPWMA_B3	XBAR0_IN6	
72	105	A12	PTC2	ADCD_CH6c/CMP1_IN0	ADCD_CH6c/CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FLEXPWMA_B3	XBAR0_IN6	
73	46	36	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
73	106	A11	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
74	47	—	VSS	VSS	VSS							
74	107	H8	VSS	VSS	VSS							
75	48	—	VDD	VDD	VDD							
75	108	—	VDD	VDD	VDD							
76	49	37	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	
76	109	A9	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	



Pinout

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
77	50	38	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	XBAR0_IN2		CMP0_OUT	FTM0_CH2
77	110	D8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	XBAR0_IN2		CMP0_OUT	FTM0_CH2
78	51	39	PTC6/ LLWU_P10	CMP2_IN4/ CMP0_IN0	CMP2_IN4/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	XBAR0_IN3	UART0_RX	XBAR0_ OUT6	I2C0_SCL
78	111	C8	PTC6/ LLWU_P10	CMP2_IN4/ CMP0_IN0	CMP2_IN4/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	XBAR0_IN3	UART0_RX	XBAR0_ OUT6	I2C0_SCL
79	52	40	PTC7	CMP3_IN4/ CMP0_IN1	CMP3_IN4/ CMP0_IN1	PTC7	SPI0_SIN		XBAR0_IN4	UART0_TX	XBAR0_ OUT7	I2C0_SDA
79	112	B8	PTC7	CMP3_IN4/ CMP0_IN1	CMP3_IN4/ CMP0_IN1	PTC7	SPI0_SIN		XBAR0_IN4	UART0_TX	XBAR0_ OUT7	I2C0_SDA
80	53	—	PTC8	ADCB_CH7c/ CMP0_IN2	ADCB_CH7c/ CMP0_IN2	PTC8		FTM3_CH4				
80	113	A8	PTC8	ADCD_CH7c/ CMP0_IN2	ADCD_CH7c/ CMP0_IN2	PTC8		FTM3_CH4	FLEXPWMB_ A2			
81	54	—	PTC9	ADCB_CH6d/ CMP0_IN3	ADCB_CH6d/ CMP0_IN3	PTC9		FTM3_CH5				
81	114	D7	PTC9	ADCD_CH6d/ CMP0_IN3	ADCD_CH6d/ CMP0_IN3	PTC9		FTM3_CH5	FLEXPWMB_ B2			
82	55	—	PTC10	ADCB_CH7d	ADCB_CH7d	PTC10		FTM3_CH6				
82	115	C7	PTC10	ADCD_CH7d	ADCD_CH7d	PTC10	I2C1_SCL	FTM3_CH6	FLEXPWMB_ A3			
83	56	—	PTC11/ LLWU_P11	ADCB_CH6e	ADCB_CH6e	PTC11/ LLWU_P11		FTM3_CH7				
83	116	B7	PTC11/ LLWU_P11	ADCD_CH6e	ADCD_CH6e	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	FLEXPWMB_ B3			
84	—	—	PTC12	DISABLED		PTC12			FTM_CLKIN0		FTM3_FLT0	
84	117	A7	PTC12	DISABLED		PTC12	CAN2_TX		FTM_CLKIN0	FLEXPWMB_ A1	FTM3_FLT0	SPI2_PCS1
85	—	—	PTC13	DISABLED		PTC13			FTM_CLKIN1			
85	118	D6	PTC13	DISABLED		PTC13	CAN2_RX		FTM_CLKIN1	FLEXPWMB_ B1		
86	—	—	PTC14	DISABLED		PTC14		I2C0_SCL				
86	119	C6	PTC14	DISABLED		PTC14	I2C1_SCL	I2C0_SCL		FLEXPWMB_ A0		
87	—	—	PTC15	DISABLED		PTC15		I2C0_SDA				
87	120	B6	PTC15	DISABLED		PTC15	I2C1_SDA	I2C0_SDA		FLEXPWMB_ B0		
88	—	—	VSS	VSS	VSS							
88	121	—	VSS	VSS	VSS							
89	—	—	VDD	VDD	VDD							
89	122	—	VDD	VDD	VDD							
90	—	—	PTC16	DISABLED		PTC16	CAN1_RX					



100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
90	123	A6	PTC16	DISABLED		PTC16	CAN1_RX	UART3_RX	ENET0_1588_TMR0	FLEXPWMB_A2		
91	—	—	PTC17	DISABLED		PTC17	CAN1_TX					
91	124	D5	PTC17	DISABLED		PTC17	CAN1_TX	UART3_TX	ENET0_1588_TMR1	FLEXPWMB_B2		
92	—	—	PTC18	DISABLED		PTC18						
92	125	C5	PTC18	DISABLED		PTC18		UART3_RTS_b	ENET0_1588_TMR2	FLEXPWMB_A3		
93	57	41	PTD0/LLWU_P12	DISABLED		PTD0/LLWU_P12	SPI0_PCS0		FTM3_CH0	FTM0_CH0	FLEXPWMA_A0	
93	127	A5	PTD0/LLWU_P12	DISABLED		PTD0/LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0	FTM0_CH0	FLEXPWMA_A0	
94	58	42	PTD1	ADCA_CH7f	ADCA_CH7f	PTD1	SPI0_SCK		FTM3_CH1	FTM0_CH1	FLEXPWMA_B0	
94	128	D4	PTD1	ADCC_CH7c	ADCC_CH7c	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1	FTM0_CH1	FLEXPWMA_B0	
95	59	43	PTD2/LLWU_P13	DISABLED		PTD2/LLWU_P13	SPI0_SOUT		FTM3_CH2	FTM0_CH2	FLEXPWMA_A1	I2C0_SCL
95	129	C4	PTD2/LLWU_P13	DISABLED		PTD2/LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FTM0_CH2	FLEXPWMA_A1	I2C0_SCL
96	60	44	PTD3	DISABLED		PTD3	SPI0_SIN		FTM3_CH3	FTM0_CH3	FLEXPWMA_B1	I2C0_SDA
96	130	B4	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FTM0_CH3	FLEXPWMA_B1	I2C0_SDA
97	61	45	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FLEXPWMA_A2	EWM_IN	SPI0_PCS0
97	131	A4	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FLEXPWMA_A2	EWM_IN	SPI1_PCS0
98	62	46	PTD5	ADCA_CH6g	ADCA_CH6g	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	FLEXPWMA_B2	EWM_OUT_b	SPI0_SCK
98	132	A3	PTD5	ADCC_CH6b	ADCC_CH6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	FLEXPWMA_B2	EWM_OUT_b	SPI1_SCK
99	63	47	PTD6/LLWU_P15	ADCA_CH7g	ADCA_CH7g	PTD6/LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FTM1_CH0	FTM0_FLT0	SPI0_SOUT
99	133	A2	PTD6/LLWU_P15	ADCC_CH7b	ADCC_CH7b	PTD6/LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FTM1_CH0	FTM0_FLT0	SPI1_SOUT
100	64	48	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7	FTM1_CH1	FTM0_FLT1	SPI0_SIN
100	136	A1	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7	FTM1_CH1	FTM0_FLT1	SPI1_SIN



5.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

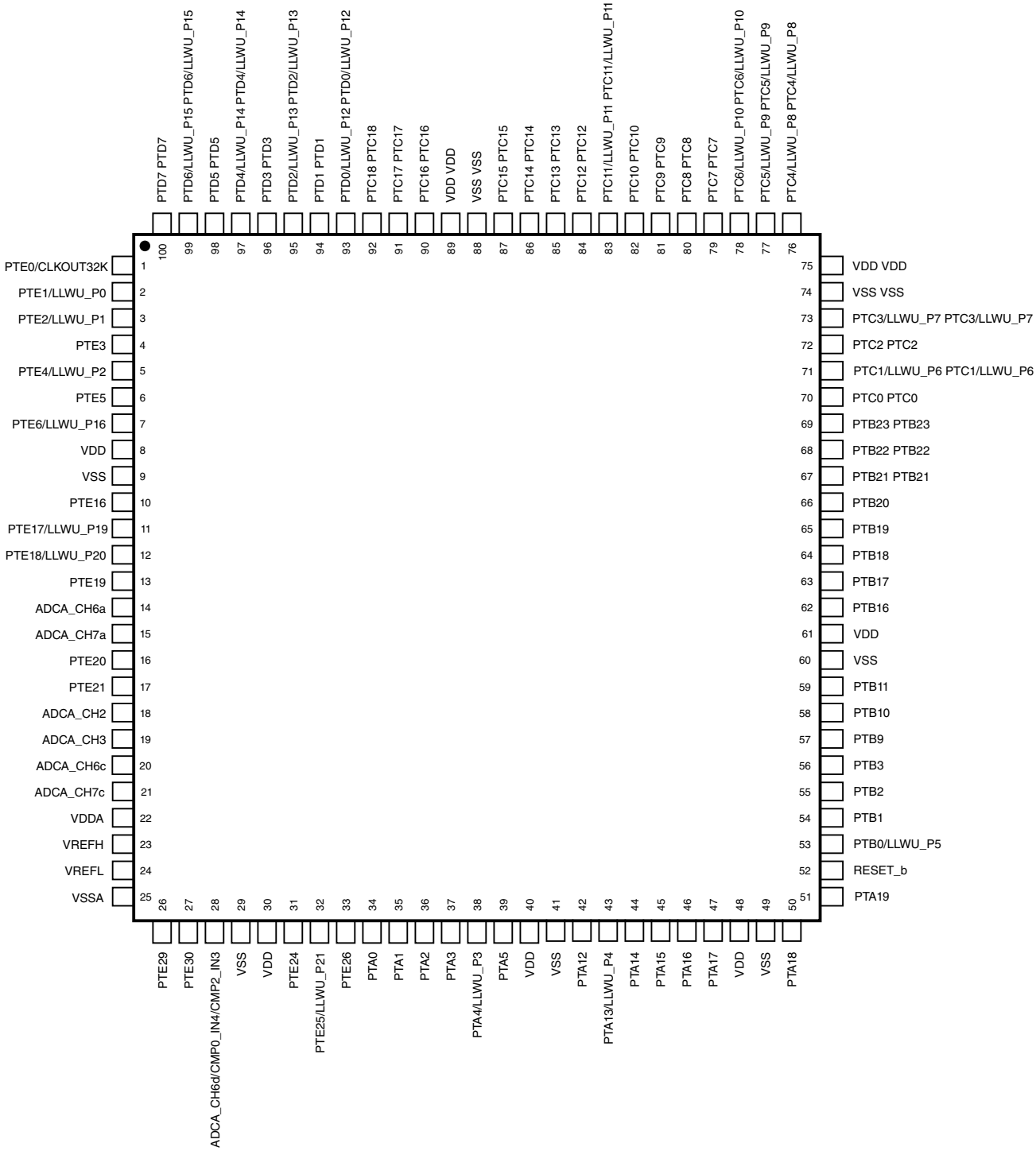


Figure 22. 100-pin LQFP

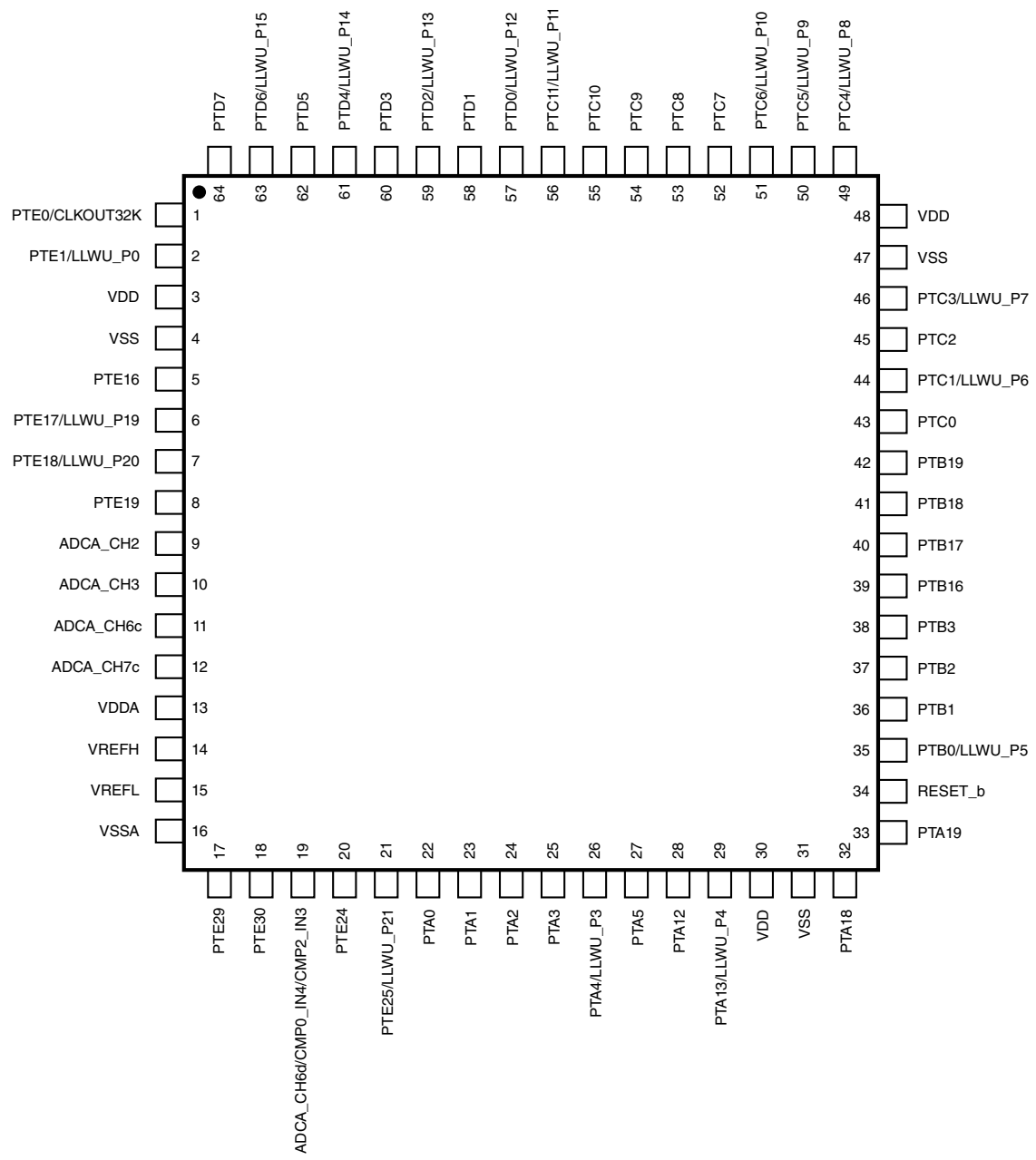


Figure 23. 64-pin LQFP

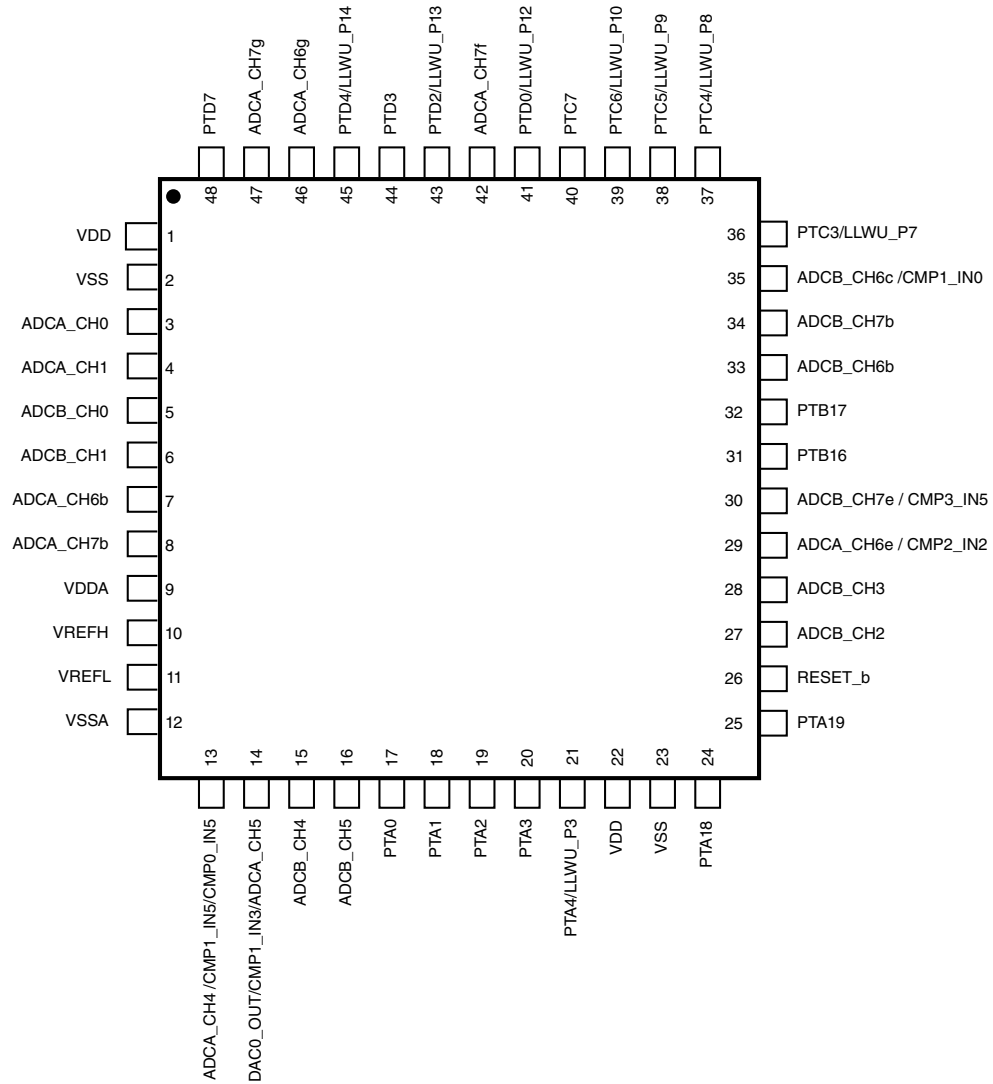


Figure 24. 48-pin LQFP

6 Ordering parts



6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the MKV4x device numbers.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KV## A FFF T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification
KV##	Kinetis family	<ul style="list-style-type: none"> KV40 KV41 KV43 KV44 KV45 KV46
A	Key attribute	<ul style="list-style-type: none"> F = Cortex-M4 w/ DSP and FPU
FFF	Program flash memory size	<ul style="list-style-type: none"> 64 = 64 KB 128 = 128 KB 256 = 256 KB
T	Temperature range (°C)	<ul style="list-style-type: none"> V = -40 to 105
PP	Package identifier	<ul style="list-style-type: none"> LF = 48 LQFP (7 mm x 7 mm)

Table continues on the next page...

Field	Description	Values
		<ul style="list-style-type: none"> LH = 64 LQFP (10 mm x 10 mm) LL = 100 LQFP (14 mm x 14 mm)
CCC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> 15 = 150 MHz
N	Packaging type	<ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays

7.4 Example

This is an example part number:

MKV46F256VLL15

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

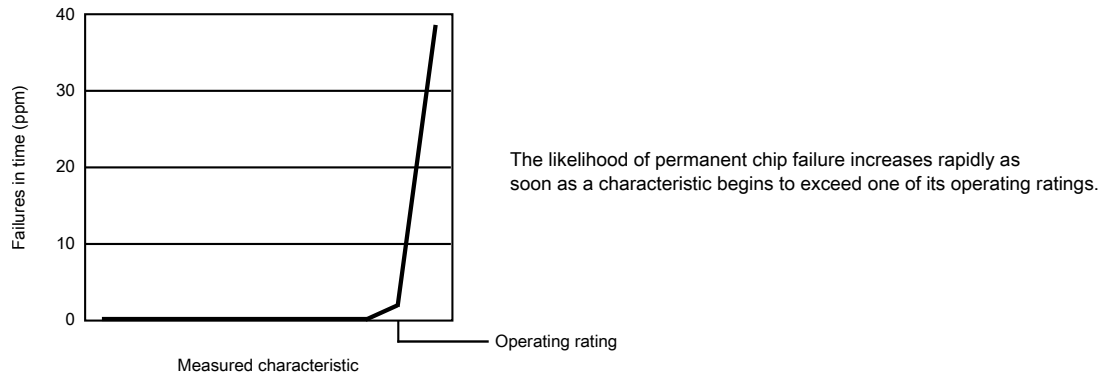
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

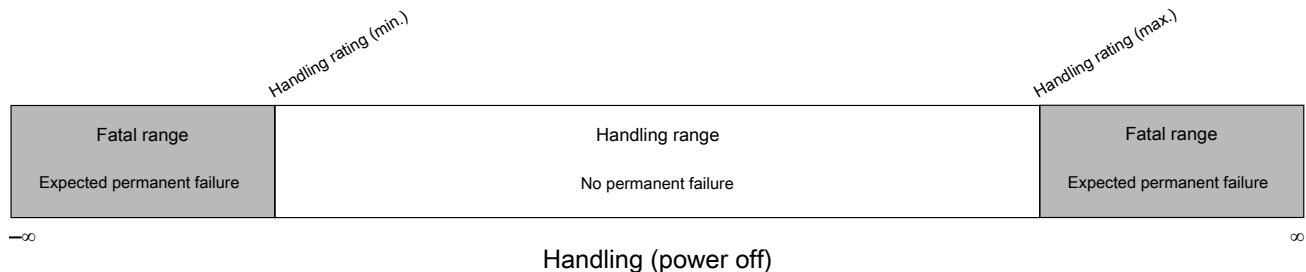
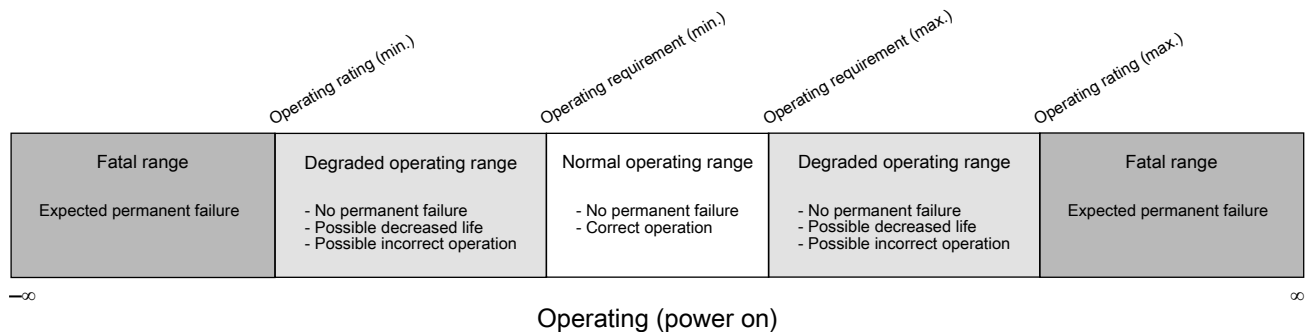
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

8.5 Result of exceeding a rating



8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

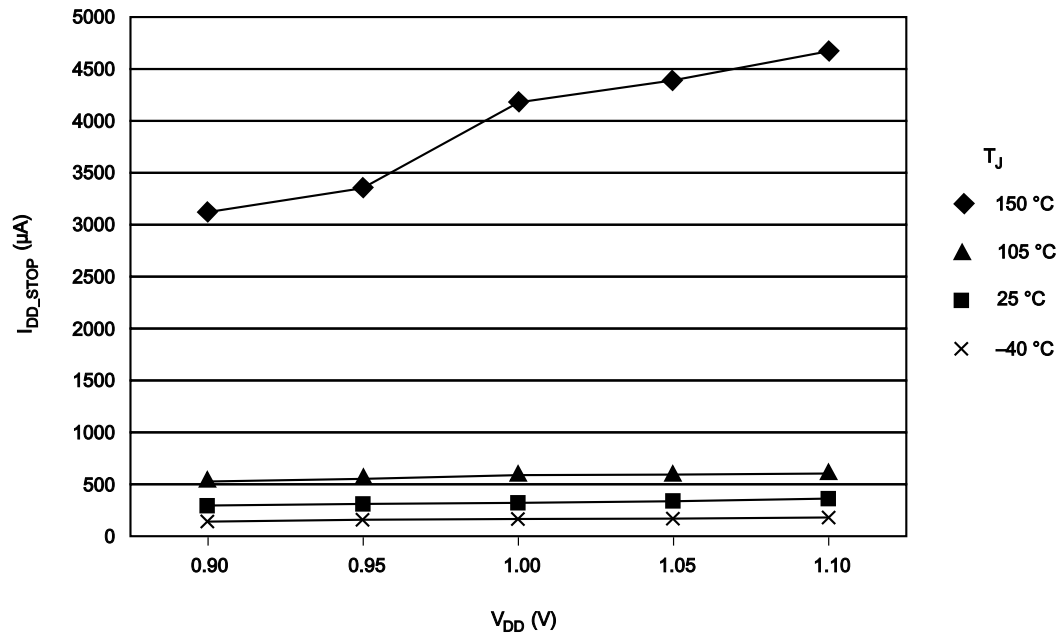
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 41. Revision history

Rev. No.	Date	Substantial Changes
0	7/2014	Initial NDA release.
1	2/2015	<ul style="list-style-type: none"> • Added information about 48 LQFP package in the following sections: <ul style="list-style-type: none"> • Ordering information • Fields

Table 41. Revision history

Rev. No.	Date	Substantial Changes
		<ul style="list-style-type: none"> • Obtaining package dimensions • Pinout • In table "Power consumption operating behaviors", removed the text "Maximum core frequency of 150 Mhz" from note for I_{DDA}. • In table "Typical device clock specifications", removed information about High Speed run mode.

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