

August 1991

N-P-N/P-N-P Transistor Arrays

Applications

- Five-Independent Transistors
 - Three N-P-N and
 - Two P-N-P
- Differential Amplifiers
- DC Amplifiers
- Sense Amplifiers
- Level Shifters
- Timers
- Lamp and Relay Drivers
- Thyristor Firing Circuits
- Temperature-Compensated Amplifiers
- Operational Amplifiers

Description

The CA3096C, CA3096, and CA3096A are general purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

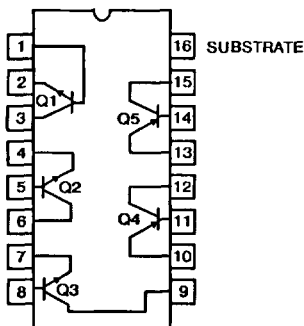
Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in I_{CBO} , I_{CEO} , and $V_{CE(SAT)}$. The CA3096C is a relaxed version of the CA3096.

The CA3096C, CA3096, and CA3096A are supplied in 16-lead dual-in-line plastic packages (E-suffix), and in 16-lead Small Outline packages (M suffix). The CA3096 is also available in chip form (H suffix).

CA3096A, CA3096, CA3096C Essential Differences

CHARACTERISTIC	CA3096A	CA3096	CA3096C	
$V_{(BR)CEO}$ (V) Min.	n-p-n	35	35	24
	p-n-p	-40	-40	-24
$V_{(BR)CBO}$ (V) Min.	n-p-n	45	45	30
	p-n-p	-40	-40	-24
h_{FE} @ 1 mA	n-p-n	150-500	150-500	100-670
	p-n-p	20-200	20-200	15-200
h_{FE} @ 100 μ A	n-p-n	40-250	40-250	30-300
	p-n-p	40-250	40-250	30-300
I_{CBO} (nA) Max.	n-p-n	40	100	100
	p-n-p	-40	-100	-100
I_{CEO} (nA) Max.	n-p-n	100	1000	1000
	p-n-p	-100	-1000	-1000
$V_{CE(SAT)}$ (V) Max.	n-p-n	0.5	0.7	0.7
	p-n-p	0.5	0.7	0.7
$ V_{IO} $ (mV) Max.	n-p-n	5	-	-
	p-n-p	5	-	-
I_{IO} (μ A) Max.	n-p-n	0.6	-	-
	p-n-p	0.25	-	-

Pinout CA3096, CA3096A, CA3096C 16 PIN PACKAGES TOP VIEW



Schematic Diagram

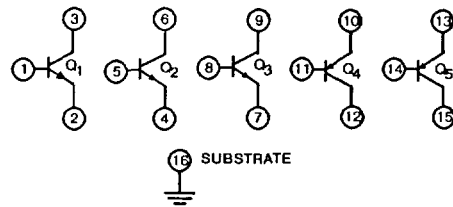


FIGURE 1.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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CA3096, CA3096A, CA3096C

MAXIMUM RATINGS, Absolute-Maximum Values:

	EACH N-P-N	EACH P-N-P	
COLLECTOR-TO-EMITTER VOLTAGE, V_{CE0} :			
CA3096A, CA3096	35	-40	V
CA3096C	24	-24	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO} :			
CA3096A, CA3096	45	-40	V
CA3096C	30	-24	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO} :			
CA3096A, CA3096	45	-	V
CA3096C	30	-	V
EMITTER-TO-SUBSTRATE VOLTAGE, V_{EIO} :			
CA3096A, CA3096	-	-40	V
CA3096C	-	-24	V
EMITTER-TO-BASE VOLTAGE, V_{EBO} :			
CA3096A, CA3096	6	-40	V
CA3096C	6	-24	V
COLLECTOR CURRENT, I_C (All Types)	50	-10	mA
POWER DISSIPATION, P_D :			
Up to $T_A = 55^\circ\text{C}$:			
Device (Total)	750		mW
Each Transistor	200		mW
Above $T_A = 55^\circ\text{C}$ derate linearly at	6.67		mW/ $^\circ\text{C}$
AMBIENT-TEMPERATURE RANGE, T_A :			
Operating		-55 to +125	$^\circ\text{C}$
Storage		-65 to +150	$^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):			
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm)			
from case for 10 s max.			265 $^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096A			CA3096			CA3096C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	$V_{CB} = 10\text{ V}$, $I_E = 0$	-	0.001	40	-	0.001	100	-	0.001	100	nA
I_{CEO}	$V_{CE} = 10\text{ V}$, $I_B = 0$	-	0.006	100	-	0.006	1000	-	0.006	1000	nA
$V_{(BR)CEO}$	$I_C = 1\text{ mA}$, $I_B = 0$	35	50	-	35	50	-	24	35	-	V
$V_{(BR)CBO}$	$I_C = 10\ \mu\text{A}$, $I_E = 0$	45	100	-	45	100	-	30	80	-	V
$V_{(BR)CIO}$	$I_{CI} = 10\ \mu\text{A}$, $I_B = I_E = 0$	45	100	-	45	100	-	30	80	-	V
$V_{(BR)EBO}$	$I_E = 10\ \mu\text{A}$, $I_C = 0$	6	8	-	6	8	-	6	8	-	V
V_Z	$I_Z = 10\ \mu\text{A}$	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	$I_C = 10\text{ mA}$, $I_B = 1\text{ mA}$	-	0.24	0.5	-	0.24	0.7	-	0.24	0.7	V
V_{BE} (Note 1)	$I_C = 1\text{ mA}$,	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE} (Note 1)	$V_{CE} = 5\text{ V}$	150	390	500	150	390	500	100	390	670	
$ \Delta V_{BE}/\Delta T $ (Note 1)	$I_C = 1\text{ mA}$, $V_{CE} = 5\text{ V}$	-	1.9	-	-	1.9	-	-	1.9	-	mV/ $^\circ\text{C}$

CA3096, CA3096A, CA3096C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ (Cont'd)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096A			CA3096			CA3096C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each p-n-p Transistor											
I_{CBO}	$V_{CB} = -10\text{V}$, $I_E = 0$	-	0.006	-40	-	0.06	-100	-	-0.06	-100	nA
I_{CEO}	$V_{CE} = -10\text{V}$, $I_B = 0$	-	0.12	-100	-	0.12	-1000	-	-0.12	-1000	nA
$V_{(BR)CEO}$	$I_C = -100\mu\text{A}$, $I_B = 0$	40	75	-	40	-75	-	-24	-30	-	V
$V_{(BR)CBO}$	$I_C = -10\mu\text{A}$, $I_E = 0$	40	80	-	40	-80	-	-24	-60	-	V
$V_{(BR)EBO}$	$I_E = -10\mu\text{A}$, $I_C = 0$	-40	-100	-	-40	-100	-	-24	-80	-	V
$V_{(BR)EIO}$	$I_E = -10\mu\text{A}$, $I_B = I_C = 0$	-40	-100	-	-40	-100	-	-24	-80	-	V
$V_{CE(SAT)}$	$I_C = -1\text{mA}$, $I_B = -100\mu\text{A}$	-	0.16	0.4	-	0.16	0.4	-	-0.16	-0.4	V
V_{BE} (Note 1)	$I_C = -100\mu\text{A}$, $V_{CE} = -5\text{V}$	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	V
h_{FE} (Note 1)	$I_C = -100\mu\text{A}$, $V_{CE} = -5\text{V}$	40	85	250	40	85	250	30	85	300	
	$I_C = -1\text{mA}$, $V_{CE} = -5\text{V}$	20	47	200	20	47	200	15	47	200	
$ \Delta V_{BE}/\Delta T $ (Note 1)	$I_C = -100\mu\text{A}$, $V_{CE} = -5\text{V}$	-	2.2	-	-	2.2	-	-	2.2	-	mV/ $^\circ\text{C}$

I_{CBO} Collector-Cutoff Current
 I_{CEO} Collector-Cutoff Current
 $V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage
 $V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage
 $V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage
 $V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

V_Z Emitter-to-Base Zener Voltage
 $V_{CE(SAT)}$ Collector-to-Emitter Saturation Voltage
 V_{BE} Base-to-Emitter Voltage
 h_{FE} DC Forward-Current Transfer Ratio
 $|\Delta V_{BE}/\Delta T|$ Magnitude of Temperature Coefficient: (for each transistor)

NOTES:

1. Actual forcing current is via the emitter for this test.

CA3096, CA3096A, CA3096C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ (CA3096A Only)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		CA3096A			
		Min.	Typ.	Max.	
For Transistors Q1 and Q2 (as a Differential Amplifier)					
Absolute Input Offset Voltage, $ V_{IO} $	$V_{CE} = 5\text{ V}, I_C = 1\text{ mA}$	—	0.3	5	mV
Absolute Input Offset Current, $ I_{IO} $		—	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{ \Delta V_{IO} }{\Delta T}$		—	1.1	—	$\mu\text{V}/^\circ\text{C}$
For Transistors Q4 and Q5 (As a Differential Amplifier)					
Absolute Input Offset Voltage, $ V_{IO} $	$V_{CE} = -5\text{ V}, I_C = -100\mu\text{A}$ $R_S = 0$	—	0.15	5	mV
Absolute Input Offset Current, $ I_{IO} $		—	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{ \Delta V_{IO} }{\Delta T}$		—	0.54	—	$\mu\text{V}/^\circ\text{C}$

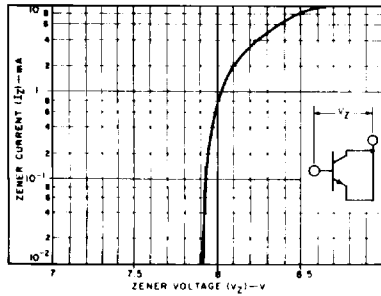


Fig. 1 — Base-to-emitter zener characteristic (n-p-n).

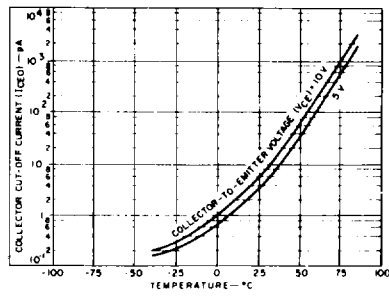


Fig. 2 — Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

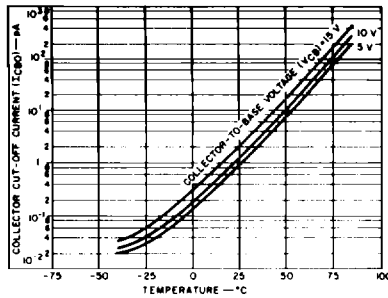


Fig. 3 — Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

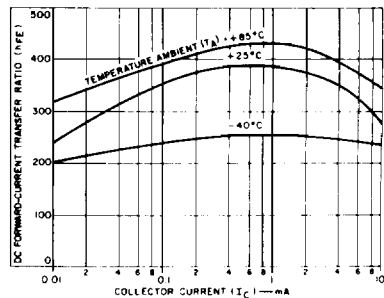


Fig. 4 — Transistor (n-p-n) h_{FE} as a function of collector current.

CA3096, CA3096A, CA3096C

DYNAMIC

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

Typical Values Intended Only for Design Guidance

CHARACTERISTICS	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor			
Noise Figure (low frequency), NF	$f = 1\text{ kHz}, V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, R_S = 1\text{ k}\Omega$	2.2	dB
Low-Frequency Input Resistance, R_i	$f = 1.0\text{ kHz}, V_{CE} = 5\text{ V}, I_C = 1\text{ mA}$	10	$\text{k}\Omega$
Low-Frequency Output Resistance, R_o		80	$\text{k}\Omega$
Admittance Characteristics:			
Forward Transfer Admittance, $\frac{g_{fe}}{y_{fe} b_{fe}}$	$f = 1\text{ MHz}, V_{CE} = 5\text{ V}, I_C = 1\text{ mA}$	7.5	mmho
		-j13	
Input Admittance, $\frac{g_{ie}}{y_{ie} b_{ie}}$		2.2	mmho
		j3.1	
Output Admittance, $\frac{g_{oe}}{y_{oe} b_{oe}}$		0.76	mmho
		j2.4	
Gain-Bandwidth Product, f_T	$V_{CE} = 5\text{ V}, I_C = 1.0\text{ mA}$	280	MHz
	$V_{CE} = 5\text{ V}, I_C = 5\text{ mA}$	335	
Emitter-to-Base Capacitance, C_{EB}	$V_{EB} = 3\text{ V}$	0.75	μF
Collector-to-Base Capacitance, C_{CB}	$V_{CB} = 3\text{ V}$	0.46	μF
Collector-to-Substrate Capacitance, C_{CI}	$V_{CI} = 3\text{ V}$	3.2	μF
For Each p-n-p Transistor			
Noise Figure (low frequency), NF	$f = 1\text{ kHz}, I_C = 100\text{ }\mu\text{A}, R_S = 1\text{ k}\Omega$	3	dB
Low-Frequency Input Resistance, R_i	$f = 1\text{ kHz}, V_{CE} = 5\text{ V}, I_C = 100\text{ }\mu\text{A}$	27	$\text{k}\Omega$
Low-Frequency Output Resistance, R_o		680	$\text{k}\Omega$
Gain-Bandwidth Product, f_T	$V_{CE} = 5\text{ V}, I_C = 100\text{ }\mu\text{A}$	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}	$V_{EB} = -3\text{ V}$	0.85	μF
Collector-to-Base Capacitance, C_{CB}	$V_{CB} = -3\text{ V}$	2.25	μF
Base-to-Substrate Capacitance, C_{BI}	$V_{BI} = 3\text{ V}$	3.05	μF

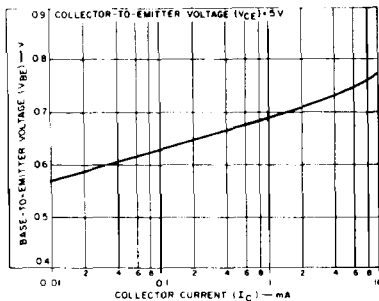


Fig. 5 - V_{BE} (n-p-n) as a function of collector current.

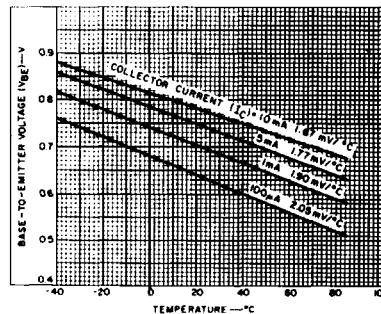


Fig. 6 - V_{BE} (n-p-n) as a function of temperature.

CA3096, CA3096A, CA3096C

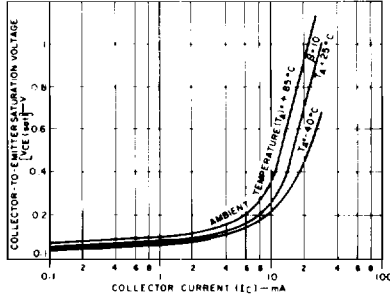


Fig. 7 - $V_{CE(SAT)}$ (n-p-n) as a function of collector current.

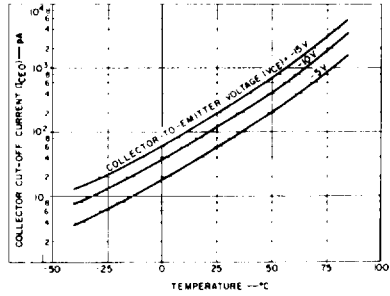


Fig. 8 - Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

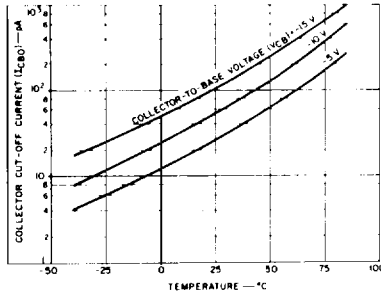


Fig. 9 - Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

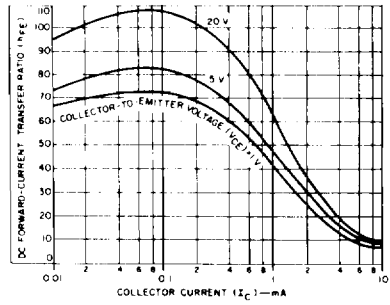


Fig. 10 - Transistor (p-n-p) h_{FE} as a function of collector current.

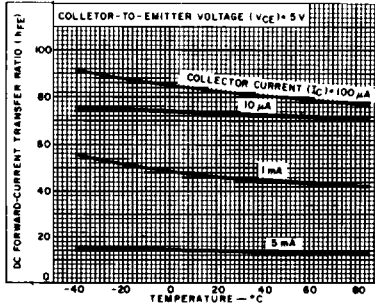


Fig. 11 - Transistor (p-n-p) h_{FE} as a function of temperature.

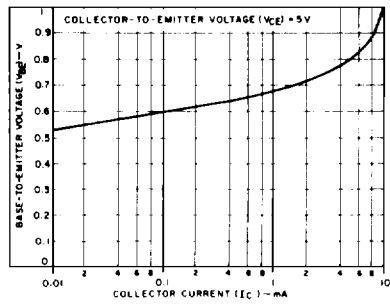


Fig. 12 - V_{BE} (p-n-p) as a function of collector current.

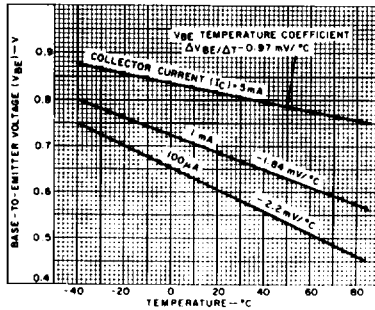


Fig. 13 - V_{BE} (p-n-p) as a function of temperature.

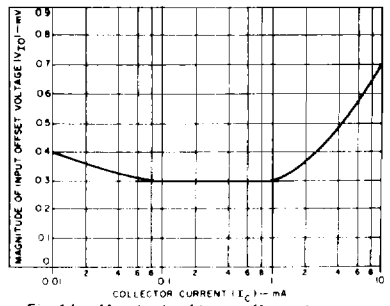


Fig. 14 - Magnitude of input offset voltage ($|V_{IO}|$) as a function of collector current for n-p-n transistor Q_1-Q_2 .

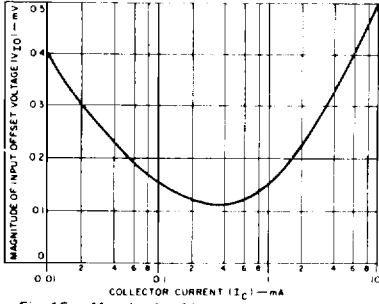


Fig. 15 - Magnitude of input offset voltage V_{IO} as a function of collector current for p-n-p transistor Q_4-Q_5

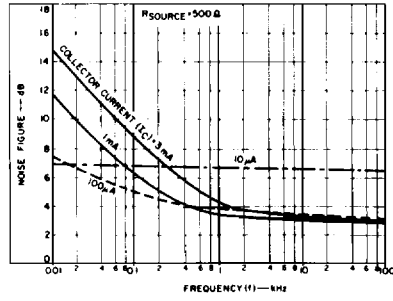


Fig. 16 - Noise figure as a function of frequency for n-p-n transistors.

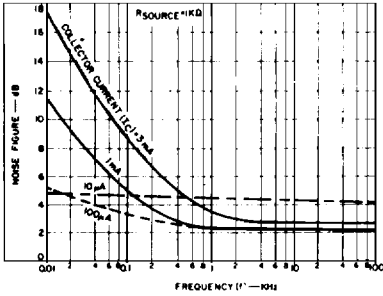


Fig. 17 - Noise figure as a function of frequency for n-p-n transistors.

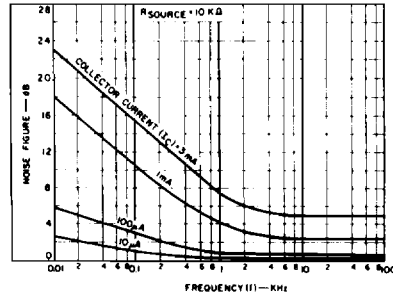


Fig. 18 - Noise as a function of frequency for n-p-n transistors.

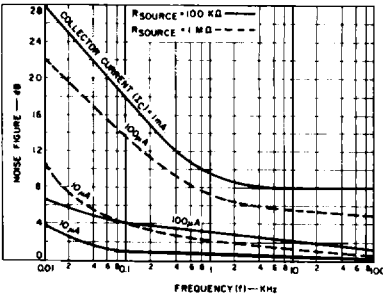


Fig. 19 - Noise figure as a function of frequency for n-p-n transistors.

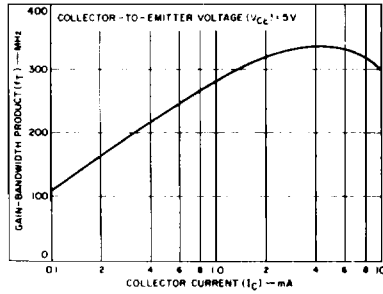


Fig. 20 - Gain-bandwidth product as a function of collector current (n-p-n).

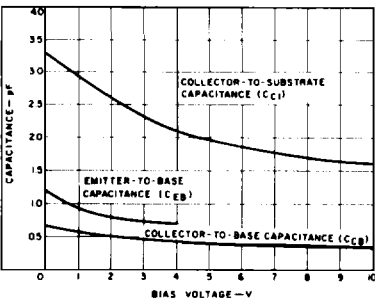


Fig. 21 - Capacitance as a function of bias voltage (n-p-n).

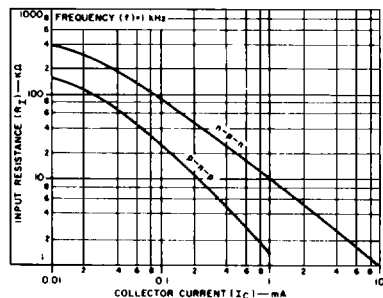


Fig. 22 - Input resistance as a function of collector current.

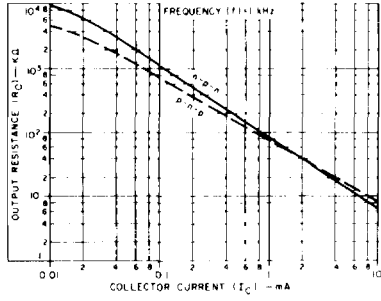


Fig. 23 - Output resistance as a function of collector current.

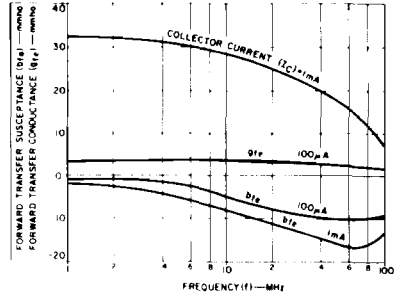


Fig. 24 - Forward transconductance as a function of frequency.

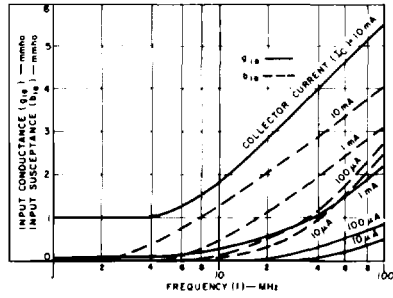


Fig. 25 - Input admittance as a function of frequency.

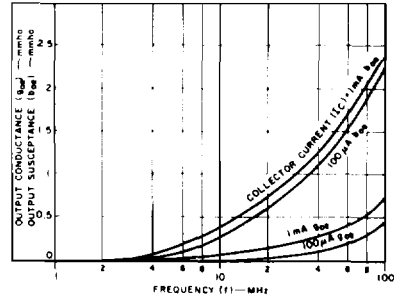


Fig. 26 - Output admittance as a function of frequency.

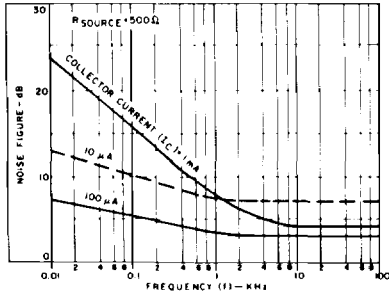


Fig. 27 - Noise figure as a function of frequency (p-n-p).

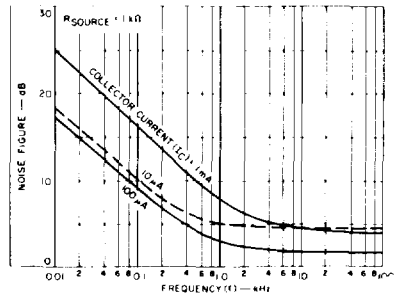


Fig. 28 - Noise figure as a function of frequency (p-n-p).

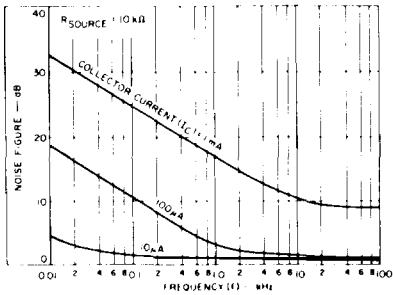


Fig. 29 - Noise figure as a function of frequency (p-n-p).

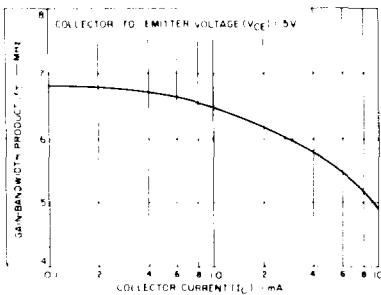


Fig. 30 - Gain-bandwidth product as a function of collector current (p-n-p).

CA3096, CA3096A, CA3096C

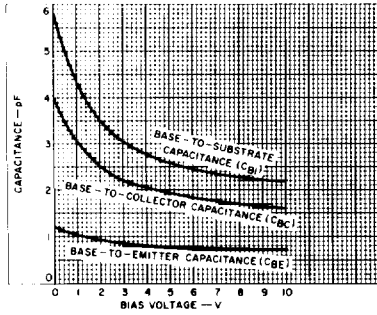


Fig. 31 - Capacitance as a function of bias voltage (p-n-p).

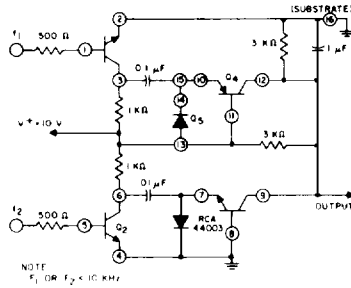


Fig. 32 - Frequency comparator using CA3096

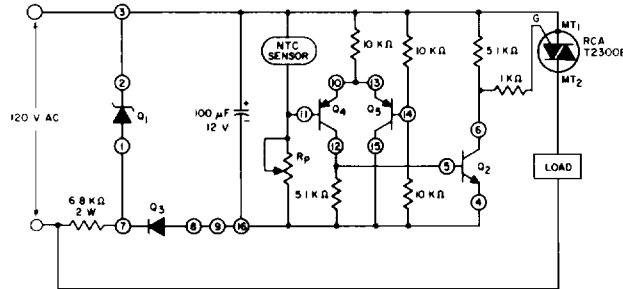


Fig. 33 - Line-operated level switch using CA3096A or CA3096

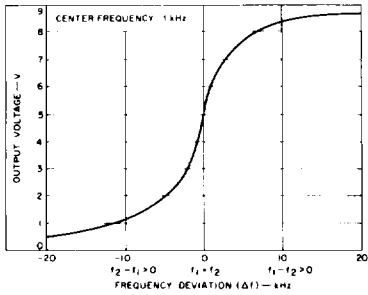


Fig. 34 - Frequency comparator characteristics.

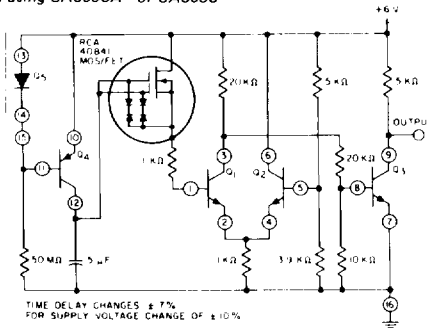


Fig. 35 - One-minute timer using CA3096A and a MOS/FET.

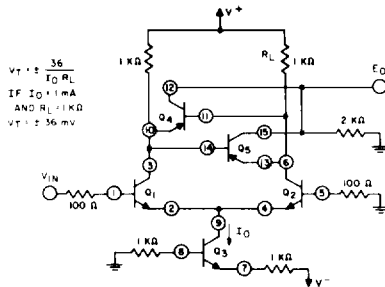
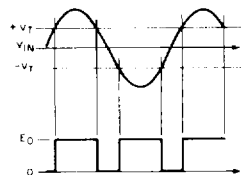


Fig. 36 - CA3096A small-signal zero voltage detector having noise immunity.



CA3096, CA3096A, CA3096C

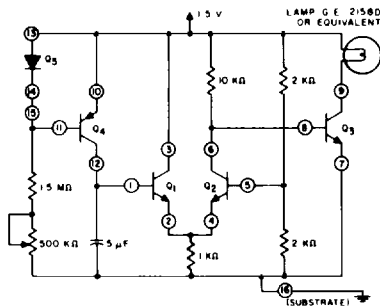


Fig. 37 - Ten-second timer operated from 1.5-volt supply using CA3096

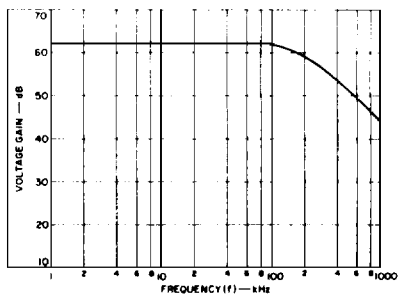


Fig. 38 - Gain-frequency characteristics.

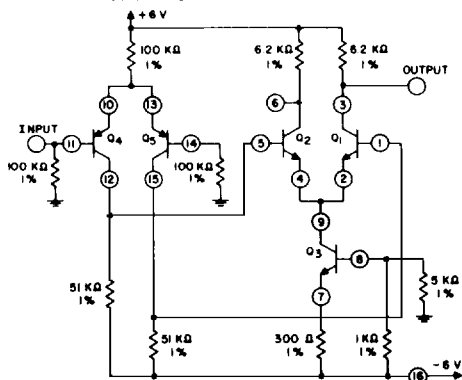
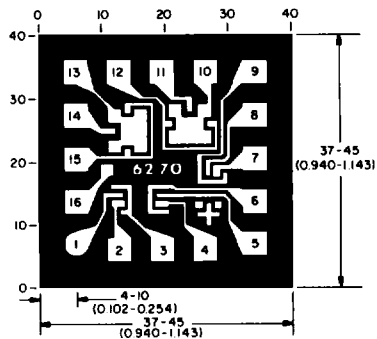


Fig. 39 - Cascade of differential amplifiers using CA3096A

Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to -5 V.
3. Low bias current: $< 1 \mu A$.



CA3096H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.