Click here for production status of specific part numbers.

MAX4800A/MAX4802A

Low-Charge-Injection, 8-Channel, High-Voltage Analog Switches with 20MHz Serial Interface

General Description

The MAX4800A/MAX4802A provide high-voltage switching on eight channels for ultrasonic imaging and printer applications. The devices utilize BCDMOS process technology to provide eight high-voltage low-charge-injection SPST switches, controlled by a 20MHz serial interface. Data is clocked into an internal 8-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on reset function ensures that all switches are open on power-up.

The devices operate with a wide range of high-voltage supplies including: V_{PP}/V_{NN} = +100V/-100V, +185V/-15V, and +40V/-160V. The digital interface operates from a separate V_{DD} supply from +2.7V to +6V. Digital inputs DIN, CLK, $\overline{LE}$, and CLR are +6V tolerant, independent of the V_{DD} supply voltage. The MAX4802A provides integrated 35kΩ bleed resistors on each switch terminal to discharge capacitive loads.

The devices are drop-in replacements for the Supertex HV2203 and HV2303. They are available in the 48-pin LQFP, 26-bump CSBGA, and 28-pin PLCC packages. All devices are specified for the commercial 0°C to +70°C temperature range.

Applications

- Ultrasound Imaging
- Printers

Features

- Fast SPI™ Interface 20MHz
- Pin-Compatible Replacement for Supertex HV2203 (MAX4800A)
- Pin-Compatible Replacement for Supertex HV2303 (MAX4802A)
- Flexible High-Voltage Supplies Up to V_{PP} - V_{NN} = 200V
- Low-Charge-Injection, Low-Capacitance 22Ω Switches
- DC to 50MHz Analog-Signal Frequency Range
- -77dB Off-Isolation at 5MHz
- Low 10µA Quiescent Current
- Integrated Bleed Resistors (MAX4802A Only)
- Available in Standard PLCC, LQFP, and CSBGA Packages

SPI is a trademark of Motorola, Inc.

19-4120; Rev 2; 4/19

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{DD} Logic Supply Voltage.....-0.3V to +7V
V_{PP} - V_{NN} Supply Voltage 220V
V_{PP} Positive Supply Voltage .....-0.3V to (V_{NN} + 220V)
V_{NN} Negative Supply Voltage .....+0.3V to -220V
Logic Inputs $\overline{LE}$, CLR, CLK, DIN.....-0.3V to +7V
DOUT .....-0.3V to (V_{DD} + 0.3V)
RGND (MAX4802A) .....-4.5V to +0.3V
COM_, NO_..... V_{NN} to V_{PP}

Continuous Power Dissipation (T_A = +70°C)
26-Bump CSBGA (derate 11.8mW/°C above +70°C).... 941mW
28-Pin PLCC (derate 10.5mW/°C above +70°C) 842mW
48-Pin LQFP (derate 22.7mW/°C above +70°C) 1818mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (excluding CSBGA, soldering, 10s) ..+300°C
Soldering Temperature (reflow)
28 PLCC .....+245°C
All other packages.....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 26 CSBGA	
Package Code	X07265+1
Outline Number	**21-0158**
Land Pattern Number	**90-0184**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	85°C/W
Junction to Case (θ_{JC})	23°C/W

PACKAGE TYPE: 28 PLCC	
Package Code	Q28+13
Outline Number	**21-0049**
Land Pattern Number	**90-0235**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	44°C/W
Junction to Case (θ_{JC})	10°C/W

PACKAGE TYPE: 48 LQFP	
Package Code	C48+6
Outline Number	**21-0054**
Land Pattern Number	**90-0093**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	44°C/W
Junction to Case (θ_{JC})	10°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +2.7V to +6V, V_{PP} = +40V to (V_{NN} + 200V), V_{NN} = -40V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog-Signal Range	$V_{COM_}$, $V_{NO_}$	(Note 2)			V_{NN} + 10		V_{PP} - 10	V
Small-Signal Switch On-Resistance	R_{ONS}	V_{PP} = +40V, V_{NN} = -160V, $V_{COM_}$ = 0V	I_{COM} = 5mA	T_A = 0°C			30	Ω
				T_A = +25°C		26	38	
				T_A = +70°C			48	
			I_{COM} = 200mA	T_A = 0°C			25	
				T_A = +25°C		22	27	
				T_A = +70°C			32	
		V_{PP} = +100V, V_{NN} = -100V, $V_{COM_}$ = 0V	I_{COM} = 5mA	T_A = 0°C			25	
				T_A = +25°C		22	27	
				T_A = +70°C			30	
			I_{COM} = 200mA	T_A = 0°C			18	
				T_A = +25°C		18	24	
				T_A = +70°C			27	
Small-Signal Switch On-Resistance	R_{ONS}	V_{PP} = +160V, V_{NN} = -40V	I_{COM} = 5mA	T_A = 0°C			23	Ω
				T_A = +25°C		20	25	
				T_A = +70°C			30	
			I_{COM} = 200mA	T_A = 0°C			22	
				T_A = +25°C		16	25	
				T_A = +70°C			27	
Small-Signal Switch On-Resistance Matching	ΔR_{ONS}	V_{PP} = +100V, V_{NN} = -100V, $V_{COM_}$ = 0V, I_{COM} = 5mA				5	20	%
Large-Signal Switch On-Resistance	R_{ONL}	$V_{COM_}$ = V_{PP} - 10V, I_{COM} = 1A				15		Ω
Shunt Resistance (MAX4802A only)	R_{INT}	NO_ or COM_ to RGND, switch off			30	35	50	kΩ
Switch-Off Leakage	$I_{COM_(OFF)}$, $I_{NO_(OFF)}$	$V_{COM_}$, $V_{NO_}$ = V_{PP} - 10V or unconnected; (MAX4800A only)				0	2	µA
							10	
Switch-Off DC Offset		R_L = 100kΩ (MAX4800A), no load (MAX4802A)				0	10	mV
Switch-On DC Offset		R_L =100kΩ (MAX4800A), no load (MAX4802A)				0	10	mV
Switch-Output Peak Current (Note 3)		$I_{COM_}$ duty cycle ≤ 0.1%		T_A = 0°C	3			A
				T_A = +25°C	2	3		
				T_A = +70°C	2			
Switch-Output Isolation Diode Current		300ns pulse width, 2% duty cycle (Note 3)			300			mA

Electrical Characteristics (continued)

(V_{DD} = +2.7V to +6V, V_{PP} = +40V to (V_{NN} + 200V), V_{NN} = -40V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISITICS								
Off-Isolation (Note 3)	V_{ISO}	f = 5MHz, R_L = 1kΩ, C_L = 15pF			-30	-33		dB
		f = 5MHz, R_L = 50Ω			-58	-77		
Crosstalk	V_{CT}	f = 5MHz, R_L = 50Ω (Note 3)			-60	-80		dB
COM_, NO_ Off-Capacitance	$C_{COM_(OFF)}$, $C_{NO_(OFF)}$	$V_{COM_}$ = 0V, $V_{NO_}$ = 0V, f = 1MHz (Note 3)			4	11	18	pF
COM_ On-Capacitance	$C_{COM_(ON)}$	$V_{COM_}$ = 0V, f = 1MHz (Note 3)			20	36	56	pF
Output Voltage Spike	V_{SPK}	R_L = 50Ω (Note 3)			-150		+150	mV
Charge Injection (MAX4802A only)	Q	V_{PP} = +40V, V_{NN} = -160V, $V_{COM_}$ = 0V				820		pC
		V_{PP} = +100V, V_{NN} = -100V, $V_{COM_}$ = 0V				600		
		V_{PP} = +160V, V_{NN} = -40V, $V_{COM_}$ = 0V				350		
LOGIC LEVELS								
Logic-Input Low Voltage	V_{IL}						0.75	V
Logic-Input High Voltage	V_{IH}				V_{DD} - 0.75			V
Logic Input Capacitance	C_{IN}	(Note 3)					10	pF
Logic Input Leakage	I_{IN}				-1		+1	µA
DOUT Low Voltage	V_{OL}	I_{SINK} = 1mA					0.4	V
DOUT High Voltage	V_{OH}	I_{SOURCE} = 0.75mA			V_{DD} - 0.5			V
POWER SUPPLIES								
V_{DD} Supply Voltage	V_{DD}				2.7		6.0	V
V_{PP} Supply Voltage	V_{PP}				40		V_{NN} + 200	V
V_{NN} Supply Voltage	V_{NN}				-160		-15	V
V_{DD} Supply Quiescent Current	I_{DDQ}	V_{IL} = 0V, V_{IH} = V_{PSD}, f_{CLK} = 0Hz					3	µA
V_{DD} Supply Dynamic Current	I_{DD}	V_{DD} = +5V, V_{IL} = 0V, V_{IH} = +5V, f_{CLK} = 5MHz					2	mA
V_{PP} Supply Quiescent Current	I_{PPQ}	All switches remain on or off, $I_{COM_(ON)}$ = 5mA				10	50	µA
V_{PP} Supply Dynamic Current	I_{PP}	50kHz output switching frequency with no load	V_{PP} = +40V, V_{NN} = -160V	T_A = 0°C			6.5	mA
				T_A = +25°C			6.5	
				T_A = +70°C			6.5	
			V_{PP} = +100V, V_{NN} = -100V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	
			V_{PP} = +160V, V_{NN} = -40V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	
V_{NN} Supply Quiescent Current	I_{NNQ}	All switches remain on or off, $I_{COM_(ON)}$ = 5mA				10	50	µA

Electrical Characteristics (continued)

(V_{DD} = +2.7V to +6V, V_{PP} = +40V to (V_{NN} + 200V), V_{NN} = -40V to -160V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
V_{NN} Supply Dynamic Current	I_{NN}	50kHz output switching frequency with no load	V_{PP} = +40V, V_{NN} = -160V	T_A = 0°C			6.5	mA
				T_A = +25°C			6.5	
				T_A = +70°C			6.5	
			V_{PP} = +100V, V_{NN} = -100V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	
			V_{PP} = +160V, V_{NN} = -40V	T_A = 0°C			4.0	
				T_A = +25°C			4.0	
				T_A = +70°C			4.0	
ANALOG SWITCH								
Turn-On Time	t_{ON}	$V_{NO_}$ = V_{PP} - 10V, R_L = 10kΩ, V_{NN} = -40V to -160V					5	µs
Turn-Off Time	t_{OFF}	$V_{NO_}$ = V_{PP} - 10V, R_L = 10kΩ, V_{NN} = -40V to -160V					5	µs
Output Switching Frequency	f_{SW}	Duty cycle = 50%					50	kHz
Maximum $V_{COM_}$, $V_{NO_}$ Slew Rate	dV/dt	(Note 3)			20			V/ns
LOGIC TIMING (Figure 1)								
CLK Frequency	f_{CLK}	Daisy chaining	V_{DD} = +5V ±10%				20	MHz
			V_{DD} = +3V ±10%				10	
DIN to CLK Setup Time	t_{DS}	V_{DD} = +5V ±10%			10			ns
		V_{DD} = +3V ±10%			16			
DIN to CLK Hold Time	t_{DH}	V_{DD} = +5V ±10%			3			ns
		V_{DD} = +3V ±10%			3			
CLK to $\overline{LE}$ Setup Time	t_{CS}	V_{DD} = +5V ±10%			36			ns
		V_{DD} = +3V ±10%			65			
$\overline{LE}$ Low Pulse Width	t_{WL}	V_{DD} = +5V ±10%			14			ns
		V_{DD} = +3V ±10%			22			
CLR High Pulse Width	t_{WC}	V_{DD} = +5V ±10%			20			ns
		V_{DD} = +3V ±10%			40			
CLK Rise and Fall Times (Note 3)	t_R, t_F	V_{DD} = +5V ±10%					50	ns
		V_{DD} = +3V ±10%					50	
CLK to DOUT Delay	t_{DO}	V_{DD} = +5V ±10%, C_L ≤ 20pF			6		42	ns
		V_{DD} = +3V ±10%, C_L ≤ 20pF			12		80	

Note 1: Specifications at 0°C are guaranteed by correlation and design.

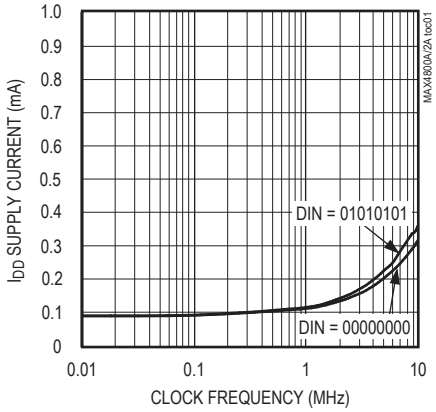
Note 2: The analog-signal input $V_{COM_}$ and $V_{NO_}$ must satisfy V_{NN} ≤ ($V_{COM_}$, $V_{NO_}$) ≤ V_{PP}, or remain unconnected during power-up and power-down.

Note 3: Guaranteed by design and characterization; not production tested.

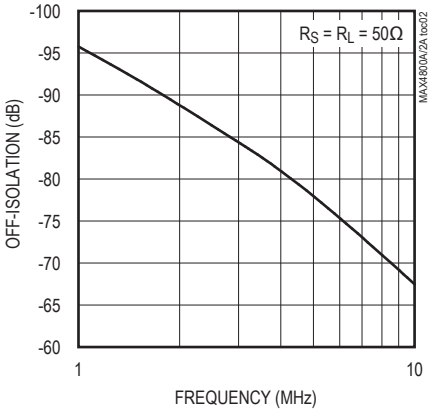
Typical Operating Characteristics

(V_{DD} = +5V, V_{PP} = +100V, V_{NN} = -100V, T_A = +25°C, unless otherwise noted.)

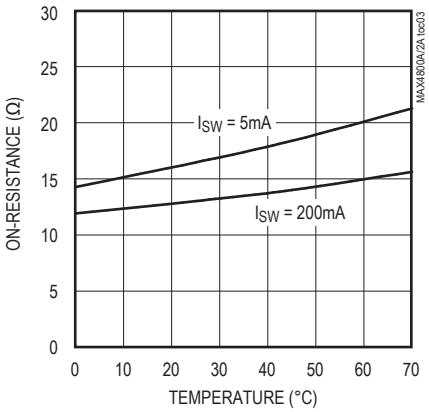
I_{DD} SUPPLY CURRENT vs. CLOCK FREQUENCY



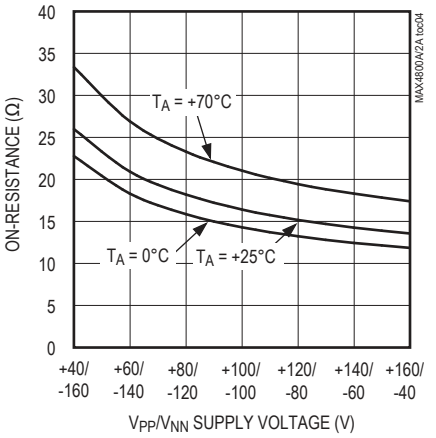
OFF-ISOLATION vs. FREQUENCY



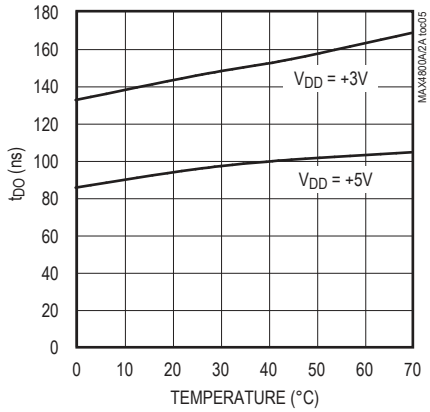
ON-RESISTANCE vs. TEMPERATURE



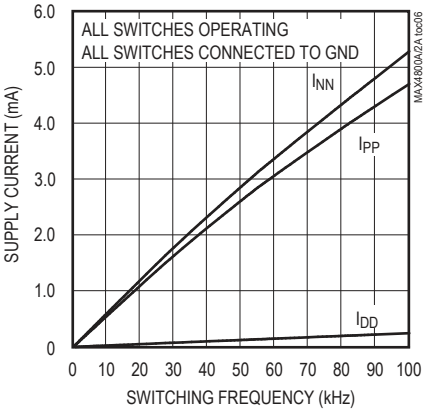
ON-RESISTANCE vs. V_{PP}/V_{NN} SUPPLY VOLTAGE



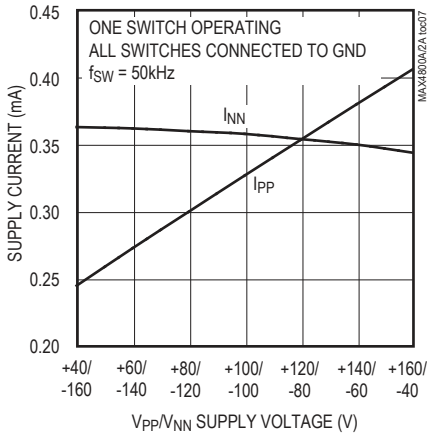
CLK TO DOUT DELAY vs. TEMPERATURE



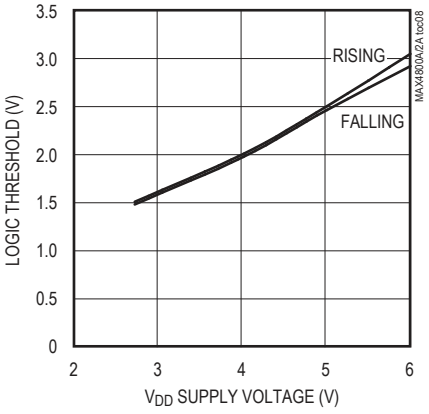
SUPPLY CURRENT vs. SWITCHING FREQUENCY



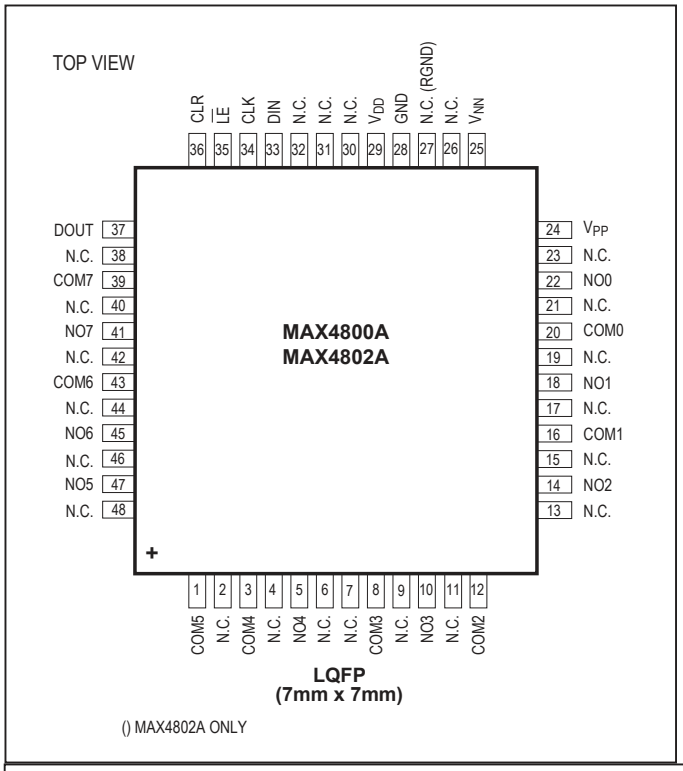
SUPPLY CURRENT vs. V_{PP}/V_{NN} SUPPLY VOLTAGE

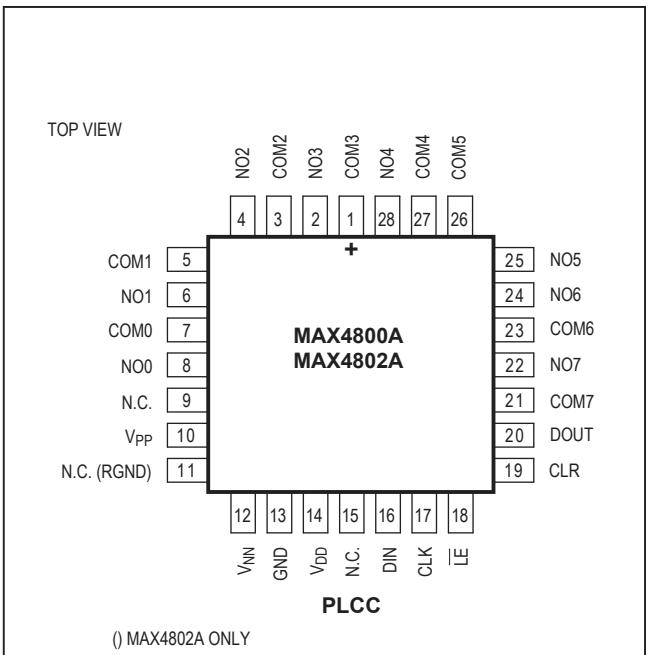


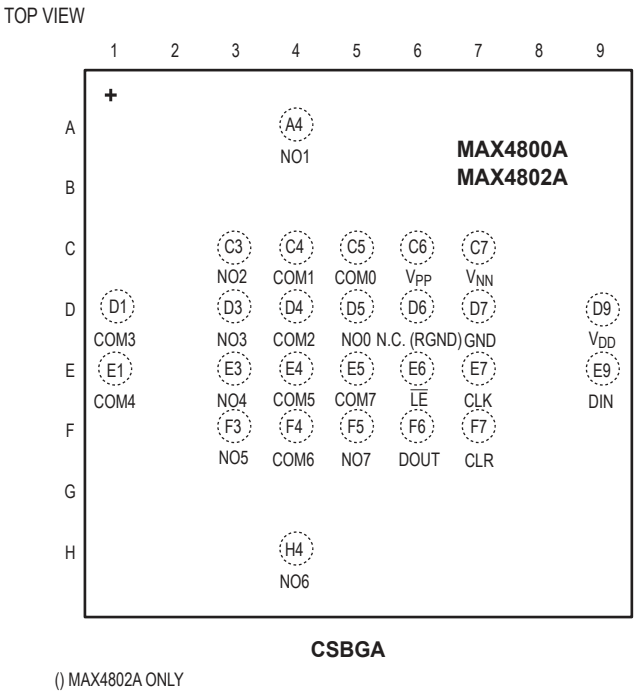
LOGIC THRESHOLD vs. V_{DD} SUPPLY VOLTAGE



Pin/Bump Configurations







Pin/Bump Descriptions

PIN/BUMP			NAME	FUNCTION
MAX4800A LQFP	MAX4800A CSBGA	MAX4800A PLCC		
1	E4	26	COM5	Analog Switch 5—Common Terminal
2, 4, 6, 7, 9, 11, 13, 15, 17, 19, 21, 23, 26, 27, 30, 31, 32, 38, 40, 42, 44, 46, 48	D6	9, 11, 15	N.C.	No Connection. Not connected internally.
3	E1	27	COM4	Analog Switch 4—Common Terminal
5	E3	28	NO4	Analog Switch 4—Normally Open Terminal
8	D1	1	COM3	Analog Switch 3—Common Terminal
10	D3	2	NO3	Analog Switch 3—Normally Open Terminal
12	D4	3	COM2	Analog Switch 2—Common Terminal
14	C3	4	NO2	Analog Switch 2—Normally Open Terminal
16	C4	5	COM1	Analog Switch 1—Common Terminal
18	A4	6	NO1	Analog Switch 1—Normally Open Terminal
20	C5	7	COM0	Analog Switch 0—Common Terminal
22	D5	8	NO0	Analog Switch 0—Normally Open Terminal
24	C6	10	V_{PP}	Positive High-Voltage Supply. Bypass V_{PP} to GND with a 0.1µF or greater ceramic capacitor.
25	C7	12	V_{NN}	Negative High-Voltage Supply. Bypass V_{NN} to GND with a 0.1µF or greater ceramic capacitor.
28	D7	13	GND	Ground
29	D9	14	V_{DD}	Digital Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.
33	E9	16	DIN	Serial-Data Input
34	E7	17	CLK	Serial-Clock Input
35	E6	18	$\overline{LE}$	Latch-Enable Input, Active Low
36	F7	19	CLR	Latch Clear Input
37	F6	20	DOUT	Serial-Data Output
39	E5	21	COM7	Analog Switch 7—Common Terminal
41	F5	22	NO7	Analog Switch 7—Normally Open Terminal
43	F4	23	COM6	Analog Switch 6—Common Terminal
45	H4	24	NO6	Analog Switch 6—Normally Open Terminal
47	F3	25	NO5	Analog Switch 5—Normally Open Terminal

Pin/Bump Descriptions (continued)

PIN/BUMP			NAME	FUNCTION
MAX4802A LQFP	MAX4802A CSBGA	MAX4802A PLCC		
1	E4	26	COM5	Analog Switch 5—Common Terminal
2, 4, 6, 7, 9, 11,13, 15, 17, 19, 21, 23, 26, 30, 31, 32, 38, 40, 42, 44, 46, 48	—	9, 15	N.C.	No Connection. Not connected internally.
3	E1	27	COM4	Analog Switch 4—Common Terminal
5	E3	28	NO4	Analog Switch 4—Normally Open Terminal
8	D1	1	COM3	Analog Switch 3—Common Terminal
10	D3	2	NO3	Analog Switch 3—Normally Open Terminal
12	D4	3	COM2	Analog Switch 2—Common Terminal
14	C3	4	NO2	Analog Switch 2—Normally Open Terminal
16	C4	5	COM1	Analog Switch 1—Common Terminal
18	A4	6	NO1	Analog Switch 1—Normally Open Terminal
20	C5	7	COM0	Analog Switch 0—Common Terminal
22	D5	8	NO0	Analog Switch 0—Normally Open Terminal
24	C6	10	V_{PP}	Positive High-Voltage Supply. Bypass V_{PP} to GND with a 0.1µF or greater ceramic capacitor.
25	C7	12	V_{NN}	Negative High-Voltage Supply. Bypass V_{NN} to GND with a 0.1µF or greater ceramic capacitor.
27	D6	11	RGND	Bleed Resistor Ground
28	D7	13	GND	Ground
29	D9	14	V_{DD}	Digital Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.
33	E9	16	DIN	Serial-Data Input
34	E7	17	CLK	Serial-Clock Input
35	E6	18	$\overline{LE}$	Latch-Enable Input, Active Low
36	F7	19	CLR	Latch Clear Input
37	F6	20	DOUT	Serial-Data Output
39	E5	21	COM7	Analog Switch 7—Common Terminal
41	F5	22	NO7	Analog Switch 7—Normally Open Terminal
43	F4	23	COM6	Analog Switch 6—Common Terminal
45	H4	24	NO6	Analog Switch 6—Normally Open Terminal
47	F3	25	NO5	Analog Switch 5—Normally Open Terminal

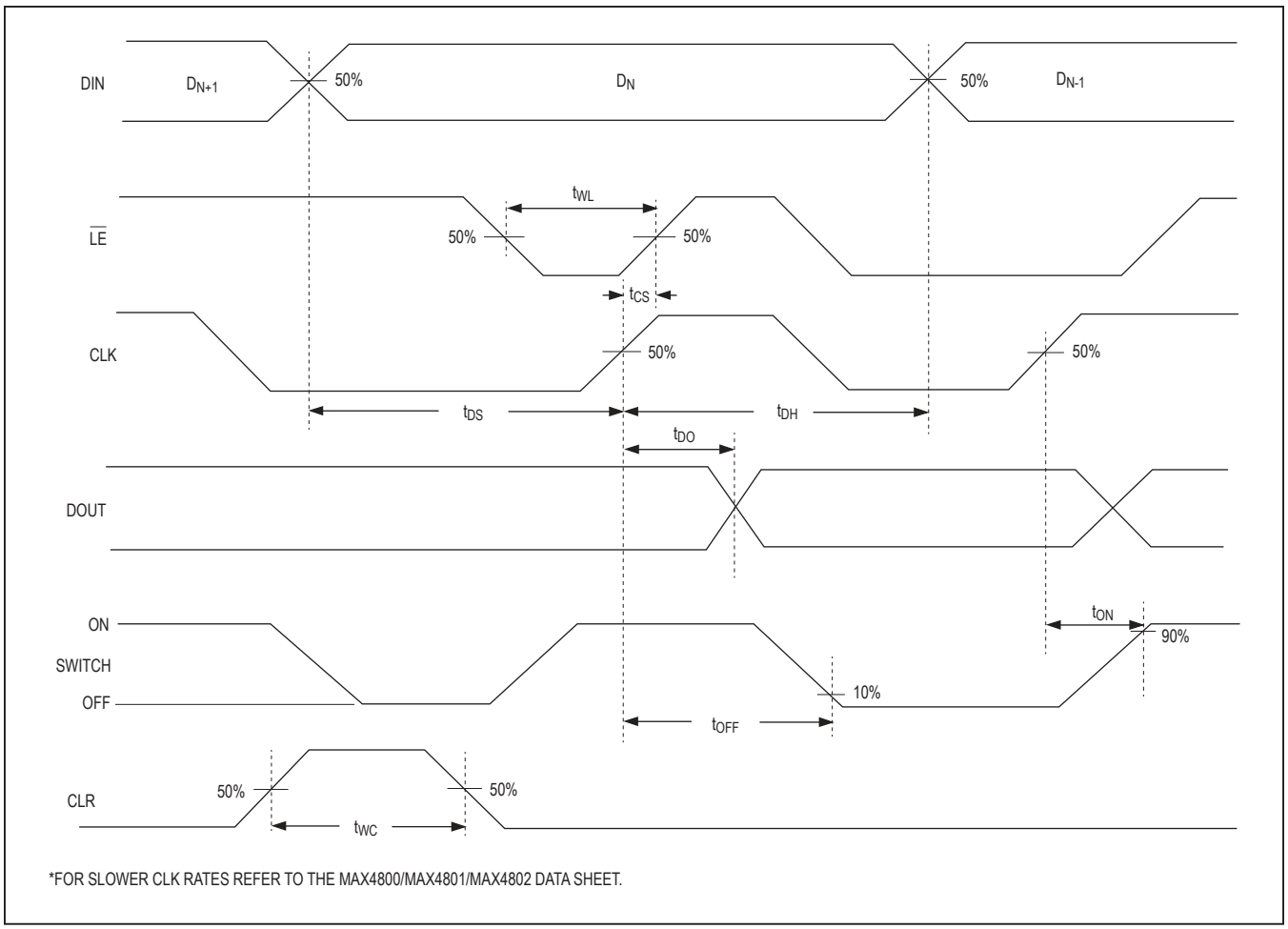


*Figure 1. Serial Interface Timing**

Detailed Description

The MAX4800A/MAX4802A provide high-voltage switching on eight channels for ultrasound imaging and printer applications. The devices utilize BCDMOS process technology to provide eight high-voltage low-charge-injection SPST switches, controlled by a 20MHz serial interface. Data is clocked into an internal 8-bit shift register and retained by a programmable latch with enable and clear inputs. A power-on reset function ensures that all switches are open on power-up.

The devices operate with a wide range of high-voltage supplies including: V_{PP}/V_{NN} = +100V/-100V, +185V/-15V, or +40V/-160V. The digital interface operates from a separate V_{DD} supply from +2.7V to +6V. Digital inputs DIN, CLK, $\overline{LE}$, and CLR are +6V tolerant, independent of the V_{DD} supply voltage. The MAX4802A provides integrated 35kΩ bleed resistors on each switch terminal to discharge capacitive loads.

The devices are drop-in replacements for the Supertex HV2203 and HV2303, respectively.

Analog Switch

The devices allow a peak-to-peak analog-signal range from V_{NN} + 10V to V_{PP} - 10V. Analog switch inputs must be unconnected, or satisfy $V_{NN} \le (V_{COM_}, V_{NO_}) \le V_{PP}$ during power-up and power-down.

High-Voltage Supplies

The devices allow a wide range of high-voltage supplies. The devices operate with V_{NN} from -160V to -15V and V_{PP} from +40V to (V_{NN} + 200V). When V_{NN} is connected to GND (single-supply applications), the devices operate with V_{PP} up to +200V.

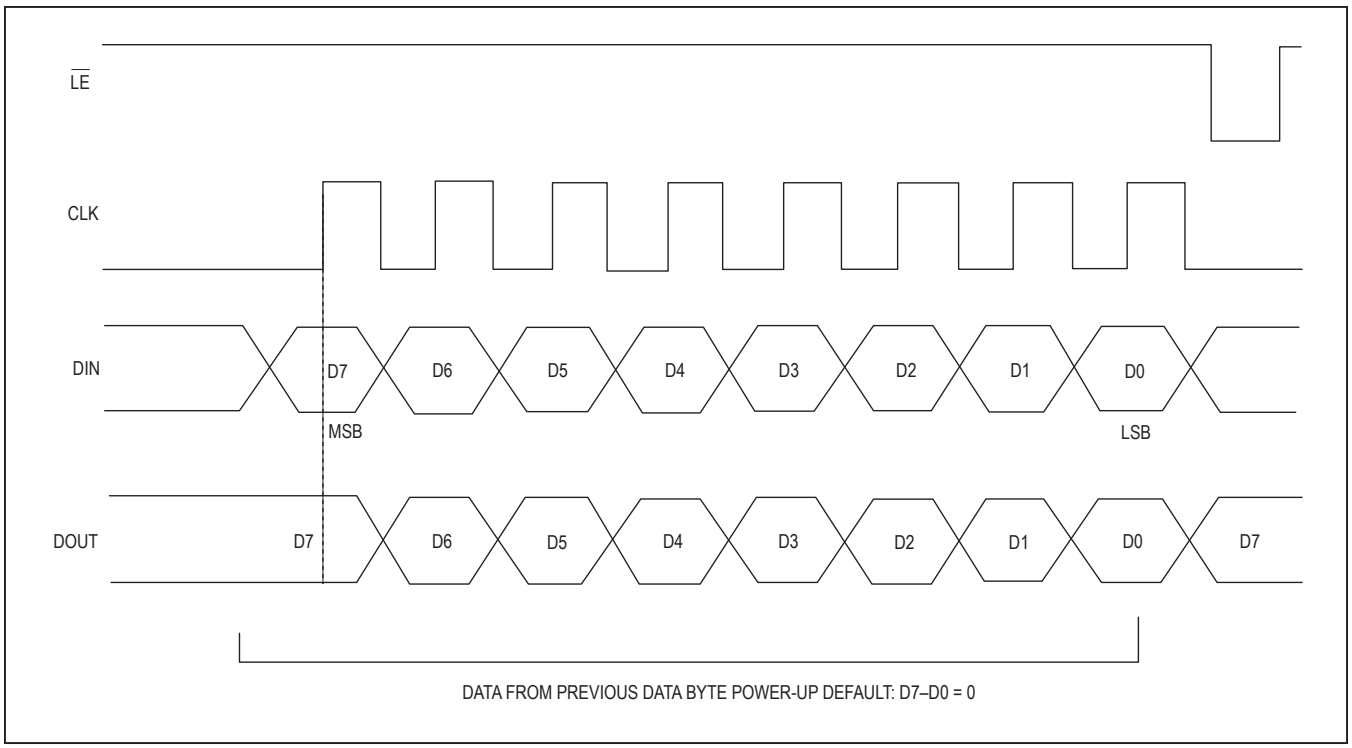


Figure 2. Latch-Enable Interface Timing

The V_{PP} and V_{NN} high-voltage supplies are not required to be symmetrical, but the voltage difference V_{PP} - V_{NN} must not exceed 200V.

Bleed Resistors (MAX4802A)

The MAX4802A features integrated 35kΩ bleed resistors to discharge capacitive loads such as piezoelectric transducers. Each analog-switch terminal is connected to RGND with a bleed resistor.

Serial Interface

The devices are controlled by a serial interface with an 8-bit serial shift register and transparent latch. Each of the eight data bits controls a single analog switch (see Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by eight clock cycles (see Figures 1 and 2).

Latch Enable ($\overline{LE}$)

Drive $\overline{LE}$ logic-low to change the contents of the latch and update the state of the high-voltage switches (Figure 2). Drive $\overline{LE}$ logic-high to freeze the contents of the latch and prevent changes to the switch states. To reduce noise due to clock feedthrough, drive $\overline{LE}$ logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse $\overline{LE}$ logic-low to load the contents of the shift register into the latch.

Latch Clear (CLR)

The devices feature a latch clear input. Drive CLR logic-high to reset the contents of the latch to zero and open all switches. CLR does not affect the contents of the data shift register. Pulse $\overline{LE}$ logic-low to reload the contents of the shift register into the latch.

Power-On Reset

The devices feature a power-on reset circuit to ensure all switches are open at power-on. The internal 8-bit serial shift register and latch are set to zero on power-up.

Table 1. Serial Interface Programming

DATA BITS								CONTROL BITS		FUNCTION							
D0 (LSB)	D1	D2	D3	D4	D5	D6	D7 (MSB)	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	Off	Off	Off	Off	Off	Off	Off	Off

X = Don't care.

Applications Information

Logic Levels

The devices' digital interface inputs CLK, DIN, $\overline{LE}$, and CLR are tolerant of up to +6V, independent of the V_{DD} supply voltage, allowing compatibility with higher voltage controllers.

Daisy Chaining Multiple Devices

Digital output DOUT is provided to allow the connection of multiple devices by daisy-chaining (Figure 3). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK, $\overline{LE}$, and CLR inputs of all devices, and drive $\overline{LE}$ logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously. Additional shift registers may be included anywhere in series with the MAX4800A/MAX4802A data chain.

Supply Sequencing and Bypassing

The devices do not require special sequencing of the V_{DD}, V_{PP}, and V_{NN} supply voltages; however, analog switch inputs must be unconnected, or satisfy $V_{NN} \le (V_{COM_}, V_{NO_}) \le V_{PP}$ during power-up and power-down. Bypass V_{DD}, V_{NN}, and V_{PP} to GND with a 0.1µF ceramic capacitor as close to the device as possible.

Chip Information

PROCESS: BCDMOS

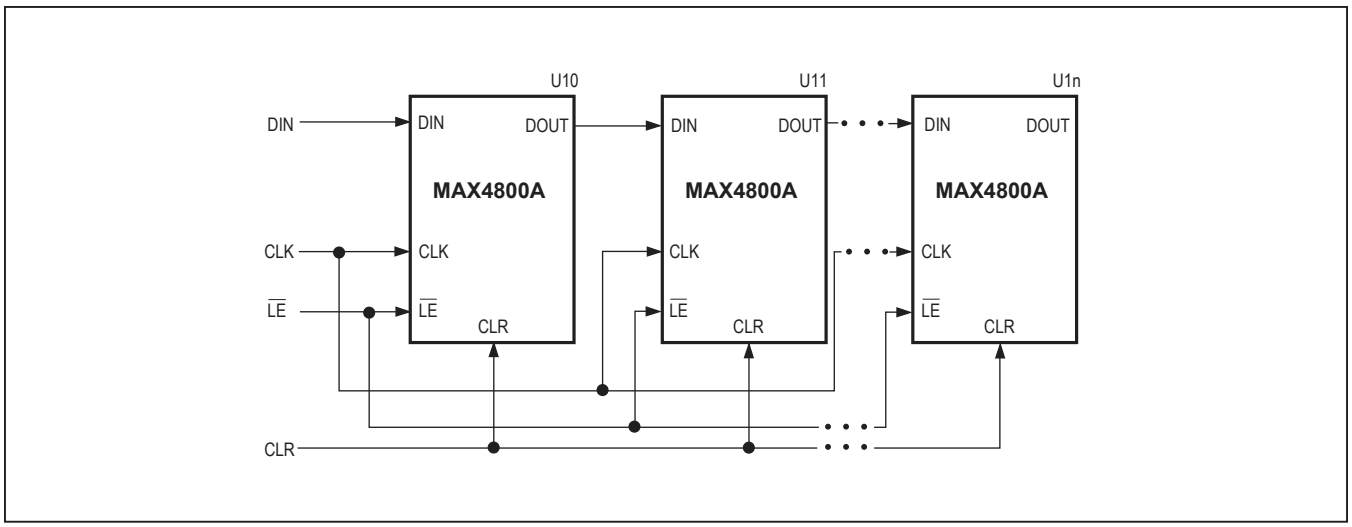
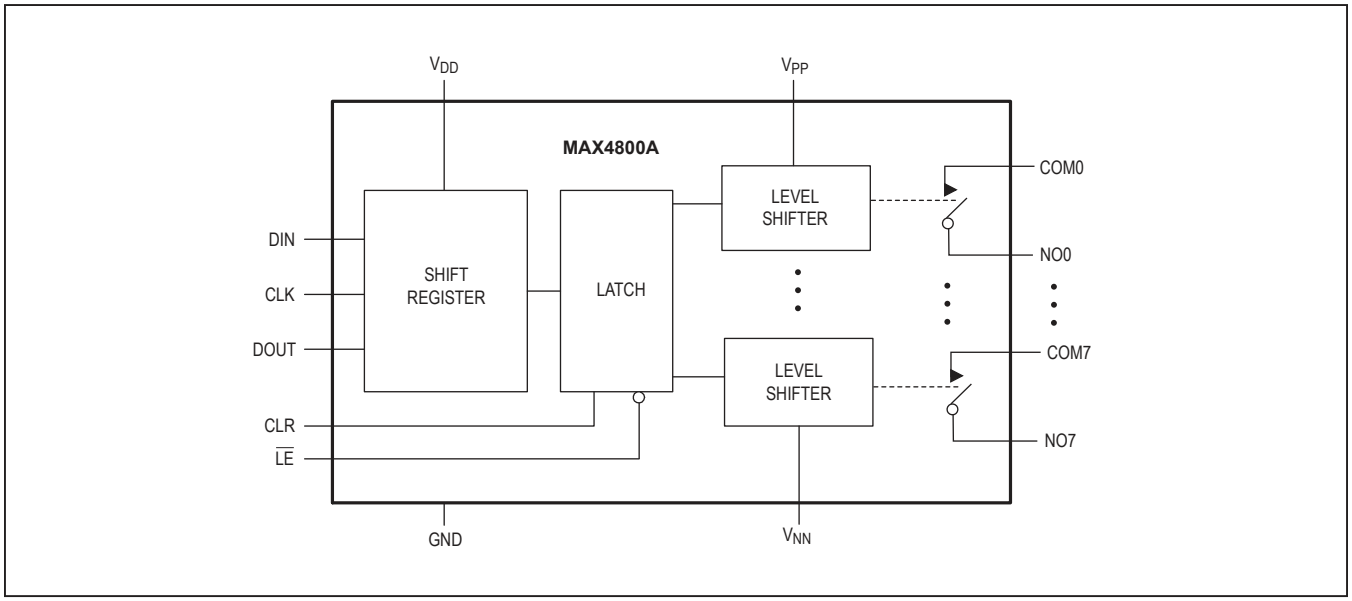
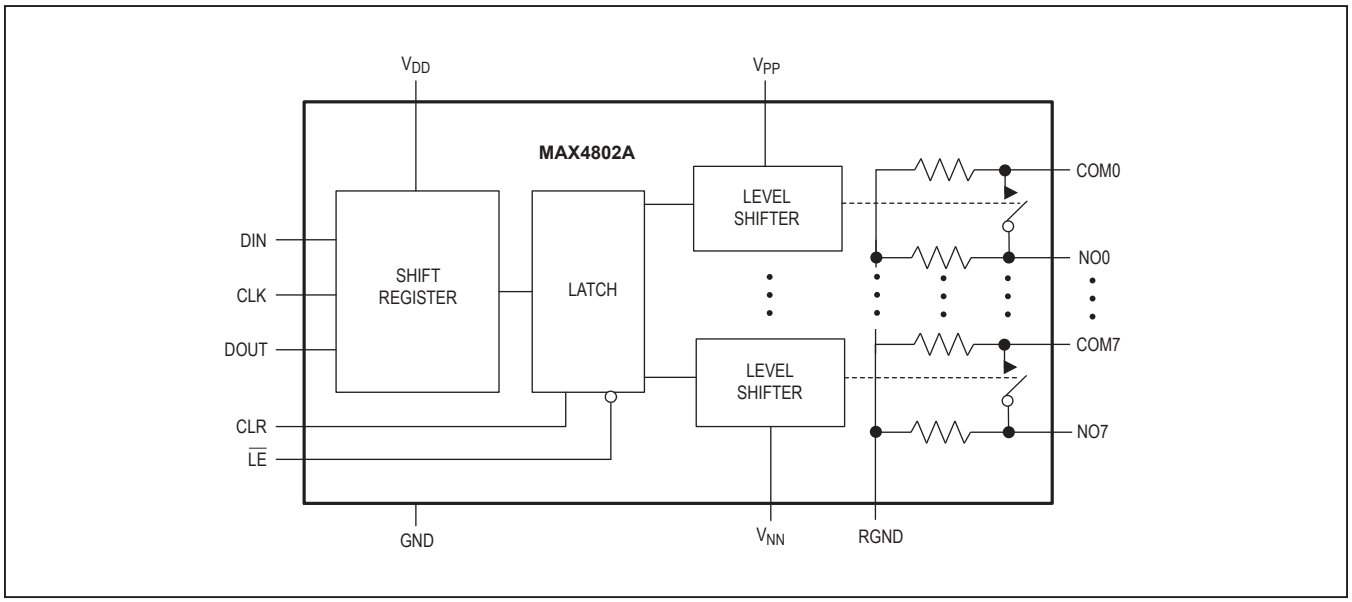


Figure 3. Interfacing Multiple Devices by Daisy-Chaining

Functional Diagrams



Functional Diagrams (continued)



Ordering Information/ Selector Guide

PART	BLEED RESISTORS	SECOND SOURCE	PIN-PACKAGE
MAX4800ACXZ+*	No	—	26 CSBGA
MAX4800ACQI+	No	HV2203PJ-G	28 PLCC
MAX4800ACCM+*	No	HV2203FG-G	48 LQFP
MAX4802ACXZ+*	Yes	—	26 CSBGA
MAX4802ACQI+	Yes	HV2303PJ-G	28 PLCC
MAX4802ACCM+*	Yes	HV2303FG-G	48 LQFP

Note: *All devices are specified over the commercial 0°C to +70°C temperature range.*

**Future product—contact factory for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	2/11	Changed the DC analog-signal frequency range to 50MHz in the *Features* section; changed the TQFP package to LQFP in the *General Description*, *Ordering Information*, *Features*, *Pin/Bump Configuration*s, *Pin/Bump Descriptions*, and *Package Information*	1, 8, 14
2	4/19	Updated the *Electrical Characteristics* section	5

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