19-4605; Rev 0; 6/09

16-Bit, Mixed-Signal Microcontroller with Op Amps, ADC, and DACs for All-in-One Servo Loop Control

MAXQ8913

General Description

The MAXQ8913 is a single-chip servo controller designed as a complete solution for dual axis optical image stabilization (OIS) applications. The device incorporates all the necessary elements for conditioning of sensor signals, analog-to-digital conversion, digital servo algorithm implementation using a 16-bit RISC microcontroller, and digital-to-analog conversion, as well as including dual servo amplifiers.

Even though the device is targeted for OIS applications, it can be effectively used in many other types of servo control. The MAXQ8913 supports both voice coil and stepper motor applications.

The MAXQ8913 includes four op amps; a 7-channel, 12-bit ADC; dual 10-bit differential DACs; and dual 8-bit single-ended DACs. It also contains 64KB of flash memory, 4KB of RAM, 4KB of ROM, a 16-bit timer/counter, a universal asynchronous/synchronous receiver-transmitter (USART), an I^2C port, and an SPI™ master/slave port.

For the ultimate in low-power performance, the OIS device includes a low-power sleep mode, the ability to selectively disable peripherals, and multiple power-saving operating modes.

Applications

Digital Camera and Cell Phone Optical Image Stabilization

Servo Loop Control

Tone Generation with Speaker Drive

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXQ8913EWG+T	-40°C to +85°C	58 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Pin Configuration appears at end of data sheet.

Features

- **High-Performance, Low-Power, 16-Bit MAXQ® RISC Core**
- **One-Cycle, 16 x 16 Hardware Multiply/Accumulate with 48-Bit Accumulator**
- **Two Current Sinks for Driving Hall-Effect Elements**
- **Four DACs**
- **DC to 10MHz Operation; Approaching 1MIPS per MHz**
- **2.7V to 3.6V Logic/Analog Operating Voltage**
- **33 Instructions, Most Single Cycle**
- **Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement**
- **16-Level Hardware Stack**
- **16-Bit Instruction Word, 16-Bit Data Bus**
- **16 x 16-Bit General-Purpose Working Registers**
- **Optimized for C Compilers**
- **Memory Features**
  - 64KB Flash Memory
  - 4KB of Internal Data RAM
  - 4KB of Utility ROM
  - JTAG Bootloader for Programming and Debug
- **Peripherals**
  - Four Operational Amplifiers
  - 12-Bit SAR ADC with Internal Reference and Autoscan
    - Up to 312ksps Sample Rate
    - Seven-Input Mux (Four Internally Connected to Op-Amp Outputs, One Internally Connected to Temp Sensor, and Two Connected to Uncommitted External Pins)
  - Brownout Reset Generation
  - 16-Bit Programmable Timer/Counter
  - USART, I^2C, and SPI Master/Slave
  - On-Chip Power-On Reset/Brownout Reset
  - Programmable Watchdog
- **Low-Power Consumption**
  - 3mA (max) at 10MHz Flash Operation at 3.3V
  - 4.5µA (max) in Stop Mode
  - Low-Power Power-Management Mode (PMM)

SPI is a trademark of Motorola, Inc.

MAXQ is a registered trademark of Maxim Integrated Products, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

16-Bit, Mixed-Signal Microcontroller with Op Amps, ADC, and DACs for All-in-One Servo Loop Control

ABSOLUTE MAXIMUM RATINGS

Voltage Range on All Pins (including AVDD, DVDD) Relative to Ground .....-0.5V to +3.6V
Voltage Range on Any Pin Relative to Ground except AVDD, DVDD.....-0.5V to (V_{DVDD} + 0.5V)
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	V_{DVDD}	V_{AVDD} = V_{DVDD}	V_{RST}	3.3	3.6	V
Digital Operating Voltage			V_{RST}		3.6	V
Regulator Voltage Output	V_{REG18}	(Note 2)	1.71	1.8	1.89	V
Analog Supply Voltage	V_{AVDD}	V_{AVDD} = V_{DVDD}	2.7		3.6	V
Ground	GND	AGND = DGND	0	0	0	V
Digital Power-Fail Reset Voltage	V_{RST}	Monitors V_{DVDD}	2.58		2.68	V
Active Current (Note 3)	I_{DD_HFX3}	f_{CK} = 10MHz, V_{DVDD} = 2.7V			2.2	mA
	I_{DD_HFX4}	f_{CK} = 10MHz, V_{DVDD} = 3.3V			3.0	
Stop-Mode Current	I_{STOP_1}	(Notes 4, 5)		0.2	4.5	µA
	I_{STOP_2}	(Notes 4, 6)			40	
	I_{STOP_3}	(Notes 4, 7)			500	
Stop-Mode Resume Time	t_{STOP_1}	Internal regulator on		15		µs
	t_{STOP_2}	Internal regulator off, brownout or SVM on		375		
Input Low Voltage on HFXIN	V_{IL1}		V_{DGND}		0.20 x V_{DVDD}	V
Input Low Voltage on All Other Port Pins	V_{IL2}		V_{DGND}		0.30 x V_{DVDD}	V
Input High Voltage on HFXIN	V_{IH1}		0.75 x V_{DVDD}		V_{DVDD}	V
Input High Voltage on All Other Port Pins	V_{IH2}		0.70 x V_{DVDD}		V_{DVDD}	V
Input Hysteresis (Schmitt)	V_{IHYS}			0.18		V
Output Low Voltage for All Port Pins Except SHDNL, SHDNR	V_{OL}	I_{OL} = 4mA (Note 8)	V_{DGND}		0.4	V
Output Low Voltage for SHDNL, SHDNR	V_{OL}	I_{OL} = 1.5mA	V_{DGND}		0.4	V
Output High Voltage for All Port Pins	V_{OH}	I_{OH} = -4mA (Note 8)	V_{DVDD} - 0.4			V
I/O Pin Capacitance	C_{IO}	Guaranteed by design			15	pF

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Current for Port Pins	I_{IL}	V_{IN} = 0.4V			100	µA
Input-Leakage Current	I_L	Internal pullup disabled	-300		+300	nA
Input Pullup Resistor	R_{PU}		30	70	110	kΩ
CLOCK SOURCE						
External Clock Frequency	f_{HFIN}		DC		10	MHz
External Clock Duty Cycle	t_{XCLK_DUTY}		40		60	%
Internal Ring Oscillator				1		MHz
System Clock Frequency	f_{CK}		DC		10	MHz
FLASH AC CHARACTERISTICS						
System Clock During Flash Programming/Erase			2			MHz
Program Time	t_{PROG}		20		40	µs
Page Erase Time	$t_{ERASETME}$		20		40	ms
Mass Erase Time			20		40	ms
Write/Erase Cycles			1000			Cycles
Data Retention		T_A = +25°C	100			Years
ANALOG-TO-DIGITAL CONVERTER (Note 9)						
ADC Clock Frequency	f_{SCLK}		0.1		5	MHz
Input Voltage Range	V_{AIN}	Unipolar (single-ended)	0		V_{REF}	V
		Bipolar (differential) (Note 10)	$-V_{REF}/2$		$+V_{REF}/2$	
Analog Input Capacitance	C_{AIN}			16		pF
Current Consumption	I_{AVDD1}	f_{SCLK} = 5MHz, internal reference			3.0	mA
	I_{AVDD2}	f_{SCLK} = 5MHz, external reference (internal reference disabled)			800	µA
	I_{ASTOP}	Power-down mode			2.5	
ANALOG-TO-DIGITAL CONVERTER PERFORMANCE (V_{REF} = 3V, 0.1µF capacitor on REFA, f_{SCLK} = 5MHz)						
Resolution				12		Bits
Integral Nonlinearity	INL			±1	±2	LSB
Differential Nonlinearity	DNL	No missing codes from +25°C to +85°C			±1	LSB
Offset Error					±10	LSB
Gain Error					±1	%
Gain Temperature Coefficient				±0.5		ppm/°C
Signal-to-Noise Plus Distortion	SINAD	f_{IN} = 1kHz	69			dB
Spurious-Free Dynamic Range	SFDR	f_{IN} = 1kHz	76			dB
Throughput		16f_{SCLK} samples			312	ksps
ADC Setup Time	t_{ADC_SETUP}	(Note 11)			4	µs
Input-Leakage Current	I_{ILA}	Shutdown or conversion stopped; AIN0/AIN1 and V_{AEREF}			±1	µA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Autoscan Throughput		All channels active			39	ksps per channel
ANALOG-TO-DIGITAL CONVERTER REFERENCE						
Internal Reference Voltage	V_{AIREF}		1.44	1.5	1.56	V
Internal Reference Voltage Startup Time	t_{AIREF}				50	µs
External Reference Voltage Input	V_{AEREF}		0.9		V_{AVDD} + 0.05	V
Internal Reference Voltage Drift	V_{ADRIFT}	Guaranteed by design			±50	ppm/°C
Reference Settle Time (Switching ADC Reference from Either Internal or External Reference to AVDD)	t_{AAVDD_SETUP}	(Note 12)			4	Samples
Reference Output	V_{REFA}			V_{REF}		V
SUPPLY VOLTAGE MONITOR						
Supply Voltage Set Point	S_{VTR}		2.7		3.5	V
Supply Voltage Increment Resolution			80	100	120	mV
Supply Voltage Default Set Point				2.7		V
Supply Voltage Monitor Start Time	t_{SVMST}				50	µs
Supply Voltage Monitor Setup Time	t_{SVM_SU1}	Changing from one set point to another set point			2	µs
	t_{SVM_SU2}	Exit from stop mode			8	
CLASS D AMPLIFIER CONTROL DACs, 10-BIT DACs						
Resolution			10			Bits
Full-Scale Output Voltage	VFS	Code 0 = -2.5, code 1023 = +2.5, V_{REF} = 1.5V	±2.3	±2.5	±2.8	V
Output Common-Mode Voltage	VCM		1.15	1.25	1.4	V
DC Output Impedance	ZOUT	At DC, per side		10		kΩ
Integral Nonlinearity	INL			±2		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic by design	-1	±0.10		LSB
Settling Time		From 1/4 FS to 3/4 FS to 1 LSB		2		µs
Digital Feedthrough				0.15		nV-s
Glitch Impulse		Major carry transition		12		nV-s
Update Rate		(Note 13)	100			ksps

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC3 AND DAC4 INCLUDING BUFFER						
Resolution			8			Bits
Full-Scale Output Voltage	VFS	Code 0 = 0.35, code 255 = 2.35, V_{REF} = 1.5	0.30 to 2.20	0.35 to 2.35	0.45 to 2.7	V
Output Common-Mode Voltage	VCM	Code = 128, V_{REF} = 1.5V	1.25	1.35	1.55	V
DC Drive Capability	I_{DRIVE}	(Note 14)	1			mA
Integral Nonlinearity	INL			±1		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic by design	-1	±0.5		LSB
Settling Time		From 1/4 FS to 3/4 FS to 1 LSB		5		µs
Update Rate		(Note 14)	100			ksps
OP AMP A, B, C, D						
Offset Voltage	V_{OS}	V_{CM} = 2V	-8	±2	+8	mV
Offset Drift	$V_{OSDRIFT}$	V_{CM} = 2V		10		µV/°C
Input Bias Current	I_{BIAS}	T_A = +25°C (Note 13)			1	nA
Common-Mode Rejection Ratio	CMMR		60	80		dB
Gain Bandwidth Product	GB			> 200		kHz
Input Common-Mode Range	CMR_{NG}		1		V_{AVDD}	V
TEMPERATURE SENSOR						
Sensitivity		Code 0 = -273.15C; absolute 0; 8 LSB/°C for V_{REF} = 1.5V, 12-bit ADC; 4 LSB/°C for V_{REF} = 3.0V		2.9304		mV/°C
Raw Accuracy		No correction, T = 300°K (Note 14)	-6		+6	°C
CURRENT SINK						
Resolution		Code 0 = 0, code 1 = 62.5µA, code 255 = 15.94mA	8			Bits
Full-Scale Sink Current	I_{S15}	Code = 255, V_{DS} = 2V, V_{REF} = 1.5V	14.9	15.94	18.0	mA
Zero-Scale Sink Current	I_{S0}	Code = 0, V_{DS} = 2V		0	1	µA
LSB Size	LSB	V_{DS} = 2V, V_{REF} = 1.5V		62.5		µA
SPI: MASTER MODE (See Figures 1, 2)						
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{SYS}/2$	MHz
SCLK Output Pulse Width-High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2 - t_{RF}$			ns
I/O Rise/Fall Time (This parameter is device dependent.)	t_{RF}	C_L = 15pF, pullup = 560Ω			16	ns
MOSI Output Valid to SCLK Sample Edge (MOSI Setup)	t_{MOV}		$t_{MCK}/2 - t_{RF}$			ns
MOSI Output Hold After SCLK Sample Edge	t_{MOH}		$t_{MCK}/2 - t_{RF}$			ns

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DVDD} = V_{AVDD} = 2.7V to 3.6V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Last Sample Edge to MOSI Output Change (MOSI Last Hold)	t_{MLH}		t_{MCK}/ 2 - t_{RF}			ns
MISO Input Valid to SCLK Sample Edge (MISO Setup)	t_{MIS}	(Note 13)	$2t_{RF}$			ns
MISO Input Hold After SCLK Sample Edge	t_{MIH}		0			ns
SPI: SLAVE MODE (See Figures 1, 3)						
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{SYS}/4$	kHz
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		t_{SCK}/ 2 - t_{RF}			ns
I/O Rise/Fall Time (This parameter is device dependent.)	t_{RF}	C_L = 15pF, pullup = 560Ω			16	ns
$\overline{SSEL}$ Active to First Shift Edge	t_{SSE}		t_{RF}			ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		t_{RF}			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		t_{RF}			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}	(Note 13)			$2t_{RF}$	ns
$\overline{SSEL}$ Inactive to Next $\overline{SSEL}$ Asserted	t_{SSH}		t_{SYS} + t_{RF}			ns
SCLK Inactive to $\overline{SSEL}$ Deasserted	t_{SD}		t_{RF}			ns
MISO Output Disabled After $\overline{SSEL}$ Edge Deasserted	t_{SLH}				$2t_{SYS}$ + $2t_{RF}$	ns

Note 1: Specifications to -20°C are guaranteed by design and are not production tested.
Note 2: Connect to ground through a 1µF capacitor.
Note 3: Crystal connected to HFXIN, HFXOUT. Operating in /1 mode. Measured on the DVDD pin and the device not in reset. All inputs are connected to GND or DVDD. Outputs do not source/sink any current. One timer B enabled, with the device executing code from flash.
Note 4: I_{STOP} is the total current into the device when the device is in stop mode.
Note 5: Regulator, brownout disabled. Stop mode current through AVDD and DVDD.
Note 6: Regulator disabled, brownout enabled. Stop mode current through AVDD and DVDD.
Note 7: Regulator enabled, brownout enabled.
Note 8: $I_{OH(MAX)}$ + $I_{OL(MAX)}$ for all outputs combined should not exceed 35mA to meet the specification.
Note 9: V_{REF} = V_{AVDD}.
Note 10: The operational input voltage range for each individual input of a differentially configured pair is from GND to AVDD. The operational input voltage difference is from -V_{REF}/2 to +V_{REF}/2.
Note 11: The typical value is applied when a conversion is requested with ADPMO = 0. Under these conditions, the minimum delay is met. If ADPMO = 1, the user is responsible for ensuring the 4µs delay time is met.
Note 12: Total on-board decoupling capacitance on the AVDD pin < 100nF. The output impedance of the regulator driving the AVDD pin < 10Ω.
Note 13: This value is the sum of input R/F and output R/F.
Note 14: Guaranteed by design and characterization.

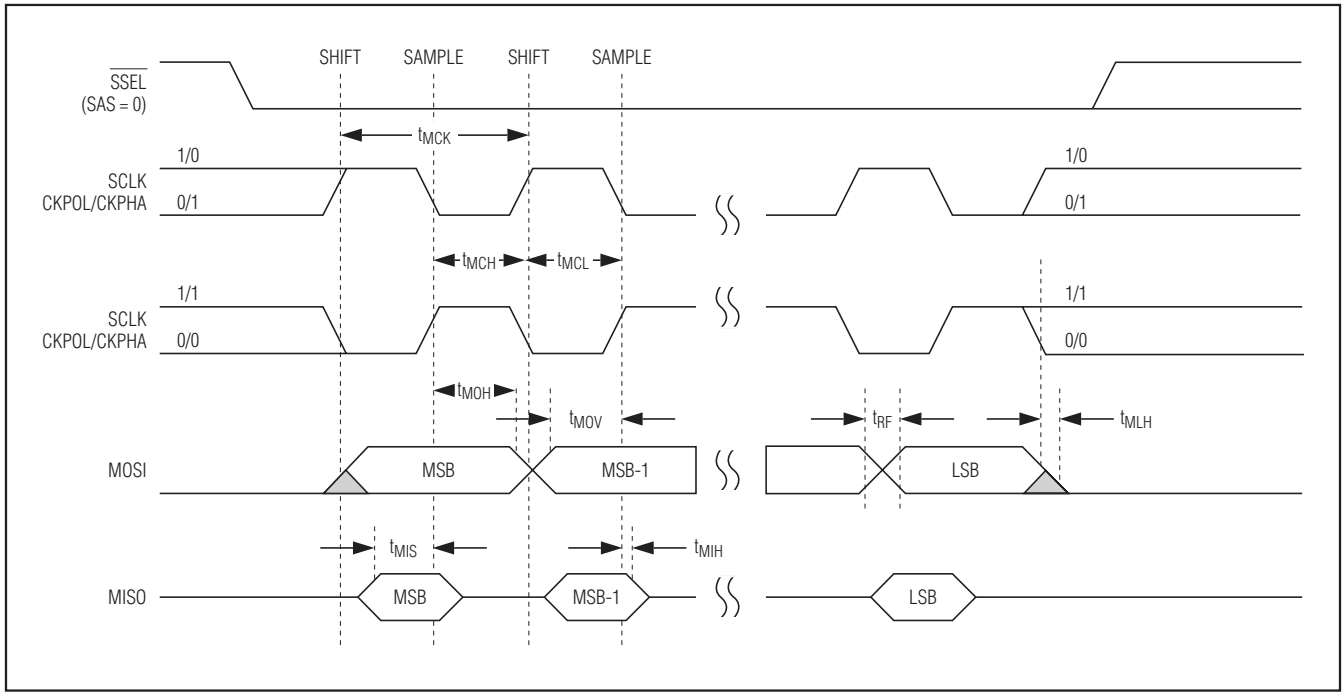

Figure 1. Enhanced SPI Master Timing

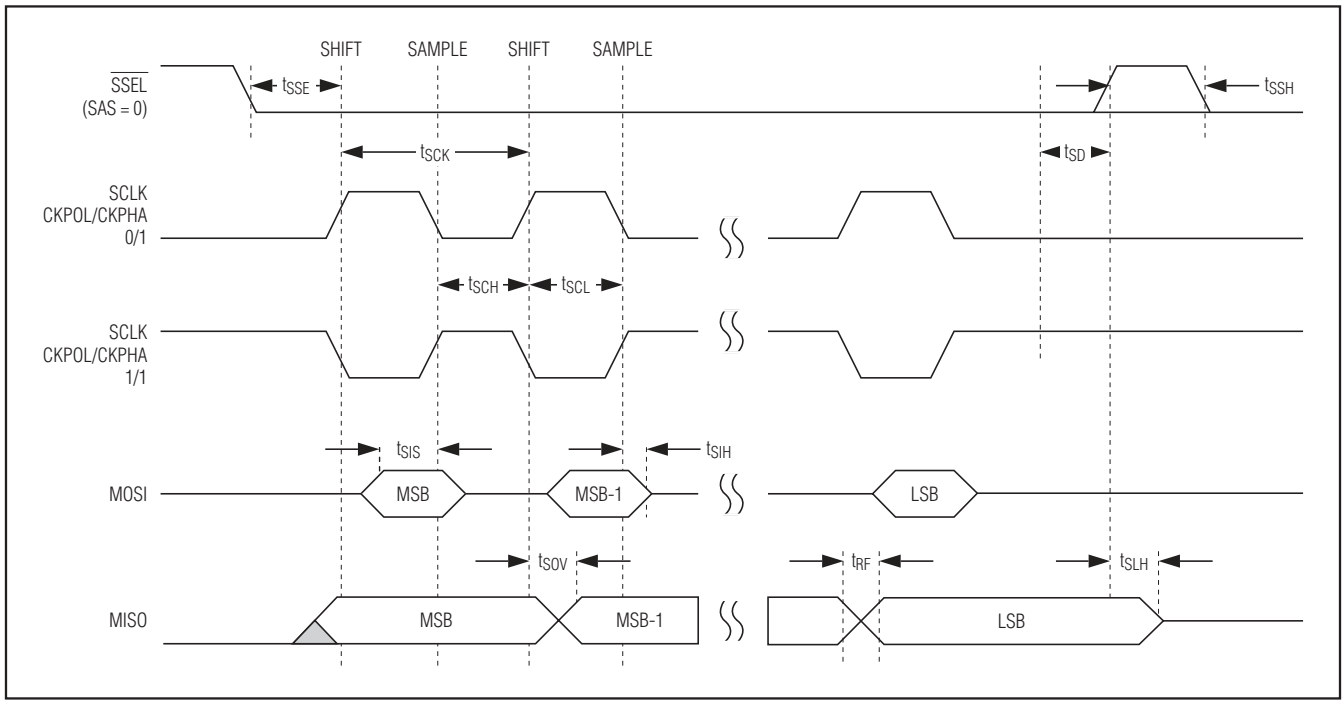

Figure 2. Enhanced SPI Slave Mode Timing (CKPHA = 1)

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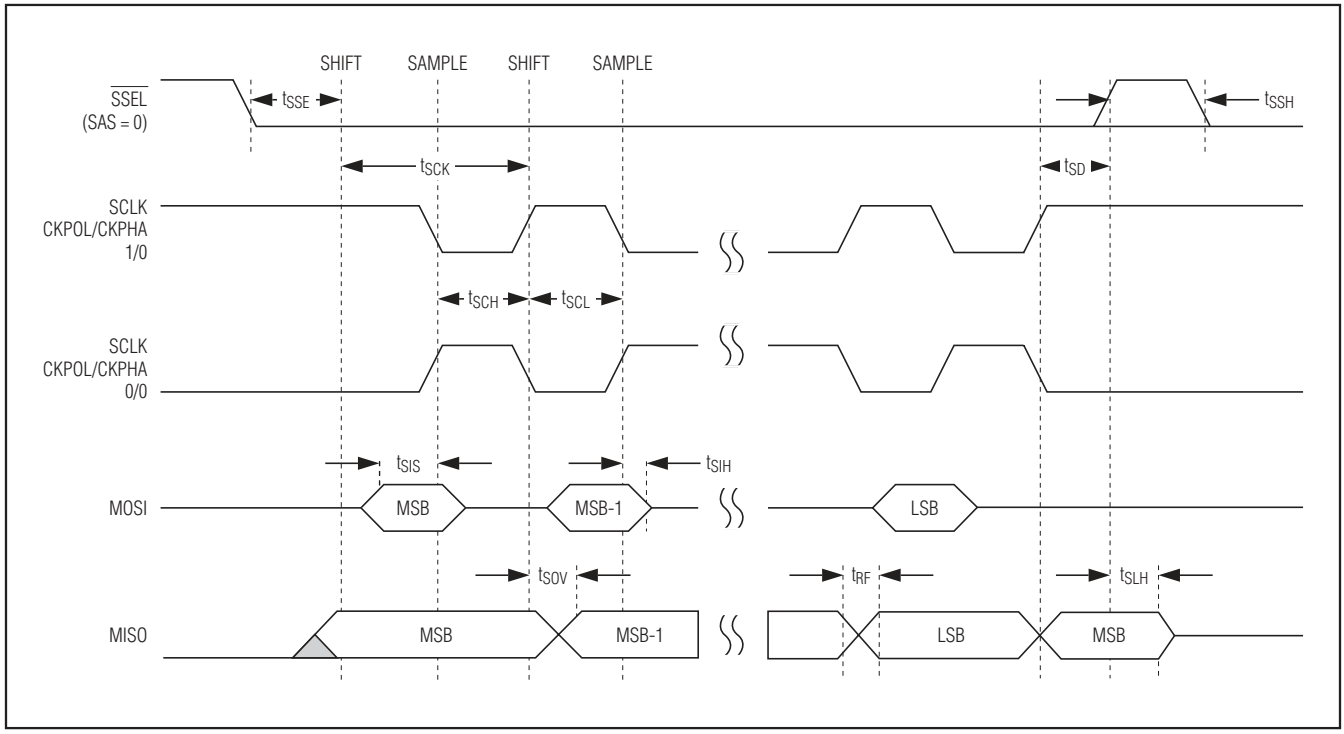

Figure 3. Enhanced SPI Slave Mode Timing (CKPHA = 0)

I²C BUS CONTROLLER AC CHARACTERISTICS

(V_{DVDD} = 1.8V to 3.6V, T_A = -40°C to +85°C.) (See Figure 4.)

PARAMETER	SYMBOL	TEST CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Input Low Voltage	V_{IL_I2C}		-0.5	0.3 x V_{DVDD}	-0.5	0.3 x V_{DVDD} (Note 15)	V
Input High Voltage	V_{IH_I2C}		0.7 x V_{DVDD}		0.7 x V_{DVDD}	(Note 16)	V
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	V_{DVDD} > 2V			0.05 x V_{DVDD}		V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DVDD} > 2V, 3mA sink current	0	0.4	0	0.4	V
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with Bus Capacitance from 10pF to 400pF (Notes 17, 18)	t_{OF_I2C}			250	20 + 0.1C_B	250	ns
Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter	t_{SP_I2C}				0	50	ns
Input Current Each I/O Pin with an Input Voltage Between 0.1 x V_{DVDD} and 0.9 x $V_{DVDD(MAX)}$ (Note 19)	I_{IN_I2C}		-10	+10	-10	+10	µA
I/O Capacitance	C_{IO_I2C}			10		10	pF

Note 15: Devices that use nonstandard supply voltages that do not conform to the intended I²C-bus system levels must relate their input levels to the V_{DVDD} voltage to which the pullup resistors R_P are connected.

Note 16: Maximum V_{IH_I2C} = $V_{DVDD(MAX)}$ + 0.5V.

Note 17: C_B = capacitance of one bus line in pF.

Note 18: The maximum fall time of 300ns for the SDA and SCL bus lines as shown in the *I²C Bus Controller Timing* table is longer than the specified maximum t_{OF_I2C} of 250ns for the output stages. This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in the *I²C Bus Controller Timing (Acting as I²C Slave)* table without exceeding the maximum specified fall time. See Figure 4.

Note 19: I/O pins of fast-mode devices must not obstruct the SDA and SCL lines if V_{DVDD} is switched off.

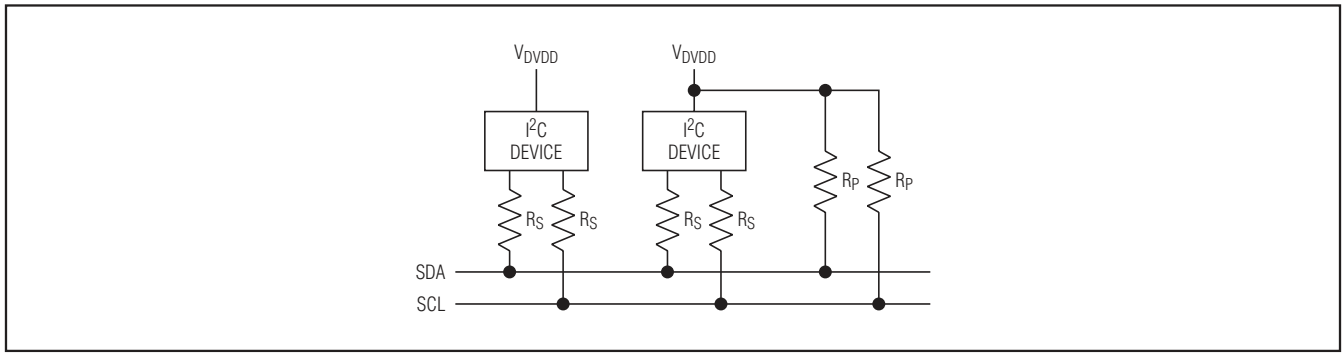

Figure 4. Series Resistors (R_S) for Protecting Against High-Voltage Spikes

I²C BUS CONTROLLER TIMING

(All values referenced to $V_{IH\_I2C(MIN)}$ and $V_{IL\_I2C(MAX)}$. See Figure 5.)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
Operating Frequency	f_{I2C}	0	100	0	400	kHz
Hold Time After (Repeated) START	$t_{HD:STA}$	4.0		0.6		µs
Clock Low Period	t_{LOW_I2C}	4.7		1.3		µs
Clock High Period	t_{HIGH_I2C}	4.0		0.6		µs
Setup Time for Repeated START	$t_{SU:STA}$	4.7		0.6		µs
Hold Time for Data (Notes 20, 21)	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Setup Time for Data (Note 22)	$t_{SU:DAT}$	250		100		ns
SDA/SCL Fall Time (Note 23)	t_{F_I2C}		300	$20 + 0.1C_B$	300	ns
SDA/SCL Rise Time (Note 23)	t_{R_I2C}		1000	$20 + 0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$	4.0		0.6		µs
Bus-Free Time Between STOP and START	t_{BUF}	4.7		1.3		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{NL_I2C}	$0.1 \times V_{DVDD}$		$0.1 \times V_{DVDD}$		V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{NH_I2C}	$0.2 \times V_{DVDD}$		$0.2 \times V_{DVDD}$		V

Note 20: A device must internally provide a hold time of at least 300ns for the SDA signal (referenced to the $V_{IH\_I2C(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 21: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW_I2C}) of the SCL signal.

Note 22: A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R\_I2C(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ (according to the standard-mode I²C specification) before the SCL line is released.

Note 23: C_B = Total capacitance of one bus line in pF.

I²C BUS CONTROLLER TIMING (ACTING AS I²C MASTER)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
System Frequency	f_{SYS}	1		3.60		MHz
Operating Frequency	f_{I2C}		$f_{SYS}/8$		$f_{SYS}/8$	Hz
Hold Time After (Repeated) START	$t_{HD:STA}$	t_{HIGH_I2C}		t_{HIGH_I2C}		µs
Clock Low Period	t_{LOW_I2C}	5		5		t_{SYS}
Clock High Period	t_{HIGH_I2C}	3		3		t_{SYS}
Setup Time for Repeated START	$t_{SU:STA}$	t_{LOW_I2C}		t_{LOW_I2C}		µs
Hold Time for Data	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Setup Time for Data	$t_{SU:DAT}$	250		100		ns
SDA/SCL Fall Time	t_{F_I2C}		300	$20 + 0.1C_B$	300	ns
SDA/SCL Rise Time	t_{R_I2C}		1000	$20 + 0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$	t_{HIGH_I2C}		t_{HIGH_I2C}		µs
Bus-Free Time Between STOP and START	t_{BUF}	t_{LOW_I2C}		t_{LOW_I2C}		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{NL_I2C}	$0.1 \times V_{DVDD}$		$0.1 \times V_{DVDD}$		V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{NH_I2C}	$0.2 \times V_{DVDD}$		$0.2 \times V_{DVDD}$		V

I²C BUS CONTROLLER TIMING (ACTING AS I²C SLAVE)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
System Frequency	f_{SYS}	1		3.60		MHz
Operating Frequency	f_{I2C}		$f_{SYS}/8$		$f_{SYS}/8$	Hz
System Clock Period	t_{SYS}	$1/f_{I2C}$			$1/f_{I2C}$	µs
Hold Time After (Repeated) START	$t_{HD:STA}$	$3t_{SYS}$		$3t_{SYS}$		µs
Clock Low Period	t_{LOW_I2C}	$5t_{SYS}$		$5t_{SYS}$		µs
Clock High Period	t_{HIGH_I2C}	$3t_{SYS}$		$3t_{SYS}$		µs
Setup Time for Repeated START	$t_{SU:STA}$	$5t_{SYS}$		$5t_{SYS}$		µs
Hold Time for Data	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Setup Time for Data	$t_{SU:DAT}$	250		100		ns
SDA/SCL Fall Time	t_{F_I2C}		300	$20 + 0.1C_B$	300	ns
SDA/SCL Rise Time	t_{R_I2C}		1000	$20 + 0.1C_B$	300	ns
Setup Time for STOP	$t_{SU:STO}$	$3t_{SYS}$		$3t_{SYS}$		µs
Bus-Free Time Between STOP and START	t_{BUF}	$5t_{SYS}$		$5t_{SYS}$		µs
Capacitive Load for Each Bus Line	C_B		400		400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{NL_I2C}	$0.1 \times V_{DVDD}$		$0.1 \times V_{DVDD}$		V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{NH_I2C}	$0.2 \times V_{DVDD}$		$0.2 \times V_{DVDD}$		V

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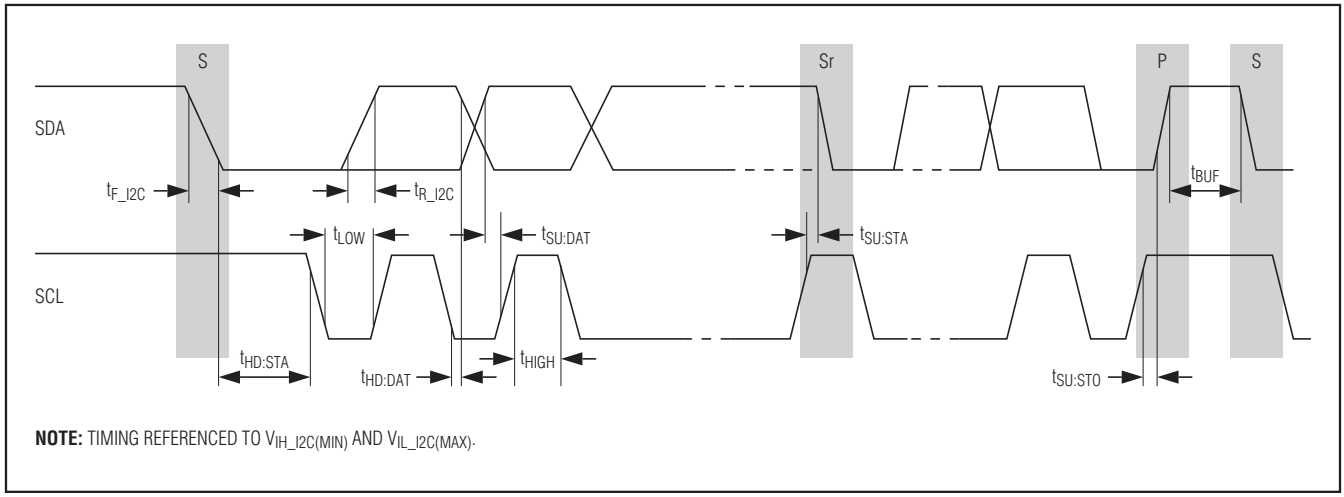

NOTE: TIMING REFERENCED TO $V_{IH\_I2C(MIN)}$ AND $V_{IL\_I2C(MAX)}$.

Figure 5. I²C Timing Diagram

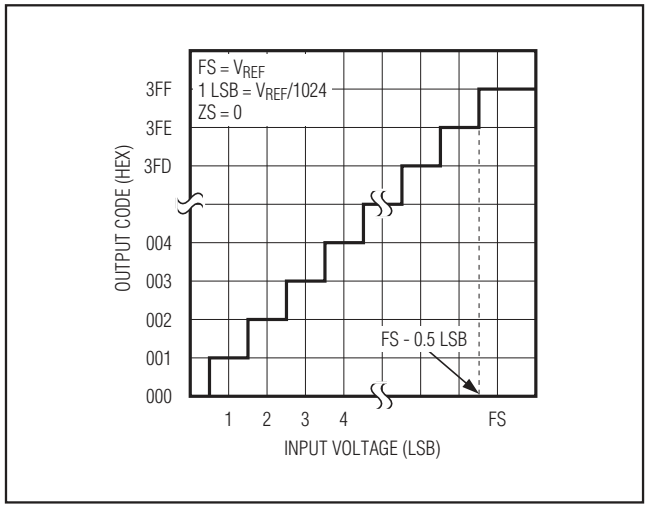

Figure 6. Single-Ended Unipolar Transfer Function

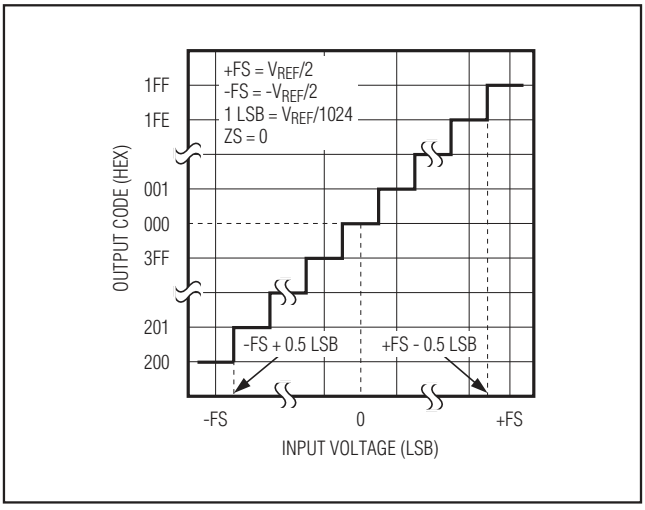

Figure 7. Differential Bipolar Transfer Function

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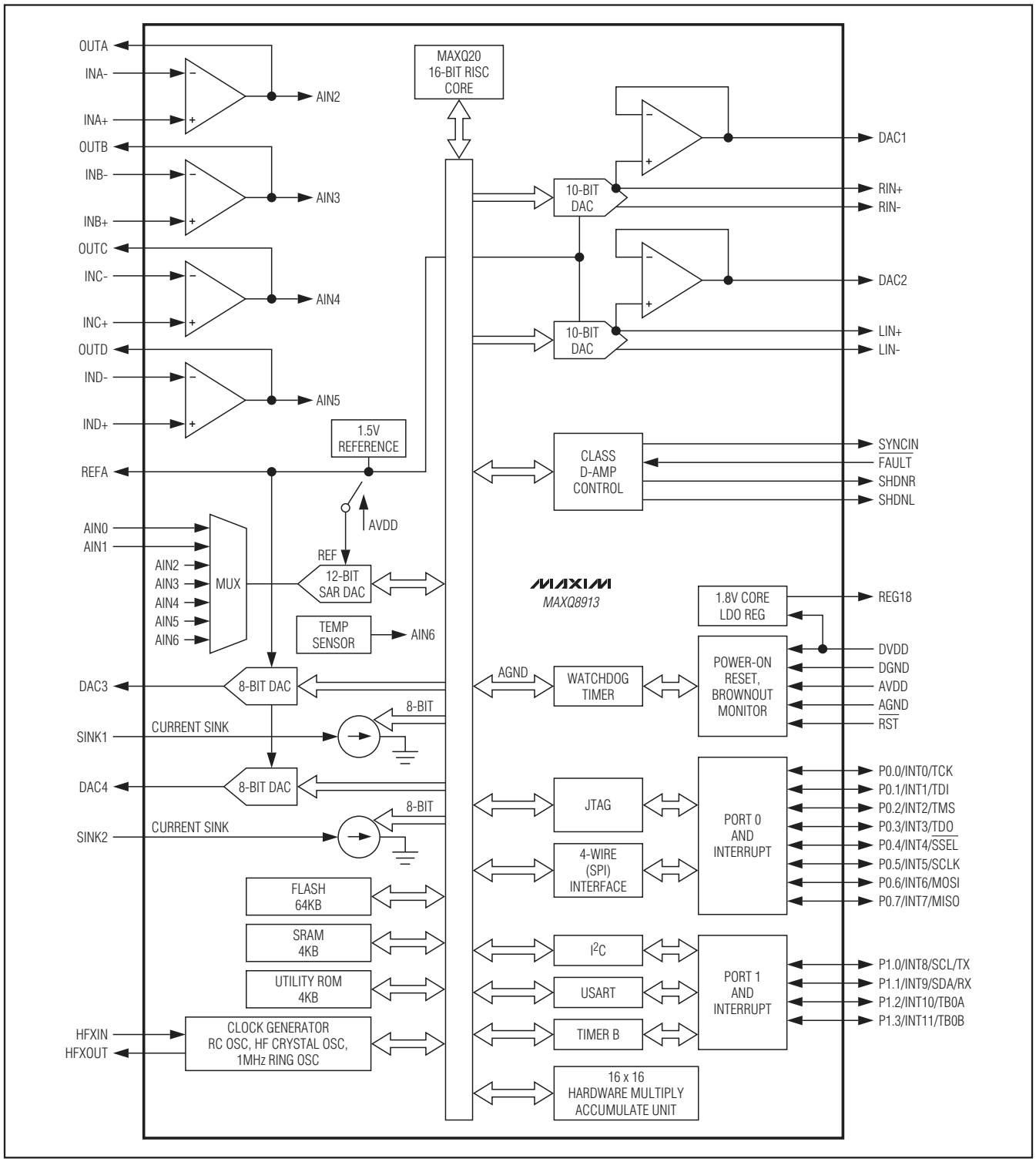
Block Diagram



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Pin Description

PIN	NAME	FUNCTION
		POWER PINS
L4	DVDD	Digital Supply Voltage
M5	DGND	Digital Ground
E4	AVDD	Analog Supply Voltage
B5	AGND	Analog Ground
K1	REG18	Regulator Output. This pin must be connected to ground through a 1.0µF capacitor. It provides the 1.8V internal regulated output. This pin is not meant to provide power externally.
		ANALOG MEASUREMENT PINS
G2	REFA	Analog Voltage Reference. When using an external reference source, this pin must be connected to 1µF and a 0.01µF filter capacitors in parallel. When using an internal reference source, this pin must be connected to a 0.01µF capacitor. The external reference can only be used for the ADC.
A8	INA+	Operational Amplifier A Noninverting Input. This analog input pin serves as the operational amplifier A noninverting input.
B7	INA-	Operational Amplifier A Inverting Input. This analog input pin serves as the operational amplifier A inverting input.
B9	OUTA	Operational Amplifier A Output. This analog input pin serves as the operational amplifier A output. This pin is also internally connected to the ADC input mux.
D3	INB+	Operational Amplifier B Noniverting Input. This analog input pin serves as the operational amplifier B noninverting input.
A2	INB-	Operational Amplifier B Inverting Input. This analog input pin serves as the operational amplifier B inverting input.
B3	OUTB	Operational Amplifier B Output. This analog input pin serves as the operational amplifier B output. This pin is also internally connected to the ADC input mux.
E2	INC+	Operational Amplifier C Noninverting Input. This analog input pin serves as the operational amplifier C noninverting input.
C2	INC-	Operational Amplifier C Inverting Input. This analog input pin serves as the operational amplifier C inverting input.
B1	OUTC	Operational Amplifier C Output. This analog input pin serves as the operational amplifier C output. This pin is also internally connected to the ADC input mux.
F1	IND+	Operational Amplifier D Noninverting Input. This analog input pin serves as the operational amplifier A noninverting input.
F3	IND-	Operational Amplifier D Inverting Input. This analog input pin serves as the operational amplifier D inverting input.
D1	OUTD	Operational Amplifier D Output. This analog input pin serves as the operational amplifier D output. This pin is also internally connected to the ADC input mux.
H1	AIN0	ADC Input 0, 1. These two analog pins function as single-ended ADC inputs or a differential pair.
H3	AIN1	
C6	DAC3	DAC3 Single-Ended Output
C4	DAC4	DAC4 Single-Ended Output
A6	SINK1	Programmable Current Sink 1
A4	SINK2	Programmable Current Sink 2

Pin Description (continued)

PIN	NAME	FUNCTION
C8	DAC1	DAC1 Buffer Output. Positive terminal of the differential DAC1's output buffered signal.
D7	DAC2	DAC2 Buffer Output. Positive terminal of the differential DAC2's output buffered signal.
E6	LIN+	DAC2 Output. Positive DAC output voltage to drive the left Class D amplifier.
D9	LIN-	DAC2 Output. Negative DAC output voltage to drive the left Class D amplifier.
H9	RIN+	DAC1 Output. Positive DAC output voltage to drive the right Class D amplifier.
H7	RIN-	DAC1 Output. Negative DAC output voltage to drive the right Class D amplifier.
RESET PIN		
N6	$\overline{RST}$	Digital, Active-Low, Reset Input/Output. The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes a pullup current source and should be driven by an open-drain external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
CLOCK PINS		
M1	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external high-frequency CMOS clock source when HFXOUT is floating.
J2	HFXOUT	High-Frequency Crystal Output. Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, float HFXOUT when an external high-frequency CMOS clock source is connected to the HFXIN pin.
F9	SYNCIN	SYNCIN Clock. This pin acts as the input clock to the Class D amplifier's sawtooth generator. SYNCIN is a divided system clock with the divide ratio set by programmable bits.
GENERAL-PURPOSE I/O, SPECIAL FUNCTION PINS		
M9	P.0.0/INT0/ TCK	P0.0 I/O with Interrupt or JTAG Test Clock. This pin defaults as an input with weak pullup after a reset and functions as a general-purpose I/O with interrupt capability. Enabling the pin's special function disables the general-purpose I/O on the pin and makes the pin function as the test clock input. Note that the JTAG function can be disabled using the TAP bit in the SC register.
L8	P0.1/INT1/ TDI	P0.1 I/O with Interrupt or JTAG Test Data In. This pin defaults as an input with a weak pullup after a reset and functions as a general-purpose I/O with interrupt capability. Enabling the pin's special function disables the general-purpose I/O on the pin and makes the pin function as the test data input. Note that the JTAG function can be disabled using the TAP bit in the SC register.
K7	P0.2/INT2/ TMS	P0.2 I/O with Interrupt or JTAG Test Mode Select. This pin defaults as an input with a weak pullup after a reset and functions as a general-purpose I/O with interrupt capability. Enabling the pin's special function disables the general-purpose I/O on the pin and makes the pin function as the test mode select. Note that the JTAG function can be disabled using the TAP bit in the SC register. The TMS should be gated high when JTAG is disabled.
J6	P0.3/INT3/ TDO	P0.3 I/O with Interrupt or JTAG Test Data Out. This pin defaults as an input with a weak pullup after a reset and functions as a general-purpose I/O with interrupt capability. The output function of the test data is only enabled during the TAP's Shift_IR or Shift_DR states. Enabling the pin's special function disables the general-purpose I/O on the pin and makes the pin function as the test data output. Note that the JTAG function can be disabled using the TAP bit in the SC register.
N8	P0.4/INT4/ $\overline{SSEL}$	P0.4 I/O with Interrupt or SPI Chip Select. This port pin functions as a bidirectional I/O pin with interrupt capability or as the SPI chip select. This port pin defaults to an input with a weak pullup after a reset and functions as a general-purpose I/O. The port pad also contains a Schmitt input circuit.
M7	P0.5/INT5/ SCLK	P0.5 I/O with Interrupt or SPI Clock. This port pin functions as a bidirectional I/O pin with interrupt capability or as the SPI clock. This port pin defaults to an input with a weak pullup after a reset and functions as a general-purpose I/O. The port pad also contains a Schmitt input circuit.

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Pin Description (continued)

PIN	NAME	FUNCTION
L6	P0.6/INT6/ MOSI	P0.6 I/O with Interrupt or Master Out-Slave In. This port pin functions as a bidirectional I/O pin with interrupt capability or as the SPI master out-slave in. This port pin defaults to an input with a weak pullup after a reset and functions as a general-purpose I/O. The port pad also contains a Schmitt input circuit.
K5	P0.7/INT7/ MISO	P0.7 I/O with Interrupt or Master In-Slave Out. This port pin functions as a bidirectional I/O pin with interrupt capability or as the SPI master in-slave out. This port pin defaults to an input with a weak pullup after a reset and functions as a general-purpose I/O. The port pad also contains a Schmitt input circuit.
N4	P1.0/INT8/ SCL/TX	P1.0 I/O with Interrupt or I^2C Clock or USART Transmit. This pin defaults to an input with a weak pullup after reset and functions as a general-purpose I/O with interrupt capability. The port pad contains a Schmitt input circuit. Enabling the pin's special function disables the general-purpose I/O on the pin and enables the I^2C clock or USART transmitter function.
M3	P1.1/INT9/ SDA/RX	P1.1 I/O with Interrupt or I^2C Data or USART Receive. This pin defaults to an input with a weak pullup after reset and functions as a general-purpose I/O with interrupt capability. The port pad contains a Schmitt input circuit. Enabling the pin's special function disables the general-purpose I/O on the pin and enables the I^2C data or USART receiver function.
K3	P1.2/INT10/ TB0A	P1.2 I/O with Interrupt or Timer B0 Pin A. This pin defaults to an input with a weak pullup after reset and functions as a general-purpose I/O. The port pad contains a Schmitt input circuit. Enabling the pin's special function disables the general-purpose I/O on the pin and enables the timer B pin A function.
L2	P1.3/INT11/ TB0B	P1.3 I/O with Interrupt or Timer B0 Pin B. This pin defaults to an input with a weak pullup after reset and functions as a general-purpose I/O. The port pad contains a Schmitt input circuit. Enabling the pin's special function disables the general-purpose I/O on the pin and enables the timer B pin B function.
MISCELLANEOUS PINS		
E8	SHDNL	Shutdown for Left Motor Driver. Shutdown signal for the motor drivers.
G8	SHDNR	Shutdown for Right Motor Driver. Shutdown signal for the motor drivers.
F7	$\overline{FAULT}$	Fault Indicator. Thermal or short circuit fault indicator from the driver IC.
NO CONNECTION PINS		
D5, F5, G6, G4, H5, J4, J8, K9, N2	N.C.	No Connection. Reserved for future use. Leave these pins unconnected.

Detailed Description

The following is an introduction to the primary features of the microcontroller. More detailed descriptions of the device features can be found in the data sheets, errata sheets, and user's guides described later in the *Additional Documentation* section.

MAXQ Core Architecture

The MAXQ core is a low-cost, high-performance, CMOS, fully static, 16-bit RISC microcontroller with flash memory. The MAXQ8913 supports 7 channels of high-performance measurement using a 10-bit successive approximation register (SAR) ADC with internal reference. These parts are structured on a highly advanced, accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining because the instruction contains both the op code and data. The result is a streamlined microcontroller performing at up to 1 million instructions per second (MIPS) for each MHz of the system operating frequency.

The highly efficient core is supported by a 16-level hardware stack, enabling fast subroutine calling and task switching. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment or decrement following an operation, eliminating the need for software intervention. As a result, application speed is greatly increased.

Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special function registers control the peripherals and are subdivided into register modules. The family architecture is modular so new devices and modules can reuse code developed for existing products.

The architecture is transport triggered. This means that writes or reads from certain register locations can also cause side effects to occur. These side effects form the basis for the higher level op codes defined by the assembler, such as ADDC, OR, JUMP, etc. The op codes are actually implemented as MOVE instructions between certain register locations, while the assembler handles the encoding, which need not be a concern to the programmer.

The 16-bit instruction word is designed for efficient execution. Bit 15 indicates the format for the source field of the instruction. Bits 0 to 7 represent the source for the transfer. Depending on the value of the format field, this can be either an immediate value or a source register. If this field represents a register, the lower 4 bits contain the module specifier and the upper 4 bits contain the register index in that module. Bits 8 to 14 represent the destination for the transfer. This value always represents a destination register, with the lower 4 bits containing the module specifier and the upper 3 bits containing the register subindex within that module. Any time that it is necessary to directly select one of the upper 24 registers as a destination, the prefix register, PFX, is needed to supply the extra destination bits. This prefix register write is inserted automatically by the assembler and requires only one additional execution cycle.

Memory Organization

The device incorporates several memory areas:

- 4KB utility ROM
- 64KB of flash memory for program storage
- 4KB of SRAM for storage of temporary variables
- 16-level stack memory for storage of program return addresses and general-purpose use

The incorporation of flash memory allows the devices to be reprogrammed multiple times allowing modifications to user applications post production. Additionally, the flash can be used to store application information including configuration data and log files.

The default memory organization is organized as a Harvard architecture, with separate address spaces for program and data memory. Pseudo-Von Neumann memory organization is supported through the utility ROM for applications that require dynamic program modification and execution from RAM. The pseudo-Von Neumann memory organization places the code, data and utility ROM memories into a single contiguous memory map.

Stack Memory

A 16-bit-wide hardware stack provides storage for program return addresses and can also be used as general-purpose data storage. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store values in the stack explicitly by using the PUSH, POP, and POPI instructions.

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On reset, the stack pointer, SP, initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Utility ROM

The utility ROM is a 4KB block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include the following:

- In-system programming (bootstrap loader) using JTAG interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash programming and fast table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of user-application code, or to one of the special routines mentioned. Routines within the utility ROM are user accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the *MAXQ Family User's Guide: MAXQ8913 Supplement*.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh.

A single password lock (PWL) bit is implemented in the SC register. When the PWL is set to one (power-on reset default) and the contents of the memory at addresses 0010h to 001Fh are any value other than FFh or 00h, the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to zero, these utilities are fully accessible without password. The password is automatically set to all ones following a mass erase.

Programming

The flash memory of the microcontroller can be programmed by two different methods: in-system programming and in-application programming. Both methods afford great flexibility in system design as well as reduce the life-cycle cost of the embedded system. These features can be password protected to prevent unauthorized access to code memory.

(Bootloader) In-System Programming

An internal bootstrap loader allows the device to be reloaded over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software updates enable application updates to physically inaccessible equipment. The interface hardware can be a JTAG connection to another microcontroller or a connection to a PC serial port using a serial-to-JTAG converter such as the MAXQJTAG-001, available from Maxim. If in-system programmability is not required, a commercial gang programmer can be used for mass programming.

Activating the JTAG interface and loading the test access port (TAP) with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to 1 during reset through the JTAG interface executes the bootstrap-loader mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

The following bootstrap loader functions are supported:

- Load
- Dump
- CRC
- Verify
- Erase

In-Application Programming

The in-application programming feature allows the microcontroller to modify its own flash program memory while simultaneously executing its application software. This allows on the fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains user-accessible flash programming functions that erase and program flash memory. These functions are described in detail in the *MAXQ Family User's Guide: MAXQ8913 Supplement*.

Register Set

Most functions of the device are controlled by sets of registers. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are

divided into two major types: system registers and peripheral registers. The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality that could be included by different products based on the MAXQ architecture. This functionality is broken up into discrete modules so that only the features required for a given product need to be included.

The module and register functions are covered fully in the *MAXQ Family User's Guide* and the *MAXQ Family User's Guide: MAXQ8913 Supplement*. This information includes the locations of status and control bits and a detailed description of their function and reset values. Refer to this documentation for a complete understanding of the features and operation of the microcontroller.

Programmable Timer

The microcontroller incorporates one instance of the 16-bit programmable timer/counter B peripheral. It can be used in counter/timer/capture/compare/PWM functions, allowing precise control of internal and external events. The timer/counter supports clock input prescaling and set/reset/toggle PWM/output control functionality not found on other MAXQ timer implementations. A new register, TBC, supports PWM/output control functions. A distinguishing characteristic of timer/counter B is that its count ranges from 0000h to the value stored in the 16-bit capture/reload register (TBR) counting up. The timer/counter B timer is fully described in the *MAXQ Family User's Guide: MAXQ8913 Supplement*.

Timer B operational modes include the following:

- Autoreload
- Autoreload using external pin
- Capture using external pin
- Up/down count using external pin
- Up-count PWM/output
- Up/down PWM/output
- Clock output on TBxB pin
- Up/down PWM mode with double-buffered output mode:
- On interrupt, the user loads buffered output data, which does not begin sending until current iteration is completed. This enables a glitchless PWM because there is no output pause while interrupt is being serviced, and a race condition does not occur in setting TBC before it is used. A TBC value written after timer rollover becomes effective during the following counter cycle.

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer is controlled through bits in the WDCN register. Its timeout period can be set to one of four programmable intervals ranging from 2^{12} to 2^{21} system clocks in its default mode, allowing flexibility to support different types of applications. The interrupt occurs 512 system clocks before the reset, allowing the system to execute an interrupt and place the system in a known, safe state before the device performs a total system reset. At 10MHz, watchdog timeout periods can be programmed from 410µs to 54s, depending on the system clock mode.

Op Amps

The MAXQ8913 contains four uncommitted op amps. It is electrically acceptable for op-amp outputs to exceed the reference voltage, but they saturate the ADC code. Gains and offsets introduced in the op-amp circuits should be carefully set to maintain the outputs of the op amps at or below the reference voltage if the ADC converted values are expected to be unsaturated. The device provides REFA as an output to aid in this endeavor.

The outputs of the op amps are internally connected to ADC channels 2 to 5. Unused op amps should be connected with their "+" input terminal grounded and the output and "-" input terminals shorted together.

Differential DAC and External Class D Amplifier Output Stage Operation

The power stage of the MAXQ8913 is designed to drive a stereo Class D amplifier (DAMP). These amplifiers are

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suitable for driving self-commutating DC motors or voice coil motors.

Each external DAMP is differentially driven by a 10-bit DAC. The DAC output common mode is 1.25V, based on the bandgap reference, and each differential output can swing from GND to 2.5V (if $V_{DVDD} \geq 3V$), so the effective differential peak-to-peak voltage is 5V. The DAMP has a 6dB gain, so its ouput can swing 10V (if DAMP supply = 5V).

The differential output voltage follows the simple formula:

$$V_{DIFF} = 2.5 \times (code - 512)/512V$$

There are four Class D amplifier control bits and one status bit. The SHDNR and SHDNL pins are the active-high shutdown controls for the two Class D amplifiers, respectively. The SYNCIN_DIV bits control the input clock to the Class D amplifier sawtooth generator. The SYNCIN frequency must fall within 2MHz and 2.8MHz. The optimal frequency is 2.2MHz. The frequency of the high-frequency oscillator and the divide ratio need to be chosen wisely to accomodate this requirement. For example, if a 9MHz crystal is used, a divide-by-4 ratio produces a SYNCIN frequency of 2.25MHz.

Table 1 shows the divide ratio applied to the high-frequency oscillator output based on the value of SYNCIN_DIV.

Table 1. SYNCIN Divisor vs. SYNCIN_DIV Value

SYNCIN_DIV	HF DIVIDED BY
0 (default)	SYNCIN clock off
1	2
2	3
3	4

To start operating the DACs and DAMPs, the following procedural steps should be followed:

1) Set both DAC inputs to code 512.
2) Enable the SYNCIN clock by setting an appropriate value for SYNCIN_DIV.
3) Wait 100µs. Clear the SHDNR and SHDNL bits.
4) Wait 100µs.

One or both DAMPs can be shut down at any time by setting the corresponding SHDN bit. If both DAMPs are shut down, the firmware should disable the SYNCIN signal.

The DAMP $\overline{FAULT}$ bit goes high for at least 500ns following a thermal shutdown or current-limit event. It stays low in shutdown and is glitch-free during power-up. $\overline{FAULT}$ interrupts the microcontroller if enabled. Alternatively, the firmware can poll the bit periodically to detect faults of the type previously described.

DAC1 and DAC2 Buffers

While the MAXQ8913 contains power drivers for the actuator, the positive terminal of each differential DAC output pair is buffered and available as an output pin. This feature is intended primarily for test, and no significant load should be added to the DAC1 and DAC2 pins. The specifications for these pins are not yet determined, except for the no-load output voltage, which is expected to be between GND and 2.5V.

DAC3 and DAC4

DAC3 and DAC4 are single-ended DACs. Their outputs are intended for driving the positive terminal (through a resistor) of single-supply op amps to force the virtual GND to a value that allows the op amp to operate below and above the virtual ground DC value. Operated in this fashion, the DACs can also serve as offset cancellation devices as necessary.

SINK1 and SINK2

Popular optical-image stabilization implementations include the use of Hall-effect elements for position feedback. Hall-effect elements require a current to flow through two of its terminals for proper operation. The device includes two current sinks intended to drive these elements. The current sinks are programmable between 0 and 15.94mA with 62.5mA resolution through an 8-bit code. Code 0 turns them off.

When operating Hall-effect elements from 3V, the maximum achievable current is given by $(3V - 0.5V)/R_{HALL}$, where 0.5V is the minimum voltage value at the input of the current sink. For example, if $R_{HALL} = 250\Omega$, the maximum current is 10mA.

If higher currents are desirable, the user must provide a larger supply voltage to the Hall-effect element. In this case, care must be exercised so that the output nodes of the Hall-effect element do not exceed V_{AVDD}. Exceeding V_{AVDD} could cause the input-protection diodes of the op-amp terminals to begin conduction and waste power when the device is in sleep mode. If supplying a voltage larger than V_{AVDD} to the Hall-effect element, a switchable supply is recommended to avoid the leakage path identified above.

Additional Documentation

Designers must have four documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation.

- This MAXQ8913 data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ8913 errata sheet for the specific device revision, available at **www.maxim-ic.com/errata**.
- The *MAXQ Family User's Guide*, which contains detailed information on core features and operation, including programming. This document is available on our website at **www.maxim-ic.com/MAXQUG**.
- The *MAXQ Family User's Guide: MAXQ8913 Supplement*, which contains detailed information on features specific to the MAXQ8913.

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this microcontroller are available from Maxim and third-party suppliers, including:

- Compilers
- In-circuit emulators
- Integrated development environments (IDEs)
- JTAG-to-serial converters for programming and debugging.

A partial list of development tool vendors can be found at **www.maxim-ic.com/MAXQ_tools**.

For technical support, go to **https://support.maxim-ic.com/micro**.

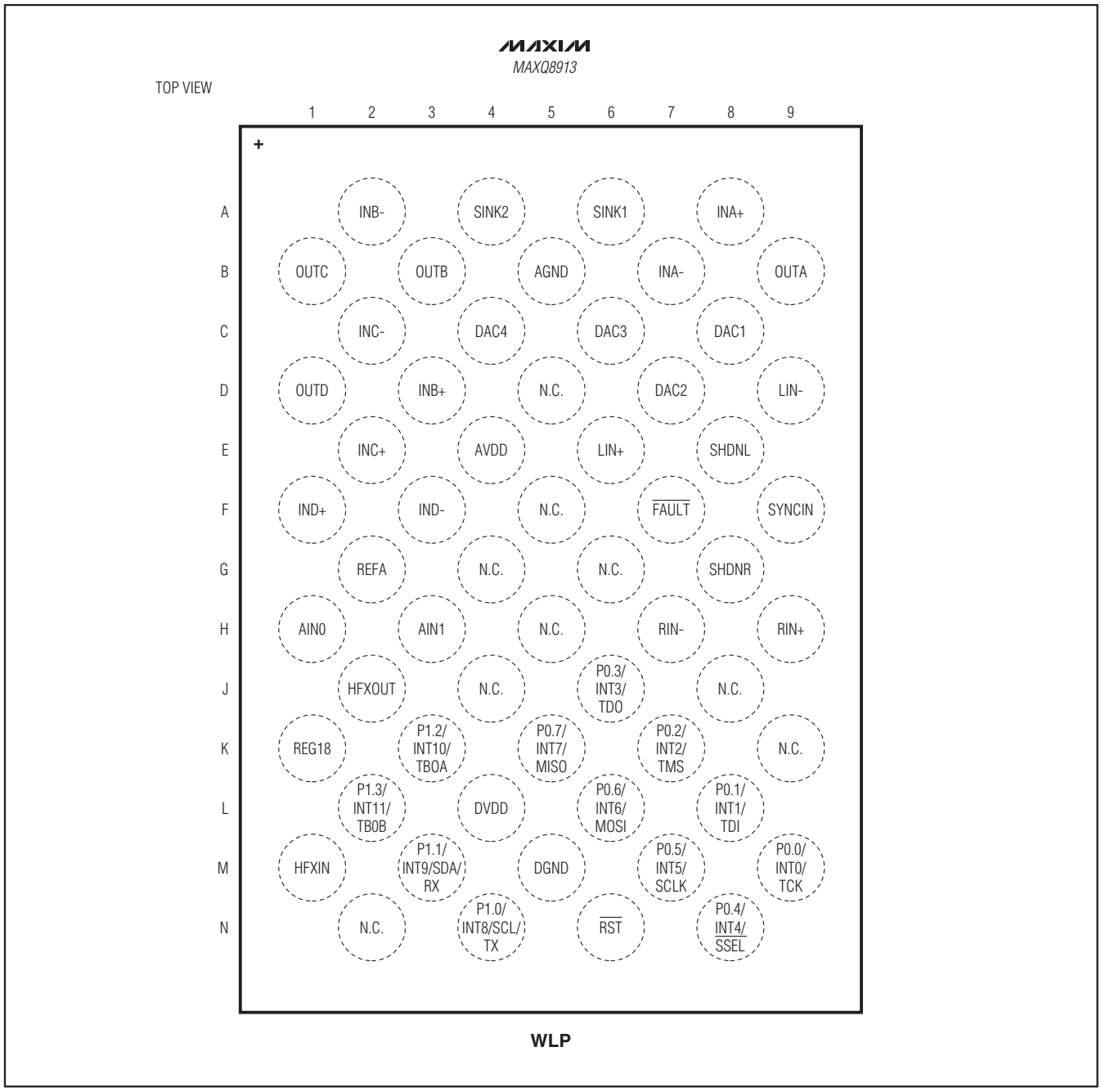
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
58 WLP	W584B2+1	**21-0220**

16-Bit, Mixed-Signal Microcontroller with Op Amps, ADC, and DACs for All-in-One Servo Loop Control

Pin Configuration



WLP