TPS657120 PMU for Baseband and RF-PA Power

1 Device Overview

1.1 Features

- 3 Step-Down Converters:
  - V_{IN} Range From 2.8 V to 5.5 V
  - Power Save Mode at Light Load Current
  - Output Voltage Accuracy in PWM Mode ±2%
  - Typical 16-µA Quiescent Current per DCDC1 and DCDC2 Converter
  - Typical 26-µA Quiescent Current for DCDC3 Converter
  - Dynamic Voltage Scaling
  - 100% Duty Cycle for Lowest Dropout
- 2 LDOs:
  - 2 × 10-mA Output Current
  - Low Noise RF-LDOs
  - Output Voltage Range 1.2 V to 3.4 V
  - 32-µA Quiescent Current
  - Pre-Regulation Support by Separate Power Inputs
  - ECO mode
  - V_{IN} Range of LDOs:
    - LDO1: 2.0 V to 5.5 V
    - LDO2: 2.8 V to 5.5 V
- 2 GPIOs
- Thermal Shutdown
- Bypass Switch
  - Used with DCDC3 Powering an RF-PA
- Interface
  - 26 MHz-MIPI RFFE Interface
- Undervoltage Lockout
- Flexible Power-Up and Power-Down Sequencing
- 2.5-mm × 2.3-mm DSBGA Package with 0.4-mm Pitch

1.2 Applications

- Data Cards
- Smartphones

1.3 Description

The TPS657120 provides three configurable step-down converters with up to 2-A output current.This device also has 2 LDO regulators. LDO1 can be supplied from either the input voltage directly or from a pre-regulated supply such as DCDC1 or DCDC2. The input voltage to LDO2 is used as an analog supply input and therefore must be tied to the input voltage at the same voltage level with VINDCDC1/2 and VINDCDC3. The internal power-up and power-down controller is configurable and can support any power-up/power-down sequences (OTP based). All LDOs and DCDC converters are controllable by a MIPI RFFE compatible interface, by pins PWRON, CLK_REQ1 and CLK_REQ2, or both. In addition, there is a nRESET as well as a RFFE address select (ADR_SELECT) input which can alternatively be used as general purpose I/Os with a 1-mA sink capability. The TPS657120 comes in a 6-ball × 5-ball DSBGA package (2.5 mm × 2.3 mm) with a 0.4-mm pitch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS657120	DSBGA (30)	2.31 mm × 2.51 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

1.4 Functional Block Diagram

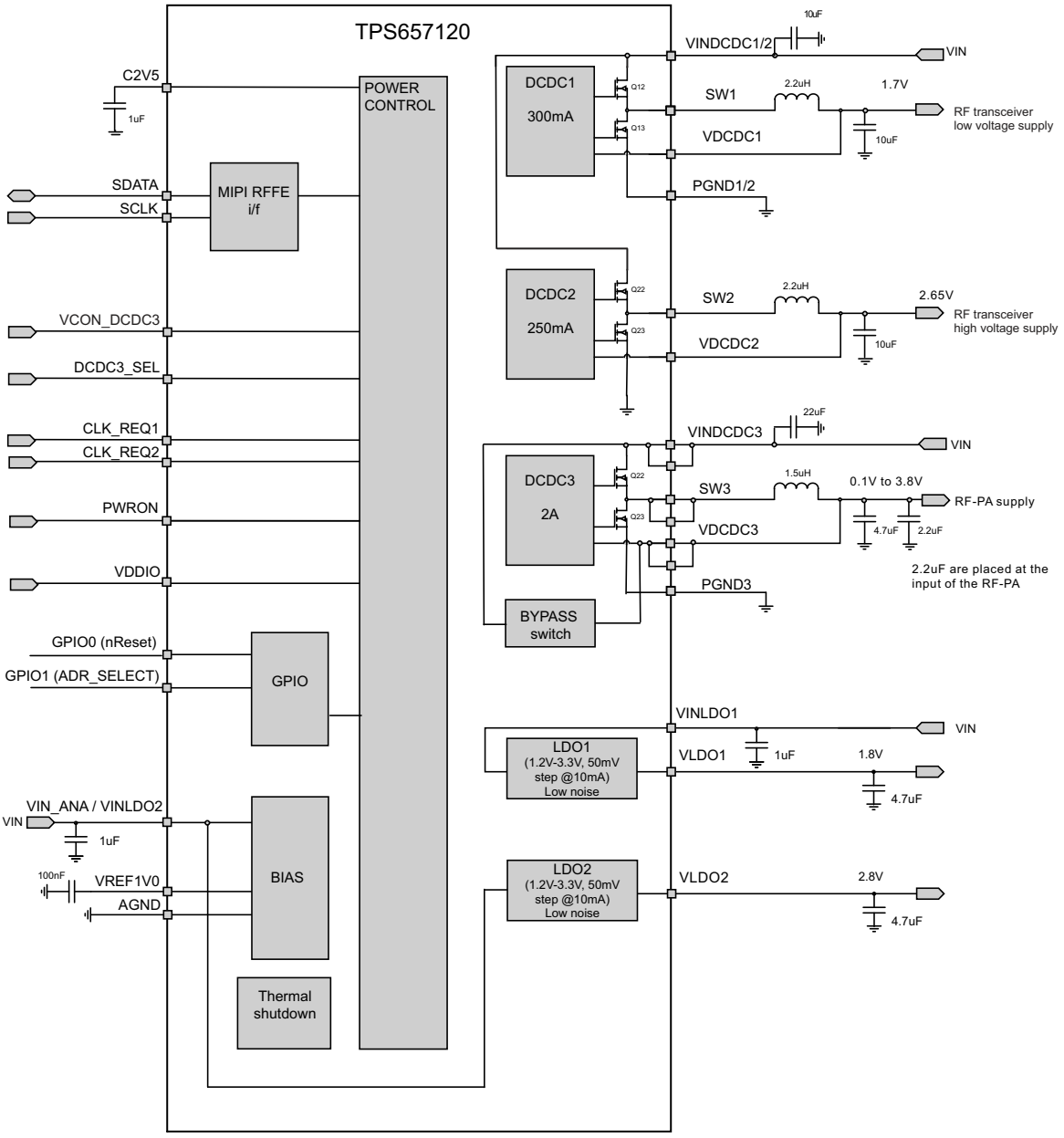

Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2013) to Revision A	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Detailed Description* section, *Device Functional Modes* section, *Applications, Implementation, and Layout* section, *Power Supply Recommendations* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added *Layout Example*	54

3 Terminal Configuration and Functions

Figure 3-1 and Figure 3-2 show the 30-pin YFF Die-Size Ball-Grid Array (DSBGA) Package pin assignments.

Figure 3-1. 30-Pin YFF DSBGA (Top View)

Figure 3-2. 30-Pin YFF DSBGA (Bottom View)

3.1 Pin Attributes

Pin Attributes

PIN		I/O	DESCRIPTION
NAME	NO.		
REFERENCE			
VIN_ANA / VINLDO2	A3	I	Analog supply voltage input; power input for LDO2; connect to the same voltage as VINDCDC1/2 and VINDCDC3
VREF1V0	A5	O	LDO reference bypass pin; connect a 100-nF capacitor to GND
C2V5	C5	O	Internal supply for logic; connect a 1-µF capacitor to GND
AGND	B5	-	Analog ground connection; connect to PGND on the PCB
GPIOs			
nRESET (GPIO0)	D4	I/O	Primary function is active low reset input (nRESET), pin needs to be pulled to a logic HIGH per defautl in order to allow start-up. After internal configuration from OTP memory has been read, it can be assigned alternatively as general purpose I/O. Its push-pull stage is referenced to VDDIO (VIF).
GPIO1 (ADR_SELECT)	B2	I/O	General purpose I/O; push-pull to VDDIO (VIF); alternatively LSB Bit address select for RFFE interface on USID[0]
STEP_DOWN CONVERTERS			
VINDCDC1/2	E5	I	Power input to DCDC1 and DCDC2 converter; connect to VINDCDC3
VDCDC1	C4	I	Voltage sense (feedback) input for DCDC1
SW1	D5	O	Switch node of DCDC1; connect output inductor
PGND1/2	F4	-	Power GND connection for DCDC1 and DCDC2 converter
VDCDC2	E4	I	Voltage sense (feedback) input for DCDC2
SW2	F5	O	Switch node of DCDC2; connect output inductor
VINDCDC3	E2, F2	I	Power input to DCDC3 converter and to the bypass switch; connect to VINDCDC1, VINDCDC2 and Vcc
VDCDC3	E3, F3	I	Voltage sense (feedback) input for DCDC3 and bypass output
SW3	E1, F1	O	Switch node of DCDC3; connect output inductor
PGND3	D1	-	Power GND connection for DCDC3 converter
LOW DROPOUT REGULATORS			
VINLDO1	A2	I	Power input for LDO1
VLDO1	A1	O	LDO1 output
VLDO2	A4	O	LDO2 output
INTERFACE			
SDATA	C2	I/O	RFFE data pin
SCLK	C3	I	RFFE clock input
ENABLE AND CONTROL			
CLK_REQ1	B3	I	Clock request signal1 used to enable and disable power resources
CLK_REQ2	B4	I	Clock request signal2 used to enable and disable power resources
DCDC3_SEL	D2	I	Voltage scaling input to change the output voltage between two settings
VCON_DCDC3	D3	I	Analog voltage scaling input for DCDC3
PWRON	B1	I	Enable input; LOW=OFF; HIGH=ON; input voltage range up to VINDCDCx, VIN_ANA
VDDIO	C1	I	Supply voltage input for GPIOs and output stages that sets the HIGH level voltage (I/O voltage); TPS657120 is held in reset if VDDIO is not in the valid range of operation

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage		all pins except A/PGND pins and pins listed below with respect to AGND	–0.3	6	V
		VLDO1, VLDO2, VDDIO with respect to AGND	–0.3	3.6	V
		pin VDCDC3 with respect to AGND	–0.3	5.5	V
		pins SDATA, SCLK, DCDC3_SEL , GPIO_0, GPIO_1, CLK_REQ1, CLK_REQ2 , with respect to AGND	–0.3	VDDIO + 0.3	V
Current		all non power pins		5	mA
		power pins		2	A
T_A	Operating free-air temperature		–40	85	°C
T_J	Maximum junction temperature			125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 4.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
DCDC CONVERTERS						
VINDCDC1, VINDCDC2, VINDCDC3	Input voltage range for step-down converter DCDC1, DCDC2, DCDC3		2.8		5.5	V
	Output voltage range for step-down converter	DCDC1, DCDC2	0.8		3.3	V
		DCDC3	0.1		3.6	V
L1, L2	Inductance at L1, L2		1	2.2	2.9	µH
L3	Inductance at L3		1	1.5	2.2	µH
$C_{VINDCDC1/2}$	Input capacitance at VINDCDC1/2 (1)		4.7	10		µF
$C_{VINDCDC3}$	Input capacitance at VINDCDC3 (1)		10	22		µF
$C_{OUTDCDC1,2}$	Output capacitance at DCDC1 and DCDC2 (1)		4.7	10	22	µF
$C_{OUTDCDC3}$	Output capacitance at DCDC3 (1)		2.0	6	12	µF
LDOs; GENERIC						
VINLDO1	Input voltage range for LDO1		2.0		5.5	V
VINLDO2(2)	Input voltage for LDO2(3)		2.8		5.5	V
V_{LDO1}, V_{LDO2}	Output voltage for LDOs		1.2		3.4	V

(1) Ceramic capacitors show an effect called DC Bias Effect. With a dc voltage applied to a ceramic capacitor , the effective capacitance is reduced. The table above therefore lists the minimum value as Capacitance. In order to meet the minimum capacitance, the nominal value may have to be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the LDOs of dcdc converters. Input capacitors need to be placed as close as possible to the pins of TPS657120.
(2) Analog supply voltage VIN_ANA
(3) As this pin is used as the analog supply voltage, it needs to be tied to VINDCDCx

Recommended Operating Conditions *(continued)*

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
C_{INLDO1} C_{INLDO2}	Input capacitance on LDO supply pins (1)	0.5			µF
$C_{outLDO1}$, $C_{outLDO2}$	Output capacitance on LDO1, LDO2 (1)	1		4.7	µF
V_{VDDIO}	for RFFE interface at 1.2 V or 1.8 V	1.1		1.95	V
C_{VDDIO}	Input capacitance on VDDIO	100			nF
C(C2V5)	Capacitance at internal supply at pin C2V5	0.5	1	10	µF
C(VREF1V0)	Bypass capacitance at internal reference VREF1V0	47	100	220	nF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

4.4 Thermal Information

THERMAL METRIC(1)		TPS657120 YFF (DSBGA) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

4.5 Electrical Characteristics: General Functions

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted), see *Section 4.12*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SB}	Standby supply current	PWRON=LOW; total current in STANDBY state into pins VINDCDC1/2, VINDCDC3 and VIN_ANA			55	µA
I_Q	Quiescent supply current	PWRON=HIGH, LDOs and DCDC converters =OFF			60	µA
I_Q	Quiescent supply current	PWRON=HIGH, LDO1 and LDO2 and DCDC1 and DCDC2 = enabled in normal mode			170	µA

4.6 Electrical Characteristics: DCDC1 and DCDC2

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted); see *Section 4.12*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.8		5.5	V
V_{DCDC1} V_{DCDC2}	DCDCx output voltage	25-mV steps up to 2.2 V; 50-mV steps above 2.2 V	0.8		3.3	V
V_{DCDC1} V_{DCDC2}	Default output voltage	VDCDC1		1.7		V
		VDCDC2		2.65		
$I_{OUT(DCDCx)}$	Continuous output current	DCDC1 (VINDCDC1 ≥ 2.8 V)			300	mA
		DCDC2 (VINDCDC2 ≥ 2.8 V)			250	
I_Q	Quiescent current	I_{LOAD} = 0 mA, DCDCx_MODE = 0, Device not switching; for each DCDC1 and DCDC2		16	25	µA
		I_{LOAD} = 0 mA, DCDCx_MODE = 1, Device switching; for each DCDC1 and DCDC2		3.5		mA

Electrical Characteristics: DCDC1 and DCDC2 *(continued)*

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted); see *Section 4.12*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DCDC1/2}$	Accuracy	DCDCx_MODE = 1, V_{IN} = 3.0 V to 5.5 V, I_{LOAD} = 0 mA, tolerance is ±2% or ±25 mV whatever is larger	–2%		2%	
		DCDCx_MODE = 0, V_{IN} = 3.0 V to 5.5 V, I_{LOAD} = 0 mA, +1% voltage scaling active	–3%	1.25%	3.5%	
	Load regulation	DCDCx_MODE = 1, V_{IN} = 3.0 V to 5.5 V; I_{LOAD} = 25 mA to 225 mA; for DCDC1 and DCDC2		0.25		%/A
f_{SW}	Switching frequency	DCDCx_MODE = 1, V_{IN} = 3.0 V to 5.5 V	1.9	2.4	2.6	MHz
$R_{DS(ON)}$	High-side FET On-resistance	For DCDC1 and DCDC2 with VINDCDCx = 3.6 V, D = 100%		250	400	mΩ
$R_{DS(ON)}$	Low-side FET On-resistance	For DCDC1 and DCDC2 with VINDCDCx = 3.6 V, D = 100%		220	350	mΩ
I_{LK_HS}	High-side FET leakage current	T_J = 85°C; DCDC1, DCDC2; VINDCDC1 = VINDCDC2 = 5.5 V			2	µA
I_{LK_LS}	Low-side FET leakage current	T_J = 85°C; DCDC1, DCDC2; VINDCDC1 = VINDCDC2 = 5.5 V			3	µA
I_{HS_LIMF}	High-side forward current limit	2.9 V ≤ V_{IN_DCDC1} ≤ 5.5 V; for DCDC1	500	650	800	mA
I_{LS_LIMF}	Low-side forward current limit	2.9 V ≤ V_{IN_DCDC1} ≤ 5.5 V; for DCDC1	500	650	800	mA
I_{HS_LIMF}	High-side forward current limit	2.9 V ≤ V_{IN_DCDC2} ≤ 5.5 V; for DCDC2	425	600	775	mA
I_{LS_LIMF}	Low-side forward current limit	2.9 V ≤ V_{IN_DCDC2} ≤ 5.5 V; for DCDC2	425	600	775	mA
	DCDC1, DCDC2 output voltage ripple	V_{IN} = 3.6 V; V_{OUT} = 1.7 V to 2.65 V; Io = 10 mA to 300 mA; L = 1.5uH, RSL = 50 mR; Co = 10 µF		10	25	mVpp
	Efficiency	VINDCDCx = 3.7 V, Vo = 1.7 V or Vo = 2.65 V; Io = 80 mA to 150 mA	88%	93%		
		VINDCDCx = 3.7 V, Vo = 1.7 V or Vo = 2.65 V; Io = 300 µA	80%			
		VINDCDCx = 3.7 V, Vo = 1.7 V or Vo = 2.65 V; Io = 100 µA		45%		
	Pulse skipping threshold	Output current when device switches from PFM to PWM automatically; V_{IN} = 3.6 V, V_{OUT} = 1.7 V		140		mA
		output current when device switches from PFM to PWM automatically; V_{IN} = 3.6 V, V_{OUT} = 2.65 V		60		
PSRR	Power supply rejection ratio	V_{IN} = 3.6 V, I_{LOAD} = 150 mA, 10 Hz < f < 10 kHz, Vo = 1.7 V and Vo = 2.65 V		40		dB
	Output noise	V_{IN} = 3.6 V, I_{LOAD} = 100 mA, Vo = 1.7 V and Vo = 2.65 V				µV/√Hz
		1 kHz < f < 100 kHz			2	
		100 kHz < f < 1 MHz			0.2	
		1 MHz < f < 10 MHz; not including f(sw)			0.1	
$V_{DCDCPG\text{-}falling}$	Power good threshold	VDCDCx falling	VDCDCx –15%		VDCDCx – 7%	
$V_{DCDCPG\text{-}rising}$	Power good threshold	VDCDCx rising		VDCDCx – 3%		
t_{Start}	Start-up time	Time to start switching, measured from end of MIPI command enabling converter			225	µs
t_{Ramp}	V_{OUT} Ramp UP time	Time to ramp from 5% to 95% of V_{OUT}			200	µs
$R_{Discharge}$	Discharge resistor		250	400	600	Ω

4.7 Electrical Characteristics: DCDC3

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted); see *Section 4.12*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.8		5.5	V
V_{DCDC3}	DCDC3 output voltage	output voltage defined by internal resistor divider; DCDC3_CTRL:VCON = 0	0.8		3.60	V
		output voltage defined by VCON input; DCDC3_CTRL:VCON = 1	0.1		3.60	
$I_{OUT(DCDC3)}$	Continuous output current	DCDC3			2200	mA
I_Q	Quiescent current	I_{LOAD} = 0 mA, DCDC3_MODE = 0, Device not switching		26	46	µA
		I_{LOAD} = 0 mA, DCDC3_MODE = 1, Device switching		6		mA
V_{DCDC3}	Accuracy; output voltage setting with register; DCDC3_CTRL:VCON = 0	DCDC3_MODE = 1, I_{LOAD} = 0 mA, T_A = 25°C; C_{OUT} = 2 x 4.7 µF + 2.2 µF	–2%		2%	
		DCDC3_MODE = 1, I_{LOAD} = 0 mA, T_A = –40 – 85°C; C_{OUT} = 2 x 4.7 µF + 2.2 µF	–2.5%		2.5%	
		DCDC3_MODE = 0, I_{LOAD} = 0 mA, T_A = 25°C; C_{OUT} = 2 x 4.7 µF + 2.2 µF the output voltage tolerance is ±3% or ±45 mV whichever is larger	–3%		3%	
		DCDC3_MODE = 0, I_{LOAD} = 0 mA, T_A = –40 – 85°C; C_{OUT} = 2 x 4.7 µF + 2.2 µF the output voltage tolerance is ±3% or ±45 mV whichever is larger	–3%		3%	
	Accuracy for VCON operation; DCDC3_CTRL:VCON = 1	Vo = 0.1 V to 3.6 V; C_{OUT} = 2 x 4.7 µF + 2.2 µF; PWM mode forced automatically; accuracy in VCON mode is ±5% or ±25 mV, whichever is larger	–5%		5%	
f_{SW}	Switching frequency	DCDC3_MODE = 1 or DCDC3_CTRL:VCON = 1	2100	2300	2700	kHz
$R_{DS(ON)}$	High-side MOSFET on-resistance	V_{IN_DCDC3} = 3.6 V, 100% duty cycle		75	120	mΩ
	Low-side MOSFET on-resistance	V_{IN_DCDC3} = 3.6 V, 0% duty cycle		110	180	mΩ
I_{LK_HS}	High-side leakage current	T_J = 85°C; VINDCDC3=4.2 V			3	µA
I_{LK_LS}	Low-side leakage current	T_J = 85°C; VINDCDC3=4.2 V			3	µA
I_{LIM}	High-side current limit	2.9 V ≤ V_{IN_DCDC3} ≤ 5.5 V	2400	3000	3600	mA
I_{LIM}	Low-side current limit	2.9 V ≤ V_{IN_DCDC3} ≤ 5.5 V	2200	2800	3400	mA
I_{LIM}	Low-side negative current limit	2.9 V ≤ V_{IN_DCDC3} ≤ 5.5 V; EN_nILIM_xl=1	1000	1500	2000	mA
		2.9 V ≤ V_{IN_DCDC3} ≤ 5.5 V; EN_nILIM_xl=0		200		mA
	Duty cycle	V_{IN} = 3.6 V	2%		100%	
	DCDC3 output voltage ripple	V_{IN} = 5 V; V_{OUT} = 3.4 V; Io=2 A; L=1.5 µH, ESR=90 mR; Co=10 µF		10	50	mVpp
	DCDC3 load transient response	V_{IN} = 5 V; V_{OUT} = 3.4 V; Io=200 mA to 1.8 A; L=1.5 µH, ESR=90 mR; Co=10 µF; dt=10 µs		100		mV
	Efficiency	VINDCDCx=3.7 V, Vo=3.4 V; Io=1500 mA	80%			
		VINDCDCx=3.7 V, Vo=3.4 V; Io=400 mA	90%			
		VINDCDCx=3.7 V, Vo=2.0 V; Io=10 mA	80%			

Electrical Characteristics: DCDC3 *(continued)*

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted); see *Section 4.12*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output noise	V_{IN} = 3.6 V, I_{LOAD} = 100 mA, Vo=2.65 V				µV/√Hz
		1 kHz < f < 100 kHz			3	
		100 kHz < f < 1 MHz			0.2	
		1 MHz < f < 10 MHz			0.1	
$V_{DCDCPG-falling}$	Power good threshold	VDCDCx falling	VDCDCx - 14%		VDCDCx - 7%	
$V_{DCDCPG-rising}$	Power good threshold	VDCDCx rising		VDCDCx - 5%		
t_{Start}	Start-up time	Time to start switching, measured from end of RFFE command enabling converter			175	µs
t_{Ramp}	V_{OUT} Ramp UP time	Time to ramp from 5% to 95% of V_{OUT} ; DCDC3_CTRL:IMMEDIATE = 1; V_{OUT} = 3.4 V			30	µs
	Rise and fall time	dVo=±1 V; Io=450 mA; Co=10 µF; DCDC3_SEL mode			30	µs
	Ramp time in VCON mode				10	µs
	VCON input voltage		0.2		2.1	V
	VCON slew rate			300		mV/µs
	VCON input resistance			1		MΩ
	VCON gain	Typical adjustable range	1.3		2.7	
	VCON offset		–350		0	mV
$R_{Discharge}$	Discharge resistor		250	400	500	Ω
	Voltage between VINDCDC3 and VDCDC3				5.5	V
	Bypass switch current limit	VINDCDCx= 2.8 V to 5.5 V; not tested in production	2000	2500	3000	mA
	Bypass switch current limit response time			10		µs
	Resistance from VINDCDC3 to VDCDC3	Bypass switch closed; not including the parallel path through high side switch and inductor		100	170	mΩ
	Leakage current from VINDCDC3 to VDCDC3	When bypass switch is open			10	µA
	Bypass switch over-voltage protection	Sensed at VDCDC3; bypass enabled bit is cleared when voltage is exceeded; rising edge		4.0		V
		Sensed at VDCDC3; bypass enabled bit is cleared when voltage is exceeded; falling edge		3.7		

4.8 Electrical Characteristics: RF-LDOs

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted); see *Section 4.12*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	LDO1	2.0		5.5	V
		LDO2, analog supply voltage input	2.8		5.5	
V_{LDOx}	LDO output voltage for RF-LDOs	50-mV steps	1.2		3.4	V
	LDO voltage accuracy	ECO = 0	–2%		2%	
		ECO = 1	–5%		5%	

Electrical Characteristics: RF-LDOs *(continued)*

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted); see *Section 4.12*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OUT(LDOx)}$	LDO continuous output current	LDO1	10			mA
		LDO2	10			
$I_{SHORT(LDOx)}$	LDO current limit	LDO1	20		80	mA
		LDO2	20		80	
$V_{DO(LDOx)}$	Dropout voltage (1)	$I_{OUT(LDO1)}$ = 10 mA; VINLDO1=2.0 V			250	mV
		$I_{OUT(LDO2)}$ = 10 mA; VINLDO2=3.0 V			250	
	Line regulation	V_{IN} = V_{LDO} + 0.5 V & I_{LOAD} = 10 mA for LDO1 and for LDO2	–1%		1%	
	Load regulation; ECO = 0	LDO1 and LDO2: I_{LOAD} = 50 µA to 10 mA			40	mV
	Load regulation; ECO = 1	LDO1 and LDO2: I_{LOAD} = 0 mA to 1 mA	–5%		5%	
	Line transient response	dV/dt = ±0.5 V/µs	–50		50	mV
	Load transient response	for LDO1 and LDO2: dI/dt = 100 mA/µs; 1-mA to 10-mA load step			50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 1 kHz, V_{IN} - V_{OUT} ≥ 0.5 V, I_{LOAD} = 10 mA	63			dB
	Output voltage noise	f = 10 Hz to 100 kHz, V_{IN} - V_{OUT} ≥ 0.5 V , I_{LOAD} = 10 mA		30		µVrms
I_q	Quiescent current	ECO = 1; I_{LOAD} ≤ 1 mA for LDO1, LDO2			16	µA
		ECO = 0; I_{LOAD} ≤ 10 mA for LDO1, LDO2			40	µA
	ECO exit time	Minimum wait time before the full current can be drawn after ECO is set 0			50	µs
t_{Ramp}	V_{OUT} ramp up time	Time to ramp from 5% to 95% of V_{OUT} ; I_{OUT} = 10 mA; Co=4.7 µF; Vo=1.8 V		850	1000	µs
t_{Ramp}	V_{OUT} ramp up time	Time to ramp from 5% to 95% of V_{OUT} ; I_{OUT} = 10 mA; Co=4.7 µF; Vo=2.8 V		1000	1200	µs
$V_{LDOPG-falling}$	Power good threshold	VDCDCx falling	VLDOx - 14%		VLDOx - 7%	
$V_{LDOPG-rising}$	Power good threshold	VDCDCx rising		VLDOx - 5%		
$R_{Discharge}$	Discharge resistance at LDOx output	LDOx disabled	200	325	450	Ω

(1) V_{DO} = V_{IN} - V_{OUT}, where V_{OUT} = $V_{OUT(NOM)}$ - 2%

4.9 Electrical Characteristics: Digital Inputs, Digital Outputs

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RFFE INTERFACE						
V_{VDDIO}	VDDIO voltage	VDDIO = 1.2 V	1.1	1.2	1.3	V
		VDDIO = 1.8 V	1.65	1.8	1.95	V
I_{VIO-IN}	I/O voltage average input current for SDATA, SCLK	VDDIO=1.8 V; average during a 26-MHz write			1.25	mA
CL	Load capacitance	Half-speed readback; not including TPS657120 pin capacitance			50	pF
V_{OL}	Low level output voltage for SDATA, SCLK	I_{OL}= 2 mA	0		0.2 × VDDIO	V

Electrical Characteristics: Digital Inputs, Digital Outputs *(continued)*

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage for SDATA, SCLK	I_{OH}= –2 mA	0.8 × VDDIO		VDDIO	V
V_{TP}	INPUT: Positive going threshold voltage	VDDIO = 1.2 V or 1.8 V	0.4 × VDDIO		0.7 × VDDIO	V
V_{TN}	INPUT: Negative going threshold voltage	VDDIO = 1.2 V	0.28 × VDDIO		0.6 × VDDIO	V
V_{TN}	INPUT: Negative going threshold voltage	VDDIO = 1.8 V	0.3 × VDDIO		0.6 × VDDIO	V
V_H	INPUT: Hysteresis voltage (VTP-VTN)	VDDIO = 1.2 V or 1.8 V	0.1 × VDDIO		0.4 × VDDIO	V
V_{IORST}	RFFE I/O voltage reset voltage level	RFFE interface is in reset when VDDIO is below that voltage			0.95	V
I_{IH}	SDATA = 0.8 x VDDIO		–2		10	uA
	SCLK = 0.8 x VDDIO		–1		10	
I_{IL}	SDATA = 0.2 x VDDIO		–2		5	uA
	SCLK = 0.2 x VDDIO		–1		1	
GENERIC I/Os						
V_{IL}	Low-level input voltage	PWRON	0		0.4	V
		GPIO_0, GPIO_1, CLK_REQ1, CLK_REQ2 , DCDC3_SEL; SDATA, SCLK	0		0.3 × VDDIO	
V_{IH}	High-level input voltage	PWRON	1.1		Vcc	V
		GPIO_0, GPIO_1, CLK_REQ1, CLK_REQ2 , DCDC3_SEL, SDATA, SCLK	0.7 × VDDIO		VDDIO	
V_{OL}	Low-level output voltage	I_{OL}= 1 mA for VDDIO=1.8 V	0		0.2	V
V_{OH}	High-level output voltage	For pins configured as push-pull ouput to VDDIO; I_{OH}= 1 mA for VDDIO=1.8 V	VDDIO - 0.2		VDDIO	V
		For pins configured as open-drain ouput			Vcc	
I_{OL}	Low-level output current Low-level output current	VDDIO ≥ 1.8 V			1	mA
		VDDIO = 1.2 V			0.1	
I_{OH}	High-level output current	VDDIO ≥ 1.8 V			1	mA
		VDDIO = 1.2 V			0.1	
I_{LKG}	Input leakage current	Input pins tied to V_{IL}or V_{IH}			0.2	µA
TdHL	CLK_REQ1, CLK_REQ2, DCDC3_SEL delay for HIGH to LOW change				2	µs
TdLH	CLK_REQ1, CLK_REQ2, DCDC3_SEL delay for LOW to HIGH change				2	µs
TdLH	PWRON delay for LOW to HIGH change	For TPS657120 in STANDBY mode going to ACTIVE		4	30%	ms

4.10 Electrical Characteristics: Thermal Shutdown, Undervoltage Lockout

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature rising threshold		136	148	160	°C
Thermal shutdown temperature hysteresis	Temperature falling		20		°C
UVLO threshold	Supply voltage rising			2.7	V
UVLO threshold	Supply voltage falling			2.6	V

4.11 Electrical Characteristics: RFFE Timing Parameters

T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{CLK}	SCLK frequency	For write access	0.032		26	MHz
f_{CLK_HALF}	SCLK half-speed frequency	For read access	0.032		13	MHz
T_{SCLKIH}	SCLK input high time	For full-speed write access	11.25			ns
T_{SCLKIL}	SCLK input low time	For full-speed write access	11.25			ns
T_S	Data setup time	VDDIO = 1.8 V	1			ns
		VDDIO = 1.2 V	4			
T_H	Data hold time		5			ns
T_D	Time for data output valid from SCLK rising edge	TPS657120 is a half-speed device for read operations	0		22	ns
$T_{SDATAOTRL}$	SDATA output transition (rise/fall) time		2.1		6.5	ns
T_{SDATAZ}	Data drive release time				10	ns

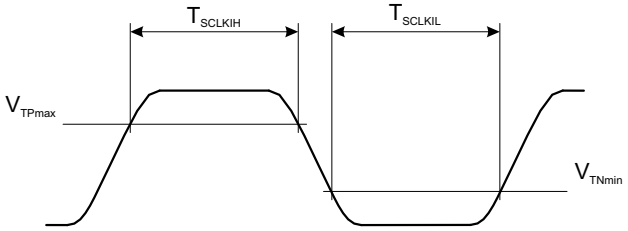


Figure 4-1. MIPI RFFE Received Clock Signal Constraints

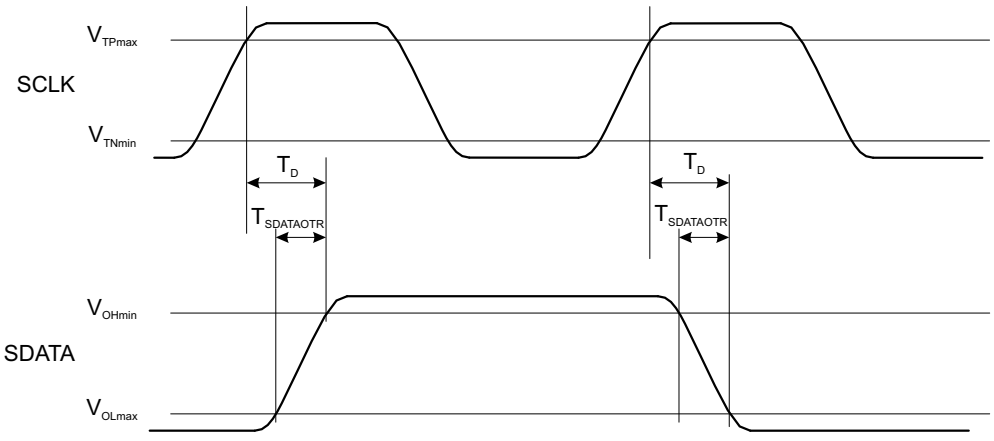


Figure 4-2. MIPI RFFE Bus Active Data Transmission Timing Specification

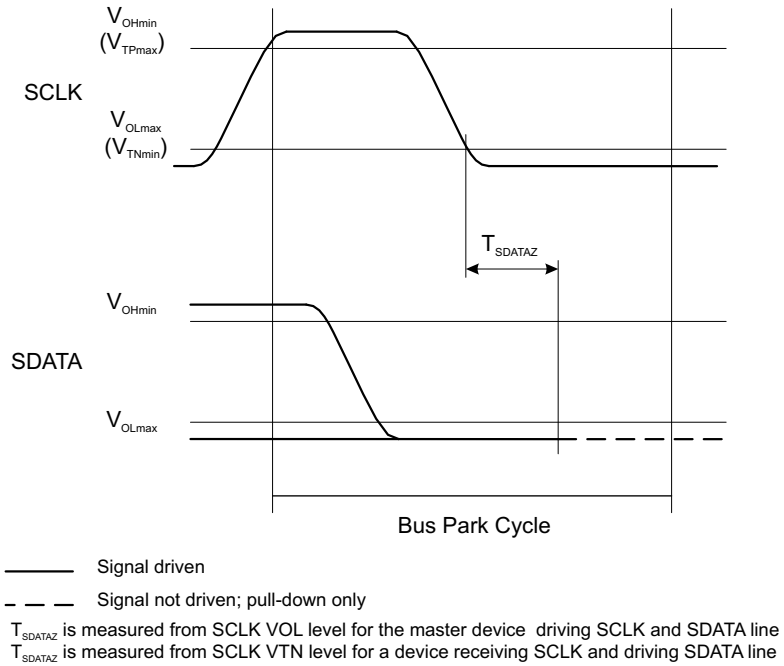


Figure 4-3. MIPI RFFE Bus Park Cycle Timing

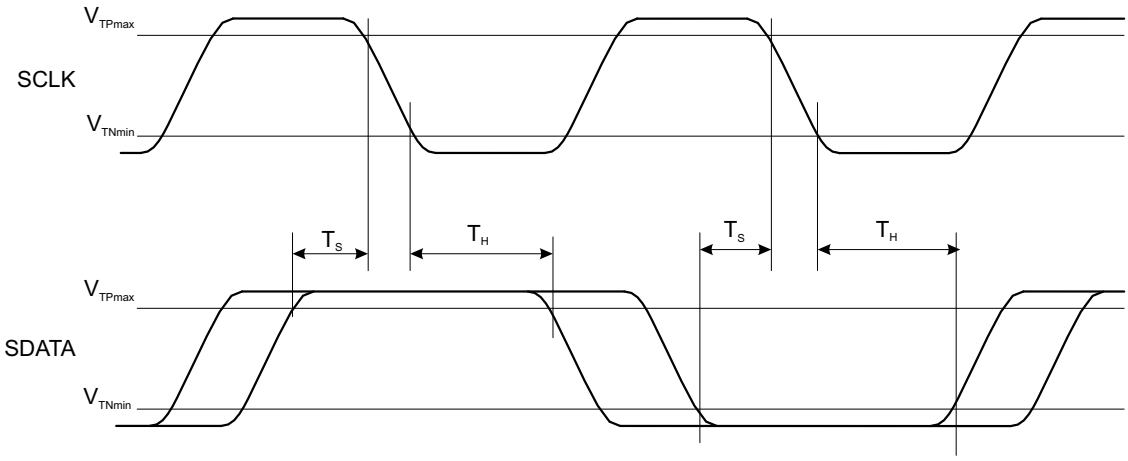


Figure 4-4. MIPI RFFE Data Setup and Hold Timing

4.12 Typical Characteristics

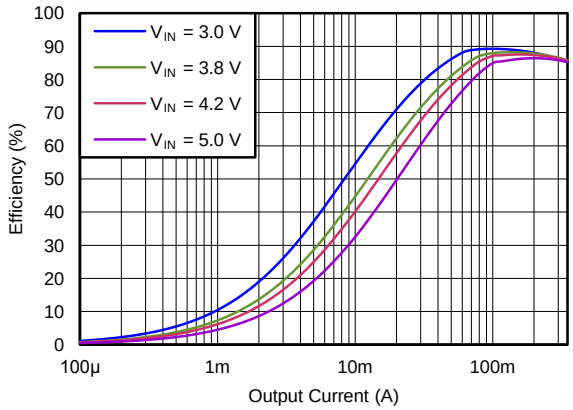
at T_A = 25°C (unless otherwise noted)

The graphs have been generated using the evaluation module (EVM) with the passive components as specified in the recommended operating conditions unless listed below at T_A = 25°C, unless otherwise specified:

- L1 = L2 = DFE201610C-2R2
- L3 = DFE252010-1R5
- CoutDCDC1,2 = 10 µF (GRM188R61A106ME69)
- CoutDCDC3 = 4.7 µF + 2.2 µF (GRM188R60J475KE19 + GRM185R60J225)
- CoutLDO1,2 = 4.7 µF (GRM188R60J475KE19)

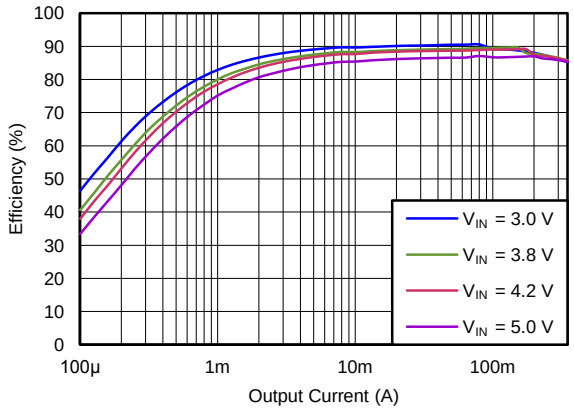
Table 4-1. Table of Graphs

		FIGURE
Efficiency DCDC1 vs Load current / PWM mode	V_O = 1.7 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-5
Efficiency DCDC1 vs Load current / PFM mode	V_O = 1.7 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-6
Efficiency DCDC2 vs Load current / PWM mode	V_O = 2.65 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-7
Efficiency DCDC2 vs Load current / PFM mode	V_O = 2.65 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-8
Efficiency DCDC3 vs Load current / PWM mode	V_O = 0.85 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-9
Efficiency DCDC3 vs Load current / PFM mode	V_O = 0.85 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-10
Efficiency DCDC3 vs Load current / PWM mode	V_O = 2.0 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-11
Efficiency DCDC3 vs Load current / PFM mode	V_O = 2.0 V; V_I = 3.0 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-12
Efficiency DCDC3 vs Load current / PWM mode	V_O = 3.4 V; V_I = 3.6 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-13
Efficiency DCDC3 vs Load current / PFM mode	V_O = 3.4 V; V_I = 3.6 V, 3.8 V, 4.2 V, 5.0 V	Figure 4-14
Load transient response DCDC1 in PWM mode	I_O= 30 mA to 270 mA; V_O = 1.7 V; V_I = 3.6 V	Figure 4-15
Load transient response DCDC1 in PFM mode	I_O= 30 mA to 270 mA; V_O = 1.7 V; V_I = 3.6 V	Figure 4-16
Load transient response DCDC2 in PWM mode	I_O= 30 mA to 270 mA; V_O = 2.65 V; V_I = 3.6 V	Figure 4-17
Load transient response DCDC2 in PFM mode	I_O= 30 mA to 270 mA; V_O = 2.65 V; V_I = 3.6 V	Figure 4-18
Load transient response DCDC3 in PFM mode	I_O= 100 mA to 900 mA; V_O = 2.0 V; V_I = 3.6 V	Figure 4-19
Load transient response DCDC3 in PFM mode	I_O= 200 mA to 1800 mA; V_O = 3.4 V; V_I = 3.8 V	Figure 4-20
Line transient response DCDC1 in PWM mode	V_O= 1.7 V; V_I = 3.6 V to 4.2 V; I_O= 100 mA	Figure 4-21
Line transient response DCDC1 in PFM mode	V_O= 1.7 V; V_I = 3.6 V to 4.2 V; I_O= 100 mA	Figure 4-22
Line transient response DCDC2 in PWM mode	V_O= 2.65 V; V_I = 3.6 V to 4.2 V; Load = 26.5 Ω at 100 mA	Figure 4-23
Line transient response DCDC2 in PFM mode	V_O= 2.65 V; V_I = 3.6 V to 4.2 V; Load = 26.5 Ω at 100 mA	Figure 4-24
Line transient response DCDC3 in PFM mode	V_O = 2.0 V; V_I= 3.6 V to 4.2 V; Load = 1.6 Ω at 1.25 A	Figure 4-25
Line transient response DCDC3 in PFM mode	V_O = 3.4 V; V_I= 3.6 V to 4.2 V; Load = 3.1 Ω at 1.1 A	Figure 4-26
PSRR for DCDC1	V_O = 1.7 V; V_I= 3.6 V; Load = 80 mA, 150 mA	Figure 4-27
PSRR for DCDC2	V_O = 2.65 V; V_I= 3.6 V; Load = 80 mA, 150 mA	Figure 4-28
PSRR for DCDC3	V_O = 2.0 V; V_I= 3.6 V; Load = 80 mA, 150 mA	Figure 4-29
PSRR for DCDC3	V_O = 3.4 V; V_I= 3.6 V; Load = 80 mA, 150 mA	Figure 4-30
Load transient response for LDO1 in PFM mode	I_O= 1 mA to 9 mA; V_O = 1.8 V; V_I = 3.6 V	Figure 4-31
Load transient response for LDO2 in PFM mode	I_O= 1 mA to 9 mA; V_O = 2.8 V; V_I = 3.6 V	Figure 4-32
Line transient response LDO1	V_O = 1.8 V; V_I= 3.6 V to 4.2 V; Load = 180 Ω at 10 mA	Figure 4-33
Line transient response LDO2	V_O = 2.8 V; V_I= 3.6 V to 4.2 V; Load = 280 Ω at 10 mA	Figure 4-34
PSRR for LDO1	V_O = 1.8 V; Load = 10 mA; V_I = 2.7 V, 3.3 V	Figure 4-35
PSRR for LDO2	V_O = 2.8 V; Load = 10 mA; V_I = 3.3 V, 3.6 V	Figure 4-36
Output noise for LDO1	V_O = 1.8 V; Load = 180 Ω at 10 mA; V_I= 3.6 V	Figure 4-37
Output noise for LDO2	V_O = 2.8 V; Load = 280 Ω at 10 mA; V_I= 3.6 V	Figure 4-38
Startup DCDC1, DCDC2, LDO1, and LDO2	V_I= 3.6 V; Load = Open	Figure 4-39



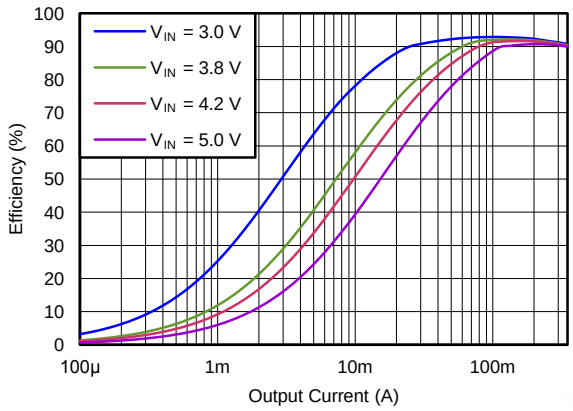
DCDC1 V_O = 1.7 V

Figure 4-5. Efficiency vs Load Current PWM Mode



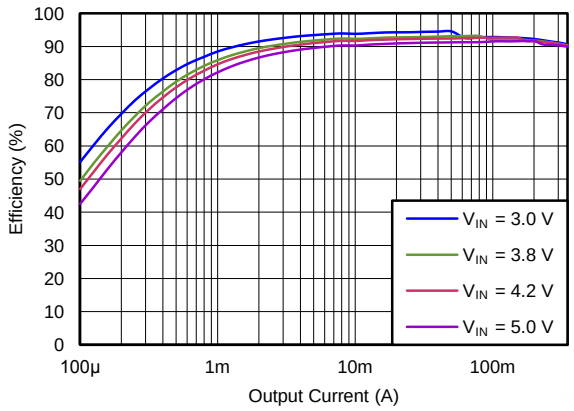
DCDC1 V_O = 1.7 V

Figure 4-6. Efficiency vs Load Current PFM Mode



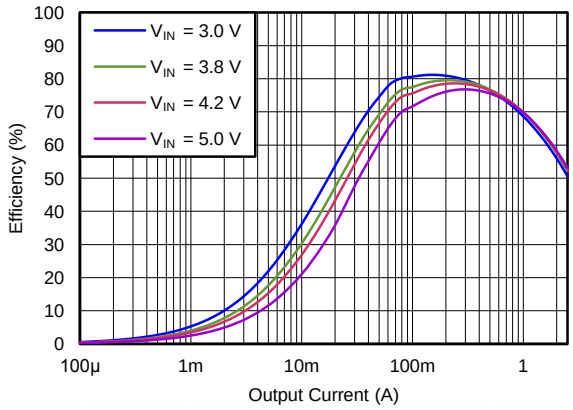
DCDC2 V_O = 2.65 V

Figure 4-7. Efficiency vs Load Current PWM Mode



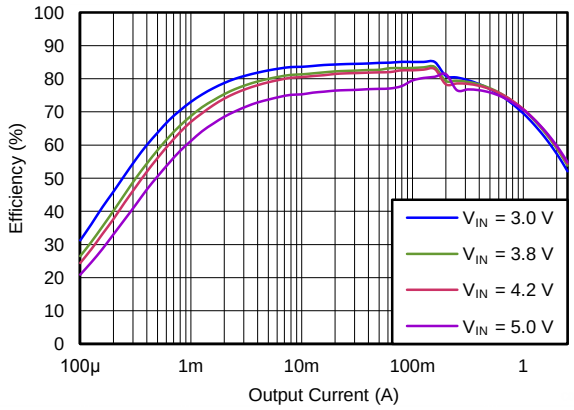
DCDC2 V_O = 2.65 V

Figure 4-8. Efficiency vs Load Current PFM Mode



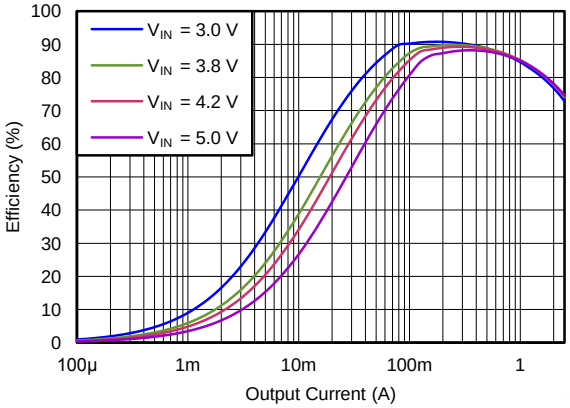
DCDC3 V_O = 0.85 V

Figure 4-9. Efficiency vs Load Current PWM Mode



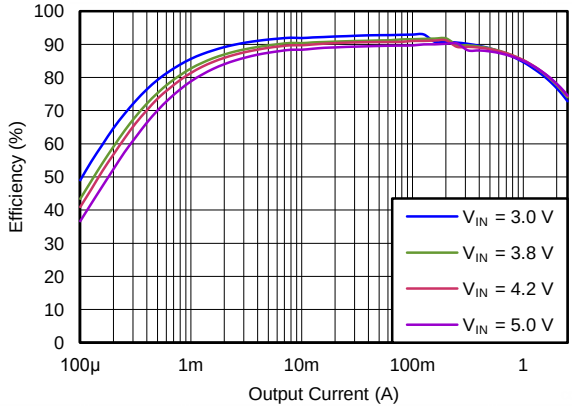
DCDC3 V_O = 0.85 V

Figure 4-10. Efficiency vs Load Current PFM Mode



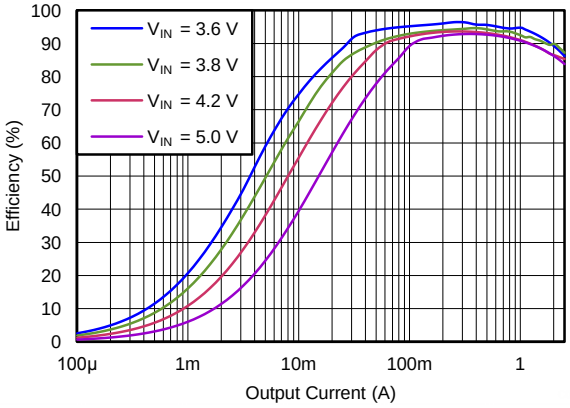
DCDC3 V_O = 2.0 V

Figure 4-11. Efficiency vs Load Current PWM Mode



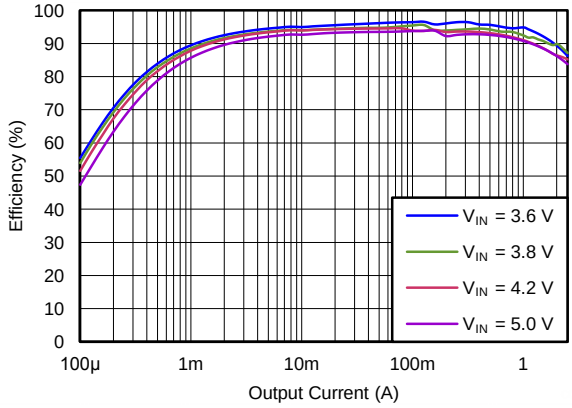
DCDC3 V_O = 2.0 V

Figure 4-12. Efficiency vs Load Current PFM Mode



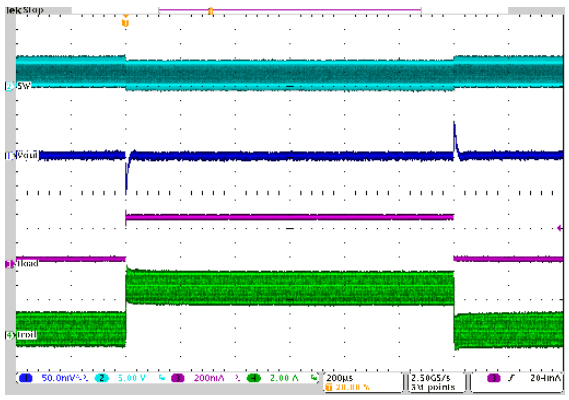
DCDC3 V_O = 3.4 V

Figure 4-13. Efficiency vs Load Current PWM Mode



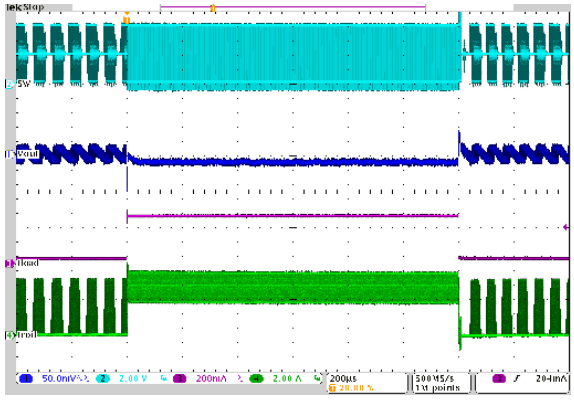
DCDC3 V_O = 3.4 V

Figure 4-14. Efficiency vs Load Current PFM Mode



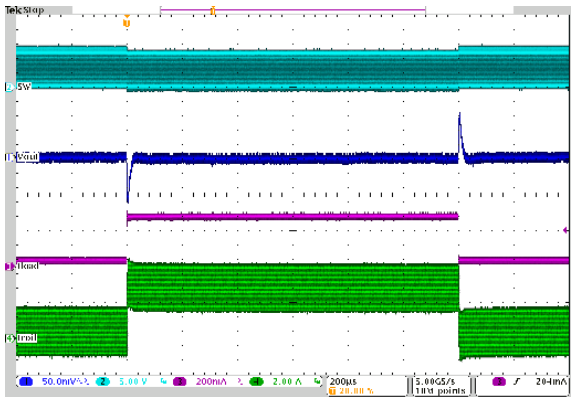
I_O= 30 mA to 270 mA V_O = 1.7 V V_I = 3.6 V

Figure 4-15. Load Transient Response DCDC1 in PFM Mode



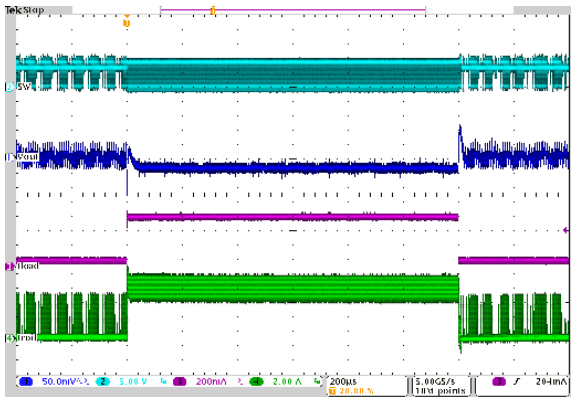
I_O= 30 mA to 270 mA V_O = 1.7 V V_I = 3.6 V

Figure 4-16. Load Transient Response DCDC1 in PFM Mode



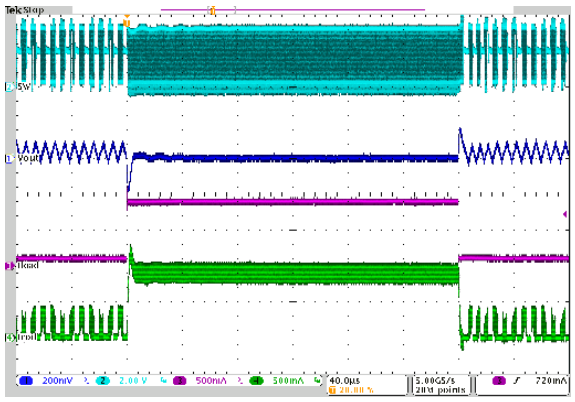
I_O= 30 mA to 270 mA V_O = 2.65 V V_I = 3.6 V

Figure 4-17. Load Transient Response DCDC2 in PFM Mode



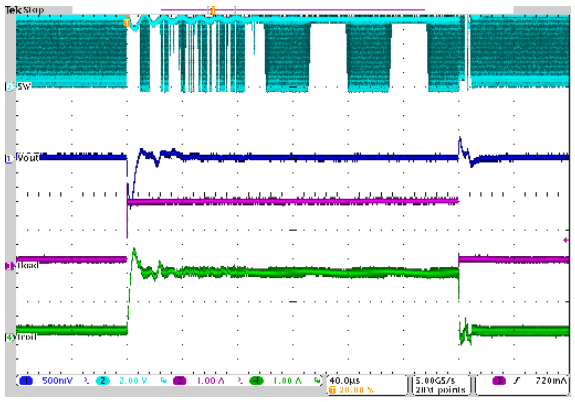
I_O= 30 mA to 270 mA V_O = 2.65 V V_I = 3.6 V

Figure 4-18. Load Transient Response DCDC2 in PFM Mode



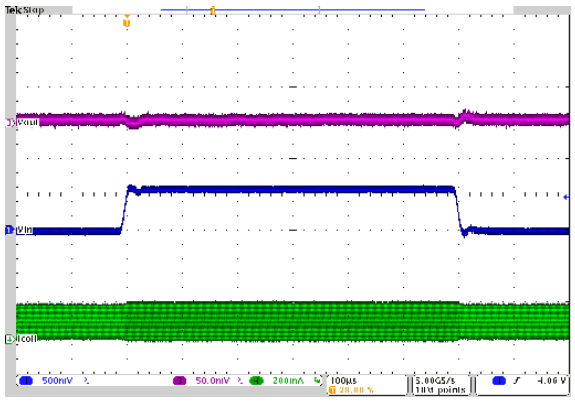
I_O= 100 mA to 900 mA V_O = 2.0 V V_I = 3.6 V

Figure 4-19. Load Transient Response DCDC3 in PFM Mode



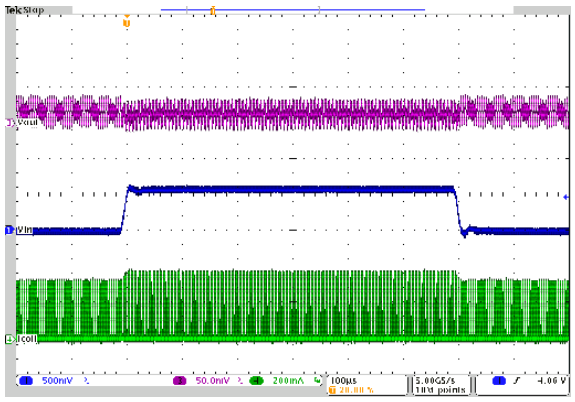
I_O= 200 mA to 1800 mA V_O = 3.4 V V_I = 3.8 V

Figure 4-20. Load Transient Response DCDC3 in PFM Mode



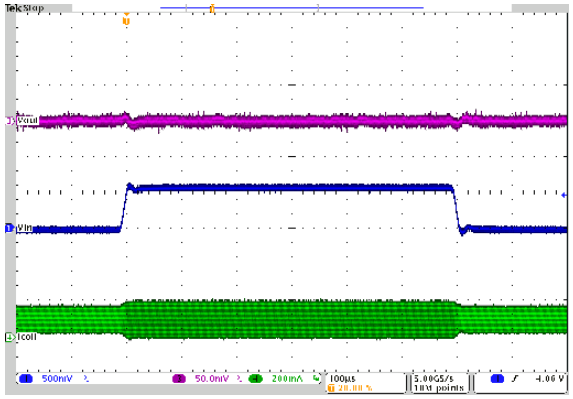
V_O= 1.7 V V_I = 3.6 V to 4.2 V I_O= 100 mA

Figure 4-21. Line Transient Response DCDC1 in PFM Mode



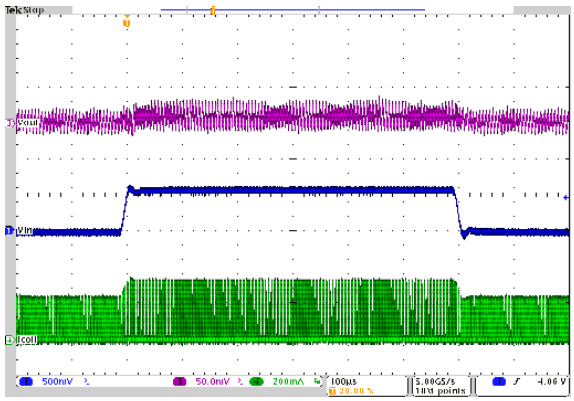
V_O= 1.7 V V_I = 3.6 V to 4.2 V I_O= 100 mA

Figure 4-22. Line Transient Response DCDC1 in PFM Mode



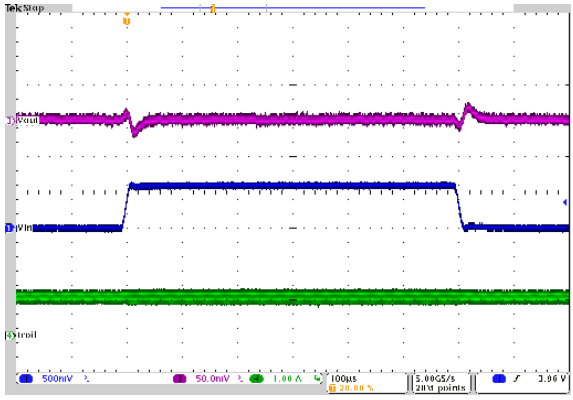
V_O= 2.65 V V_I = 3.6 V to 4.2 V Load = 26.5 Ω at 100 mA

Figure 4-23. Line Transient Response DCDC2 in PFM Mode



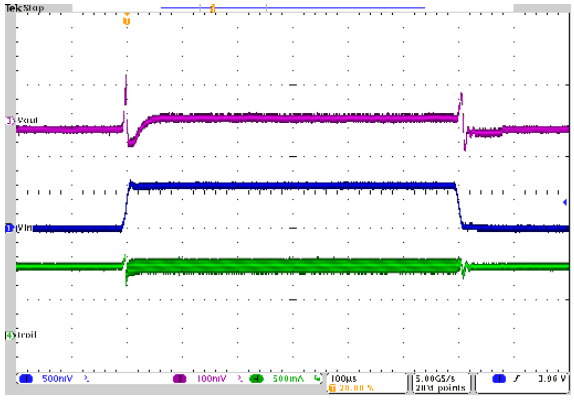
V_O= 2.65 V V_I = 3.6 V to 4.2 V Load = 26.5 Ω at 100 mA

Figure 4-24. Line Transient Response DCDC2 in PFM Mode



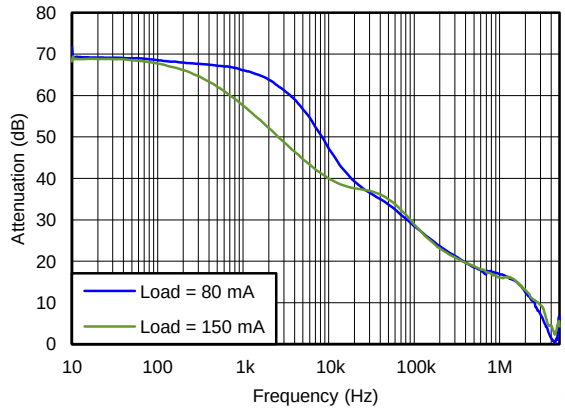
V_O = 2.0 V V_I= 3.6 V to 4.2 V Load = 1.6 Ω at 1.25 A

Figure 4-25. Line Transient Response DCDC3 in PFM Mode



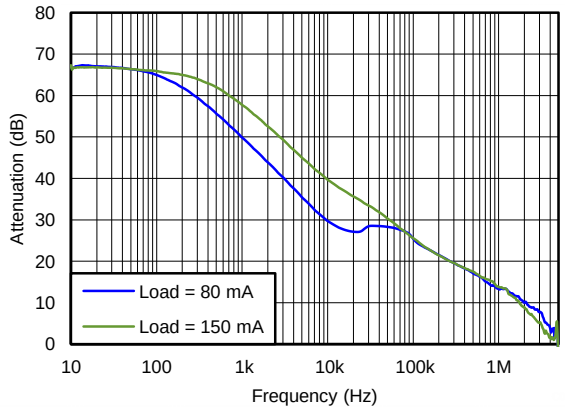
V_O = 3.4 V V_I= 3.6 V to 4.2 V Load = 3.1 Ω at 1.1 A

Figure 4-26. Line Transient Response DCDC3 in PFM Mode



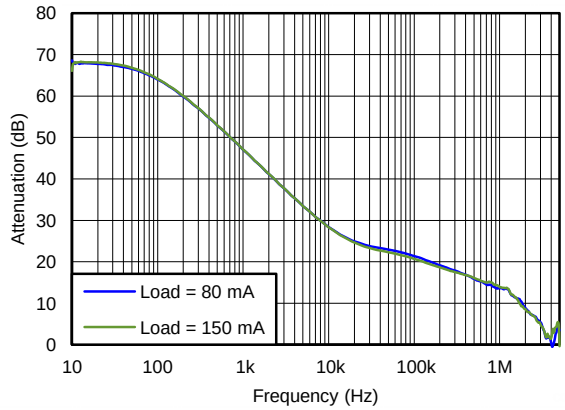
V_O = 1.7 V V_I= 3.6 V Load = 80 mA, 150 mA

Figure 4-27. PSRR for DCDC1



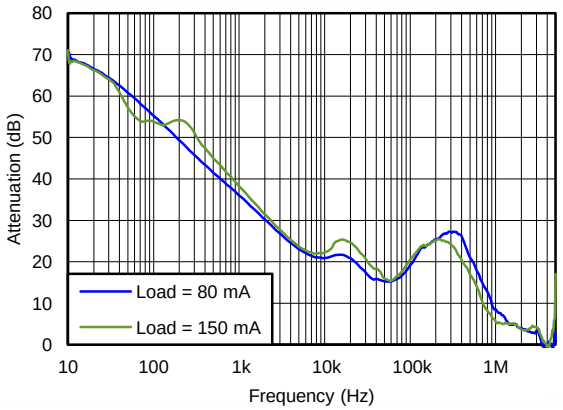
V_O = 2.65 V V_I= 3.6 V Load = 80 mA, 150 mA

Figure 4-28. PSRR for DCDC2



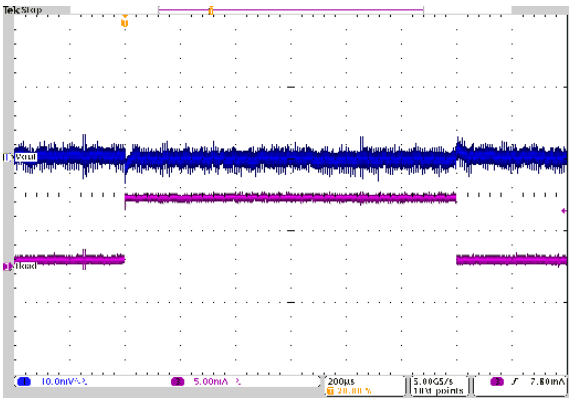
V_O = 2.0 V V_I= 3.6 V Load = 80 mA, 150 mA

Figure 4-29. PSRR for DCDC3



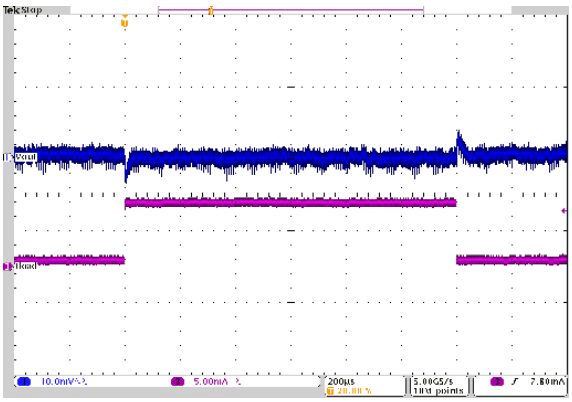
V_O = 3.4 V V_I= 3.6 V Load = 80 mA, 150 mA

Figure 4-30. PSRR for DCDC3



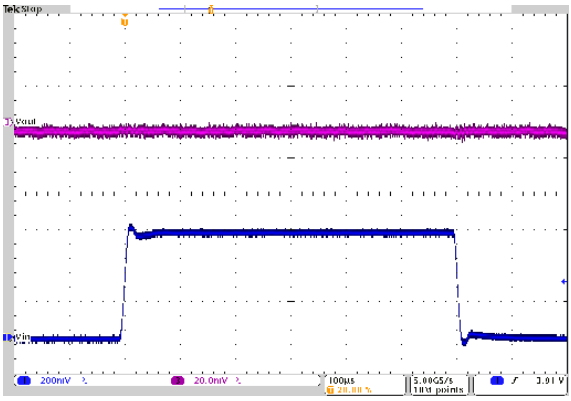
I_O= 1 mA to 9 mA V_O = 1.8 V V_I = 3.6 V

Figure 4-31. Load Transient Response LDO1 in PFM Mode



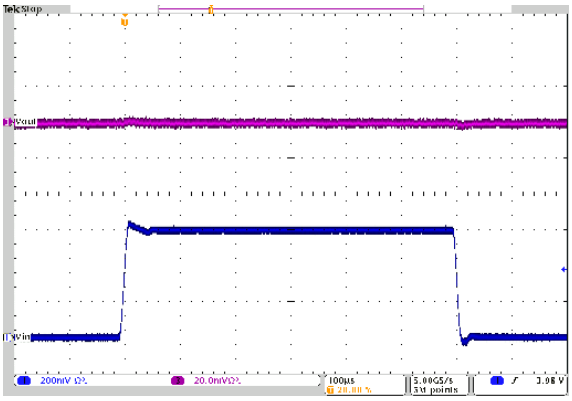
I_O= 1 mA to 9 mA V_O = 2.8 V V_I = 3.6 V

Figure 4-32. Load Transient Response LDO2 in PFM Mode



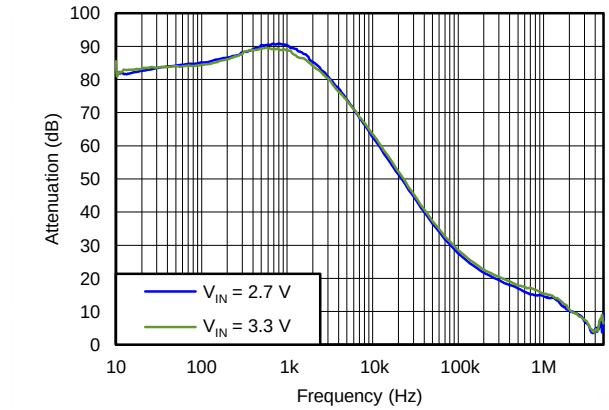
V_O = 1.8 V V_I= 3.6 V to 4.2 V Load = 180 Ω at 10 mA

Figure 4-33. Line Transient Response LDO1



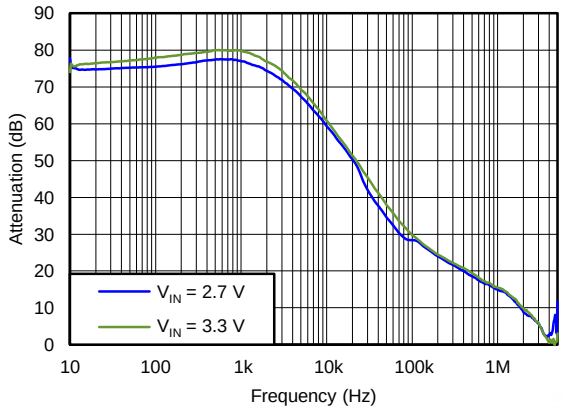
V_O = 2.8 V V_I= 3.6 V to 4.2 V Load = 280 Ω at 10 mA

Figure 4-34. Line Transient Response LDO2



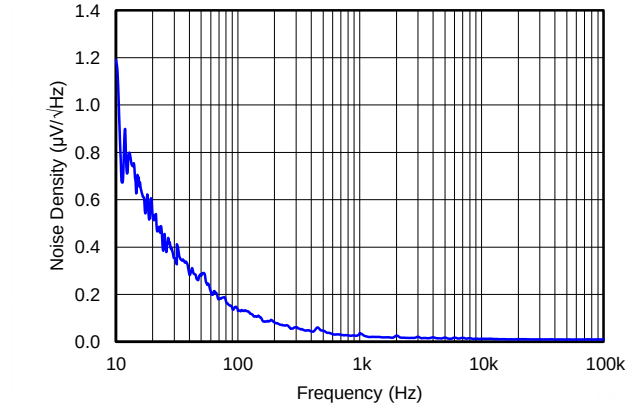
V_O = 1.8 V Load = 10 mA V_I = 2.7 V, 3.3 V

Figure 4-35. PSRR for LDO1



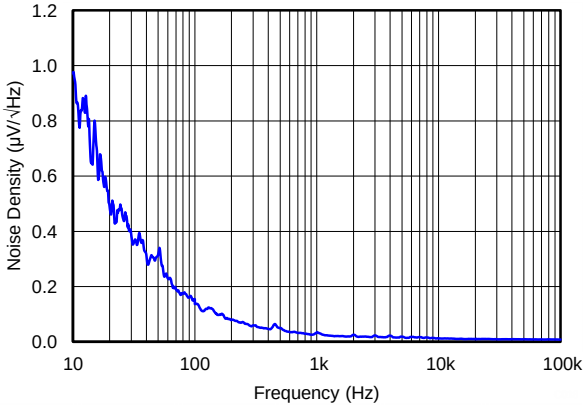
V_O = 2.8 V Load = 10 mA V_I = 3.3 V, 3.6 V

Figure 4-36. PSRR for LDO2



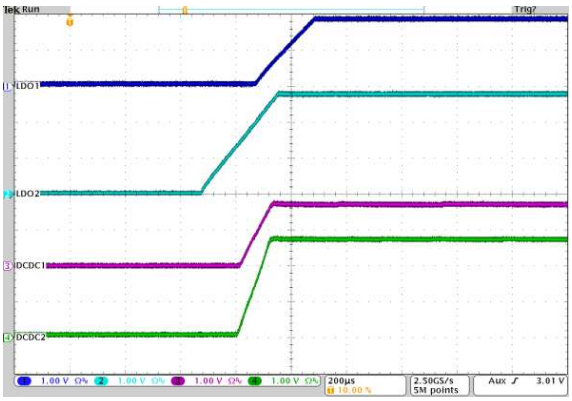
V_O = 1.8 V Load = 180 Ω at 10 mA V_I= 3.6 V

Figure 4-37. Output Noise for LDO1



V_O = 2.8 V Load = 280 Ω at 10 mA V_I= 3.6 V

Figure 4-38. Output Noise for LDO2



V_I= 3.6 V Load = Open

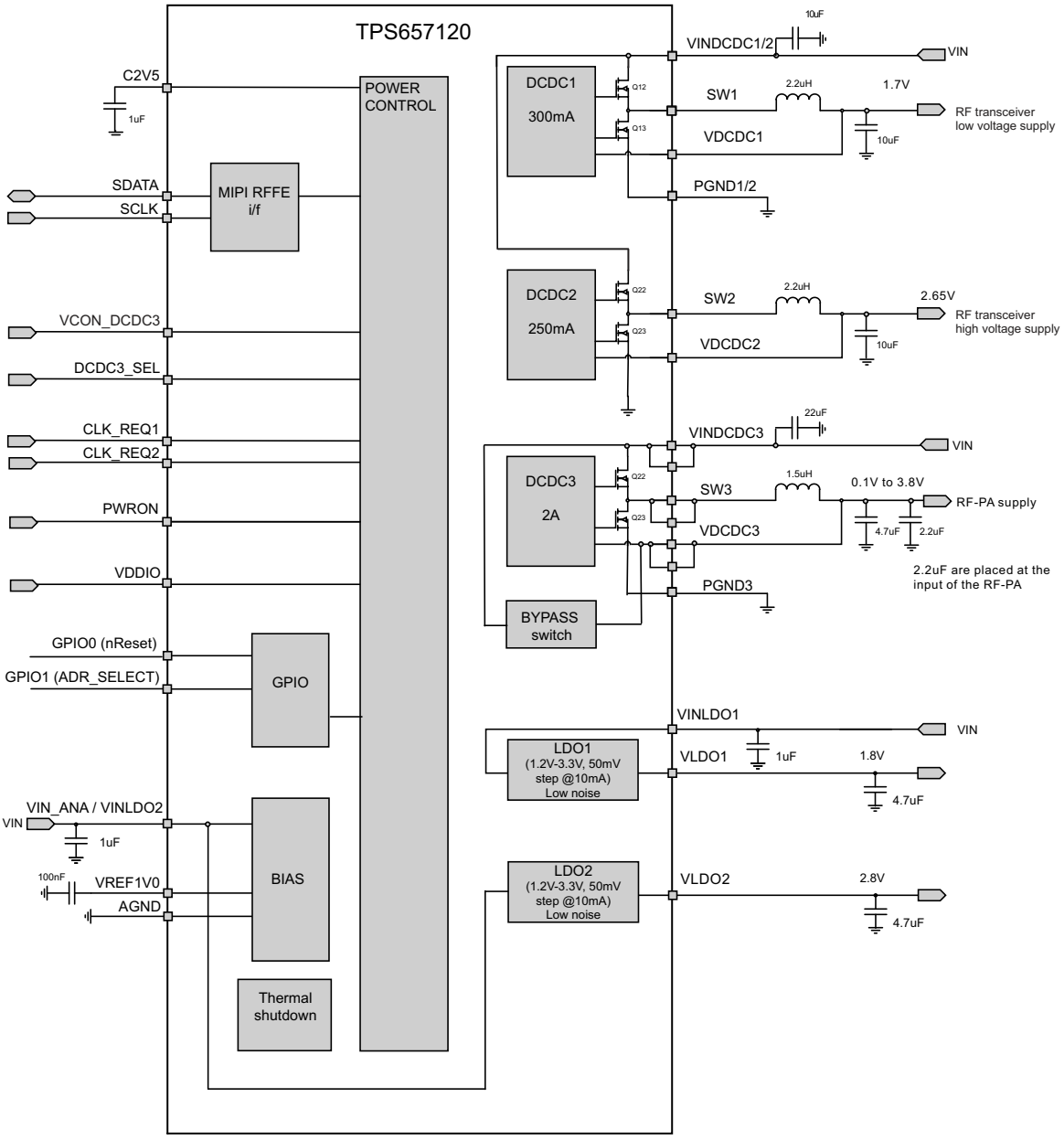
Figure 4-39. Startup DCDC1, DCDC2, LDO1, and LDO2

5 Detailed Description

5.1 Overview

The TPS657120 is an integrated power management device for Baseband and RF-PA power. The device consists of three step-down converters and two LDOs.

5.2 Functional Block Diagram



5.3 Feature Description

5.3.1 Default Settings

See Table 5-1 for the default output voltages for the DCDC converters and the LDOs. For DCDC1 to DCDC3 and LDO1 and LDO2, there are two registers defining the output voltage. DCDC3_SEL allows to switch in between the two output voltages defined in the _OP and _AVS register of DCDC3. For the other DCDC converters and LDOs, switching is possible by a register Bit.

Table 5-1. Default Output Voltages

CONVERTER / LDO REGISTER	TPS657120 DEFAULT OUTPUT VOLTAGE SETTING
DCDC1_OP / DCDC1_AVS	1.7 V / 1.7 V
DCDC2_OP / DCDC2_AVS	2.65 V / 2.65 V
DCDC3_OP / DCDC3_AVS	3.6 V / 3.6 V
LDO1_OP	1.8 V
LDO2_OP	2.8 V
CONVERTER / LDO REGISTER	**TPS657121 DEFAULT OUTPUT VOLTAGE SETTING**
DCDC1_OP / DCDC1_AVS	1.2 V / 1.2 V (for DIG)
DCDC2_OP / DCDC2_AVS	TBD (for LVANA or ANALOG)
DCDC3_OP / DCDC3_AVS	TBD (for LVANA or RF-PA)
LDO1_OP	2.7 V (for VVANA)
LDO2_OP	2.8 V (for TCXO)

5.3.2 Linear Regulators

The power management core has 2 high PSRR, low noise LDOs with different output current capabilities. Each LDO output voltage can be set independently through the communication bus (see Table 5-19) and the transition occurs immediately if the LDO is enabled.

5.3.2.1 Low Quiescent Current (Eco) Mode

Each LDO is equipped with a low quiescent current mode that can enabled or disabled separately by setting the ECO bit = 1.

5.3.2.2 Output Discharge

Each LDO is equipped with an output discharge bit. When the bit is set to 1, the output of the LDO will be discharged to ground with the equivalent of a 300-Ω resistor if the LDO is disabled. If the LDO is enabled, the discharge bit is ignored.

5.3.2.3 LDO Enable

The LDOs enable/disable is part of the flexible power-up and power-down state machine. Each LDO can be programmed such that it is powered up automatically in one of the 15 time slots after a power-on condition occurs or is controlled by a dedicated pin. Pins CLK_REQ1 and CLK_REQ2 can be mapped to any resource (LDOs, dcdc converters) to enable or disable it.

5.3.2.4 LDO Voltage Range

The output voltage range for the LDOs is 1.2 V to 3.3 V.

5.3.2.5 LDO Power Good Comparator

The output voltage of each LDO is supervised by an internal power good comparator. Its output is setting and clearing the PGOOD Bits in register PGOOD. The power good Bits are not valid if the LDO is enabled but the input voltage to the LDO is below 1 V.

5.3.3 Step-down Converters DCDC1 and DCDC2

The TPS657120 step down converters operate with typically 2.25-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. With DCDCx_MODE bit set to *0*, at light load currents the converter can automatically enter Power Save Mode and operates then in PFM mode.

During PWM operation the converter uses a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the High Side MOSFET switch is turned on. The current flows now from the input capacitor via the High Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the High Side MOSFET switch is exceeded. After an off time preventing shoot through current, the Low Side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the Low Side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the Low Side MOSFET rectifier and turning on the on the High Side MOSFET switch. A 180° phase shift between DCDC1 and DCDC2 decreases the input RMS current and synchronizes the operation of the two dcdc converts. The feedback pin (VDCDCx) must directly be connected to the output voltage of the DCDC converter and no external resistor network must be connected.

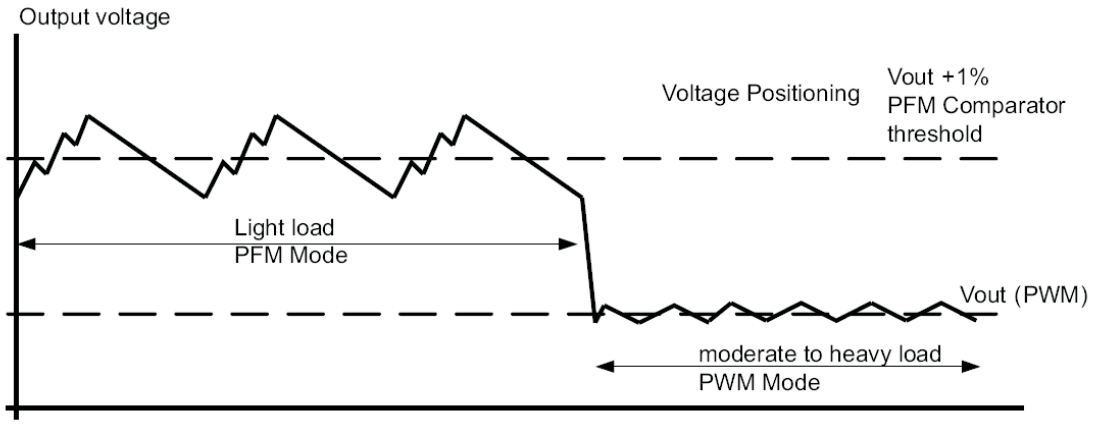
5.3.4 Power Save Mode

The Power Save Mode is enabled with the DCDCx_MODE bit set to *0*. If the load current decreases, the converter will enter Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step. The transition from PWM mode to PFM mode occurs once the inductor current in the Low Side MOSFET switch becomes zero, which indicates discontinuous conduction mode. During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of VOUT nominal +1%, the device starts a PFM current pulse. The High Side MOSFET switch will turn on, and the inductor current ramps up. After the On-time expires, the switch is turned off and the Low Side MOSFET switch is turned on until the inductor current becomes zero. The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 25-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold. With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM Pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values. The PFM mode is left and PWM mode is entered in case the output current can not longer be supported in PFM mode. The Power Save Mode can be disabled by setting Mode pin to high. The converter will then operate in fixed frequency PWM mode.

5.3.5 Dynamic Voltage Positioning (Optional)

This feature reduces the voltage under/overshoots at load steps from light to heavy load and heavy to light. It is active in Power Save Mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off. Dynamic voltage positioning is an optional feature set at TI and can be enabled / disabled on request.



5.3.6 Soft Start / Enable

Step-Down converter ENABLE

The step-down converter enable/disable is part of the flexible power-up and power-down state machine. Each converter can be programmed such that it is powered up automatically in one of the 15 time slots after a power-on condition occurs or is controlled by a dedicated pin. Pins CLK_REQ1 and CLK_REQ2 can be mapped to any resource (LDOs, dcdc converter) to enable or disable it.

Step-Down converter SOFT START

The step-down converters in TPS657120 have an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within a time defined in the electrical spec. This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used. The Soft start circuit is enabled after the start up time t_{Start} has expired. For DCDC3, there is an option to set two different values for the start-up and ramp-time. For applications that require a fast response, set DCDC3_CTRL:RAMP_TIME = 1.

During soft start, the output voltage ramp up is controlled as shown in Figure 5-1.

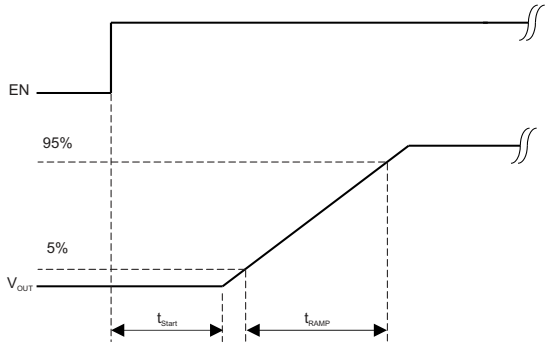


Figure 5-1. Soft Start

5.3.7 Dynamic Voltage Scaling (DVS) for DCDC1, DCDC2 and DCDC3

The DCDC converters in TPS657120 allow to change the output voltage during operation by changing the register content or by switching between the settings defined by DCDCx_OP and DCDCx_AVS registers. Switching between DCDCx_OP and DCDCx_AVS registers is done by pin DCDC3_SEL. The name indicates that the pin is used for DCDC3 exclusively but DCDC1 and/or DCDC2 could be mapped to the pin same as DCDC3 to change in between two different output voltages by toggling the pin. Mapping of the voltage scaling function is done by DCDCx_CTRL registers bit DCDCx_SEL_CTRL for each of the converters. When a change in output voltage occurs, the new voltage will be ramped to either immediately if DCDCx_CTRL:IMMEDIATE=1 or the slew rate defined by DCDCx_CTRL:TSTEP with the IMMEDIATE bit set to 0. The slew rate control is implemented such that TSTEP defines the time from one output voltage step to the next, stepping through all steps until the new target is reached. While the voltage change is active, the converter is forced to PWM mode to allow defined rise and fall times of the output voltage. DVS is not active for DCDC3 when operated in VCON mode but the converter will follow the analog signal at VCON.

The DVS state machine which ramps the output voltage to the target within the programmed time is automatically disabled when a converter is disabled. Therefore a voltage change will only be processed if the converter is active. If a converter is being disabled, the target voltage in the register now is changed with a certain TSTEP setting and the converter is enabled, the DVS will start to ramp to the target. For the two slowest TSSTEP settings, the 130-µs initial enable delay of a converter will not be long enough to cover that ramp time. This will result in a voltage, still ramping to the new target during power-up.

5.3.8 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the High Side MOSFET switch is turned on 100% for one or more cycles. With further decreasing VIN the High Side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated with Equation 1.

$$V_{IN}min = V_O max + I_O max \, (R_{DS(on)} max + R_L) \quad (1)$$

where

- $I_O$max = maximum output current plus inductor ripple current
- $R_{DS(on)}$max = maximum high side switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_O$max = nominal output voltage plus maximum output voltage tolerance

5.3.9 180° Out-of-Phase Operation

In PWM Mode, the converters operate with a 180° turn-on phase shift of the PMOS (high side) transistors. This prevents the high-side switches of both converters from being turned on simultaneously, and therefore smooths the input current. This feature reduces the surge current drawn from the supply.

5.3.10 Undervoltage Lockout for DCDC1, DCDC2, DCDC3, LDO1 and LDO2

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the DC-DC converters and LDOs at too low input voltages. See the electrical characteristics for the undervoltage lockout threshold voltage.

5.3.11 Output Voltage Discharge

The dcdc converters and LDOs contain an output capacitor discharge feature which makes sure that the capacitor is discharged when the dcdc converter or LDO is disabled.

5.3.12 Short-Circuit Protection

All outputs are short circuit protected with a maximum output current as defined in the electrical specifications.

5.3.13 Output Voltage Monitoring

Internal power good comparators monitors the switching regulator outputs and detect when the output voltage is below the target value. This information is used by the power management core to set and clear the power good Bits in the register set accordingly. A switching regulator's individual power good comparator will be blanked when the regulator is disabled or when the regulator's voltage is transitioning from one set point to another.

5.3.14 Step-Down Converter and LDO Enable; pins CLK_REQ1 and CLK_REQ2

The step-down converter and LDO enable/disable is part of the flexible power-up and power-down state machine. Each converter can be programmed such that it is powered up automatically at the beginning of on out of 8 time slots after a power-on condition occurs. Alternatively, a resource can be mapped to a dedicated pin controlling the enable function. Pins CLK_REQ1 and CLK_REQ2 serve this function for any resource (LDO, DCDC converter) to enable or disable it. As long as a resource is not mapped to a pin, the enable bit defines the status. If a resource is mapped to a pin, the status of the enable bit is ignored and the pin controls the enable function.

As soon as a resource is mapped to the CLK_REQ1 pin and there is a falling edge on that pin, all _OP and _AVS registers (for all resources) are re-loaded to their OTP default settings. For Rev 1.0 of silicon the default settings were loaded based on a falling edge of either one of the CLK_REQ pins. During the 25us it takes to re-load the registers, the RFFE interface is in reset and no communication is possible. The RFFE interface is also held in reset during a 2.5-µs period after a rising edge of the CLK_REQx pins. CLK_REQ mapping should be done with a 2-µs setup time; for example, CLK_REQ pins shall have a stable, high-level 2 µs before the pin is mapped for a converter which is on by default.

5.3.15 Step-Down Converter DCDC3

DCDC3 is intended to be used as the power supply for a RF- power amplifier (RF-PA). Its output current of up to 2.5A allows operation with 2G / 3G and 4G amplifiers. There are two different operating modes with respect to how the output voltage is set:

- **by registers DCDC3_OP or DCDC3_AVS** used for 3G/4G; the output voltage range is 0.8 V to 3.8 V; PWM/PFM mode allowed
- **by analog signal at pin VCON** used for 2G optionally; the output voltage range is 0.1 V to 3.8 V; forced PWM mode only; see details under VCON DECODER

Pin DCDC3_SEL can be mapped to any of the 3 step-down converters but typically is used for DCDC3 only. It allows to switch in between the voltage setting based on DCDC3_OP and DCDC3_AVS. Each, DCDC3_OP and DCDC3_AVS contain the Bits to set the output voltage of DCDC3, force PWM mode and also open/close the BYPASS switch.

5.3.16 DCDC3_SEL Control

5.3.16.1 DCDC3_SEL Control - Voltage Mapping Option

The DCDC3_SEL pin allows to select between two different registers defining operating parameters for DCDC3 such as:

- output voltage of DCDC3
- PWM vs PFM mode of DCDC3
- open / close of the bypass switch of DCDC3

The status of DCDC3_SEL defines which of the two registers is used to define the operating parameters and allows to switch in between by toggling the pin.

- DCDC3_SEL=LOW: parameters defined by DCDC3_OP
- DCDC3_SEL=HIGH: parameters defined by DCDC3_AVS

In addition to DCDC3, DCDC1 and/or DCDC2 could be mapped to the DCDC3_SEL pin to change their output voltage depending on the pin status.

5.3.16.2 DCDC3_SEL Control - Mapping the Enable Signal for the Negative Current Limit of DCDC3 to DCDC3_SEL; Additional Option for Rev 1.1 and Higher Only

In addition to the functionality above, the DCDC3_SEL pin can be mapped to enable and disable the negative current limit for DCDC3. This option may be useful in case of GMSK ramping. During a positive slope, the DCDC3 control loop may counter-regulate with the ramp-up support (DCDC3_EN_UP=1) . In this case disabling the negative current limit of DCDC3 will help to get a smooth ramp-up waveform. For a GMSK falling edge, the negative current limit is needed to ensure a fast down-slope, so it needs to be enabled. In order to enable and disable the negative current limit fast, the function can be mapped to pin DCDC3_SEL. The mapping is done by bit SPARE0:nILIM_MAPPING. If the bit is set = 1, the negative current limit is enabled or disabled depending on the status of the DCDC3_SEL pin which the n should be driven accordingly within a GMSK cycle. This mapping is not gating nor is it gated by other mapping options, so it needs to be made sure the voltage mapping is disabled if not required. Bit SPARE0:EN_nILIM_xl has to be set 1 at least 50 µs before the mapping is done by setting SPARE0:nILIM_MAPPING=1. See details in the register description for SPARE0.

5.3.17 Bypass Switch

There is a bypass switch for DCDC3 with the input pins shared between the bypass switch and the power stage of the step-down converter. The switch is driven manually depending on the settings of EN_BYPASS defined in register DCDC3_OP and DCDC3_AVS.

There is a overvoltage protection (OVP) with a 4.0-V threshold sensed at the output of DCDC3 to protect the RF-PA powered by DCDC3 for cases where the bypass switch is closed and the supply voltage from an unregulated charger / power path is rising immediately to 5 V. In this case, the bypass switch is forced to *open* independent of setting of EN_BYPASS. Bit DCDC_CONTROL:DCDC3_OVP is set to *1* in an OVP event and needs to be cleared in software in order to close the bypass switch again using EN_BYPASS.

When the bypass switch is closed, PWM mode of DCDC3 is blocked and its high side switch is forced ON.

5.3.18 DCDC3 Output Voltage Ramp Support

There is circuitry to ensure a fast output voltage change on DCDC3. This is accomplished by automatically enabling the bypass switch to support a ramp of DCDC3 to higher output voltages independent of the setting of EN_BYPASS. In an OVP event, when DCDC3_OVP is set, the ramp support is disabled and bit DCDC3_OVP has to be cleared for proper operation of the ramp support circuit. In addition, the ramp support can be disabled by clearing DCDC3_EN_UP. In addition, there is a down ramp support which ensures fast down-ramping of DCDC3. That function can be disabled independently from the up-ramping support by DCDC3_EN_DWN and is not affected by the status of the OVP.

From Rev 1.1 of silicon bits DCDC3_S2 and DCDC3_S1 have been added to register DCDC_CONFIG1. The bits allow to change the threshold for the ramp support circuit and therefore allow to adjust the shape of the rising edge of the output voltage during a VCON transition.

There are a couple of register bits to control the function of the ramp support as listed below.

- DCDC_CONFIG:DCDC3_EN_UP: enables the ramp support for rising VCON / output voltages
- DCDC_CONFIG:DCDC3_EN_DWN: enables the ramp support for falling VCON / output voltages
- DCDC_CONFIG:DCDC3_DWN_2X: doubles the current in the ramp down circuit to speed up the down slope
- DCDC_CONFIG:DCDC3[S2:S1]: define the threshold below the nominal output voltage when the ramp support stops supporting

- SPARE0:EN_nILIM_xl: enables or disables the negative current limit in DCDC3; a large current limit speeds up the falling edge of Vout
- SPARE0:EN_FAST_RAMP: rising edge of Vout is further speed up; it is recommended to keep this bit cleared as it may cause overshoot when set

The ramp-up and ramp-down support circuitry is intended to be used during GMSK ramping with the VCON input driven to define the output voltage of DCDC3. It is recommended to keep the ramp support disabled when the DCDC3 converter is not operated in VCON mode (when DCDC3_CTRL:VCON=0).

5.3.19 VCON Decoder

The VCON decoder allows to control the output voltage of DCDC3 by an analog signal to pin VCON. The gain and offset of the VCON decoder can be adjusted by register VCON. Typically it will be driven with an input voltage in the range of 0 mV (or 200 mV) to 2100 mV. In VCON operation, DCDC3 is forced to fixed frequency PWM operation independent of the setting of DCDC3_MODE in register DCDC3_OP or DCDC3_AVS. In addition, the converter is forced to be enabled with VCON=1 independent of the status of the ENABLE bit or status of the CLK_REQ signals if mapped.

The gain and offset settings are listed in the register description for the VCON register. DCDC3 ramp support is used also in VCON mode to ensure a fast transition of the output voltage.

The output voltage of DCDC3 in VCON mode is defined using Equation 2.

$$Vout = V(VCON) \times gain + Voffset \quad (2)$$

With a typical output voltage range at DCDC3 of 100 mV to 3.5 V, the default gain and offset settings are:

- gain: 1.8
- Voffset: –250 mV

5.3.20 Thermal Monitoring and Shutdown

The is a thermal protection module that monitors the junction temperature of the device.

When the Thermal Shutdown temperature threshold is reached the TPS657120 is set under reset and a transition to STANDBY state is initiated. The POWER ON enable conditions of the device will not be taken into consideration until the die temperature has decreased below the Thermal Shutdown threshold.

The thermal protection is enabled in ACTIVE state. The thermal protection is automatically enabled during an STANDBY to ACTIVE state transition and will be kept enabled in STANDBY state after a switch-off sequence caused by a thermal shutdown event. Recovery from this STANDBY state will be initiated (switch-on sequence) when the die temperature will fall below the Thermal Shutdown temperature threshold. In a thermal event, all resources are powered down at the same time.

5.3.21 GPIOs

There are 2 GPIOs in TPS657120. If the output stage is programmed to push-pull, it pulls to the high-voltage set by VDDIO. With VDDIO being below the VDDIO undervoltage lockout, the high side driver is disabled and the output is set to open drain. The default state of the GPIO is defined as an output with state LOW. In addition, the GPIOs allow to add an internal 4.7-kΩ pulldown resistor optionally.

A GPIO can alternatively be programmed such that it is assigned to the power-up sequencing by setting GPIO_CFG=1. In this case the GPIO output will be set according to the definition in GPIOx:GPIO_SET during one of the 8 time slots as defined by internal power-up sequencing.

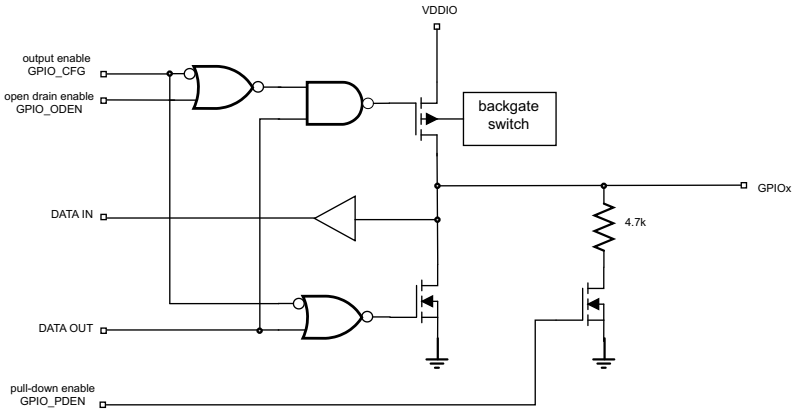


Figure 5-2. GPIO block

5.3.22 nRESET Input ; ADR_SELECT Input

GPIO0 and GPIO1 can optionally be assigned as nRESET input or ADR_SELECT input defining the USID[0] bit as defined in the register description. The alternative function is selected by a bit in the GPIOx register as described as follows:

Detailed description for GPIO0 (nRESET):

- **GPIO0:nRESET=0:** The pin is used as a GPIO based on OTP programming. However, in reset state, before internal OTP is read, the pin defaults to an nRESET input, so the pin has to be pulled to a logic HIGH per default in order to exit reset and load OTP, reconfiguring it as GPIO.
- **GPIO0:nRESET=1 (default OTP setting):** The pin is used as an active low reset input. The pin needs to be pulled to logic HIGH externally to exit reset and allow TPS657120 going to standby state. With GPIO0:nRESET=1, the pin is automatically configured as an input independent of setting of GPIO0:GPIO_CFG.

Detailed description for GPIO1 (ADR_SELECT):

- **GPIO1:ADR_SELECT=0:**The pin is used as a GPIO
- **GPIO1:ADR_SELECT=1 (default OTP setting):** The pin defaults to GPIO and is reprogrammed to an address select bit once internal OTP is read in the boot phase. With GPIO1:ADR_SEL=1, the pin is automatically configured as an input independent of setting of GPIO1:GPIO_CFG. A status change on pin ADR_SELECT will become effective immediately, so USID[0] can be updated at any time by changing the pin status.

5.3.23 Power State Machine

The Embedded Power Controller (EPC) manages the state of the device and controls the power up sequence.

The EPC will support the following states:

- **NO SUPPLY:** The main battery supply voltage is not high enough to power the internal LDO and bandgap. Everything on the device is off.
- **BOOT PHASE (READ OTP):** The internal supply and bandgap are active and the device is reading its configuration data out of OTP memory.
- **STANDBY:** The internal supply and bandgap are active, register default settings have been loaded and the device is waiting for PWRON going HIGH to start the power-up sequence
- **ACTIVE:** Device POWER ON enable conditions are met and regulated power supplies are ON or can be enabled with full current capability. Reset is released; interfaces are active

5.3.24 Implementation of Internal Power-Up and Power-Down Sequencing

TPS657120 allows to internally enable resources during power-up (going from STAND-BY to ACTIVE state) and power-down (going from ACTIVE to STANDBY state) . The internal power-sequencing is defined in OTP memory programmed at TI. The sequencing allows to enable resources in 8 time slots during power-up and power-down. A resource can be associated to any of these 8 time slots that will be processed in the opposite direction during power-down. The delay in between the time slots is fixed to 500 µs.

Resources may include:

- step-down converters
- LDOs
- GPIOs

Resources that are not part of the automatic sequencing may be configured such that they are enabled by external pins or by their enable Bit in the register set. See STEP-DOWN CONVERTER ENABLE

5.3.25 VDDIO Voltage for Push-pull Output Stages / Interface

Push-pull output stages are pulled HIGH to the voltage applied at pin VDDIO for the pins listed below:

- SDATA
- GPIO0,1: push-pull only

The signal levels on the interface pins SDATA and SCLK are on VDDIO level. No voltage must be applied exceeding the voltage level at VDDIO.

5.3.26 TPS657120 On Off Operation

The power-up sequencing in TPS657120 is flexible and can be set such that it allows to power up the converters and LDOs in any order with the down-sequencing being the reverse or all converters and LDOs powering down at the same time.

5.3.26.1 TPS657120 Power-Up

If PWRON is tied to the supply voltage so TPS65712 starts its power-up sequencing once the input voltage is above the UVLO threshold and the internal boot phase is finished.

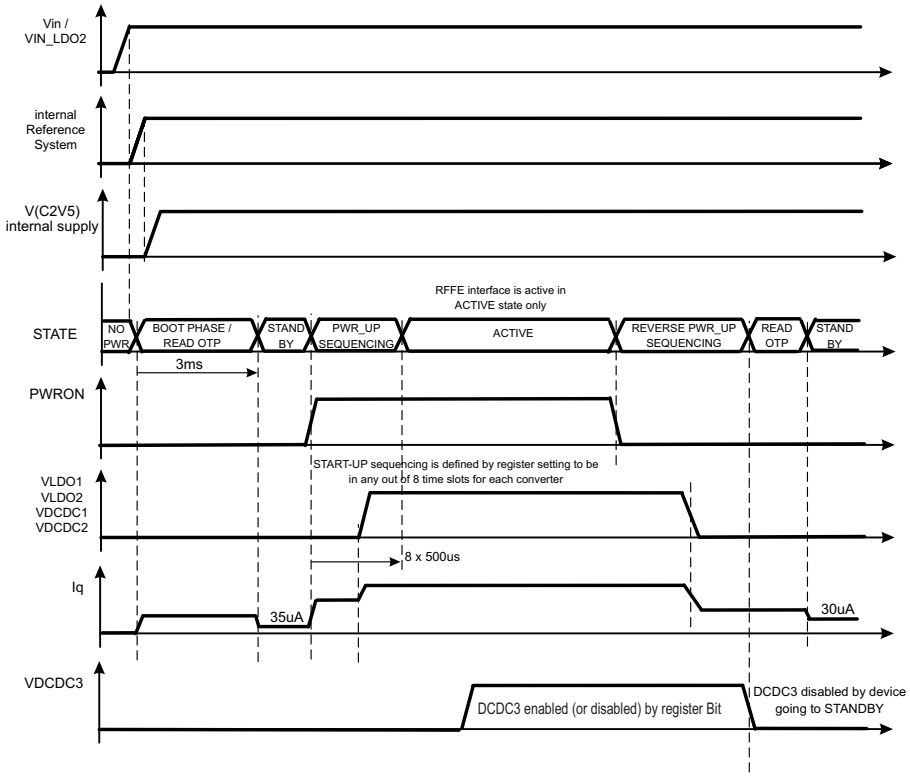


Figure 5-3. TPS657120 Power-Up

5.3.26.2 TPS657120 PWR_REQ Driving DCDC1, DCDC2 and LDO1

Once the CLK_REQ1 and CLK_REQ2 pins are enabled to take control of DCDC1, DCDC2 and LDO1, these converters/LDO are enabled if either one of the pins is driven HIGH.

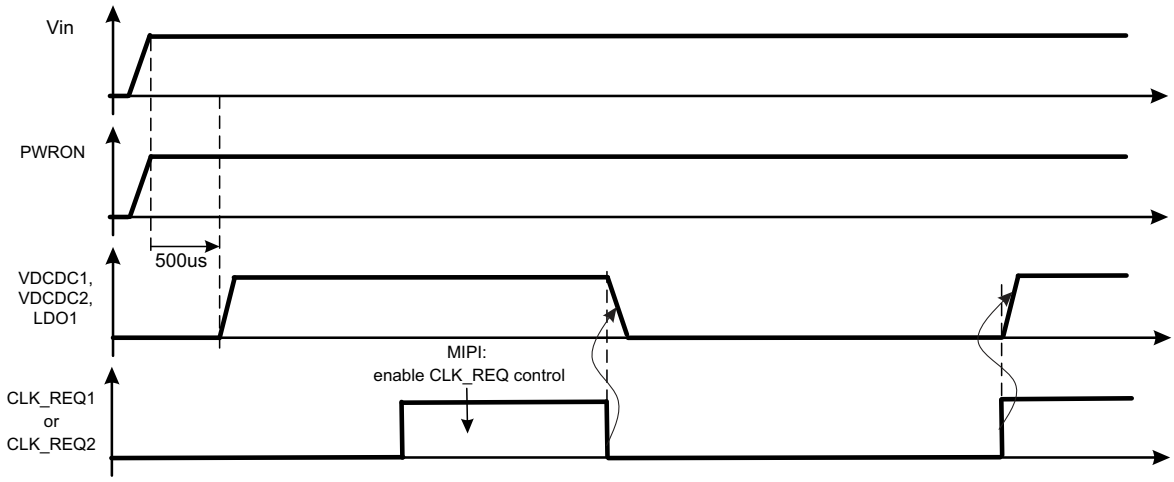


Figure 5-4. TPS657120 Power Cut

5.3.27 MIPI RFFE Interface

There is a MIPI RFFE compatible interface based on the Rev 1.00.00 specification. The interface is only active in ACTIVE state of TPS657120 - see the power-up timing diagram. RFFE communication is not possible when the _OP and _AVS register are reloaded triggered by a falling edge on CLK_REQx once any DCDC converter or LDO is mapped to that pin. During the 25 µs of re-loading the registers with the OTP content, the RFFE interface is held in reset. The RFFE interface is also held in reset during a 2.5-µs period after a rising edge of the CLK_REQx pins. The slave address bits SA3...SA0 are equivalent to the *unique slave identifier* (USID) defined in the MIPI RFFE specification. As defined in the RFFE specification, the bits are located in register USID along with the other RFFE-pre-defined registers PM_TRIG, PRODUCT_ID and MANUFACTURER_ID at address 0x1C to 0x1F.

5.3.27.1 MIPI RFFE Write Cycle

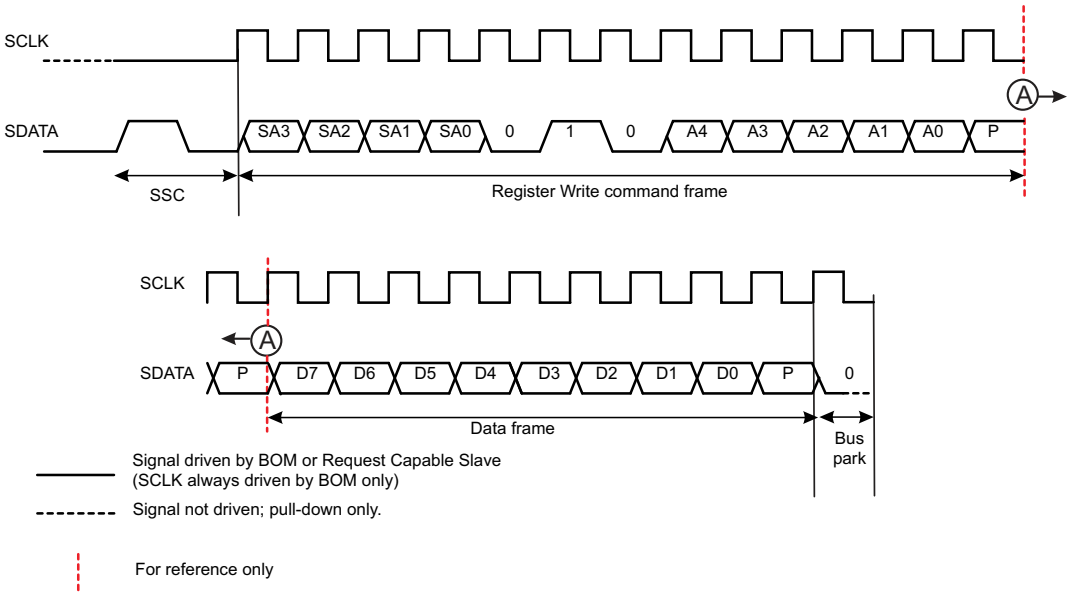


Figure 5-5. RFFE Write Cycle

5.3.27.2 MIPI RFFE Read Cycle

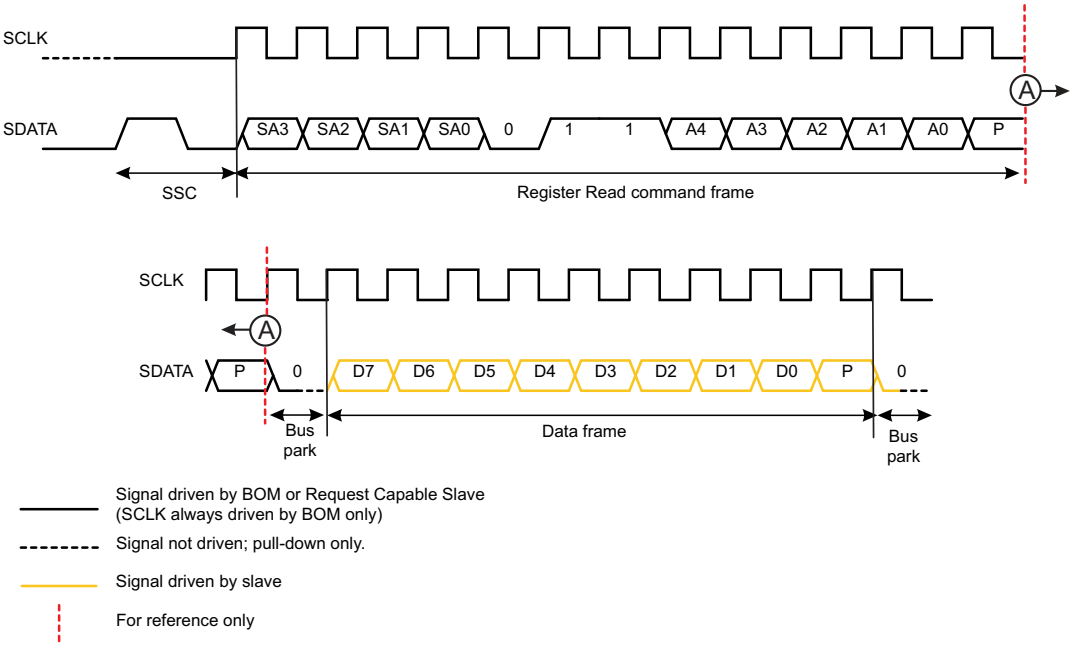


Figure 5-6. RFFE Read Cycle

5.4 Device Functional Modes

The device supports the following functional modes.

- **NO SUPPLY:** The main battery supply voltage is not high enough to power the internal LDO and bandgap. Everything on the device is off.
- **BOOT PHASE (READ OTP):** The internal supply and bandgap are active and the device is reading its configuration data out of OTP memory.
- **STANDBY:** The internal supply and bandgap are active, register default settings have been loaded and the device is waiting for PWRON going HIGH to start the power-up sequence
- **ACTIVE:** Device POWER ON enable conditions are met and regulated power supplies are ON or can be enabled with full current capability. Reset is released; interfaces are active

5.5 Register Maps

Table 5-2. DCDC1_CTRL(1); Register Address: 00h

B7	B6	B5	B4	B3	B2	B1	B0
ENABLE	RSVD	IMMEDIATE	TSTEP[1]	TSTEP[0]	DCDC1_ SEL_CTRL	DCDC1_CLK_ REQ2_CTRL	DCDC1_CLK_ REQ1_CTRL
(1)	0	1	0	0	0	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w
ENABLE	**0** DCDC1 Disabled **1** DCDC1 Enabled **(1)** DCDC1 Enabled during automatic power-up sequence						
IMMEDIATE	**0** a voltage change of DCDC1 will be done based on the settings of TSTEP[1:0] **1** a voltage change of DCDC1 will be done bypassing the voltage change state machine and therefore is limited by the response of the DCDC1 converter only. With IMMEDIATE=1, TSTEP[1,0] do not define the slope of the voltage change but the time PWM mode is forced to ensure a steep transition of the output voltage.						

(1) Register reset on Power On Reset (POR)

Table 5-2. DCDC1_CTRL(1); Register Address: 00h (continued)

B7	B6	B5	B4	B3	B2	B1	B0
TSTEP[1:0]	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is shown in Table 5-5						
RSVD	Unused bit, should be written to **0**						
DCDC1_SEL_CTRL	**0** DCDC1 output voltage / MODE settings are defined by DCDC1_OP register **1** DCDC1 output voltage / MODE settings are defined by status of pin DCDC3_SEL DCDC3_SEL = LOW := voltage / MODE settings are defined by DCDC1_OP DCDC3_SEL = HIGH := voltage / MODE settings are defined by DCDC1_AVS						
DCDC1_CLK_REQ1_CTRL	**0** DCDC1 enable function not mapped to CLK_REQ1 pin; DCDC1 enabled by ENABLE Bit or internal power-up sequencing setting **1** DCDC1 enable function mapped to pin CLK_REQ1; ENABLE bit is don´t care, CLK_REQ1= LOW := DCDC1 = off, CLK_REQ1= HIGH := DCDC1 = on						
DCDC1_CLK_REQ2_CTRL	**0** DCDC1 enable function not mapped to CLK_REQ2 pin; DCDC1 enabled by ENABLE Bit or internal power-up sequencing setting **1** DCDC1 enable function mapped to pin CLK_REQ2; ENABLE bit is don´t care, CLK_REQ2= LOW := DCDC1 = off, CLK_REQ2= HIGH := DCDC1 = on Note: CLK_REQ1 and CLK_REQ2 are logically OR´d, as soon as either one is HIGH, DCDC1 is enabled						

Table 5-3. DCDC2_CTRL(1); Register Address: 01h

B7	B6	B5	B4	B3	B2	B1	B0
ENABLE	RSVD	IMMEDIATE	TSTEP[1]	TSTEP[0]	DCDC2_SEL_CTRL	DCDC2_CLK_REQ2_CTRL	DCDC2_CLK_REQ1_CTRL
(1)	0	1	0	0	0	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w
ENABLE	**0** DCDC2 Disabled **1** DCDC2 Enabled **(1)** DCDC2 Enabled during automatic power-up sequence						
IMMEDIATE	**0** a voltage change of DCDC2 will be done based on the settings of TSTEP[1:0] **1** a voltage change of DCDC2 will be done bypassing the voltage change state machine and therefore is limited by the response of the DCDC2 converter only. With IMMEDIATE=1, TSTEP[1,0] do not define the slope of the voltage change but the time PWM mode is forced to ensure a steep transition of the output voltage.						
TSTEP[1:0]	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is shown in Table 5-5						
RSVD	Unused bit, should be written to **0**						
DCDC2_SEL_CTRL	**0** DCDC2 output voltage / MODE settings are defined by DCDC2_OP register **1** DCDC2 output voltage / MODE settings are defined by status of pin DCDC3_SEL DCDC3_SEL = LOW := voltage / MODE settings are defined by DCDC2_OP DCDC3_SEL = HIGH := voltage / MODE settings are defined by DCDC2_AVS						
DCDC2_CLK_REQ1_CTRL	**0** DCDC2 enable function not mapped to CLK_REQ1 pin; DCDC2 enabled by ENABLE Bit or internal power-up sequencing setting **1** DCDC2 enable function mapped to pin CLK_REQ1; ENABLE bit is don´t care, CLK_REQ1= LOW := DCDC2 = off, CLK_REQ1= HIGH := DCDC2 = on						
DCDC2_CLK_REQ2_CTRL	**0** DCDC2 enable function not mapped to CLK_REQ2 pin; DCDC2 enabled by ENABLE Bit or internal power-up sequencing setting **1** DCDC2 enable function mapped to pin CLK_REQ2; ENABLE bit is don´t care, CLK_REQ2= LOW := DCDC2 = off, CLK_REQ2= HIGH := DCDC2 = on Note: CLK_REQ1 and CLK_REQ2 are logically OR´d, as soon as either one is HIGH, DCDC2 is enabled						

(1) Register reset on Power On Reset (POR)

Table 5-4. DCDC3_CTRL(1); Register Address: 02h

B7	B6	B5	B4	B3	B2	B1	B0
ENABLE	VCON	IMMEDIATE	TSTEP[1]	TSTEP[0]	DCDC3_ SEL_CTRL	DCDC3_CLK_ REQ2_CTRL	DCDC3_CLK_ REQ1_CTRL
0	0	1	0	0	1	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

ENABLE	**0** DCDC3 Disabled **1** DCDC3 Enabled **(1)** DCDC3 Enabled during automatic power-up sequence
VCON	**0** DCDC3 output voltage defined by _OP or _AVS **1** DCDC3 output voltage defined by pin VCON With VCON = 1, DCDC3 is enabled independently of the ENABLE bit and the converter is forced to PWM independently of DCDC3_MODE defined in either DCDC3_OP or DCDC3_AVS.
IMMEDIATE	**0** a voltage change of DCDC3 will be done based on the settings of TSTEP[1:0] **1** a voltage change of DCDC3 will be done bypassing the voltage change state machine and therefore is limited by the response of the DCDC3 converter only. With IMMEDIATE=1, TSTEP[1,0] do not define the slope of the voltage change but the time PWM mode is forced to ensure a a steep transition of the output voltage.
TSTEP[1:0]	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is shown in Table 5-5
DCDC3_SEL_CTRL	**0** DCDC3 output voltage / MODE settings are defined by DCDC3_OP register **1** DCDC3 output voltage / MODE settings are defined by status of pin DCDC3_SEL DCDC3_SEL = LOW := voltage / MODE settings are defined by DCDC3_OP DCDC3_SEL = HIGH := voltage / MODE settings are defined by DCDC3_AVS
DCDC3_CLK_REQ1_CTRL	**0** DCDC3 enable function not mapped to CLK_REQ1 pin; DCDC3 enabled by ENABLE Bit or internal power-up sequencing setting **1** DCDC3 enable function mapped to pin CLK_REQ1; ENABLE bit is don´t care, CLK_REQ1= LOW := DCDC3 = off, CLK_REQ1= HIGH := DCDC3 = on
DCDC3_CLK_REQ2_CTRL	**0** DCDC3 enable function not mapped to CLK_REQ2 pin; DCDC3 enabled by ENABLE Bit or internal power-up sequencing setting **1** DCDC3 enable function mapped to pin CLK_REQ2; ENABLE bit is don´t care, CLK_REQ2= LOW := DCDC3 = off, CLK_REQ2= HIGH := DCDC3 = on Note: CLK_REQ1 and CLK_REQ2 are logically OR´d, as soon as either one is HIGH, DCDC3 is enabled

(1) Register reset on Power On Reset (POR)

Table 5-5. DCDCx TSTEP Settings

TSTEP[1:0]	TIME PER VOLTAGE STEP ACCORDING TO THE DCDCX VOLTAGE TABLE (µs)	EQUIVALENT SLEW RATE FOR A 25-mV STEP SIZE (mV/µs)
00	0.9	30
01	1.8	15
10	3.5	7.5
11	6.6	3.75

Table 5-6. DCDC1_OP(1); Register Address: 03h

B7	B6	B5	B4	B3	B2	B1	B0
DCDC1_MODE	RSVD	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	1	1	0	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w
DCDC1_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM						
RSVD	Unused bit, should be written to **0**						
SEL[5:0]	DCDC1 Output Voltage Selection based on Table 5-15.						

(1) Register reset on Power On Reset (POR)

Table 5-7. DCDC1_AVS(1); Register Address: 04h

B7	B6	B5	B4	B3	B2	B1	B0
DCDC1_MODE	RSVD	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	1	1	0	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w
DCDC1_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM						
RSVD	Unused bit, should be written to **0**						
SEL[5:0]	DCDC1 Output Voltage Selection based on Table 5-15.						

(1) Register reset on Power On Reset (POR)

Table 5-8. DCDC2_OP(1); Register Address: 05h

B7	B6	B5	B4	B3	B2	B1	B0
DCDC2_MODE	RSVD	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	1	0	1	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w
DCDC2_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM						
RSVD	Unused bit, should be written to **0**						
SEL[5:0]	DCDC2 Output Voltage Selection based on Table 5-15.						

(1) Register reset on Power On Reset (POR)

Table 5-9. DCDC2_AVS(1); Register Address: 06h

B7	B6	B5	B4	B3	B2	B1	B0
DCDC2_MODE	RSVD	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	1	0	1	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w
DCDC2_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM						
RSVD	Unused bit, should be written to **0**						
SEL[5:0]	DCDC2 Output Voltage Selection based on Table 5-15.						

(1) Register reset on Power On Reset (POR)

Table 5-10. DCDC3_OP(1); Register Address: 07h

B7	B6	B5	B4	B3	B2	B1	B0
DCDC3_MODE	EN_BYPASS	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
DCDC3_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM						
EN_BYPASS	**0** BYPASS switch is not forced ON **1** BYPASS switch is forced ON; over voltage protection at VDCDC3 is active and will clear this bit once VDCDC3 exceeds 4.18 V						
SEL[6:0]	DCDC3 Output Voltage Selection shown in Table 5-16.						
Note:	DCDC3_OP register settings are active when DCDC3_SEL = LOW						

(1) Register reset on Power On Reset (POR)

Table 5-11. DCDC3_AVS(1); Register Address: 08h

B7	B6	B5	B4	B3	B2	B1	B0
DCDC3_MODE	EN_BYPASS	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
DCDC3_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM						
EN_BYPASS	**0** BYPASS switch is not forced ON **1** BYPASS switch is forced ON; over voltage protection at VDCDC3 is active and will clear this bit once VDCDC3 exceeds 4.18 V						
SEL6:0]	DCDC3 Output Voltage Selection shown in Table 5-16.						
Note:	DCDC3_AVS register settings are active when DCDC3_SEL = HIGH						

(1) Register reset on Power On Reset (POR)

Table 5-12. VCON(1); Register Address: 09h

B7	B6	B5	B4	B3	B2	B1	B0
RSVD	VCON_ OFFSET[2]	VCON_ OFFSET[1]	VCON_ OFFSET[0]	VCON_GAIN[3]	VCON_GAIN[2]	VCON_GAIN[1]	VCON_GAIN[0]
0	1	0	1	0	1	1	0
	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
VCON_OFFSET[2:0]	VCON offset settings shown in Table 5-13.						
VCON_GAIN[3:0]	VCON gain settings shown in Table 5-13.						
RSVD	Unused bit, should be written to **0**						

(1) Register reset on Power On Reset (POR)

Table 5-13. VCON Gain Settings

VCON_GAIN[3:0]	GAIN	VCON_GAIN[3:0]	GAIN
0000	1.208	1000	2.000
0001	1.292	1001	2.083
0010	1.417	1010	2.208
0011	1.500	1011	2.292
0100	1.583	1100	2.417
0101	1.708	1101	2.500
0110	1.792	1110	2.583
0111	1.917	1111	2.708

Table 5-14. VCON Offset Settings

VCON_OFFSET[2:0]	OFFSET (mV)
000	0
001	-50
010	-100
011	-150
100	-200
101	-250
110	-300
111	-350

Table 5-15. DCDC1 and DCDC2 Voltage Settings

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000	0.80	100000	1.900
000001	0.90	100001	1.925
000010	1.00	100010	1.950
000011	1.05	100011	1.975
000100	1.10	100100	2.000
000101	1.15	100101	2.025
000110	1.20	100110	2.050
000111	1.25	100111	2.075
001000	1.300	101000	2.100
001001	1.325	101001	2.125
001010	1.350	101010	2.150
001011	1.375	101011	2.175
001100	1.400	101100	2.20
001101	1.425	101101	2.25
001110	1.450	101110	2.30
001111	1.475	101111	2.35
010000	1.500	110000	2.40
010001	1.525	110001	2.45
010010	1.550	110010	2.50
010011	1.575	110011	2.55
010100	1.600	110100	2.60
010101	1.625	110101	2.65
010110	1.650	110110	2.70
010111	1.675	110111	2.75
011000	1.700	111000	2.80
011001	1.725	111001	2.85
011010	1.750	111010	2.90
011011	1.775	111011	2.95
011100	1.800	111100	3.00
011101	1.825	111101	3.10
011110	1.850	111110	3.20
011111	1.875	111111	3.30

Table 5-16. DCDC3 Voltage Settings

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000	0.80	100000	2.40
000001	0.85	100001	2.45
000010	0.90	100010	2.50
000011	0.95	100011	2.55
000100	1.00	100100	2.60
000101	1.05	100101	2.65
000110	1.10	100110	2.70
000111	1.15	100111	2.75
001000	1.20	101000	2.80
001001	1.25	101001	2.85
001010	1.30	101010	2.90
001011	1.35	101011	2.95
001100	1.40	101100	3.00
001101	1.45	101101	3.05
001110	1.50	101110	3.10
001111	1.55	101111	3.15
010000	1.60	110000	3.20
010001	1.65	110001	3.25
010010	1.70	110010	3.30
010011	1.75	110011	3.35
010100	1.80	110100	3.40
010101	1.85	110101	3.45
010110	1.90	110110	3.50
010111	1.95	110111	3.55
011000	2.00	111000	3.60
011001	2.05	111001	3.60
011010	2.10	111010	3.60
011011	2.15	111011	3.60
011100	2.20	111100	3.60
011101	2.25	111101	3.60
011110	2.30	111110	3.60
011111	2.35	111111	3.60

Table 5-17. LDO_CTRL(1); Register Address: 0Ah

B7	B6	B5	B4	B3	B2	B1	B0
RSVD	RSVD	RSVD	RSVD	LDO2_CLK_REQ2_CTRL	LDO2_CLK_REQ1_CTRL	LDO1_CLK_REQ2_CTRL	LDO1_CLK_REQ1_CTRL
0	0	0	0	0	0	0	0
				OTP	OTP	OTP	OTP
r	r	r	r	r/w	r/w	r/w	r/w

RSVD	Unused bit, should be written to **0**
LDO2_CLK_REQ2_CTRL	**0** LDO2 enable function not mapped to CLK_REQ2 pin; LDO2 enabled by ENABLE Bit or internal power-up sequencing setting **1** LDO2 enable function mapped to pin CLK_REQ2 pin; ENABLE bit is don't care, CLK_REQ2= LOW := LDO2 = off, CLK_REQ2= HIGH := LDO2 = on
LDO2_CLK_REQ1_CTRL	**0** LDO2 enable function not mapped to CLK_REQ1 pin; LDO2 enabled by ENABLE Bit or internal power-up sequencing setting **1** LDO2 enable function mapped to pin CLK_REQ1 pin; ENABLE bit is don't care, CLK_REQ1= LOW := LDO2 = off, CLK_REQ1= HIGH := LDO2 = on
LDO1_CLK_REQ2_CTRL	**0** LDO1 enable function not mapped to CLK_REQ2 pin; LDO1 enabled by ENABLE Bit or internal power-up sequencing setting **1** LDO1 enable function mapped to pin CLK_REQ2 pin; ENABLE bit is don't care, CLK_REQ2= LOW := LDO1 = off, CLK_REQ2= HIGH := LDO1 = on
LDO1_CLK_REQ1_CTRL	**0** LDO1 enable function not mapped to CLK_REQ1 pin; LDO1 enabled by ENABLE Bit or internal power-up sequencing setting **1** LDO1 enable function mapped to pin CLK_REQ1 pin; ENABLE bit is don't care, CLK_REQ1= LOW := LDO1 = off, CLK_REQ1= HIGH := LDO1 = on
	Note: CLK_REQ1 and CLK_REQ2 are logically OR'd if both pins are assigned to the same LDO; as soon as either one is HIGH, LDOx is enabled

(1) Register reset on Power On Reset (POR)

LDO1_OP(1); Register Address: 0Bh

B7	B6	B5	B4	B3	B2	B1	B0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	0	1	1	0	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

ENABLE	**0** LDO1 Disabled **1** LDO1 Enabled **(1)** LDO1 Enabled during automatic power-up sequence
ECO	**0** LDO1 is in normal mode **1** LDO1 is in power save mode
SELREG	**0** LDO1 Voltage selected by LDO1_OP register **1** LDO1 Voltage selected by LDO1_AVS register
SEL[5:0]	Supply Voltage - setting shown in Table 5-19

(1) Register reset on Power On Reset (POR)

Table 5-18. LDO2_OP(1); Register Address: 0Ch

B7	B6	B5	B4	B3	B2	B1	B0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	1	1	0	0	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
ENABLE	**0** LDO2 Disabled **1** LDO2 Enabled **(1)** LDO2 Enabled during automatic power-up sequence						
ECO	**0** LDO2 is in normal mode **1** LDO2 is in power save mode						
SELREG	**0** LDO2 Voltage selected by LDO2_OP register **1** LDO2 Voltage selected by LDO2_AVS register						
SEL[5:0]	Supply Voltage - setting shown in Table 5-19						

(1) Register reset on Power On Reset (POR)

Table 5-19. LDO Voltage Settings

SEL[5:0]	LDOx OUTPUT (V)	SEL[5:0]	LDOx OUTPUT (V)
000000	1.200	100000	2.000
000001	1.225	100001	2.050
000010	1.250	100010	2.100
000011	1.275	100011	2.150
000100	1.300	100100	2.200
000101	1.325	100101	2.250
000110	1.350	100110	2.300
000111	1.375	100111	2.350
001000	1.400	101000	2.400
001001	1.425	101001	2.450
001010	1.450	101010	2.500
001011	1.475	101011	2.550
001100	1.500	101100	2.600
001101	1.525	101101	2.650
001110	1.550	101110	2.700
001111	1.575	101111	2.750
010000	1.600	110000	2.800
010001	1.625	110001	2.850
010010	1.650	110010	2.900
010011	1.675	110011	2.950
010100	1.700	110100	3.000
010101	1.725	110101	3.050
010110	1.750	110110	3.100
010111	1.775	110111	3.150
011000	1.800	111000	3.200
011001	1.825	111001	3.250
011010	1.850	111010	3.300
011011	1.875	111011	3.350
011100	1.900	111100	3.400
011101	1.925	111101	3.400
011110	1.950	111110	3.400
011111	1.975	111111	3.400

Table 5-20. DEVCTRL(1); Register Address: 0Dh

B7	B6	B5	B4	B3	B2	B1	B0
PWR_OFF_SEQ	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0	0	0	0	0	0	0	0
OTP							
r/w	r	r	r	r	r	r	r
PWR_OFF_SEQ	**0** All resources disabled at the same time **1** Power-off will be sequential, reverse of power-on sequence (first resource to power on will be the last to power off) Note: Each power-up / power-down time slot is 500 µs.						
RSVD	Unused bit read returns**0**						

(1) Register reset on Power On Reset (POR)

Table 5-21. DISCHARGE(1); Register Address: 0Eh

B7	B6	B5	B4	B3	B2	B1	B0
RSVD	DCDC3_ DISCHARGE	DCDC2_ DISCHARGE	DCDC1_ DISCHARGE	RSVD	RSVD	LDO2_ DISCHARGE	LDO1_ DISCHARGE
0	0	0	0	0	0	0	0
	OTP	OTP	OTP			OTP	OTP
r	r/w	r/w	r/w	r	r	r/w	r/w
RSVD	Unused bit read returns **0**						
DCDC3_DISCHARGE	**0** DCDC3 output is not discharged when disabled **1** DCDC3 output is discharged when disabled						
DCDC2_DISCHARGE	**0** DCDC2 output is not discharged when disabled **1** DCDC2 output is discharged when disabled						
DCDC1_DISCHARGE	**0** DCDC1 output is not discharged when disabled **1** DCDC1 output is discharged when disabled						
LDO2_DISCHARGE	**0** LDO2 output is not discharged when disabled **1** LDO2 output is discharged when disabled						
LDO1_DISCHARGE	**0** LDO1 output is not discharged when disabled **1** LDO1 output is discharged when disabled						

(1) Register reset on Power On Reset (POR)

Table 5-22. PGOOD(1); Register Address: 0Fh

B7	B6	B5	B4	B3	B2	B1	B0
RSVD	PGOOD_DCDC3	PGOOD_DCDC2	PGOOD_DCDC1	RSVD	RSVD	PGOOD_LDO2	PGOOD_LDO1
0	-	-	-	0	0	-	-
r	r	r	r	r	r	r	r
PGOOD_DCDCx	the Bit is set or cleared by the power-good comparator in the DCDC converter block **0** DCDCx output voltage is below its target regulation voltage or disabled **1** DCDCx output voltage is in regulation						
PGOOD_LDOx	the Bit is set or cleared by the power-good comparator in the LDO converter block **0** LDOx output voltage is below its target regulation voltage or disabled **1** LDOx output voltage is in regulation or in ECO mode Note: The PGOOD_LDOx Bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V.						

(1) Register reset on Power On Reset (POR)

Table 5-23. GPIO0[1]; Register Address: 10h

B7	B6	B5	B4	B3	B2	B1	B0
RSVD	nRESET	GPIO_ODEN	RSVD	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
0	1	0	0	0	0	-	0
	OTP	OTP		OTP	OTP		OTP
r	r/w	r/w	r	r/w	r/w	r	r/w

RSVD	Unused bit read returns **0**
nRESET	**0** pin is GPIO after OTP configuration has been read; connect external pull-up to a logic HIGH in order to exit reset state allowing to re-configure as GPIO **1** pin is active low reset input per default as well as after OTP configuration has been read; pin is input per default independent of setting in GPIO_CFG
GPIO_ODEN	**0** Push-pull output mode **1** Open drain output mode
GPIO_PDEN	**0** GPIO pad pull-down control - Pull-down is disabled **1** GPIO pad pull-down control - Pull-down is enabled
GPIO_CFG	**0** Configuration of the GPIO pad direction - the pad is configured as an input **1** The GPIO pad is configured as an output, GPIO assigned to power-up sequence
GPIO_STS	**0** Status of the GPIO pad **1** Status of the GPIO pad
GPIO_SET	**0** Value set to logic 1'b0 on the GPIO output when configured in output mode **1** Value set to logic 1'b1 on the GPIO output when configured in output mode

(1) Register reset on Power On Reset (POR)

Table 5-24. GPIO1[1]; Register Address: 11h

B7	B6	B5	B4	B3	B2	B1	B0
RSVD	ADR_SELECT	GPIO_ODEN	RSVD	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
0	1	0	0	0	0	-	0
	OTP	OTP		OTP	OTP		OTP
r	r/w	r/w	r	r/w	r/w	r	r/w

RSVD	Unused bit read returns **0**
ADR_SELECT	**0** pin is GPIO **1** actual pin status defines the LSB of the MIPI device address defined in USID[0]; while the device is in reset state, the pin is ADR_SELECT input independent of setting in GPIO_CFG
GPIO_ODEN	**0** Push-pull output mode **1** Open drain output mode
GPIO_PDEN	**0** GPIO pad pull-down control - Pull-down is disabled **1** GPIO pad pull-down control - Pull-down is enabled
GPIO_CFG	**0** Configuration of the GPIO pad direction - the pad is configured as an input **1** The GPIO pad is configured as an output, GPIO assigned to power-up sequence
GPIO_STS	**0** Status of the GPIO pad **1** Status of the GPIO pad
GPIO_SET	**0** Value set to logic 1'b0 on the GPIO output when configured in output mode **1** Value set to logic 1'b1 on the GPIO output when configured in output mode

(1) Register reset on Power On Reset (POR)

Table 5-25. DCDC_CONFIG1(1) ; Register Address: 12h

B7	B6	B5	B4	B3	B2	B1	B0
DCDC3_OVP	DCDC3_ DWN_2X	DCDC3_ EN_DWN	DCDC3_EN_UP	DCDC3_FA2	DCDC3_FA1	DCDC3_S2	DCDC3_S1
0	0	0	0	0	0	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w (read only)	r/w	r/w	r/w (read only)	r/w (read only)	r/w (read only)	r/w (read only)
SPARE	Unused bit read returns **0**						
DCDC3_OVP	**0** DCDC3 overvoltage protection not triggered, bypass switch and ramp support status depend on DCDC3_EN_UP and EN_BYPASS bits in DCDC3_OP and DCDC3_AVS registers **1** DCDC3 overvoltage protection triggered, bypass switch and ramp support bits are ignored and both features are disabled in OVP. Clear bit to clear OVP after an OVP event.						
DCDC3_DWN_2X	**0** DCDC3 down ramp high speed disabled **1** DCDC3 down ramp high speed enabled						
DCDC3_EN_DWN	**0** DCDC3 down ramp support disabled **1** DCDC3 down ramp suport enabled TI recommends keeping the ramp-down support disabled when DCDC3 is not operated in VCON mode (DCDC3_CTRL:VCON=0)						
DCDC3_EN_UP	**0** DCDC3 up ramp support disabled **1** DCDC3 up ramp support enabled						
DCDC3_FA2	**0** fast-on HSD not active for DCDC3 **1** fast-on HSD active for DCDC3						
DCDC3_FA1	**0** slow-off HSD not active for DCDC3 **1** slow-off HSD active for DCDC3						
DCDC3_S2:S1	Ramp-up support threshold voltage (available for Rev 1.1 only) **00** threshold = –50 mV **01** threshold = –100 mV **10** threshold = –150 mV **11** threshold = –200 mV						
Note:	r/w (read only): r/w for engineering use; read only in production						

(1) Register reset on Power On Reset (POR)

Table 5-26. DCDC_CONFIG2(1) ; Register Address: 13h

B7	B6	B5	B4	B3	B2	B1	B0
RSVD	RSVD	RSVD	RSVD	RSVD	DCDC3_ SSC_DELTA	DCDC3_ EN_SSC	DCDC3_ EN_CP_OSC
0	0	0	0	0	1	0	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r	r	r	r	r	r/w (read only)	r/w (read only)	r/w (read only)
SPARE	Unused bit read returns **0**						
DCDC3_SSC_DELTA	**0** SSC variation 200 kHz **1** SSC variation 300 kHz						
DCDC3_EN_SSC	**0** spread spectrum clocking is off **1** spread spectrum clocking is on						
DCDC3_EN_CP_OSC	**0** oscillator source dcdc3-clk **1** oscillator source bypass-cp-clk						
Note:	r/w (read only): r/w for engineering use; read only in production						

(1) Register reset on Power On Reset (POR)

Table 5-27. SPARE0(1) ; Register Address: 14h

B7	B6	B5	B4	B3	B2	B1	B0
SPARE	SPARE	EN_FAST_RAMP	DCDC1/2_FA2	DCDC1/2_FA1	DCDC3_synch	nILIM_MAPPING	EN_nILIM_xl
0	0	1	0	0	0	0	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

SPARE	Unused bit read returns **0**
Note:	**for later use**
EN_FAST_RAMP	**available from rev 1.2 of silicon**
	0 ramp speed of DCDC3 in VCON mode is as in previous versions
	1 fast ramp-up enabled, the rising edge in VCON mode is speed-up
DCDC1/2_FA2	**0** fast-on HSD not active for DCDC1 and DCDC2
	1 fast-on HSD active for DCDC1 and DCDC2
DCDC1/2_FA1	**0** slow-off HSD not active for DCDC1 and DCDC2
	1 slow-off HSD active for DCDC1 and DCDC2
DCDC3_synch	**available from rev 1.1 of silicon**
	0 DCDC3 not synchzronized to DCDC1 and DCDC2; SSC option allowed
	1 DCDC3 synchzronized to DCDC1 and DCDC2; SSC option not allowed
nILIM_MAPPING	**available from rev 1.1 of silicon**
	0 negative current limit for DCDC3 is defined by bit EN_nILIM_xl
	1 negative current limit for DCDC3 is mapped to pin DCDC3_SEL and defined as listed below:
	DCDC3_SEL = 0: negative current limit is disabled (for VCON up-ramping)
	DCDC3_SEL = 1: negative current limit is enabled (for VCON down-ramping)
	Note: nILIM_MAPPING is not gating DCDCx_SEL_CTRL bits in registers DCDCx_CTRL and vice versa
EN_nILIM_xl	**available from rev 1.1 of silicon**
	0 negative current limit for DCDC3 is disabled; the setting still allows a small negative inductor current needed to operate the converter in PWM mode at zero load current
	1 negative current limit for DCDC3 enabled; needed for a fast ramp down of the output voltage in VCON mode

(1) Register reset on Power On Reset (POR)

Table 5-28. VERNUM(1) ; Register Address: 15h

B7	B6	B5	B4	B3	B2	B1	B0
VERNUM	VERNUM	VERNUM	VERNUM	VERNUM	VERNUM	VERNUM	VERNUM
0	0	0	1	0	0	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r	r	r	r	r	r	r	r

VERNUM	Value depending on silicon revision
	0x00 - hardware revision 1.0
	0x01 - hardware revision 1.1
	0x11 - hardware revision 1.1 with programming 42
	0x12 - hardware revision 1.2 with programming 42
	0x13 - hardware revision 1.3 with programming 42

(1) Register reset on Power On Reset (POR)

Table 5-29. PM_TRIG(1) ; Register Address: 1Ch; function not supported by TPS657120

B7	B6	B5	B4	B3	B2	B1	B0
PWR_MODE[1]	PWR_MODE[0]	PM_TRIG[5]	PM_TRIG[4]	PM_TRIG[3]	PM_TRIG[2]	PM_TRIG[1]	PM_TRIG[0]
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
PM_TRIG[5:0]							
PWR_MODE[1:0]							

(1) Register reset on Power On Reset (POR)

Table 5-30. PRODUCT_ID(1) ; Register Address: 1Dh

B7	B6	B5	B4	B3	B2	B1	B0
ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
1	1	1	0	0	0	0	0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
ID[7:0]	Product Identification						

(1) Register reset on Power On Reset (POR)

Table 5-31. MANUFACTURER_ID(1) ; Register Address: 1Eh

B7	B6	B5	B4	B3	B2	B1	B0
MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]
0	0	0	0	0	0	1	0
r	r	r	r	r	r	r	r
MID[7:0]	Manufacturer Identification						

(1) Register reset on Power On Reset (POR)

Table 5-32. USID(1) ; Register Address: 1Fh

B7	B6	B5	B4	B3	B2	B1	B0
SPARE	SPARE	MID[9]	MID[8]	USID[3]	USID[2]	USID[1]	USID[0]
0	0	0	1	0	1	0	x
OTP	OTP	-	-	OTP	OTP	OTP	OTP / ADR_SELECT
r/w	r/w	r	r	r/w (read only)	r/w (read only)	r/w (read only)	r
USID[3:0]	unique slave identifier; GPIO1 can optionally be used as the adress select input for USID[0], if the option is active, USID[0] is set 1 when ADR_SELECT is pulled to a HIGH level, USID[0] is set to 0 when ADR_SELECT is set LOW again. It is allowed to change the state of ADR_SELECT during operation. and USID[0] will update accordingly.						
MID[8,9]	manufacurer ID MSB						
SPARE	for later use						
Note:	r/w (read only): r/w for engineering use; read only in production						

(1) Register reset on Power On Reset (POR)

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The target application is powering a Baseband and RF-PA.

6.2 Typical Application

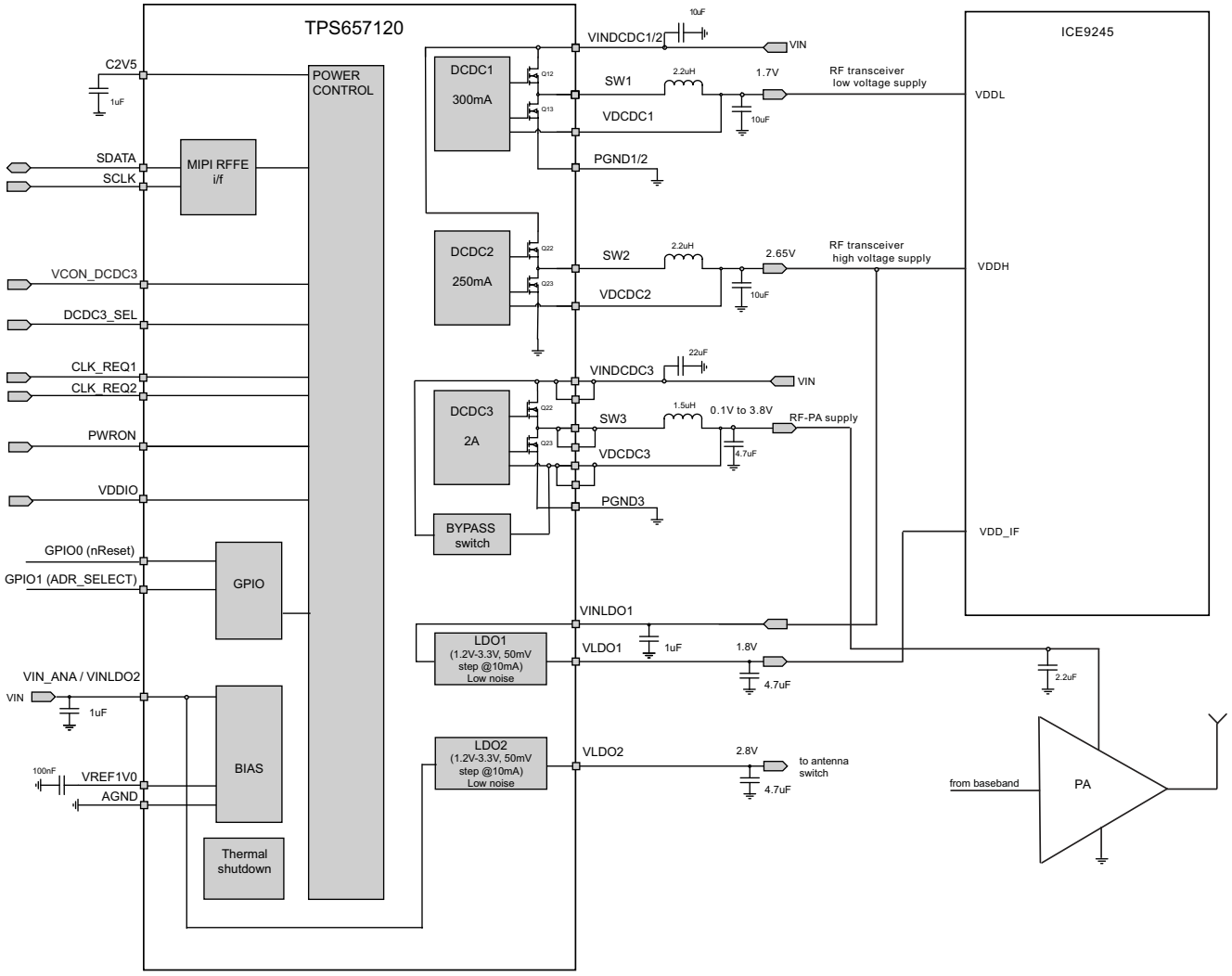


Figure 6-1. Phone Battery Connections for SP30 RF PMIC

6.2.1 Design Requirements

The design requirements are shown in Table 6-1.

Table 6-1. Design Parameters

DESIGN PARAMETER	VALUE
Typical Input Voltage	5.0 V
DCDC1 Output Voltage	1.7 V
DCDC2 Output Voltage	2.65 V
DCDC3 Output Voltage	3.8 V
LDO1 Output Voltage	1.8 V
LDO2 Output Voltage	2.8 V

6.2.2 Detailed Design Procedure

6.2.2.1 Output Filter Design (Inductor and Output Capacitor)

6.2.2.1.1 Inductor Selection

The converters operates typically with a 1.5-µH or 2.2-µH output inductor. The selected inductor has to be rated for its dc resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest dc resistance should be selected for highest efficiency.

Equation 3 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- f = Switching Frequency (2.25MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

(3)

The highest inductor current will occur at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Note that the step down converter has internal loop compensation. The internal loop compensation is designed to work with an output filter corner frequency calculated as follows:

$$f_c = \frac{1}{2\pi\sqrt{L \times Cout}} \text{ with } L = 1.5\ \mu H,\ Cout = 10\ \mu F \quad (4)$$

This leads to the fact the selection of external L-C filter has to be coped with the above equation. As a general rule the product of L x C_{OUT} should be constant while selecting smaller inductor or increasing output capacitor value.

Refer to Table 6-2 and the typical applications for possible inductors.

Table 6-2. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER	COMMENT
MDT1608-CH2R2M	2.2 µH	Toko	for DCDC1 and DCDC2 (small size)
MDT2012-CH2R2N	2.2 µH	Toko	for DCDC1 and DCDC2 (small size, good efficiency)
DFE201610C-2R2	2.2 µH	Toko	for DCDC1 and DCDC2 (high efficiency)
DFE252010-1R5N	1.5 µH	Toko	for DCDC3

6.2.2.1.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the step-down converter allows the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. For an inductor value of 1.5 µH or 2.2 µH, an output capacitor with 10 µF can be used. See the recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated using Equation 5.

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

At nominal load currents, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor; see Equation 6.

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (6)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

6.2.2.1.3 Input Capacitor / Output Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering. As the output capacitor influences the loop stability, any deviation form the required output capacitance may cause the DC-DC converter or LDO to become unstable.

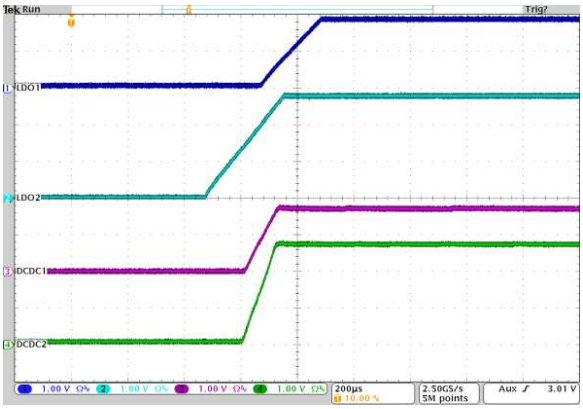
Table 6-3. Tested Capacitors

TYPE	VALUE	VOLTAGE RATING	SIZE	SUPPLIER	MATERIAL
GRM155R60J475ME87	4.7 µF	6.3 V	0402	Murata	Ceramic X5R
GRM155R60J225ME15D	2.2 µF	6.3 V	0402	Murata	Ceramic X5R
GRM185R60J225	2.2 µF	6.3 V	0603	Murata	Ceramic X5R
GRM188R60J475KE19	4.7 µF	6.3 V	0603	Murata	Ceramic X5R
GRM188R61A106ME69	10 µF	10 V	0603	Murata	Ceramic X5R
GRM21BR60J226M	22 µF	6.3 V	0805	Murata	Ceramic X5R
GRM21BR60J476ME15	47 µF	6.3 V	0805	Murata	Ceramic X5R

6.2.2.1.4 Voltage Change on DCDC1, DCDC2 and DCDC3

The output voltage of the DC-DC converters can be changed during operation by the digital interface. In addition, the DC-DC converters can be configured such that toggling DCDC3_SEL switches between two different sets of output voltages defined in registers DCDCx_OP and DCDCx_AVS.

6.2.3 Application Curve



7 Power Supply Recommendations

The power supply decoupling and bulk capacitors are shown in the application drawing.

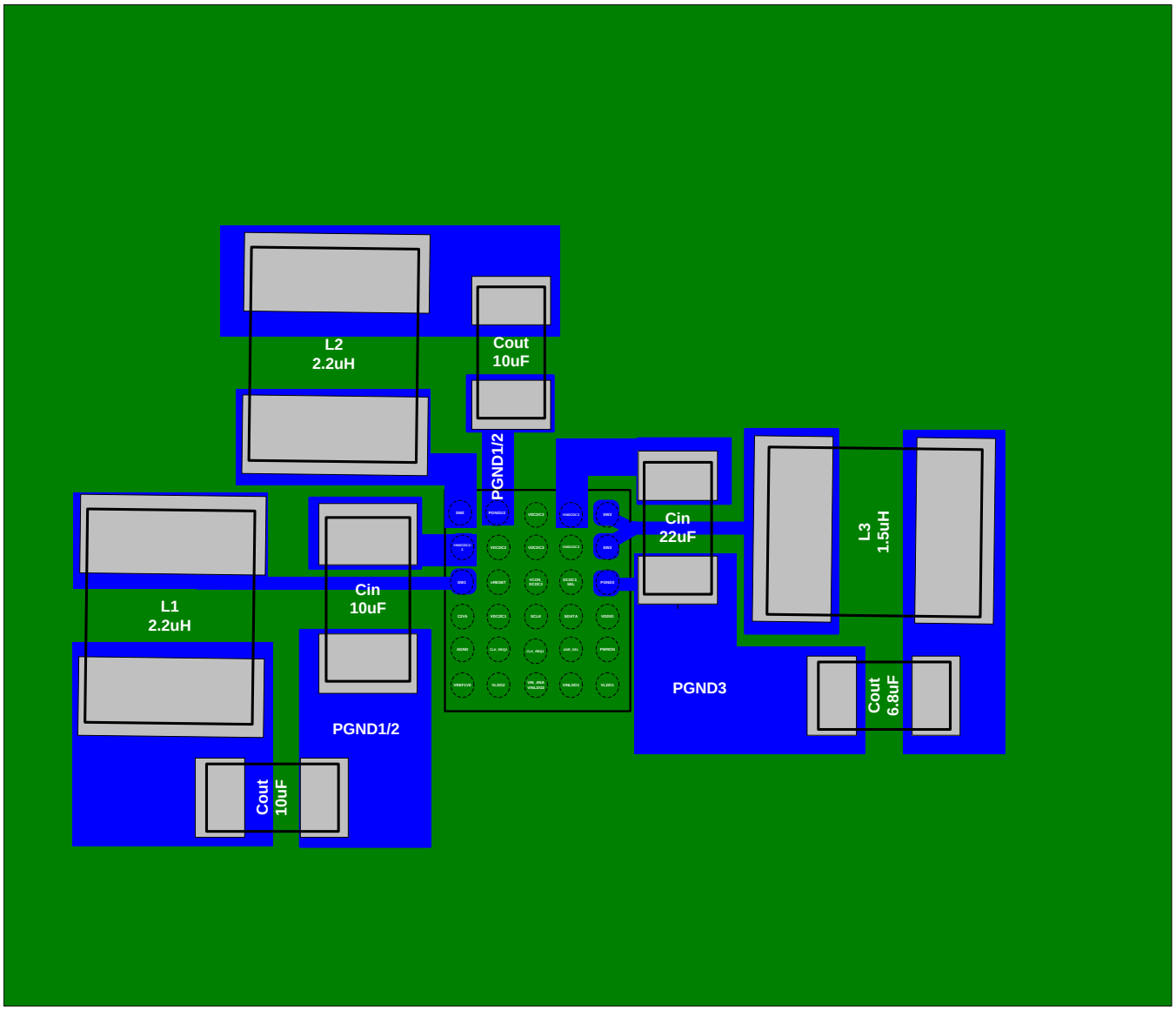
8 Layout

8.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line and/or load regulation and stability issues as well as EMI problems. It is critical to provide a low impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Keep the common path to the GND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx trace should be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, and L3 traces). See the EVM users guide for details about the layout for TPS657120.

8.2 Layout Example



9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

9.3 Trademarks

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9.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS657120YFFR	ACTIVE	DSBGA	YFF	30	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 657120	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

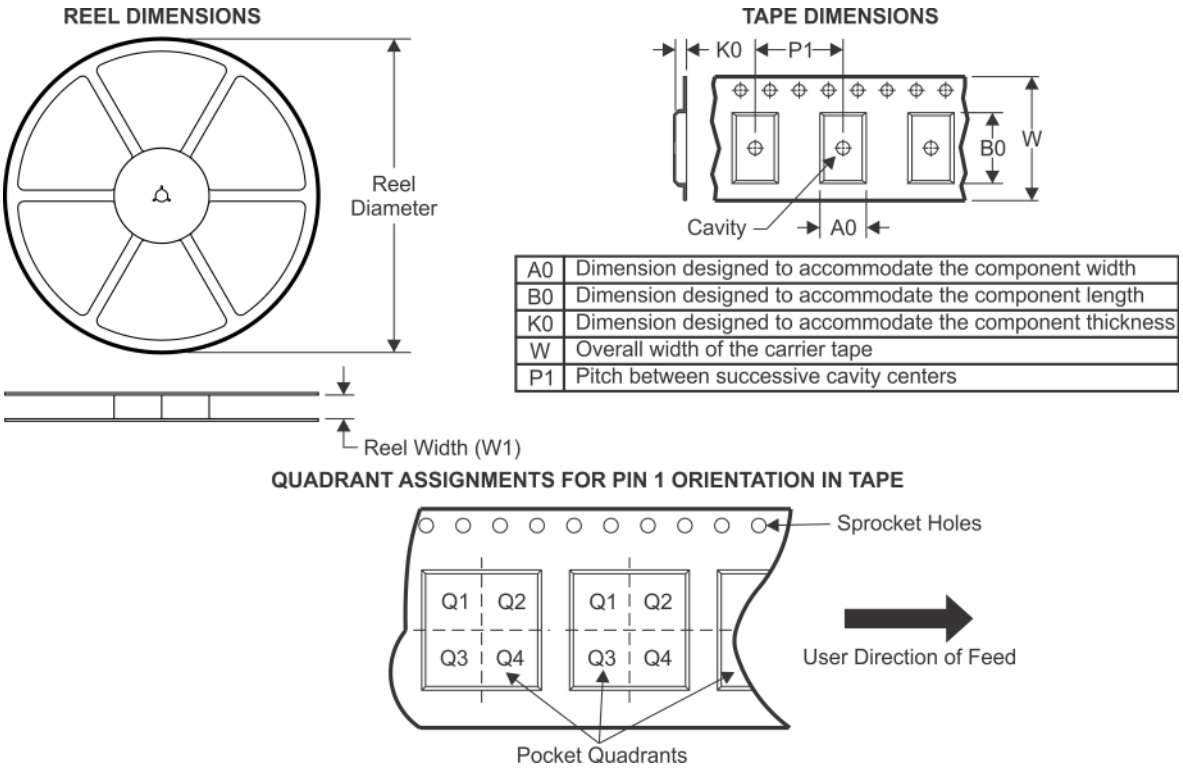
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

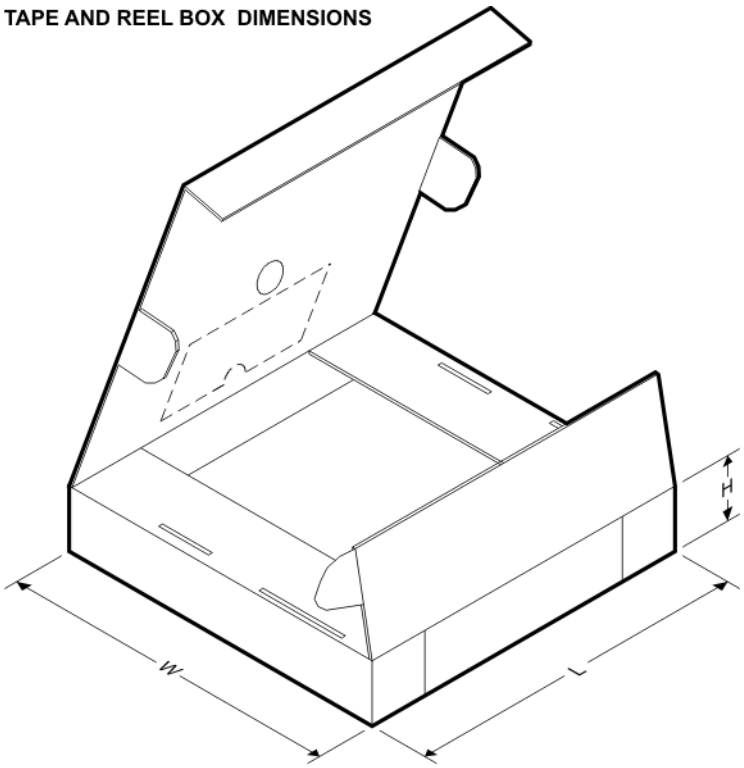


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS657120YFFR	DSBGA	YFF	30	3000	180.0	8.4	2.4	2.7	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

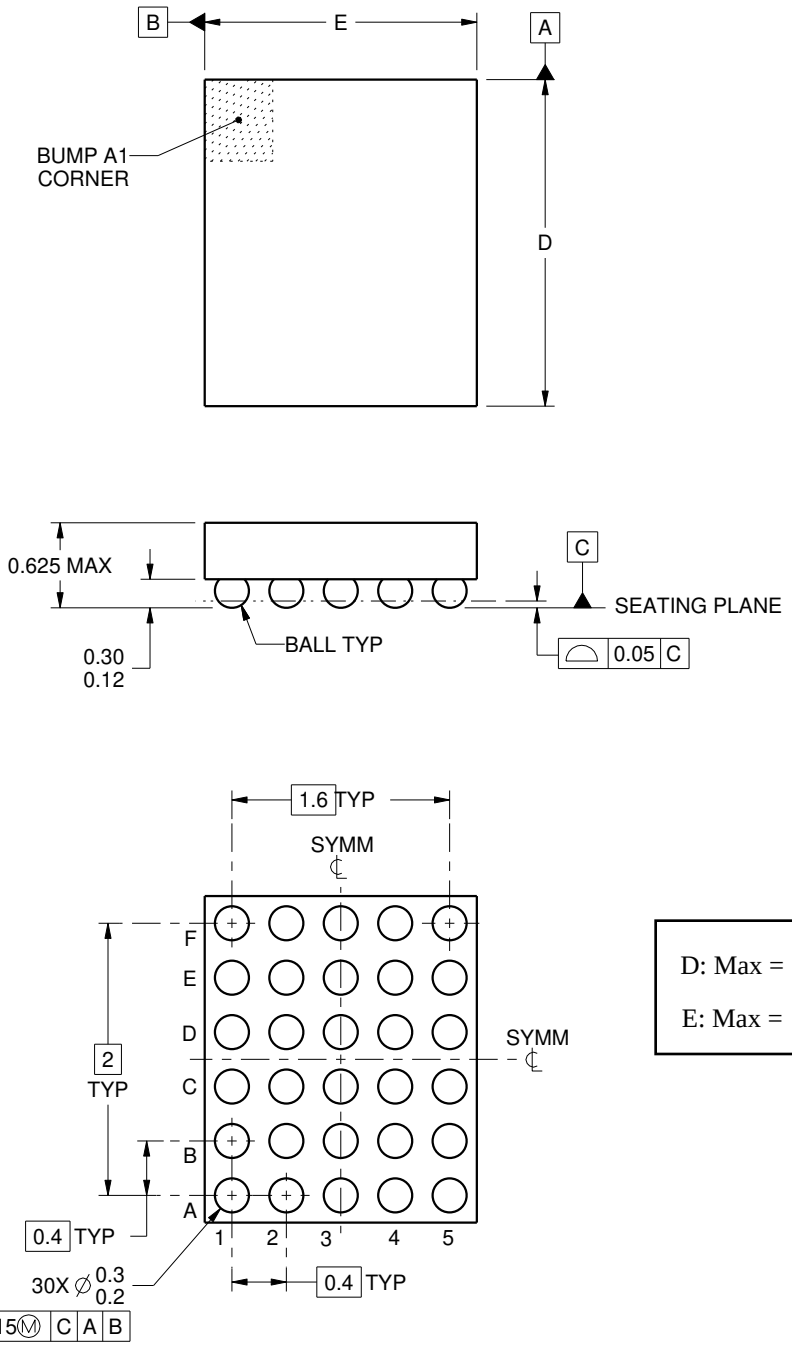
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS657120YFFR	DSBGA	YFF	30	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 2.51 mm, Min = 2.45 mm

E: Max = 2.31 mm, Min = 2.25 mm

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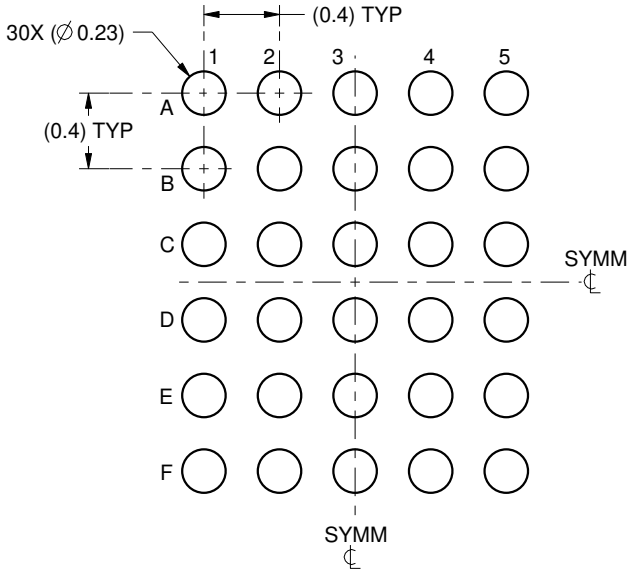
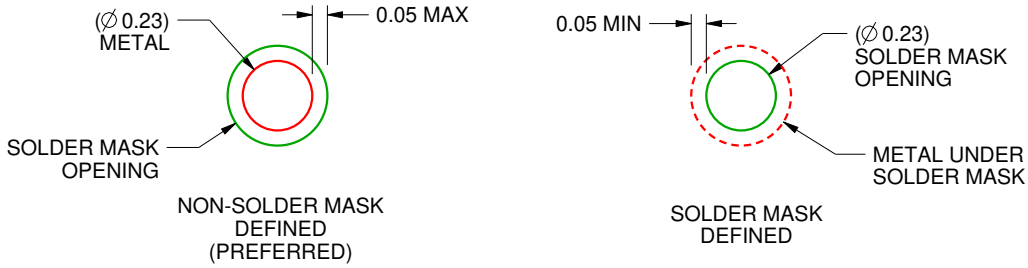
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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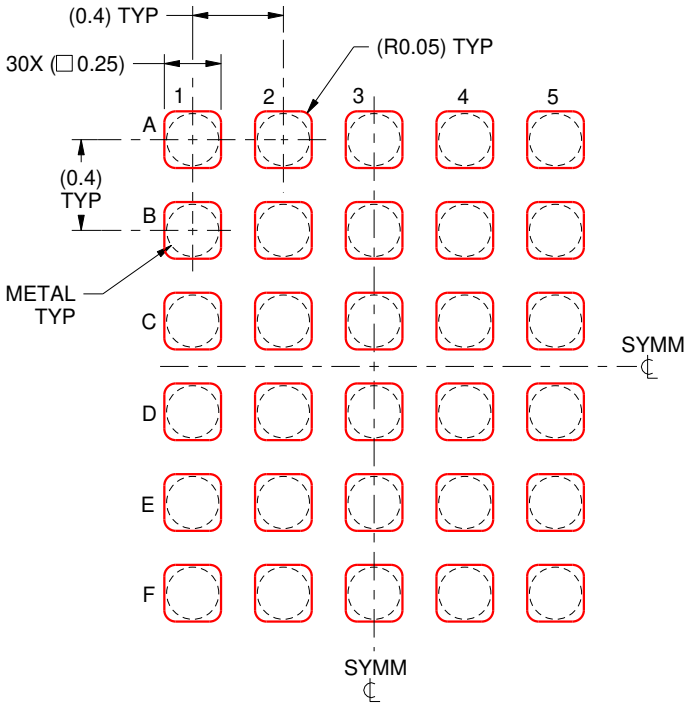
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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