# DIFFERENTIAL VIDEO AMPLIFIER

## FEATURES

- **Adjustable Gain to 400 (Typ)**
- **No Frequency Compensation Required**
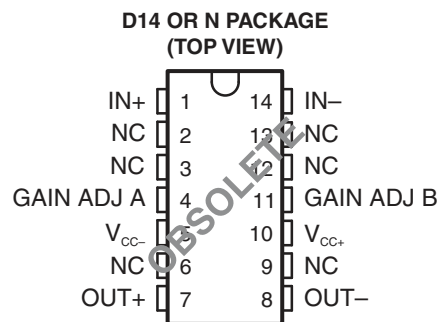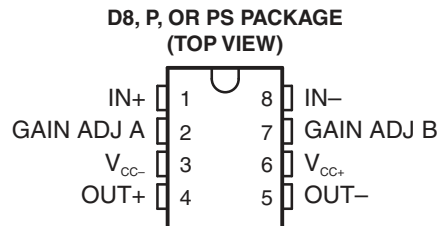- **Low Noise . . . 3-mV $V_n$ (Typ)**

## DESCRIPTION

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted for near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

**D8, P, OR PS PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| IN+ | 1 | 8 | IN− |
| GAIN ADJ A | 2 | 7 | GAIN ADJ B |
| $V_{CC−}$ | 3 | 6 | $V_{CC+}$ |
| OUT+ | 4 | 5 | OUT− |

**D14 OR N PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| IN+ | 1 | 14 | IN− |
| NC | 2 | 13 | NC |
| NC | 3 | 12 | NC |
| GAIN ADJ A | 4 | 11 | GAIN ADJ B |
| $V_{CC−}$ | 5 | 10 | $V_{CC+}$ |
| NC | 6 | 9 | NC |
| OUT+ | 7 | 8 | OUT− |

NC − No internal connection

Note: D8 and D14 are the codes to differentiate the 8-pin and 14-pin versions, respectively.

**SYMBOL**

GAIN ADJ A
IN+ — OUT+
IN− — OUT−
GAIN ADJ B
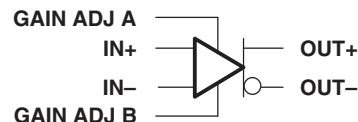
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## SCHEMATIC
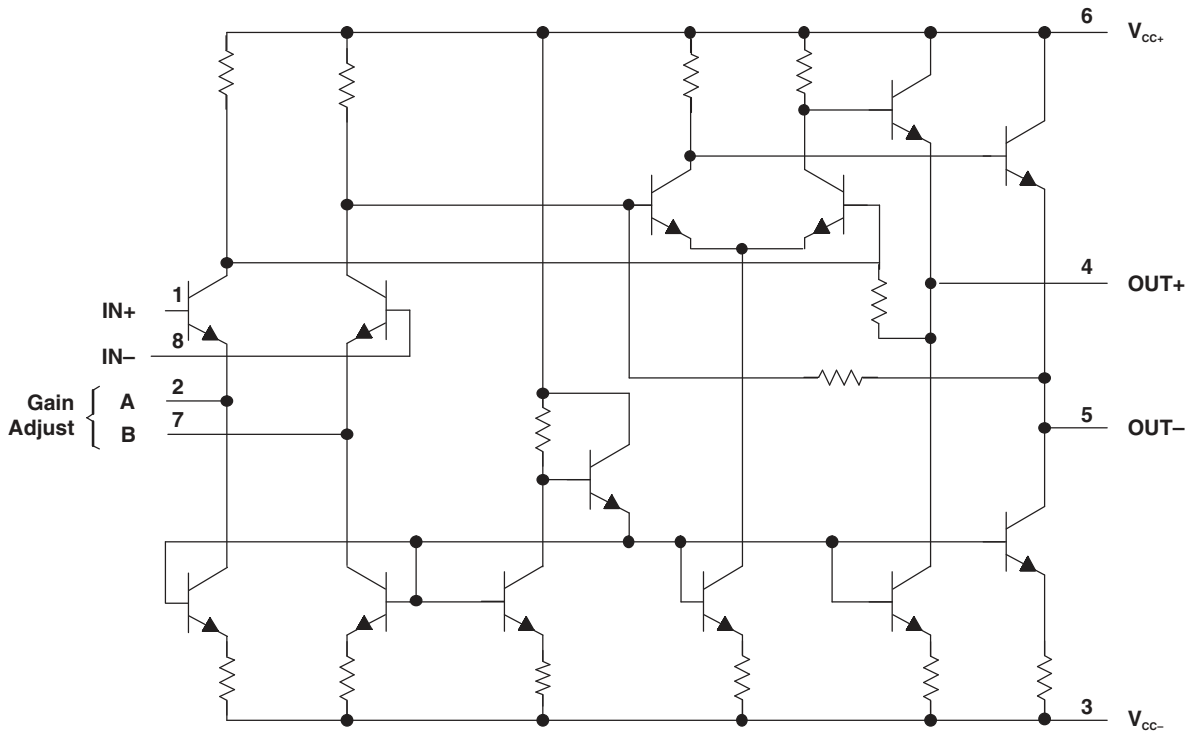


NOTE:  Pin numbers shown are for D, P, and PS packages.

## ABSOLUTE MAXIMUM RATINGS[1][2]

over operating free-air temperature range (unless otherwise noted)

| | | |
|---|---|---|
| $V_{CC+}$ | Positive supply voltage | 8 V |
| $V_{CC-}$ | Negative supply voltage | −8 V |
| $V_{DI}$ | Differential input voltage | ±5 V |
| $V_I$ | Voltage range, any input | $V_{CC+}$ to $V_{CC-}$ |
| $I_O$ | Output current | 10 mA |
| $P_D$ | Continuous total power dissipation | See Dissipation Rating Table |
| $T_A$ | Operating free-air temperature range | 0°C to 70°C |
| $T_{stg}$ | Storage temperature range | −65°C to 150°C |
| $T_{lead}$ | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1)     Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)     All voltage values except differential input voltages are with respect to the midpoint between $V_{CC+}$ and $V_{CC-}$.

## DISSIPATION RATINGS

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR | DERATE ABOVE $T_A$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|---|
| D8 | 530 mW | 5.8 mW/°C | 59 | 464 mW |
| D14 | 530 mW | N/A | N/A | 530 mW |
| N | 530 mW | N/A | N/A | 530 mW |
| P | 530 mW | N/A | N/A | 530 mW |
| PS | 530 mW | N/A | N/A | 530 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC+}$ | Positive supply voltage | 3 | 6 | 8 | V |
| $V_{CC−}$ | Negative supply voltage | −3 | −6 | −8 | V |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC\pm} = \pm6$ V, $R_L = 2$ kΩ (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS[1] | | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $A_{VD}$ | Large-signal differential voltage amplification | 1 | $V_{OPP} = 3$ V, $R_L = 2$ kΩ | $R_{AB} = 0$ | 25°C | 300 | 400 | 500 | V/V |
| | | | | | 0°C to 70°C | 250 | | 600 | |
| | | | | $R_{AB} = 1$ kΩ | 25°C | | 13 | | |
| BW | Bandwidth ( −3 dB) | 2 | $V_{OPP} = 1$ V, $R_{AB} = 0$ | | 25°C | | 50 | | MHz |
| $I_{IO}$ | Input offset current | | | | 25°C | | 0.4 | 5 | μA |
| | | | | | 0°C to 70°C | | | 6 | |
| $I_{IB}$ | Input bias current | | | | 25°C | | 9 | 30 | μA |
| | | | | | 0°C to 70°C | | | 40 | |
| $V_{ICR}$ | Common-mode input voltage range | 3 | | | 25°C | ±1 | | | V |
| | | | | | 0°C to 70°C | ±1 | | | |
| $V_{OC}$ | Common-mode output voltage | 1 | $R_L = \infty$ | | 25°C | 2.4 | 2.9 | 3.4 | V |
| $V_{OO}$ | Output offset voltage | 1 | $V_{ID} = 0$, $R_{AB} = \infty$, $R_L = \infty$ | | 25°C | | 0.35 | 0.75 | V |
| | | | | | 0°C to 70°C | | | 1.5 | |
| $V_{OPP}$ | Peak-to-peak output voltage swing | 1 | $R_L = 2$ kΩ, $R_{AB} = 0$ | | 25°C | 3 | 4 | | V |
| | | | | | 0°C to 70°C | 2.8 | | | |
| $r_i$ | Input resistance | | $V_{OD} = 1$ V, $R_{AB} = 0$ | | 25°C | | 4 | | kΩ |
| | | | | | 0°C to 70°C | | 3.6 | | |
| $r_o$ | Output resistance | | | | 0°C to 70°C | | | 30 | Ω |
| $C_i$ | Input capacitance | | | | 0°C to 70°C | | 5 | | pF |
| CMRR | Common-mode rejection ratio | 3 | $V_{IC} = \pm1$ V, $R_{AB} = 0$ | f = 100 kHz | 25°C | 60 | 86 | | dB |
| | | | | f = 5 MHz | | | 60 | | |
| | | | | f = 100 kHz | 0°C to 70°C | 50 | | | |
| | | | | f = 5 MHz | | | 60 | | |
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$) | 4 | $\Delta V_{CC+} = \pm0.5$ V, $\Delta V_{CC−} = \pm0.5$ V, $R_{AB} = 0$ | | 25°C | 50 | 70 | | dB |
| | | | | | 0°C to 70°C | 50 | | | |
| $V_n$ | Broadband equivalent input noise voltage | 4 | BW = 1 kHz to 10 MHz | | 25°C | | 3 | | μV |
| $t_{pd}$ | Propagation delay time | 2 | $\Delta V_O = 1$ V | | 25°C | | 7.5 | | ns |
| $t_r$ | Rise time | 2 | $\Delta V_O = 1$ V | | 25°C | | 10.5 | | ns |
| $I_{sink(max)}$ | Maximum output sink current | | $V_{ID} = 1$ V, $V_O = 3$ V | | | 3 | 4 | | mA |
| $I_{CC}$ | Supply current | | No load, No signal | | 25°C | | 18 | 24 | mA |
| | | | | | 0°C to 70°C | | | 27 | |

(1) $R_{AB}$ is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.
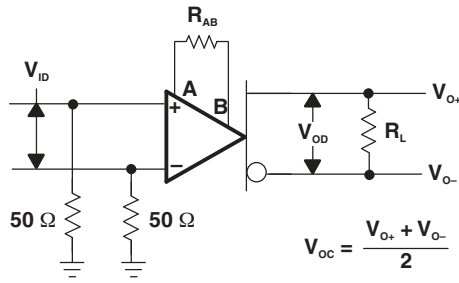
# PARAMETER MEASUREMENT INFORMATION



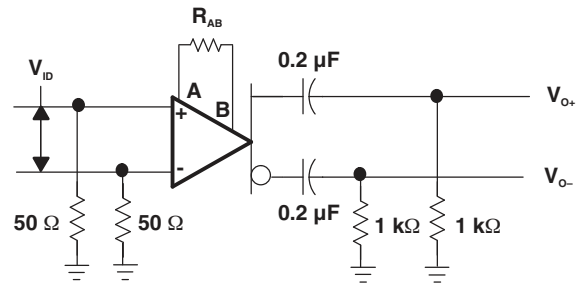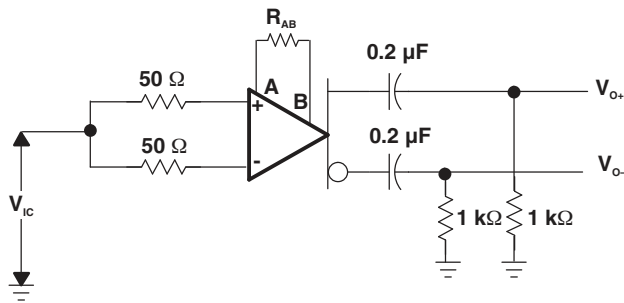$$V_{OC} = \frac{V_{O+} + V_{O-}}{2}$$

**Figure 1.**



**Figure 2.**



**Figure 3.**



**Figure 4.**

Product Folder Link(s): *TL592B*

## TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION**
**vs**
**SUPPLY VOLTAGE**



R_AB = 0
f = 1 kHz
T_A = 25°C
See Figure 1

Figure 5.

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION**
**vs**
**GAIN-ADJUSTMENT RESISTANCE**



V_CC+ = 6 V
V_CC− = -6 V
f = 10 kHz
T_A = 25°C
See Figure 1

Figure 6.

**SUPPLY CURRENT**
**vs**
**SUPPLY VOLTAGE**



No Load
No Signal
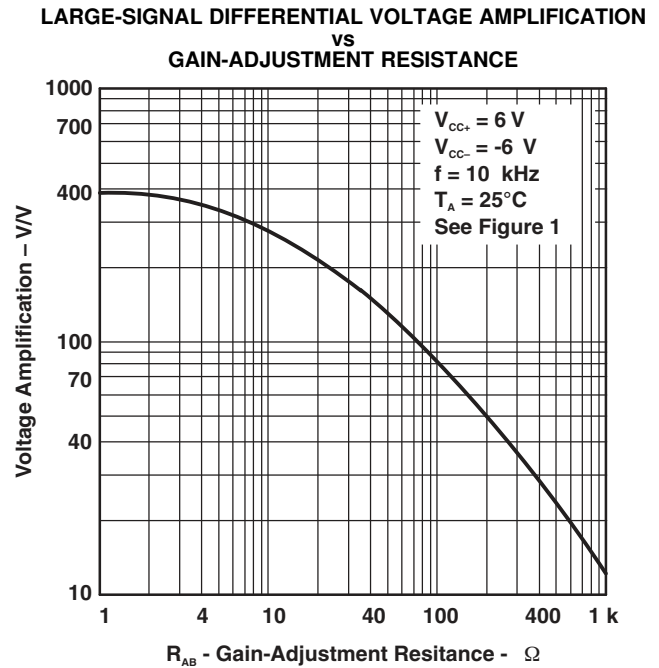T_A = 25°C

Figure 7.
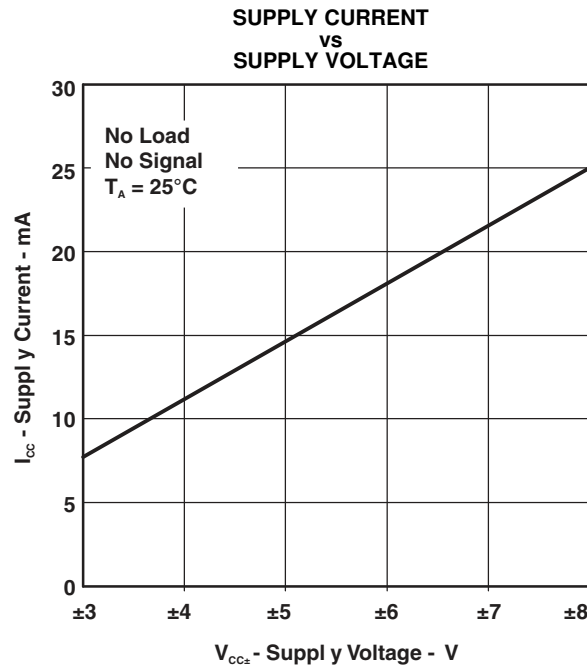
Product Folder Link(s): *TL592B*
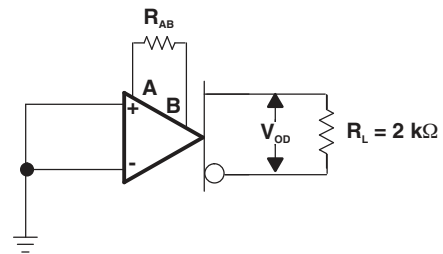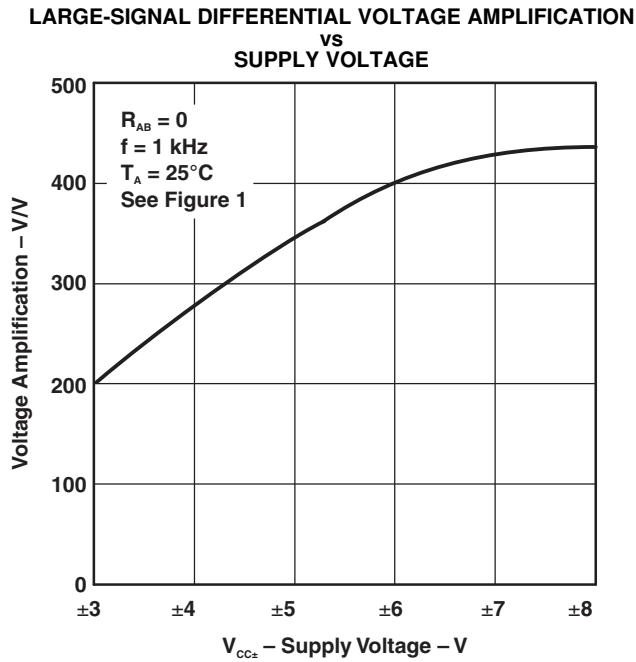
## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL592B-8D | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL592B | |
| TL592B-8DR | LIFEBUY | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL592B | |
| TL592BP | LIFEBUY | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL592BP | |
| TL592BPSR | LIFEBUY | SO | PS | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T592B | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL592B-8DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL592BPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL592B-8DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TL592BPSR | SO | PS | 8 | 2000 | 356.0 | 356.0 | 35.0 |

# PACKAGE MATERIALS INFORMATION

**TUBE**



**T - Tube height**

**L - Tube length**

**W - Tube width**

**B - Alignment groove width**

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TL592B-8D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL592BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
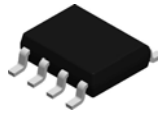
.228-.244   TYP
[5.80-6.19]

PIN 1 ID AREA

6X  .050
[1.27]

2X

.150
[3.81]

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

.189-.197
[4.81-5.00]
NOTE 3

.150-.157
[3.81-3.98]
NOTE 4

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
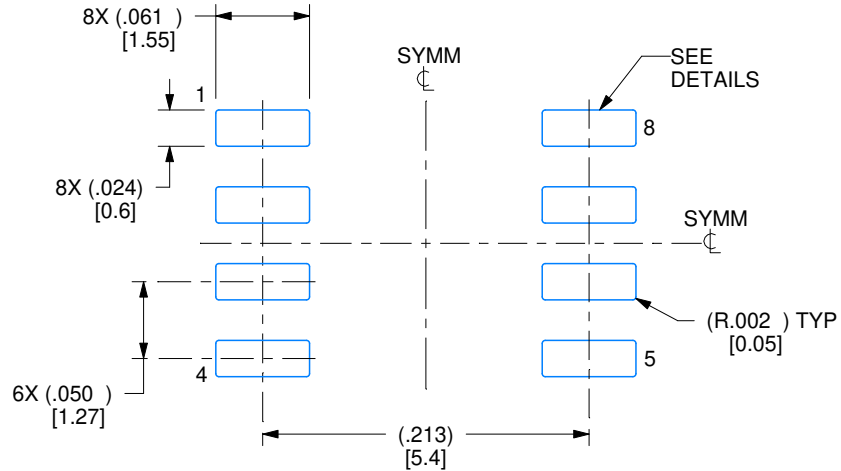[0.11-0.25]

DETAIL A
TYPICAL
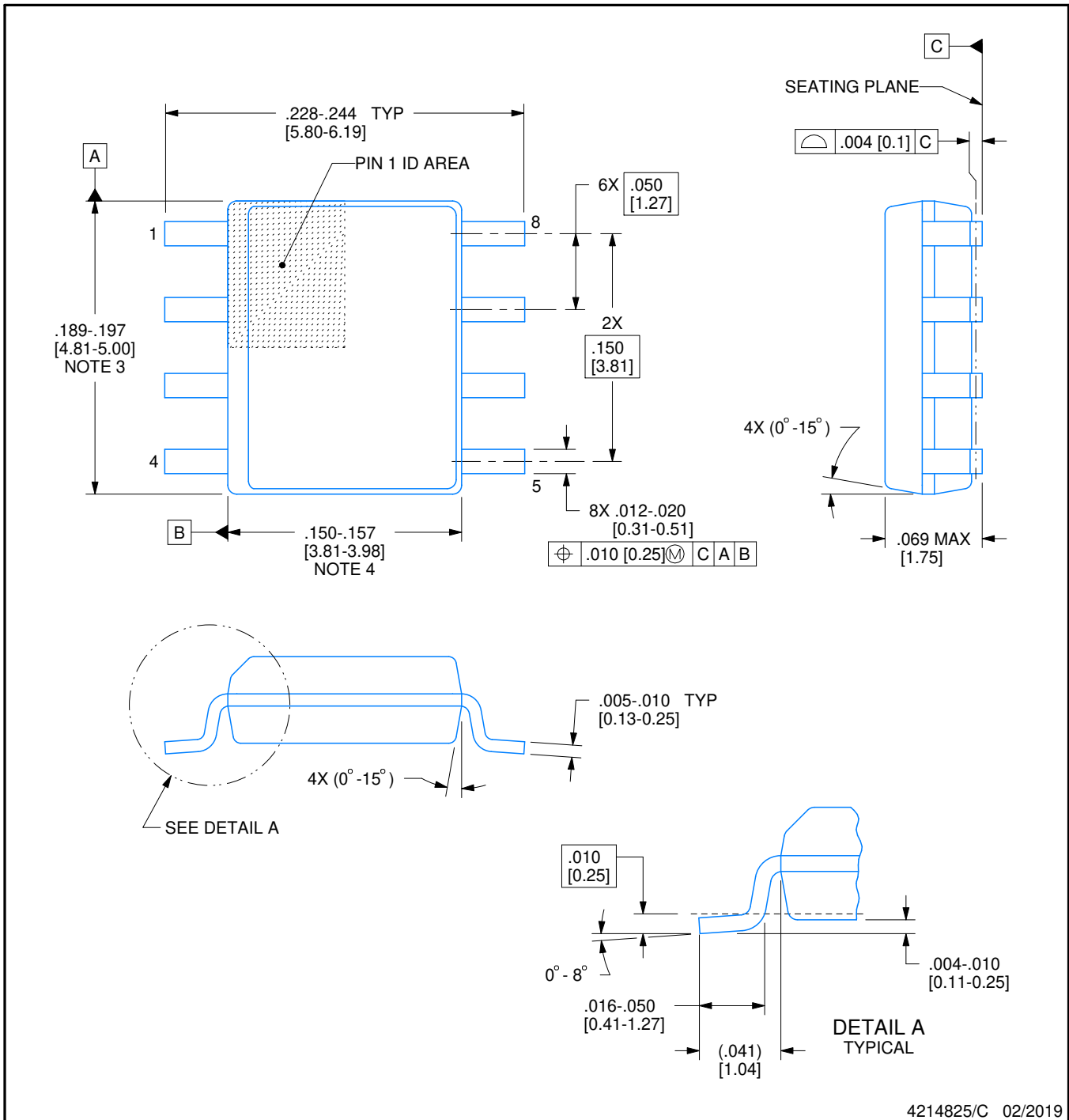
4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

  ☐  

8X (.061  )
[1.55]

SYMM

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM

(R.002  ) TYP
[0.05]

4

5

6X (.050  )
[1.27]

(.213)
[5.4]

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061 )
[1.55]

SYMM
₡

1

8X (.024)
[0.6]

SYMM
₡

8

(R.002 ) TYP
[0.05]

6X (.050 )
[1.27]

4

5

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
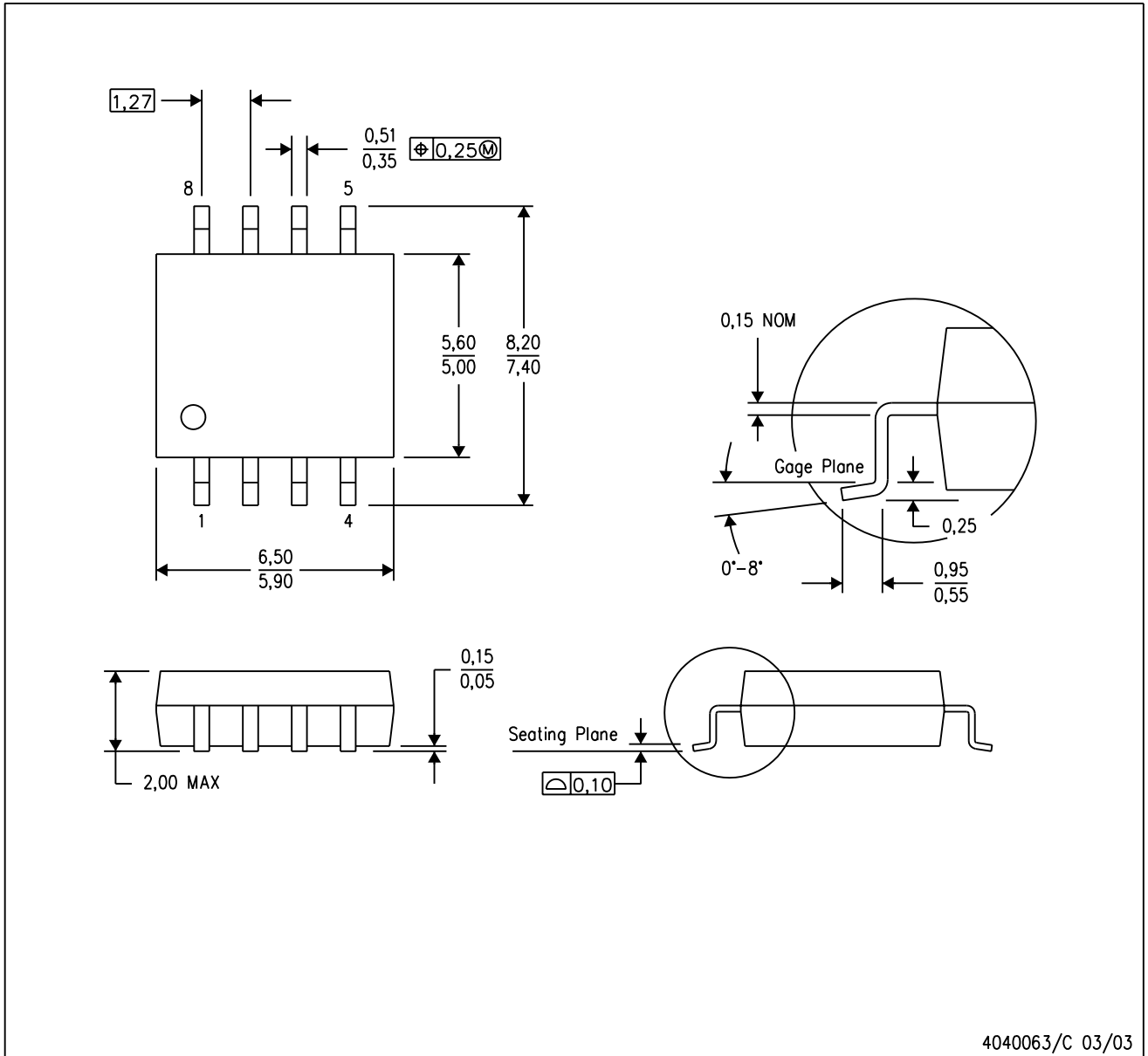SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
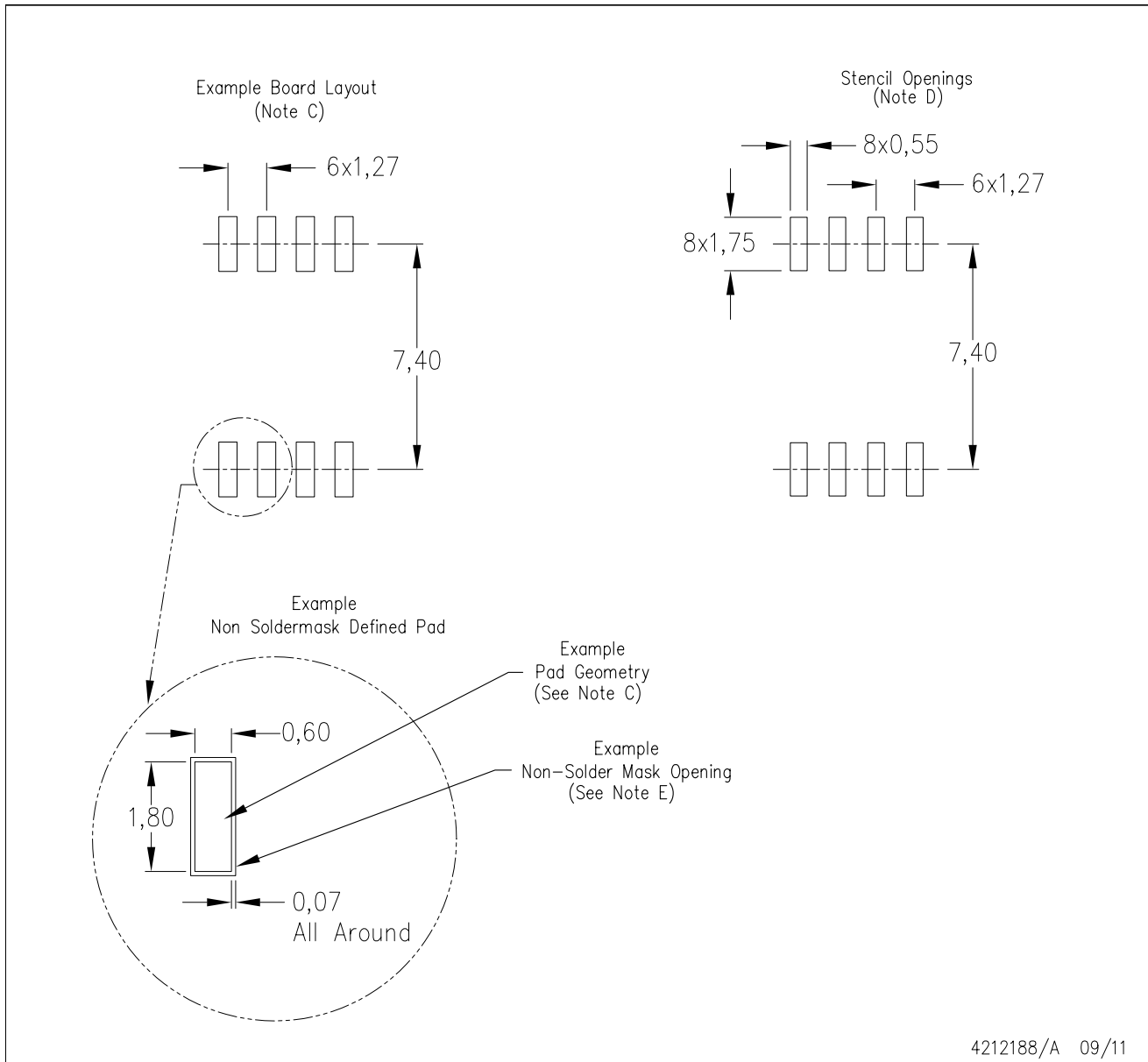
# MECHANICAL DATA

4040063/C 03/03

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Body dimensions do not include mold flash or protrusion, not to exceed 0,15.
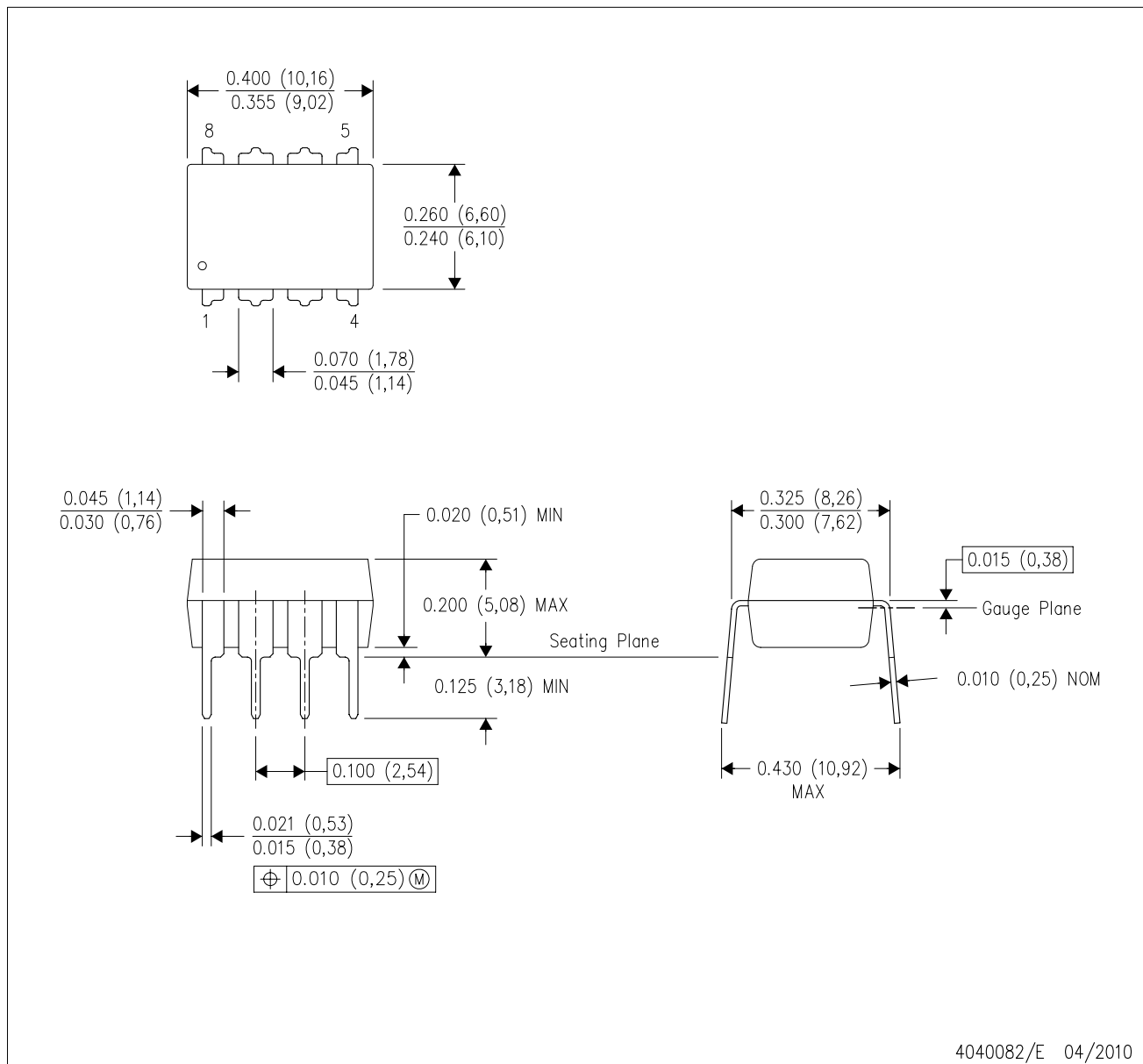
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## PS (R−PDSO−G8)　　　　　PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

7,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Non−Solder Mask Opening
(See Note E)

0,60

1,80

0,07
All Around

Stencil Openings
(Note D)

8x0,55

6x1,27

8x1,75

7,40

4212188/A  09/11

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Publication IPC−7351 is recommended for alternate designs.
　　　　　D.　Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
　　　　　　　contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
　　　　　E.　Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R−PDIP−T8)                                        PLASTIC DUAL−IN−LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8          5

0.260 (6,60)
0.240 (6,10)

1          4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92)
MAX

0.021 (0,53)
0.015 (0,38)

⊕ | 0.010 (0,25) Ⓜ

4040082/E   04/2010

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001 variation BA.

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