



3.3V CMOS 10-BIT FLIP-FLOP WITH DUAL OUTPUTS

IDT74ALVCH162820

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP package

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

DESCRIPTION:

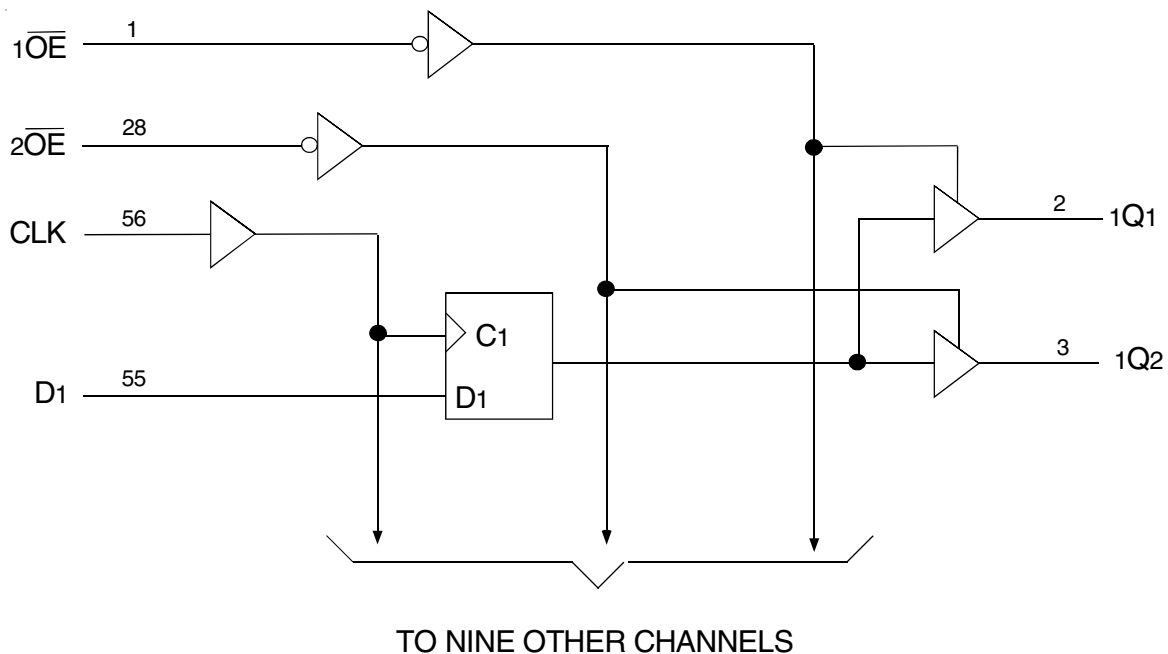
This 10-bit flip-flop is built using advanced dual metal CMOS technology. The ALVCH162820 is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface or pullup components. \overline{OE} input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

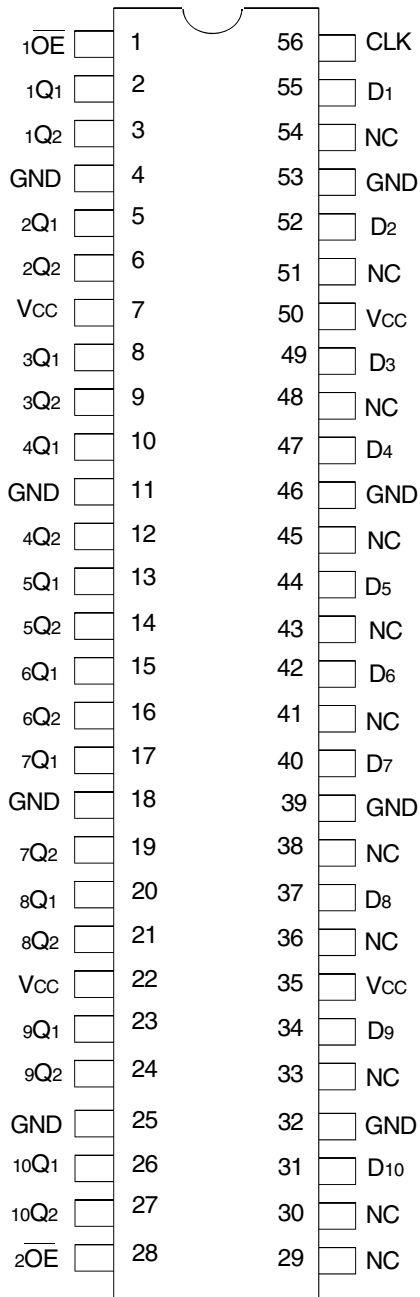
The ALVCH162820 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

The ALVCH162820 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|------------------------------------|---|-----------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to VCC+0.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | DC Output Current | -50 to +50 | mA |
| I _{IK} | Continuous Clamp Current, V _I < 0 or V _I > V _{CC} | ±50 | mA |
| I _{OK} | Continuous Clamp Current, V _O < 0 | -50 | mA |
| I _{CC} I _{SS} | Continuous Current through each V _{CC} or GND | ±100 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | 7 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | 9 | pF |
| C _{OUT} | I/O Port Capacitance | V _{IN} = 0V | 7 | 9 | pF |

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

| Pin Names | Description |
|------------------|------------------------------|
| D _x | Data Inputs ⁽¹⁾ |
| CLK | Clock Input |
| xQ _x | 3-State Outputs |
| \overline{xOE} | 3-State Output Enable Inputs |

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH FLIP-FLOP)⁽¹⁾

| Inputs | | | Output |
|------------------|--------|----------------|-------------------------------|
| \overline{xOE} | CLK | D _x | xQ _x |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q ₀ ⁽²⁾ |
| H | X | X | Z |

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|---|----------------------------------|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} | Input HIGH Current | V _{CC} = 3.6V | V _I = V _{CC} | — | — | ±5 | μA |
| I _{IL} | Input LOW Current | V _{CC} = 3.6V | V _I = GND | — | — | ±5 | μA |
| I _{OZH} I _{OZL} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | | — | — | ±10 | μA |
| | | V _O = GND | | — | — | ±10 | |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V V _{IN} = GND or V _{CC} | | — | 0.1 | 40 | μA |
| ΔI _{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | — | — | 750 | μA |

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|--|----------------------------------|----------------------------|--|------|---------------------|------|------|
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 3V | | — | — | — | μA |
| | | V _I = 2V | | -75 | — | — | |
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | | — | — | — | μA |
| | | V _I = 0.8V | | 75 | — | — | |
| I _{BHH} I _{BHL} | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | | — | — | — | μA |
| | | V _I = 1.7V | | -45 | — | — | |
| I _{BHHO} I _{BHLO} | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | | — | — | ±500 | μA |
| | | V _I = 0 to 3.6V | | — | — | ±500 | |

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|-------------|---------------------|--------------------------------|--------------|-----------|------|------|
| VOH | Output HIGH Voltage | VCC = 2.3V to 3.6V | IOH = -0.1mA | VCC - 0.2 | — | V |
| | | VCC = 2.3V | IOH = -4mA | 1.9 | — | |
| | | | IOH = -6mA | 1.7 | — | |
| | | VCC = 2.7V | IOH = -4mA | 2.2 | — | |
| | | | IOH = -8mA | 2 | — | |
| | | VCC = 3V | IOH = -6mA | 2.4 | — | |
| IOH = -12mA | 2 | | — | | | |
| VOL | Output LOW Voltage | VCC = 2.3V to 3.6V | IOL = 0.1mA | — | 0.2 | V |
| | | VCC = 2.3V | IOL = 4mA | — | 0.4 | |
| | | | IOL = 6mA | — | 0.55 | |
| | | VCC = 2.7V | IOL = 4mA | — | 0.4 | |
| | | | IOL = 8mA | — | 0.6 | |
| | | VCC = 3V | IOL = 6mA | — | 0.55 | |
| IOL = 12mA | — | | 0.8 | | | |

NOTE:
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, TA = 25°C

| Symbol | Parameter | Test Conditions | VCC = 2.5V ± 0.2V | VCC = 3.3V ± 0.3V | Unit |
|--------|--|---------------------|-------------------|-------------------|------|
| | | | Typical | Typical | |
| CPD | Power Dissipation Capacitance per Flip Flop Outputs enabled | CL = 0pF, f = 10Mhz | 68 | 66 | pF |
| CPD | Power Dissipation Capacitance per Flip Flop Outputs disabled | | 39 | 47 | |

SWITCHING CHARACTERISTICS⁽¹⁾

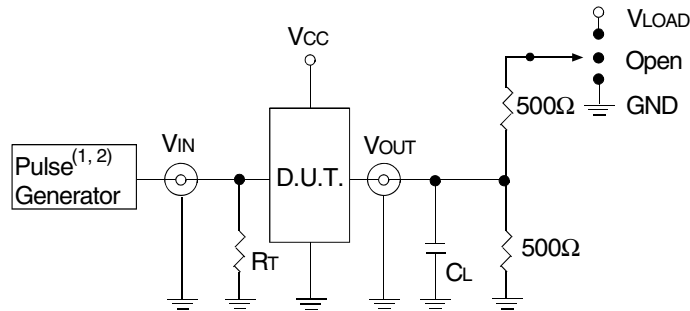
| Symbol | Parameter | VCC = 2.5V ± 0.2V | | VCC = 2.7V | | VCC = 3.3V ± 0.3V | | Unit |
|--------|--|-------------------|------|------------|------|-------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| fMAX | | 150 | — | 150 | — | 150 | — | MHz |
| tPLH | Propagation Delay | 1 | 4.5 | — | 4.5 | 1 | 4.3 | ns |
| tPHL | CLK to xQx | | | | | | | |
| tPZH | Output Enable Time | 1 | 6.9 | — | 6.8 | 1 | 5.6 | ns |
| tPZL | \overline{OE} to xQx | | | | | | | |
| tPHZ | Output Disable Time | 1 | 6.2 | — | 5.5 | 1 | 5 | ns |
| tPLZ | \overline{OE} to xQx | | | | | | | |
| tSU | Set-up Time, HIGH or LOW, data before CLK↑ | 1.7 | — | 1.8 | — | 1.4 | — | ns |
| tH | Hold Time, HIGH or LOW, data after CLK↑ | 1.1 | — | 1.1 | — | 1 | — | ns |
| tW | Pulse Width, CLK HIGH or LOW | 3.3 | — | 3.3 | — | 3.3 | — | ns |
| tSK(O) | Output Skew ⁽²⁾ | — | — | — | — | — | 500 | ps |

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. TA = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{CC} ⁽¹⁾ =3.3V±0.3V | V _{CC} ⁽¹⁾ =2.7V | V _{CC} ⁽²⁾ =2.5V±0.2V | Unit |
|-------------------|---|--------------------------------------|---|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |



Test Circuit for All Outputs

DEFINITIONS:

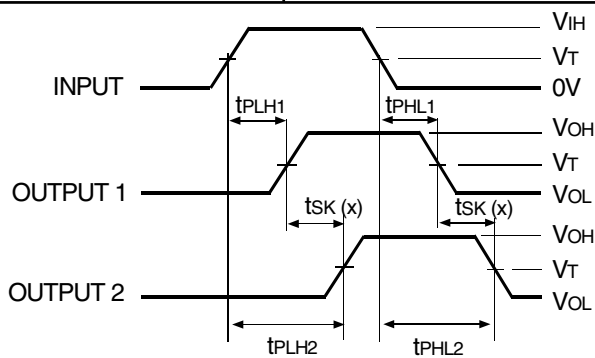
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other Tests | Open |

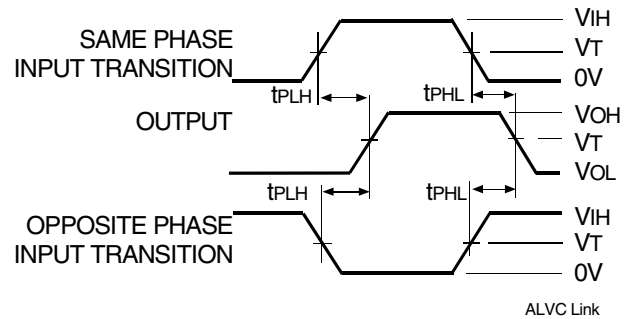


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

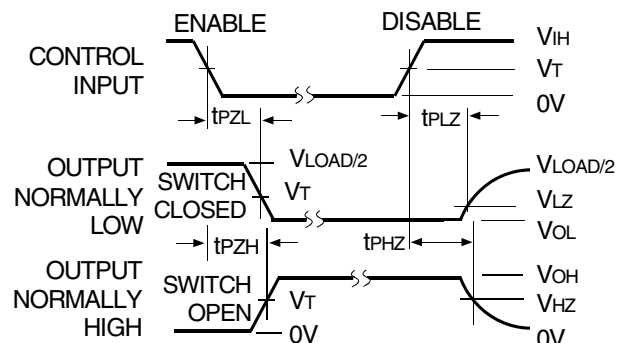
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



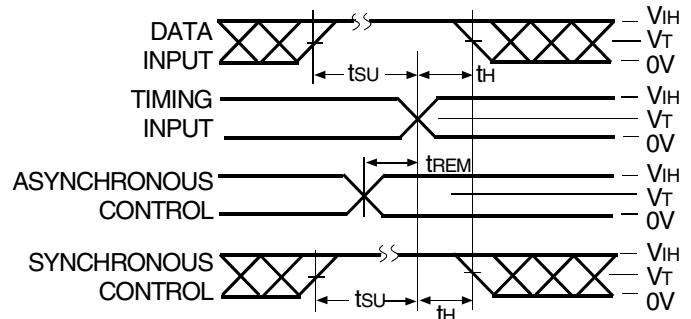
Propagation Delay



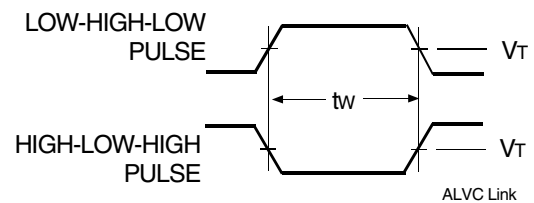
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

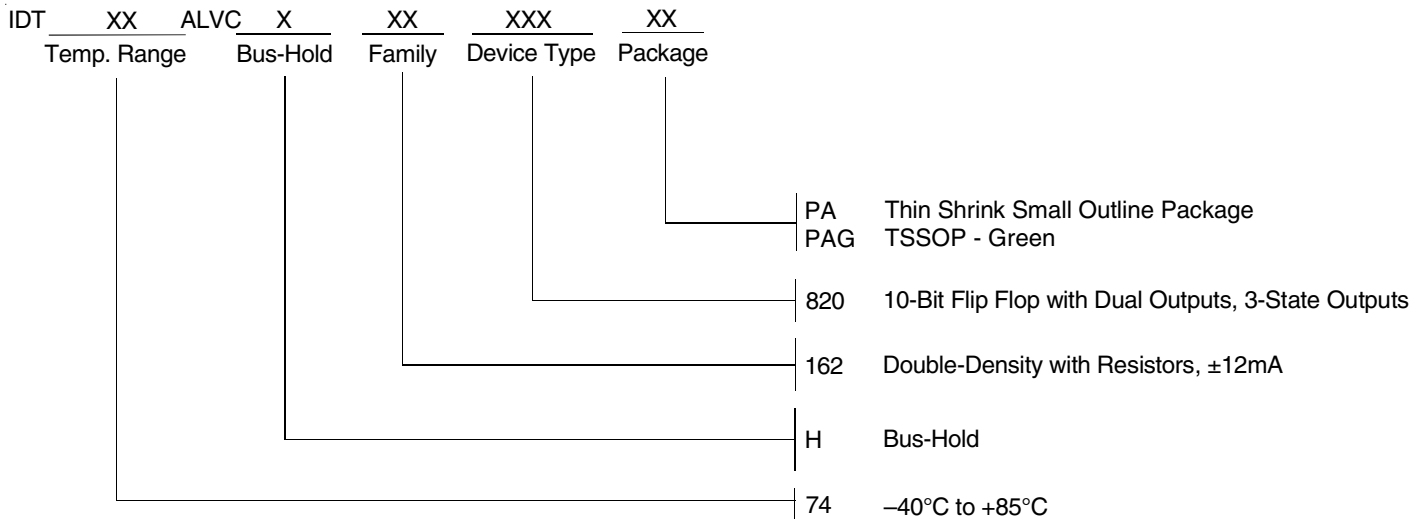


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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