

Phase-Aligned Clock Multiplier

Features

- 10 MHz to 166.67 MHz output operating range
- Four-multiplier configuration
- Single PLL architecture
- Phase aligned outputs
- Low jitter, high accuracy outputs
- Output enable pin
- 3.3 V operation
- 5 V tolerant input
- Internal loop filter
- 8-pin 150-mil small-outline integrated circuit (SOIC) package
- Commercial temperature

Functional Description

The CY2300 is a four output 3.3 V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part allows the user to obtain $1/2x$, $1x$, $\overline{1x}$ and $2x$ REF_{IN} output frequencies on respective output pins.

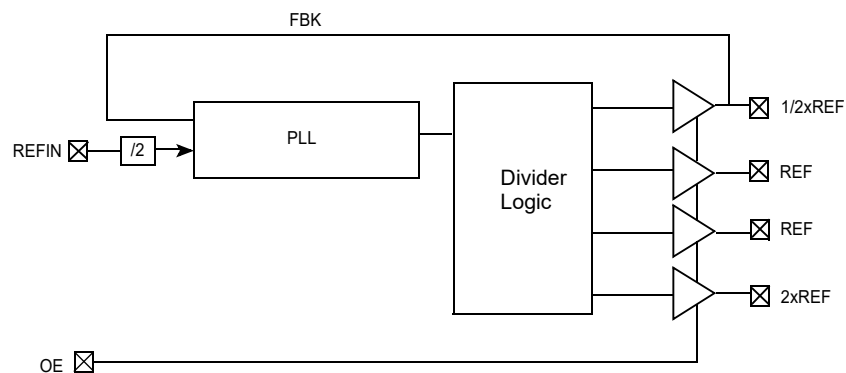
The part has an on-chip PLL which locks to an input clock presented on the REF_{IN} pin. The input-to-output skew is guaranteed to be less than ± 200 ps, and output-to-output skew is guaranteed to be less than 200 ps.

Multiple CY2300 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.

The CY2300 is available in commercial temperature range.

For a complete list of related documentation, click [here](#).

Logic Block Diagram

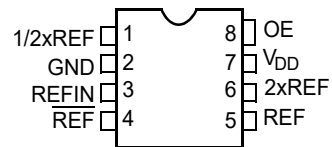


Contents

Pinouts	3	Document Conventions	9
Pin Definitions	3	Units of Measure	9
Maximum Ratings	4	Errata	10
Operating Conditions	4	Part Numbers Affected	10
Electrical Characteristics	4	CY2300 Errata Summary	10
Thermal Resistance	4	CY2300 Qualification Status of fixed silicon	10
Test Circuits	5	Document History Page	12
Switching Characteristics	5	Sales, Solutions, and Legal Information	13
Switching Waveforms	6	Worldwide Sales and Design Support	13
Ordering Information	7	Products	13
Ordering Code Definitions	7	PSoC@Solutions	13
Package Drawing and Dimensions	8	Cypress Developer Community	13
Reference Documents	9	Technical Support	13
Acronyms	9		

Pinouts

Figure 1. 8-pin SOIC pinout (Top View)



Pin Definitions

Pin	Signal ^[1]	Description
1	1/2xREF	Clock output, 1/2x reference
2	GND	Ground
3	REFIN	Input reference frequency, 5 V tolerant input
4	$\overline{\text{REF}}$	Clock output reference
5	REF	Clock output reference
6	2xREF	Clock output, 2x reference
7	V _{DD}	3.3 V Supply
8	OE	Output enable (weak pull-up)

Note

1. Weak pull-down on all outputs.

Maximum Ratings

Supply voltage to ground potential -0.5 V to +7.0 V
 DC input voltage (except ref) -0.5 V to $V_{DD} + 0.5$ V
 DC input voltage REF -0.5 V to 7 V

Storage temperature -65 °C to +150 °C
 Junction temperature 150 °C
 Static discharge voltage
 (per MIL-STD-883, method 3015) > 2000 V

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance, 10 MHz < F_{OUT} < 133.33 MHz	–	18	pF
	Load capacitance, 133.33 MHz < F_{OUT} < 166.67 MHz	–	12	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD} 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V
I_{IL}	Input LOW current	$V_{IN} = 0$ V	–	100	µA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	50	µA
V_{OL}	Output LOW voltage ^[2]	$I_{OL} = 8$ mA	–	0.4	V
V_{OH}	Output HIGH voltage ^[2]	$I_{OH} = -8$ mA	2.4	–	V
I_{DD}	Supply current	Unloaded outputs, REFIN = 66 MHz	–	45	mA
		Unloaded outputs, REFIN = 33 MHz	–	32	mA
		Unloaded outputs, REFIN = 20 MHz	–	18	mA

Thermal Resistance

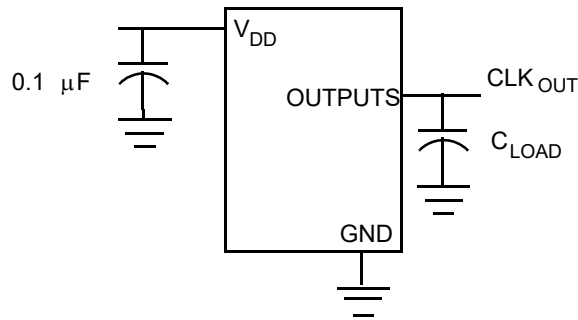
Parameter ^[3]	Description	Test Conditions	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	140	°C/W
θ_{JC}	Thermal resistance (junction to case)		54	°C/W

Notes

- Parameter is guaranteed by design and characterization. It is not 100% tested in production.
- These parameters are guaranteed by design and are not tested.

Test Circuits

Figure 2. Test Circuit #1



Switching Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
1/t ₁	Output frequency	18 pF load	10	–	133.33	MHz
		12 pF load	–	–	166.67	MHz
	Duty cycle ^[4] = t ₂ ÷ t ₁	Measured at V _{DD} /2	40	50	60	%
t ₃	Rise time ^[4]	Measured between 0.8 V and 2.0 V	–	–	1.20	ns
t ₄	Fall time ^[4]	Measured between 0.8 V and 2.0 V	–	–	1.20	ns
t ₅	Output to output skew on rising edges ^[4]	All outputs equally loaded Measured at V _{DD} /2	–	–	200	ps
t ₆	Delay, REFIN rising edge to output rising edge ^[4]	Measured at V _{DD} /2 from REFIN to any output	–	–	±200	ps
t ₇	Device to device skew ^[4]	Measured at V _{DD} /2 on the 1/2xREF pin of devices (pin 1)	–	–	400	ps
t _J	Period jitter ^[4]	Measured at F _{out} = 133.33 MHz, loaded outputs, 18 pF load	–	–	±175	ps
t _{LOCK}	PLL lock time ^[4]	Stable power supply, valid clocks presented on REFIN	–	–	1.0	ms

Note

4. All parameters are specified with equally loaded outputs.

Switching Waveforms

Figure 3. Duty Cycle Timing

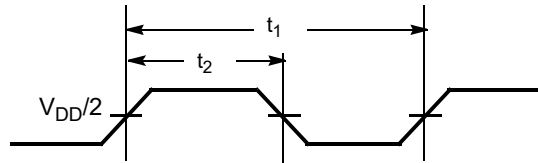


Figure 4. All Outputs Rise/Fall Time

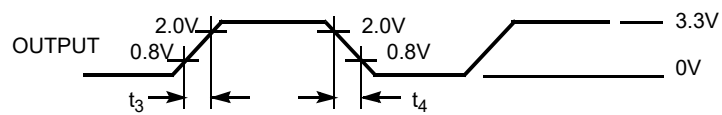


Figure 5. Output to Output Skew

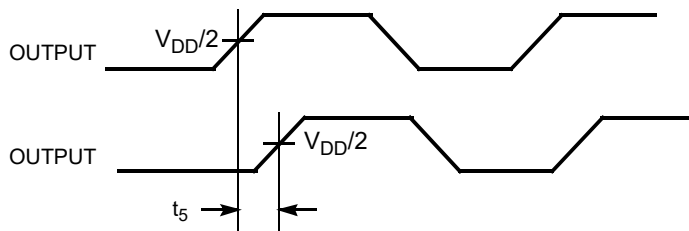


Figure 6. Input to Output Propagation Delay

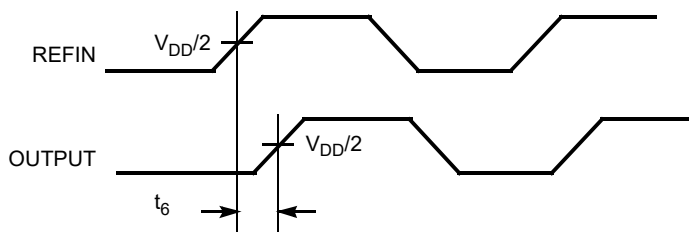
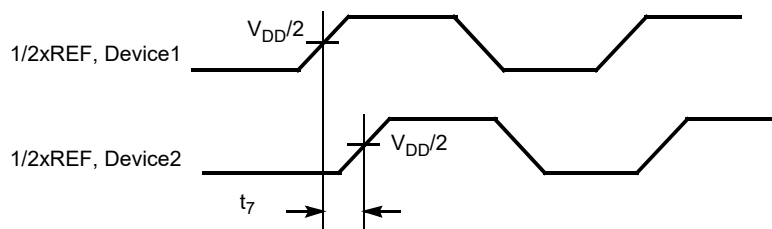


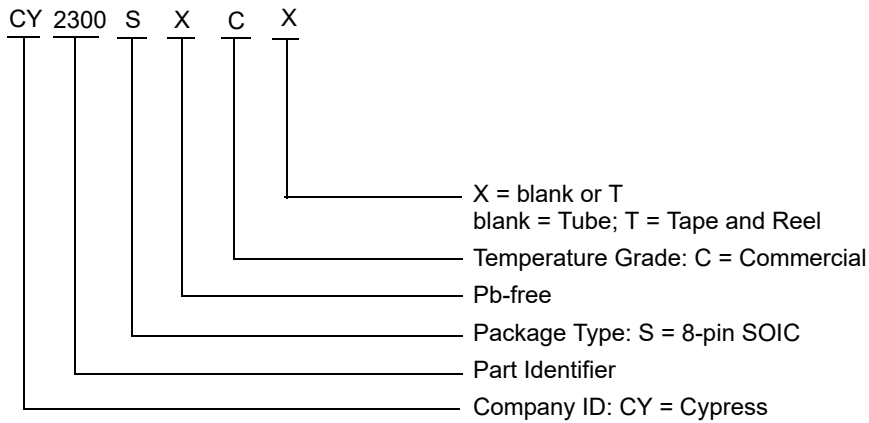
Figure 7. Device to Device Skew



Ordering Information

Ordering Code	Package Type	Operating Range
Pb-free		
CY2300SXC	8-pin SOIC	Commercial (0 °C to 70 °C)
CY2300SXCT	8-pin SOIC - Tape and Reel	Commercial (0 °C to 70 °C)

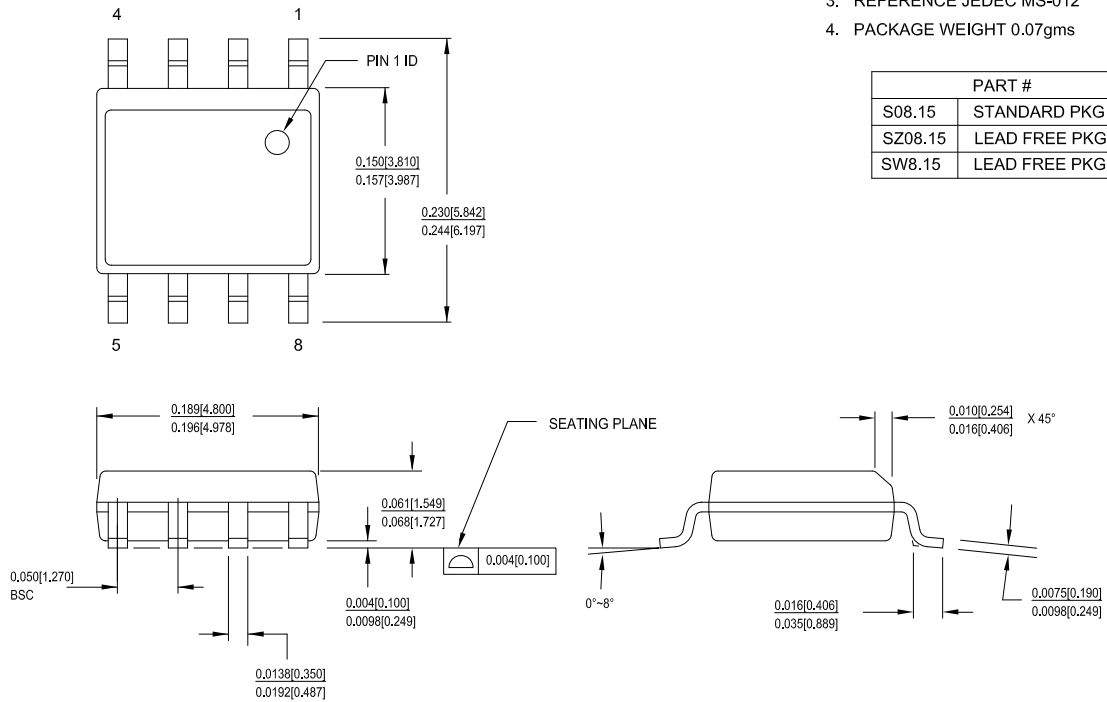
Ordering Code Definitions



Package Drawing and Dimensions

Figure 8. 8-pin SOIC (150 Mils) Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
MAX.
2. PIN 1 ID IS OPTIONAL,
ROUND ON SINGLE LEADFRAME
RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms



PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG

51-85066 *I

Reference Documents

Reference documents are available through your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

Document Number	Document Title	Description
NA	NA	NA

Acronyms

Acronym	Description
FBK	Feedback
OE	Output Enable
PLL	Phase Locked Loop
REFIN	Reference Input

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
pA	picoampere
pF	picofarad
ps	picosecond
V	volt

Errata

This section describes the errors, workaround solution and silicon design fixes for Cypress zero delay clock buffers belonging to the families CY2300. Details include errata trigger conditions, scope of impact, available workaround and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY2300SXC	All Variants
CY2300SXCT	All Variants

CY2300 Errata Summary

Items	Part Number	Fix Status
Start up lock time issue [CY2300]	All	Silicon fixed. New silicon available from WW 10 of 2013

CY2300 Qualification Status of fixed silicon

Product Status: In production

Qualification report last updated on 11/27/2012

<http://www.cypress.com/?rID=72595>

1. Start up lock time issue

■ Problem Definition

Output of CY2300 fails to locks within 1 ms upon power up (as per datasheet spec).

■ Parameters Affected

PLL lock time (t_{LOCK})

■ Trigger Condition(S)

Start up

■ Scope of Impact

It can impact the performance of system and its throughput.

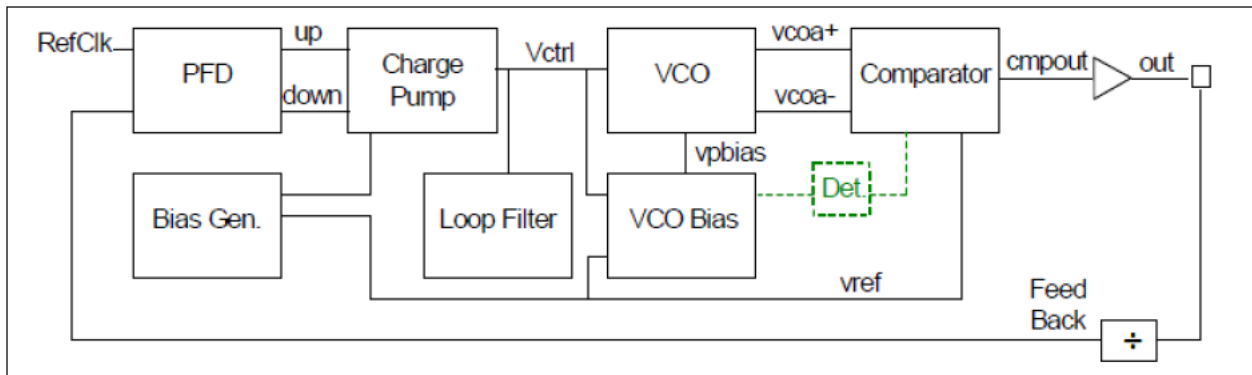
■ Workaround

Apply reference input (RefClk) before power up (VDD). If RefClk is applied after power up, noise gets coupled on the output and propagates back to the PLL causing it to take higher time to acquire lock. If reference input is present during power up, noise will not propagate to the PLL and device will start up normally without problems.

■ Fix Status

This issue is due to design marginality. Two minor design modifications have been made to address this problem.

- Addition of VCO bias detector block as shown in the following figure keeps comparator power down till VCO bias is present and thereby eliminating the propagation of noise to feedback.
- Bias generator enhancement for successful initialization.



Document History Page

Document Title: CY2300, Phase-Aligned Clock Multiplier Document Number: 38-07252				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	110517	SZV	01/07/2002	Changed from spec number 38-01039 to spec number 38-07252.
*A	121854	RBI	12/14/2002	Updated Operating Conditions : Added t _{PU} parameter and its details.
*B	246829	RGL	08/02/2004	Updated Ordering Information : Updated part numbers (Added Lead Free Devices).
*C	2568533	AESA	09/23/2008	Removed Selector Guide. Removed Operating Conditions (for CY2300SI Industrial Temperature Devices). Removed Electrical Characteristics (for CY2300SI Industrial Temperature Devices). Removed Switching Characteristics (for CY2300SI Industrial Temperature Devices). Updated Ordering Information : Updated part numbers (Removed part numbers CY2300SC, CY2300SC, CY2300SI, CY2300SI, CY2300SXI and CY2300SXI). Updated to new template.
*D	3026183	BASH	09/01/2010	Removed Benefits. Updated Operating Conditions : Updated details in "Description" column corresponding to C _L parameter (Added lower limit of 10 MHz for 18pF load capacitance). Updated Ordering Information : No change in part numbers. Added Ordering Code Definitions . Added Reference Documents, Acronyms and Units of Measure .
*E	4126294	CINM	11/25/2013	Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *D to *F. Added Errata . Updated to new template. Completing Sunset Review.
*F	4325140	CINM	03/28/2014	Updated Errata .
*G	4578443	TAVA	11/25/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end.
*H	5240894	PSR	04/25/2016	Updated Features : Added "10 MHz to 166.67 MHz output operating range". Added Thermal Resistance . Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *F to *H. Updated to new template.
*I	5542709	TAVA	12/05/2016	Updated to new template. Completing Sunset Review.
*J	6010798	PAWK	01/02/2018	Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *H to *I. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2002-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.