

# TPIC1301 3-HALF H-BRIDGE GATE-PROTECTED POWER DMOS ARRAY

SLIS037 – NOVEMBER 1994

- Low  $r_{DS(on)}$  . . . 0.23  $\Omega$  Typ
- High Voltage Output . . . 60 V
- Extended ESD Capability . . . 4000 V
- Pulsed Current . . . 11.25 A Per Channel
- Fast Commutation Speed

## description

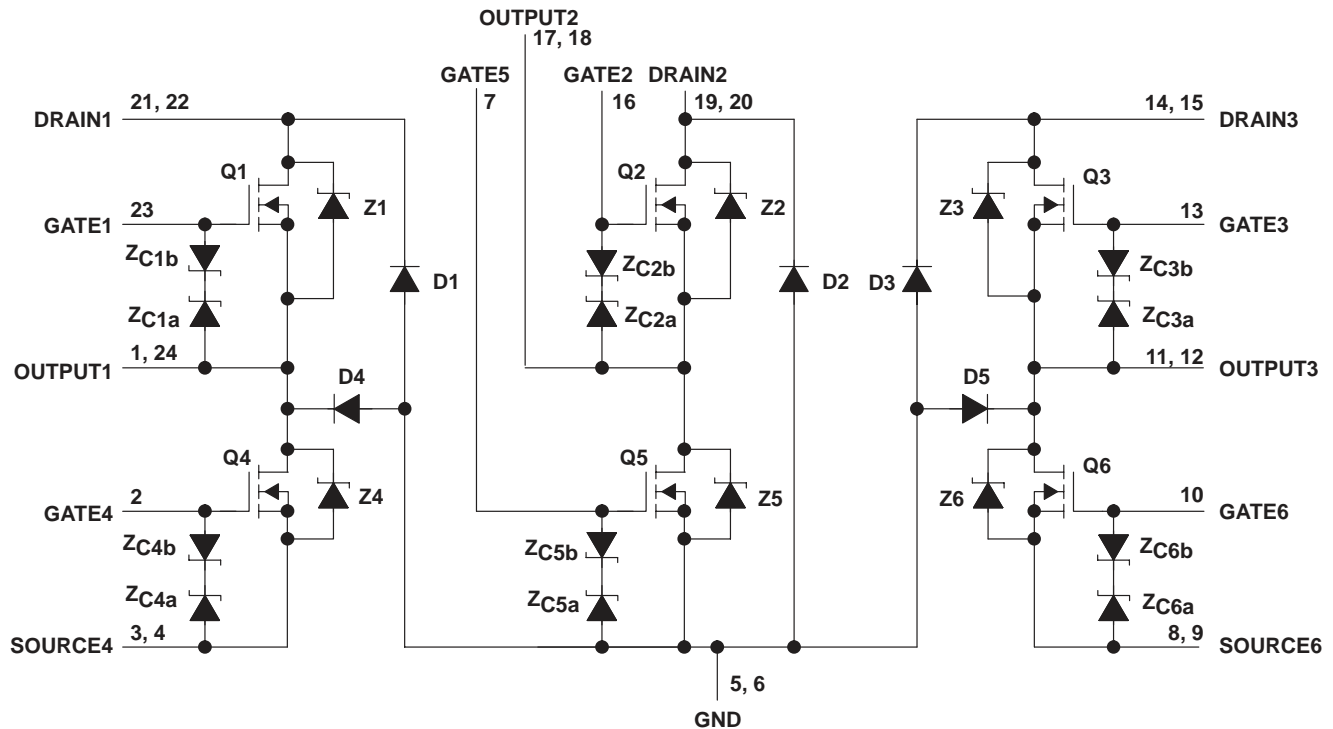
The TPIC1301 is a monolithic gate-protected power DMOS array that consists of six electrically isolated N-channel enhancement-mode DMOS transistors configured as three half H-bridges. Each transistor features integrated high-current zener diodes ( $Z_{CXa}$  and  $Z_{CXb}$ ) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k $\Omega$  resistor.

The TPIC1301 is offered in a 24-pin wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

DW PACKAGE  
(TOP VIEW)

OUTPUT1	1	24	OUTPUT1
GATE4	2	23	GATE1
SOURCE4	3	22	DRAIN1
SOURCE4	4	21	DRAIN1
GND	5	20	DRAIN2
GND	6	19	DRAIN2
GATE5	7	18	OUTPUT2
SOURCE6	8	17	OUTPUT2
SOURCE6	9	16	GATE2
GATE6	10	15	DRAIN3
OUTPUT3	11	14	DRAIN3
OUTPUT3	12	13	GATE3

## schematic



NOTE: For correct operation, no terminal pin may be taken below GND.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# TPIC1301

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### absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-GND voltage, $V_{DG}$	100 V
Drain-to-source voltage, $V_{DS}$	60 V
Output-to-GND voltage	60 V
SOURCE4, SOURCE6-to-GND voltage	60 V
Gate-to-source voltage range, $V_{GS}$	-9 V to 18 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	2.25 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	2.25 A
Pulsed drain current, each output, $I_{max}$ , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	11.25 A
Continuous gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	$\pm 50$ mA
Pulsed gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	$\pm 500$ mA
Single-pulse avalanche energy, $E_{AS}$ , $T_C = 25^\circ\text{C}$ (see Figures 4, 15, and 16)	17.2 mJ
Continuous total dissipation, $T_C = 25^\circ\text{C}$ (see Figure 15)	1.39 W
Operating virtual junction temperature range, $T_J$	$-40^\circ\text{C}$ to $150^\circ\text{C}$
Operating case temperature range, $T_C$	$-40^\circ\text{C}$ to $125^\circ\text{C}$
Storage temperature range	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ\text{C}$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

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**electrical characteristics,  $T_C = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$ , See Figure 5	$V_{DS} = V_{GS}$ ,	1.5	1.75	2.2	V
$V_{(BR)GS}$	Gate-to-source breakdown voltage	$I_{GS} = 250\ \mu\text{A}$		18			V
$V_{(BR)SG}$	Source-to-gate breakdown voltage	$I_{SG} = 250\ \mu\text{A}$		9			V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1 – D5)	Drain-to-GND current = $250\ \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 2.25\ \text{A}$ , See Notes 2 and 3	$V_{GS} = 10\ \text{V}$ ,		0.52	0.62	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 2.25\ \text{A}$ , $V_{GS} = 0$ (Z1 – Z6), See Notes 2 and 3 and Figure 12			1	1.2	V
$V_F$	Forward on-state voltage, GND-to-drain	$I_D = 2.25\ \text{A}$ (D1 – D5) See Notes 2 and 3			5		V
$I_{DSS}$	Drain current-gate shorted to source	$V_{DS} = 48\ \text{V}$ , $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1		$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	0.5	10		
$I_{GSSF}$	Forward-gate current, drain short circuited to source	$V_{GS} = 15\ \text{V}$ ,	$V_{DS} = 0$		20	200	nA
$I_{GSSR}$	Reverse-gate current, drain short circuited to source	$V_{SG} = 5\ \text{V}$ ,	$V_{DS} = 0$		10	100	nA
$I_{lkg}$	Leakage current, drain-to-GND Gate shorted to source	$V_{DGND} = 48\ \text{V}$	$T_C = 25^\circ\text{C}$	0.05	1		$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	0.5	10		
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 2.25\ \text{A}$ , See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$	0.23	0.275		$\Omega$
			$T_C = 125^\circ\text{C}$	0.35	0.4		
$g_{fs}$	Forward transconductance	$V_{DS} = 15\ \text{V}$ , See Notes 2 and 3 and Figure 9	$I_D = 1.125\ \text{A}$ ,	1.6	2.21		S
$C_{iss}$	Short-circuit input capacitance, common source				200	250	pF
$C_{oss}$	Short-circuit output capacitance, common source	$V_{DS} = 25\ \text{V}$ , $f = 1\ \text{MHz}$ ,	$V_{GS} = 0$ , See Figure 11		175	220	
$C_{rss}$	Short-circuit reverse transfer capacitance, common source				40	75	

NOTES: 2. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

**source-to-drain and GND-to-drain diode characteristics,  $T_C = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	$I_S = 1.125\ \text{A}$ , $V_{GS} = 0$ , See Figures 1 and 14	$V_{DS} = 48\ \text{V}$ , $di/dt = 100\ \text{A}/\mu\text{s}$ ,	Z1, Z2, and Z3		50		ns
$Q_{RR}$	Total diode charge					65		nC



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**resistive-load switching characteristics,  $T_C = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$ , $R_L = 20\ \Omega$ , $t_{dis} = 10\text{ ns}$ , See Figure 2 $t_{en} = 10\text{ ns}$ ,		25	50	ns
$t_{d(off)}$ Turn-off delay time			25	50	
$t_r$ Rise time			15	30	
$t_f$ Fall time			7	15	
$Q_g$ Total gate charge	$V_{DS} = 48\text{ V}$ , See Figure 3 $I_D = 1.125\text{ A}$ , $V_{GS} = 10\text{ V}$ ,		6.2	7.4	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.7	0.8	
$Q_{gd}$ Gate-to-drain charge			2.4	2.9	
$L_D$ Internal drain inductance			5		nH
$L_S$ Internal source inductance			5		
$R_g$ Internal gate resistance			0.25		$\Omega$

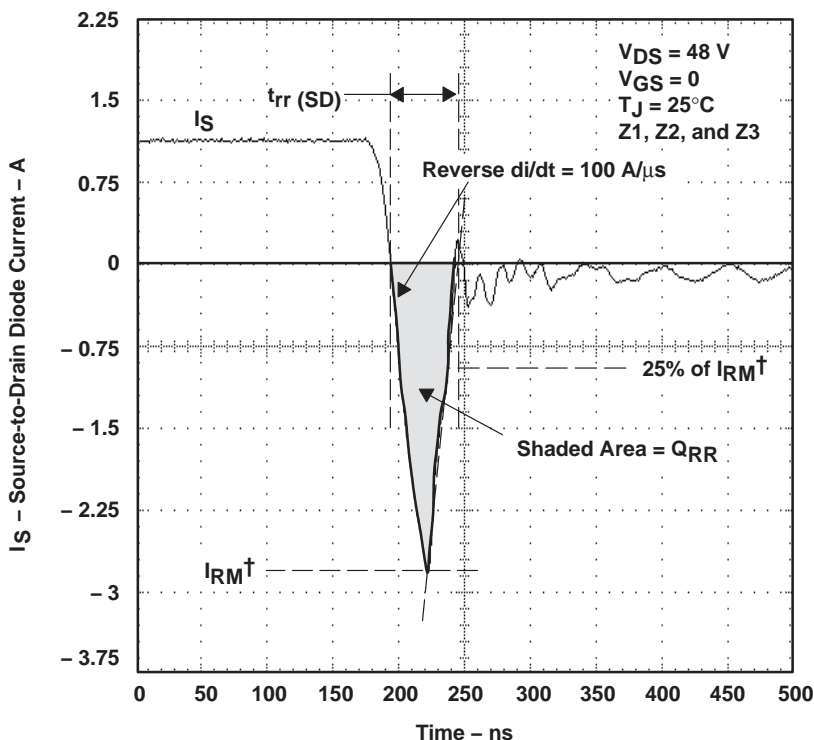
**thermal resistance**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	See Notes 4 and 7		90		$^\circ\text{C}/\text{W}$
$R_{\theta JB}$ Junction-to-board thermal resistance	See Notes 5 and 7		45		$^\circ\text{C}/\text{W}$
$R_{\theta JP}$ Junction-to-pin thermal resistance	See Notes 6 and 7		28		$^\circ\text{C}/\text{W}$

- NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.  
5. Package mounted on a 24 in<sup>2</sup>, 4-layer FR4 printed-circuit board.  
6. Package mounted in intimate contact with infinite heatsink.  
7. All outputs with equal power

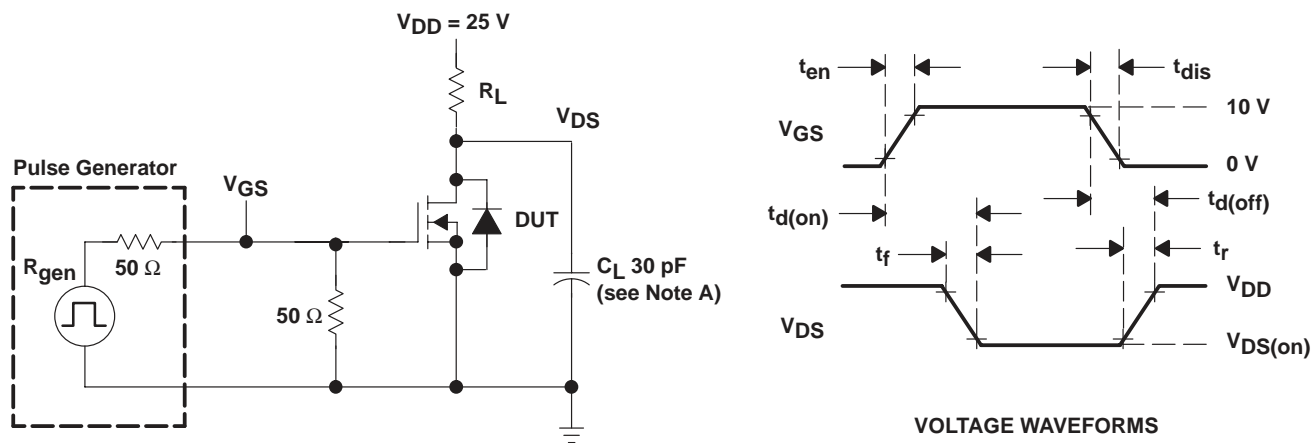


**PARAMETER MEASUREMENT INFORMATION**



$^\dagger I_{RM}$  = maximum recovery current

**Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode**



**TEST CIRCUIT**

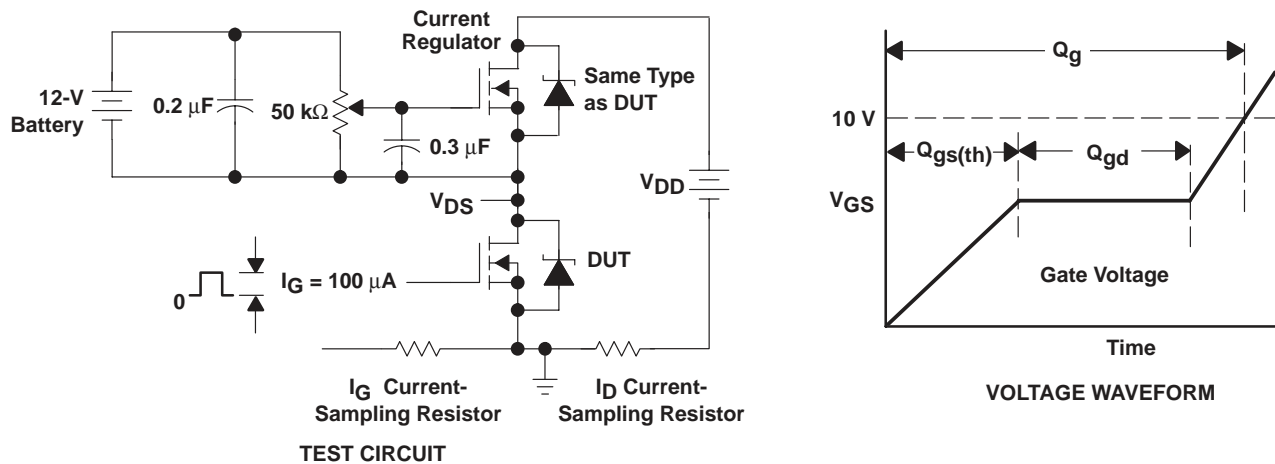
NOTE A:  $C_L$  includes probe and jig capacitance.

**Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms**

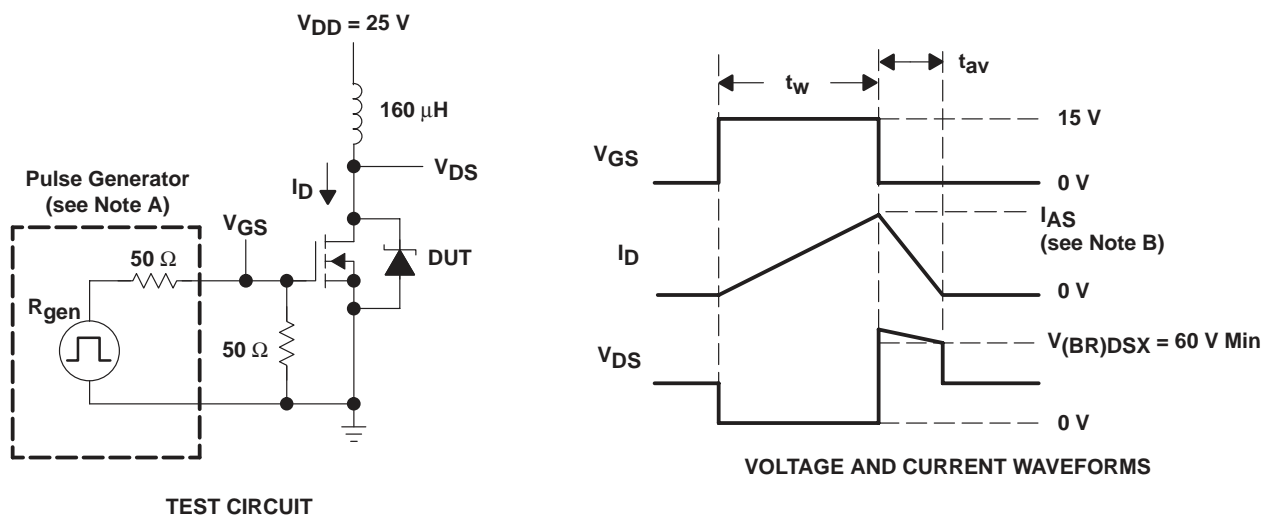
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**PARAMETER MEASUREMENT INFORMATION**



**Figure 3. Gate-Charge Test Circuit and Voltage Waveform**

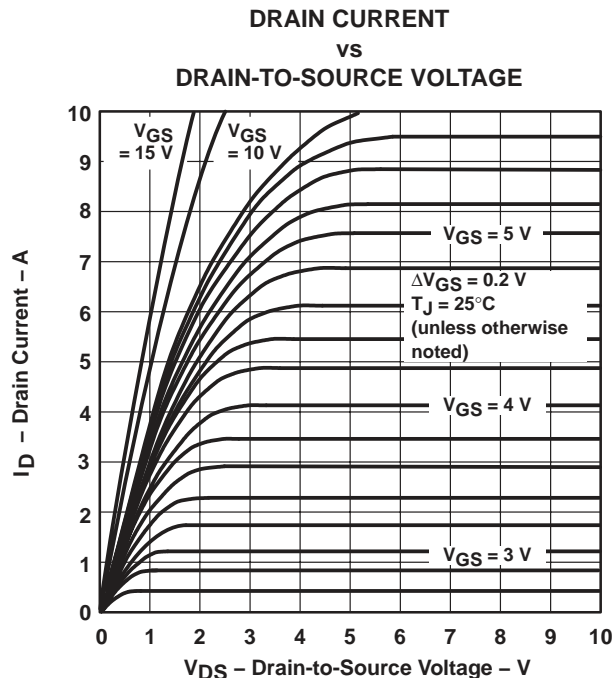
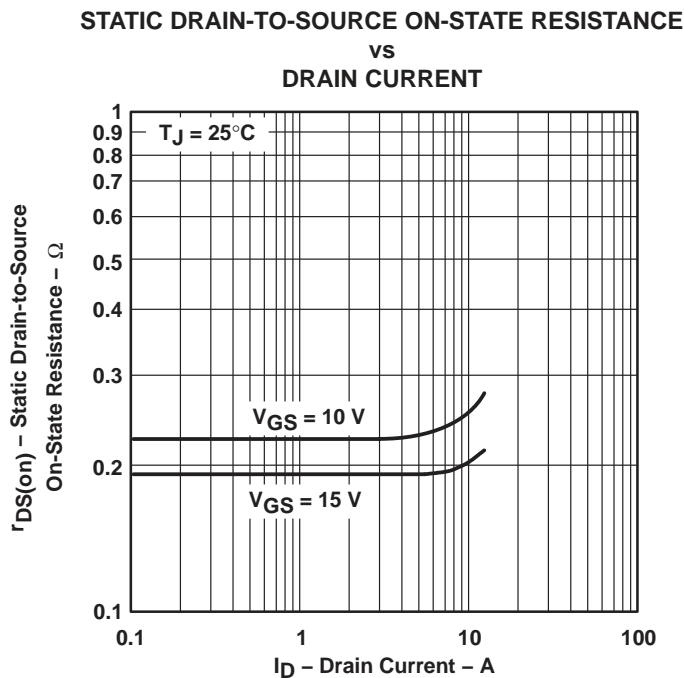
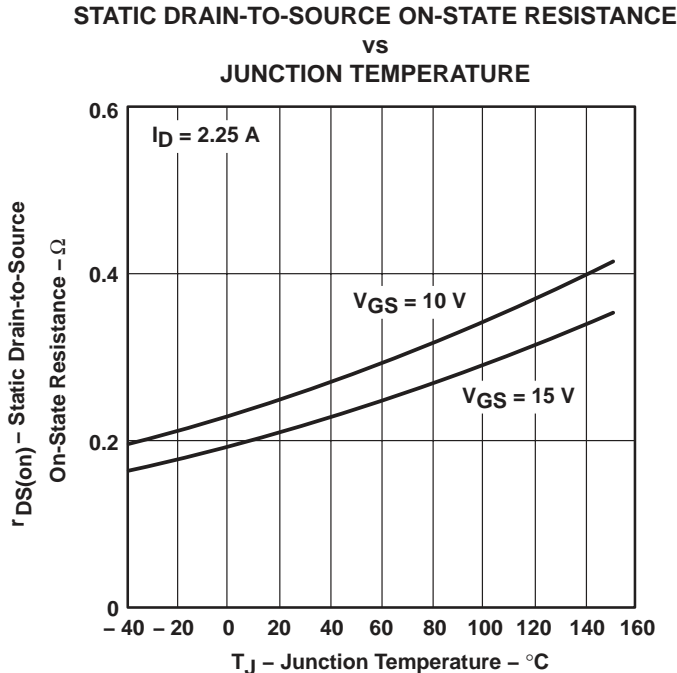
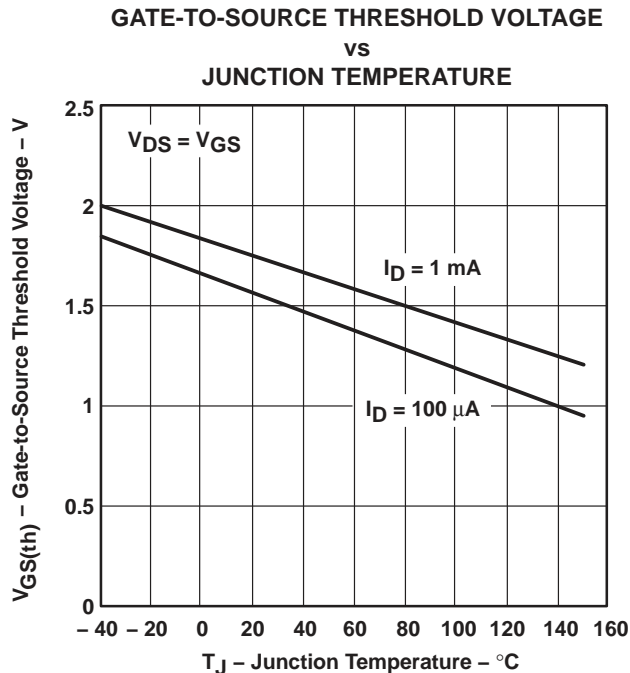


- NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_0 = 50 \Omega$ .  
 B. Input pulse duration ( $t_w$ ) is increased until peak current  $I_{AS} = 11.25$  A.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 17.2 \text{ mJ.}$$

**Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms**

**TYPICAL CHARACTERISTICS**



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## TYPICAL CHARACTERISTICS

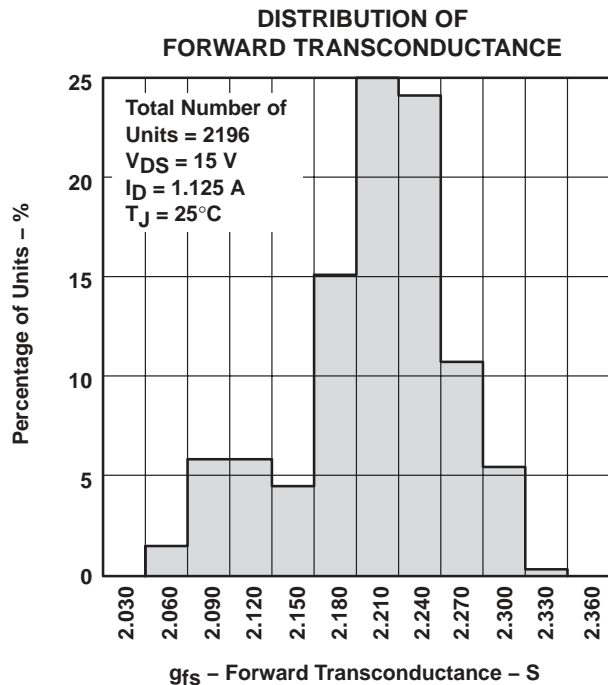


Figure 9

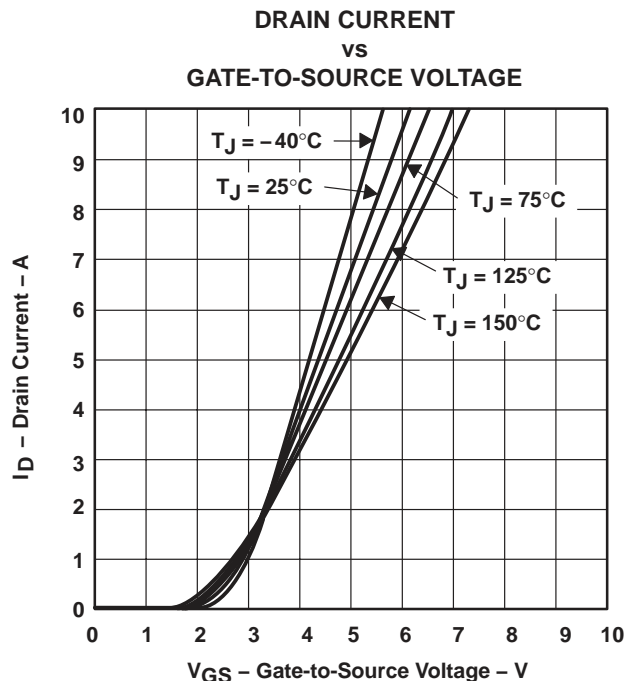


Figure 10

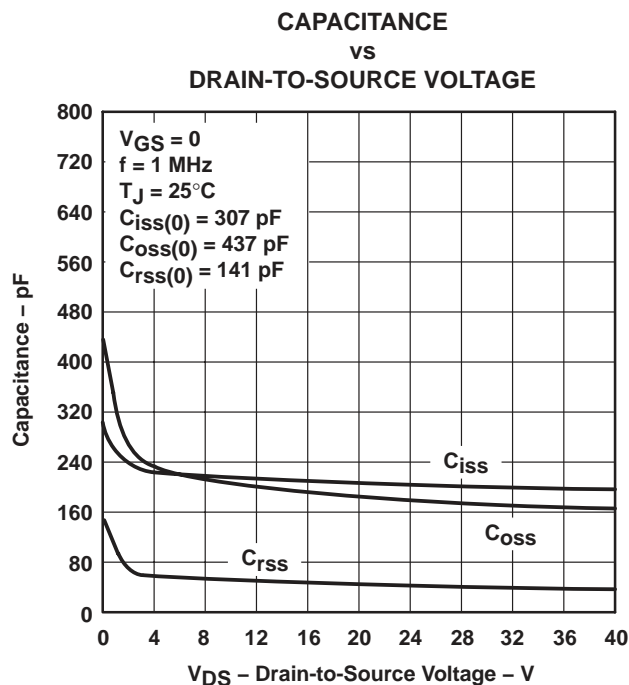


Figure 11

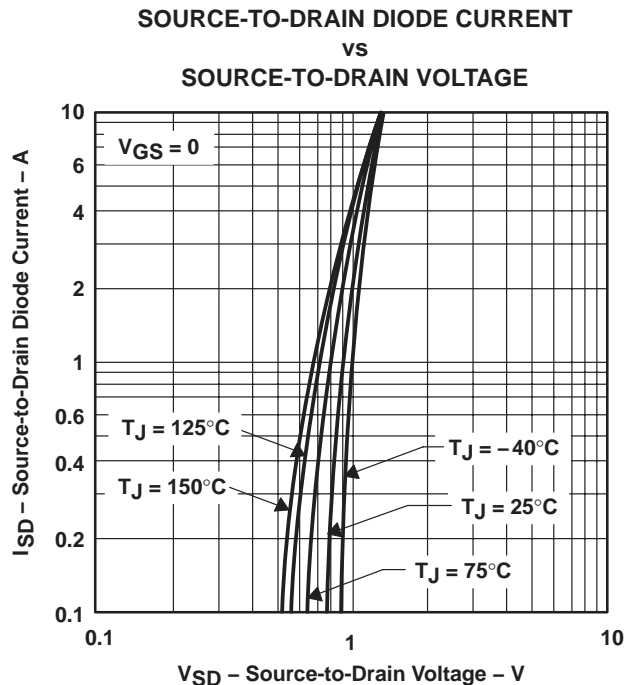


Figure 12



**TYPICAL CHARACTERISTICS**

**DRAIN-TO-SOURCE VOLTAGE AND**  
**GATE-TO-SOURCE VOLTAGE**

vs  
**GATE CHARGE**

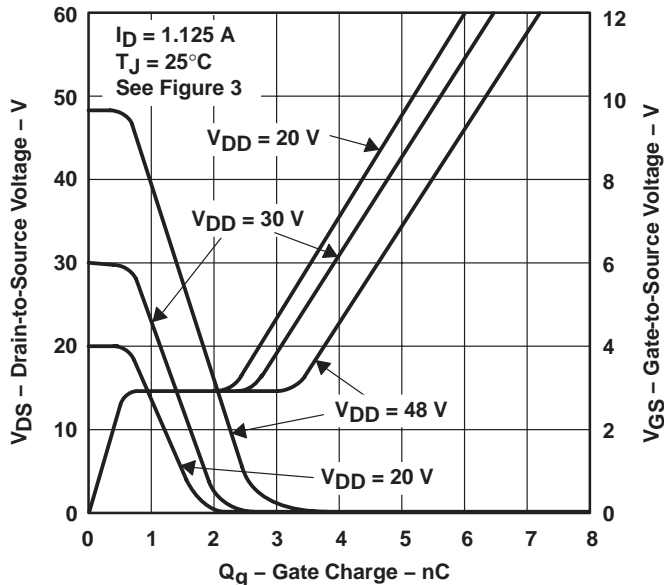


Figure 13

**REVERSE RECOVERY TIME**

vs  
**REVERSE  $di/dt$**

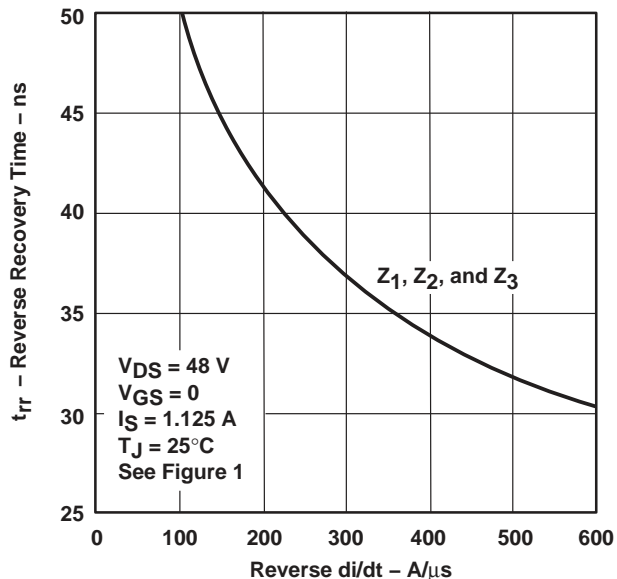


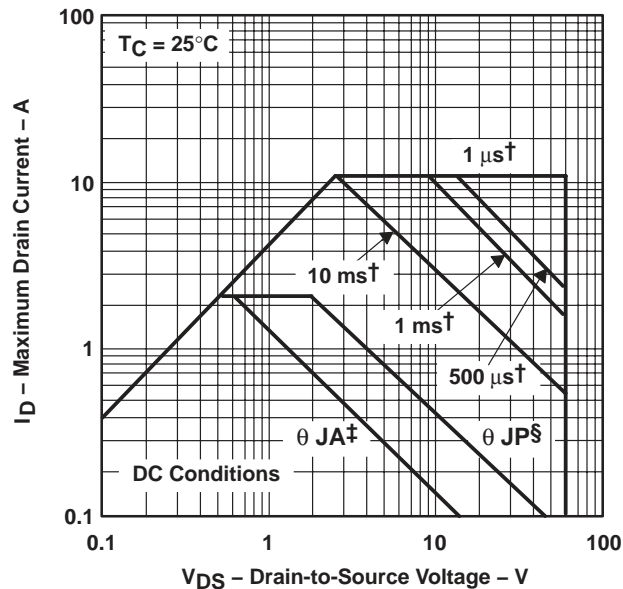
Figure 14

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**THERMAL INFORMATION**

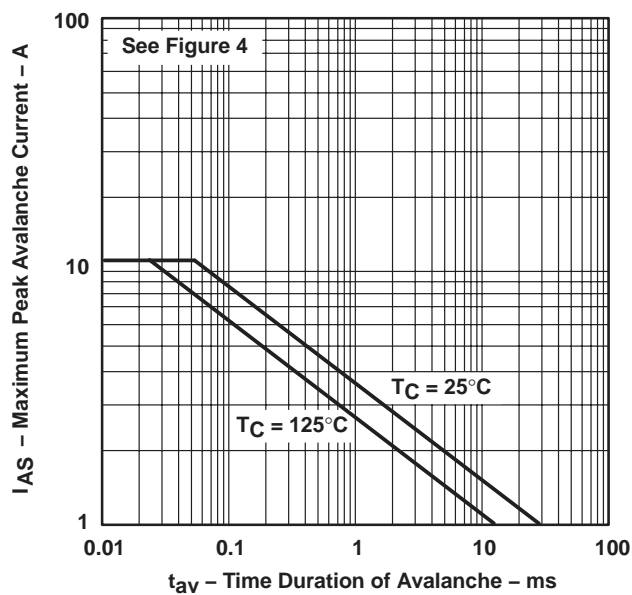
**MAXIMUM DRAIN CURRENT**  
**vs**  
**DRAIN-TO-SOURCE VOLTAGE**



† Less than 2% duty cycle  
 ‡ Device mounted on FR4 printed-circuit board with no heatsink.  
 § Device mounted in intimate contact with infinite heatsink.

**Figure 15**

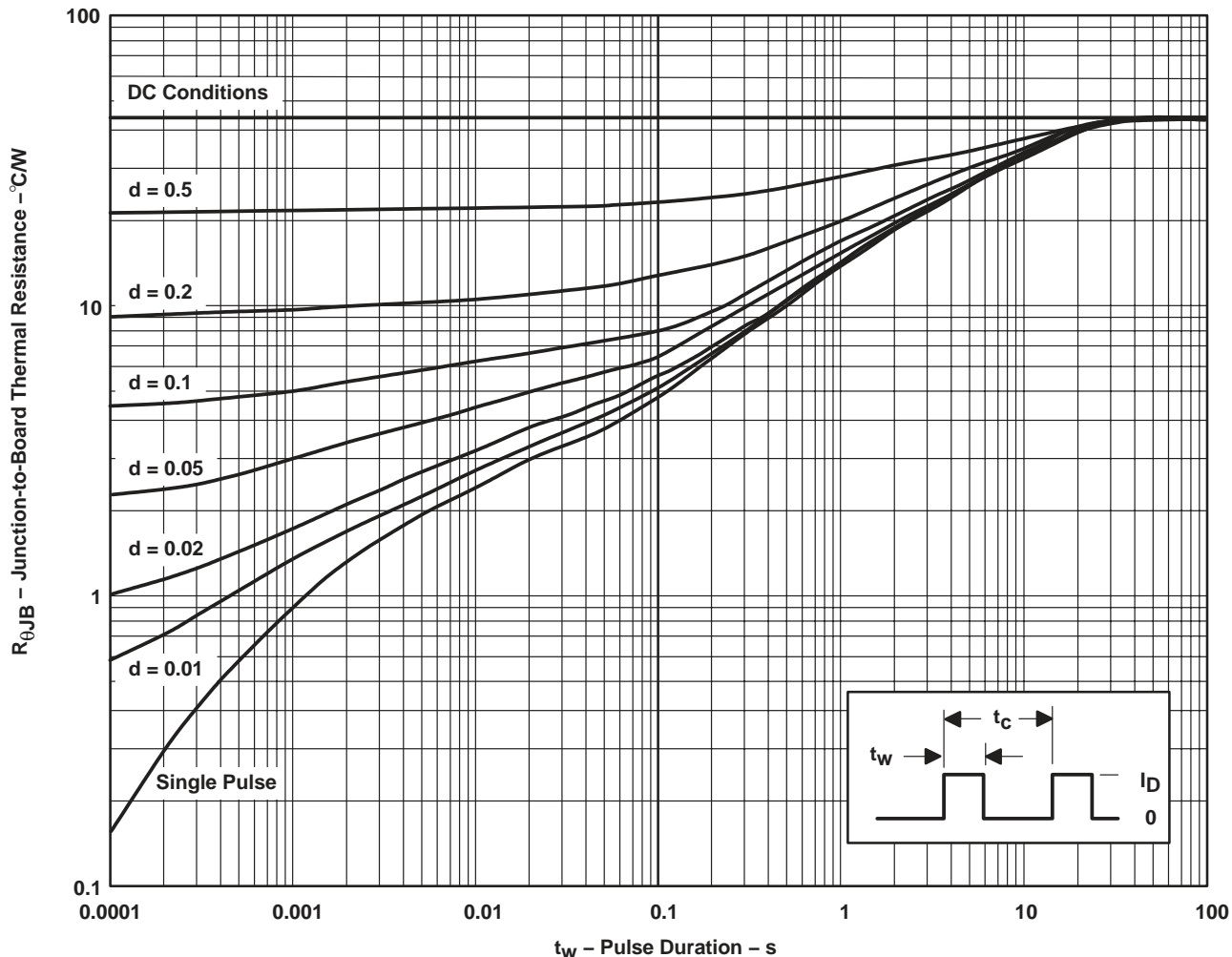
**MAXIMUM PEAK AVALANCHE CURRENT**  
**vs**  
**TIME DURATION OF AVALANCHE**



**Figure 16**

**THERMAL INFORMATION**

**DW PACKAGE†**  
**JUNCTION-TO-BOARD THERMAL RESISTANCE**  
**VS**  
**PULSE DURATION**



† Device mounted on 24 in<sup>2</sup>, 4-layer FR4 printed-circuit board with no heatsink

NOTE A.  $Z_{\theta B}(t) = r(t) R_{\theta JB}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

**Figure 17**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC1301DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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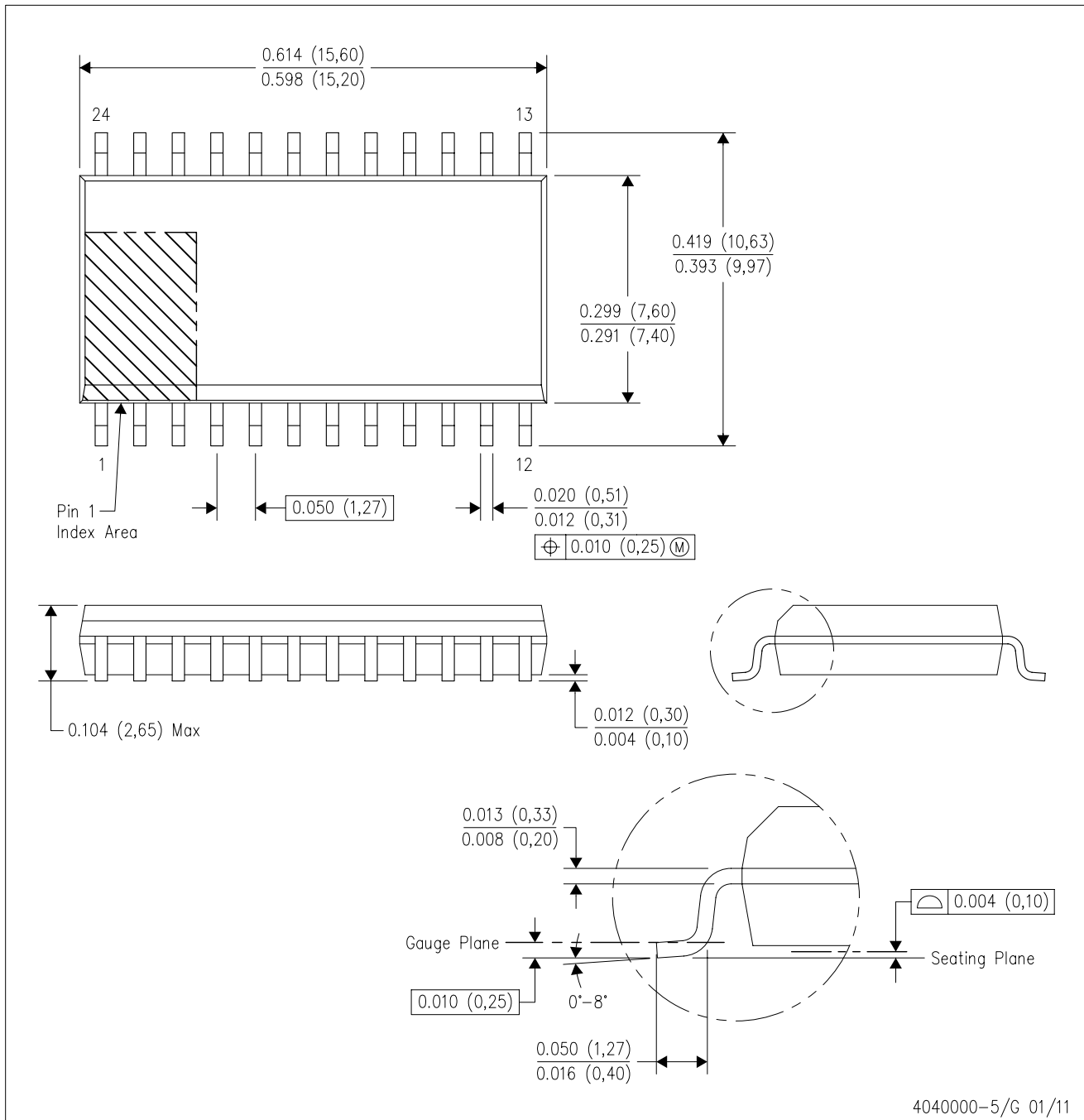
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

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