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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY7C1079DV33

32-Mbit (4 M × 8) Static RAM

Features

- High Speed
  - t_{AA} = 12 ns
- Low Active Power
  - I_{CC} = 250 mA at 12 ns
- Low CMOS Standby Power
  - I_{SB2} = 50 mA
- Operating Voltages of 3.3 ± 0.3 V
- 2.0 V Data Retention
- Automatic Power Down when Deselected
- TTL Compatible Inputs and Outputs
- Available in Pb-free 48-ball FBGA Package

Functional Description

The CY7C1079DV33 is a high performance CMOS Static RAM organized as 4,194,304 words by 8 bits.

To write to the device, take Chip Enable ($\overline{CE}$ [1]) and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{21}).

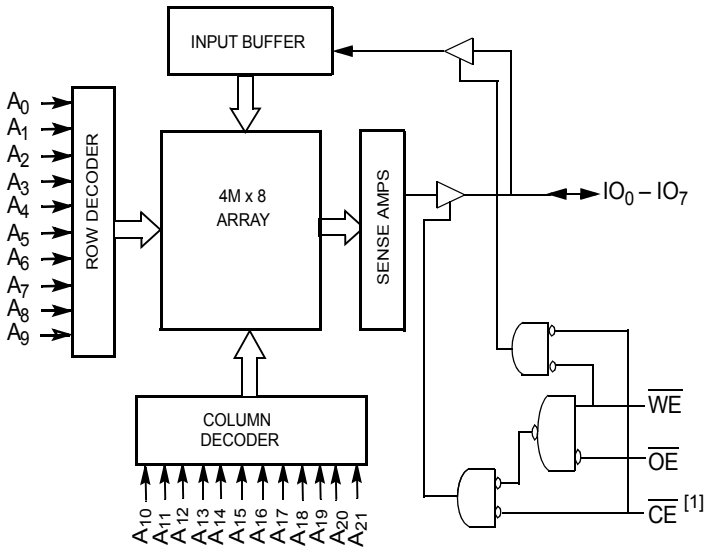
To read from the device, take Chip Enable ($\overline{CE}$ [1]) LOW and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See Truth Table (Single Chip Enable) on page 10 for a complete description of Read and Write modes.

The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ [1] HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ [1] LOW and $\overline{WE}$ LOW).

The CY7C1079DV33 is available in a 48-ball FBGA package.

For a complete list of related documentation, click here.

Logic Block Diagram



Note

1. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE_1}$ and CE_2 such that when $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.

Contents

Selection Guide

Description	-12	Unit
Maximum Access Time	12	ns
Maximum Operating Current	250	mA
Maximum CMOS Standby Current	50	mA

Pin Configuration

Figure 1. 48-ball FBGA (Single Chip Enable) pinout [2]

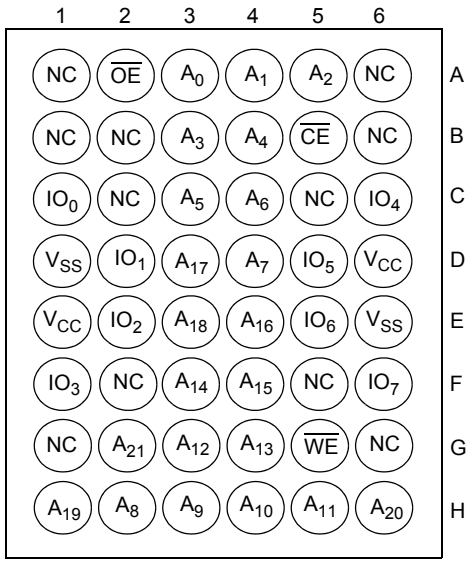
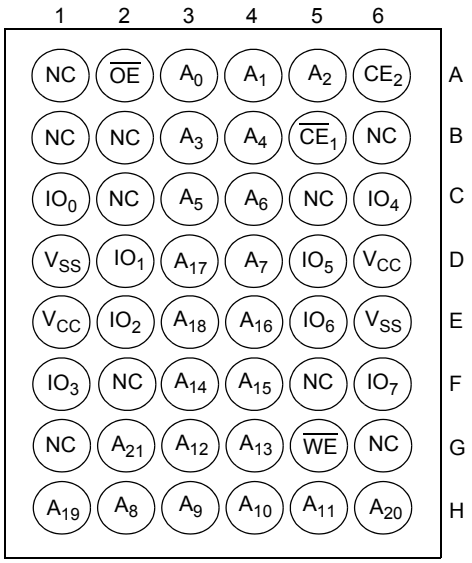


Figure 2. 48-ball FBGA (Dual Chip Enable) pinout [2]



Note
2. NC pins are not connected to the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND [3] .....–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State [3] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [3] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-12		Unit
			Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage [3]		–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$, I_{OUT} = 0 mA CMOS levels	–	250	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ [4] ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	60	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ [4] ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	–	50	mA

Notes

3. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 2 V for pulse durations of less than 20 ns.
4. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE_1}$ and CE_2 such that when $\overline{CE_1}$ is LOW and CE_2 is HIGH, CE is LOW. For all other cases CE is HIGH.

Capacitance

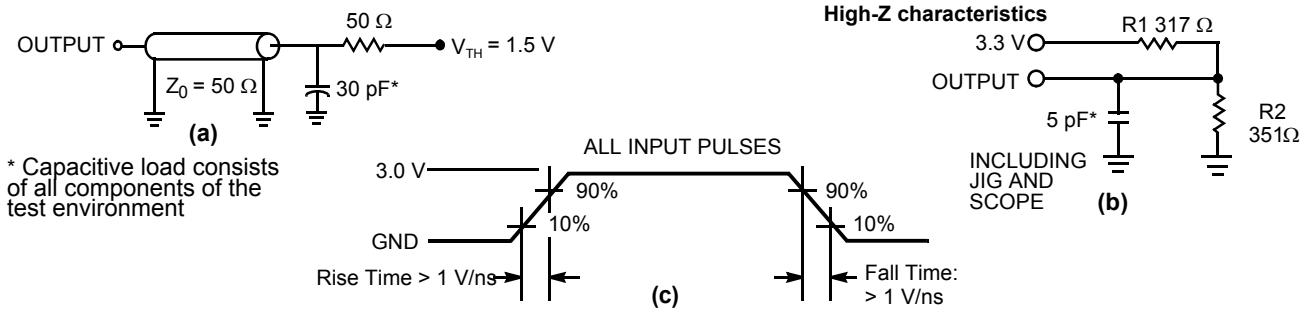
Parameter [5]	Description	Test Conditions	48-ball FBGA	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	16	pF
C_{OUT}	I/O capacitance		20	pF

Thermal Resistance

Parameter [5]	Description	Test Conditions	48-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	30.91	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13.60	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [6]



Notes

5. Tested initially and after any design or process changes that may affect these parameters.
6. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.

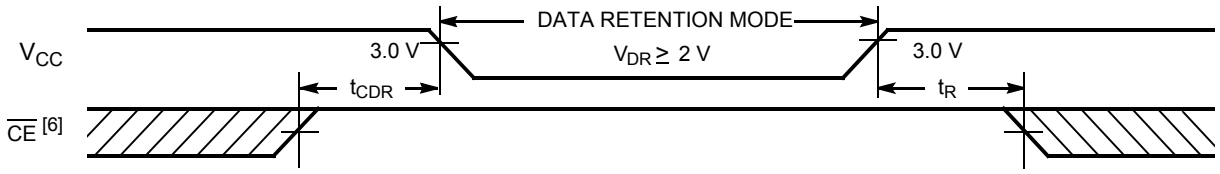
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention		2	–	–	V
I_{CCDR}	Data Retention Current	V_{CC} = 2 V, $\overline{CE}$ [7] ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V	–	–	50	mA
t_{CDR} [8]	Chip Deselect to Data Retention Time		0	–	–	ns
t_R [9]	Operation Recovery Time		t_{RC}	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

7. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ ≥ 50 µs or stable at $V_{CC(min.)}$ ≥ 50 µs.

AC Switching Characteristics

Over the Operating Range

Parameter [10]	Description	-12		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(Typical) to the First Access [11]	100	–	µs
t_{RC}	Read Cycle Time	12	–	ns
t_{AA}	Address to Data Valid	–	12	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ [12] LOW to Data Valid	–	12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	1	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [13]	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [12, 13]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH LOW to High Z [12, 13]	–	7	ns
t_{PU}	$\overline{CE}$ LOW HIGH to Power Up [12, 14]	0	–	ns
t_{PD}	$\overline{CE}$ HIGH LOW to Power Down [12, 14]	–	12	ns
Write Cycle [15, 16]				
t_{WC}	Write Cycle Time	12	–	ns
t_{SCE}	$\overline{CE}$ [12] LOW HIGH to Write End	9	–	ns
t_{AW}	Address Setup to Write End	9	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	9	–	ns
t_{SD}	Data Setup to Write End	7	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [13]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [13]	–	7	ns

Notes

10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of Figure 3 on page 5, unless specified otherwise.
11. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
12. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
13. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 5. Transition is measured ±200 mV from steady state voltage.
14. These parameters are guaranteed by design and are not tested.
15. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. $\overline{CE}$ and $\overline{WE}$ are LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 [17, 18]

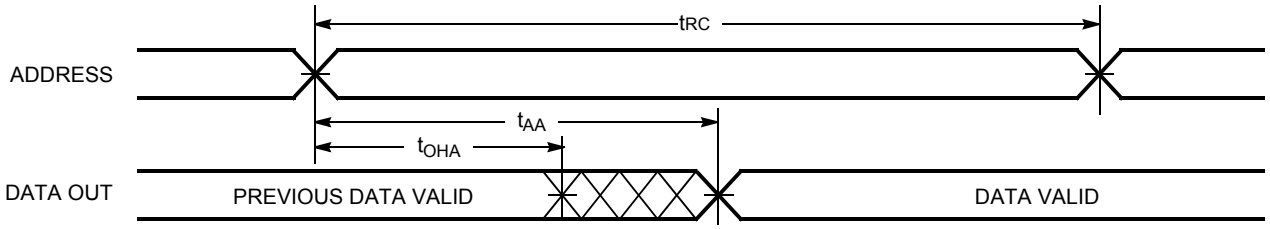
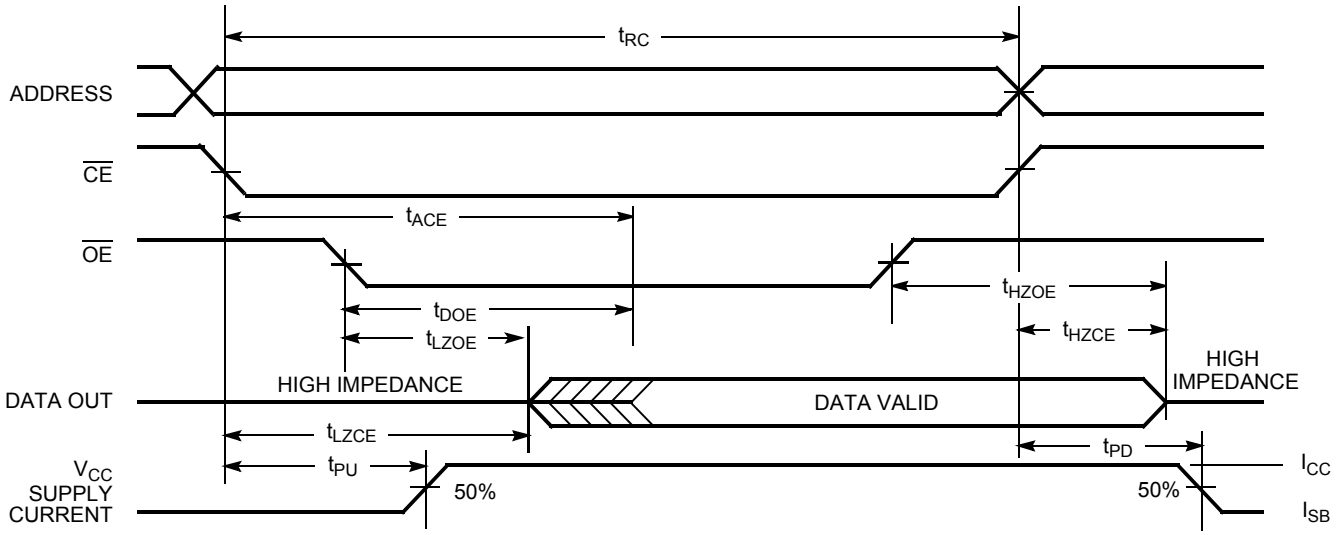


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [18, 19, 20]



Notes

17. The device is continuously selected. $\overline{CE} = V_{IL}$.
18. $\overline{WE}$ is HIGH for read cycle.
19. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, CE is LOW. For all other cases CE is HIGH.
20. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [21, 22, 23]

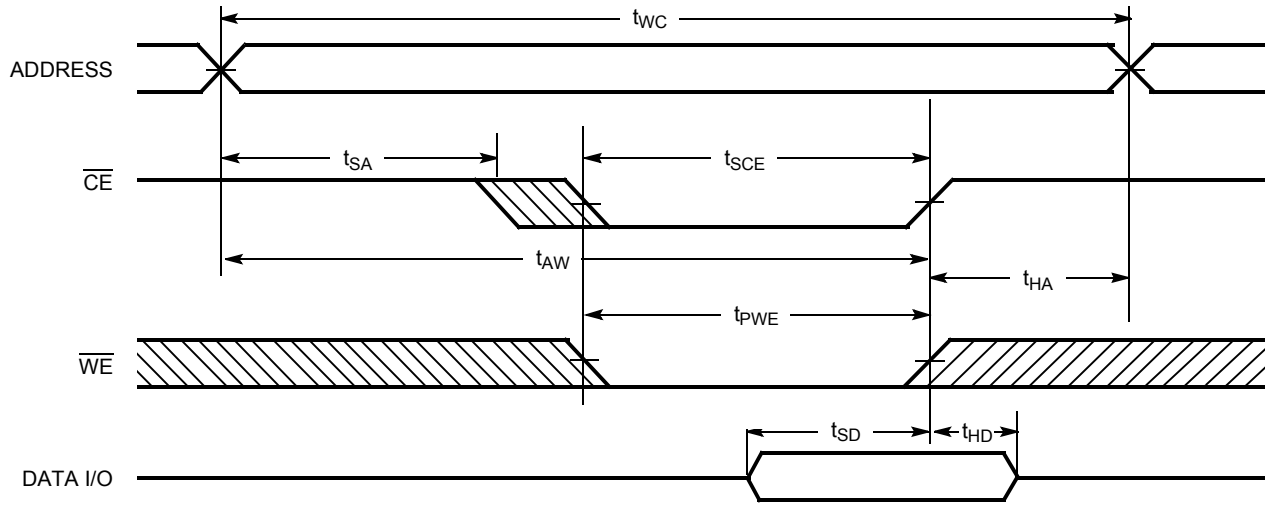
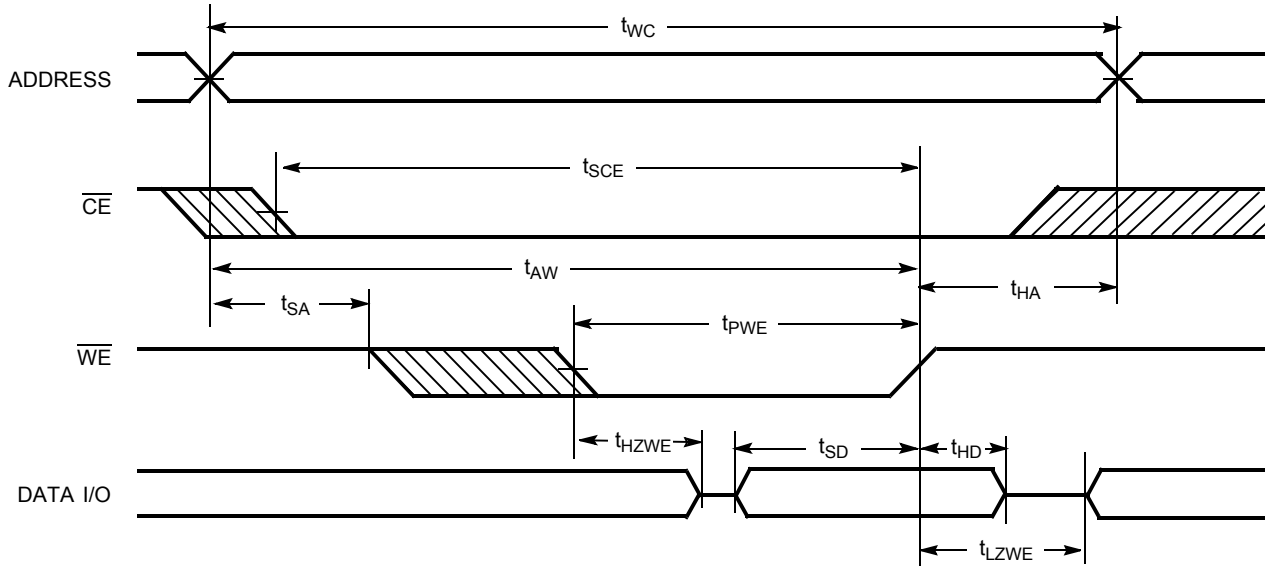


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [21, 22, 23]



Notes

21. BGA packaged device is offered in single CE and dual CE options. In this data sheet, for a dual CE device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.
22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
23. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Truth Table (Single Chip Enable)

$\overline{CE}$ [1]	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power Down	Standby (I_{SB})
L	L	H	Data Out	Read All Bits	Active (I_{CC})
L	X	L	Data In	Write All Bits	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Truth Table (Dual Chip Enable)

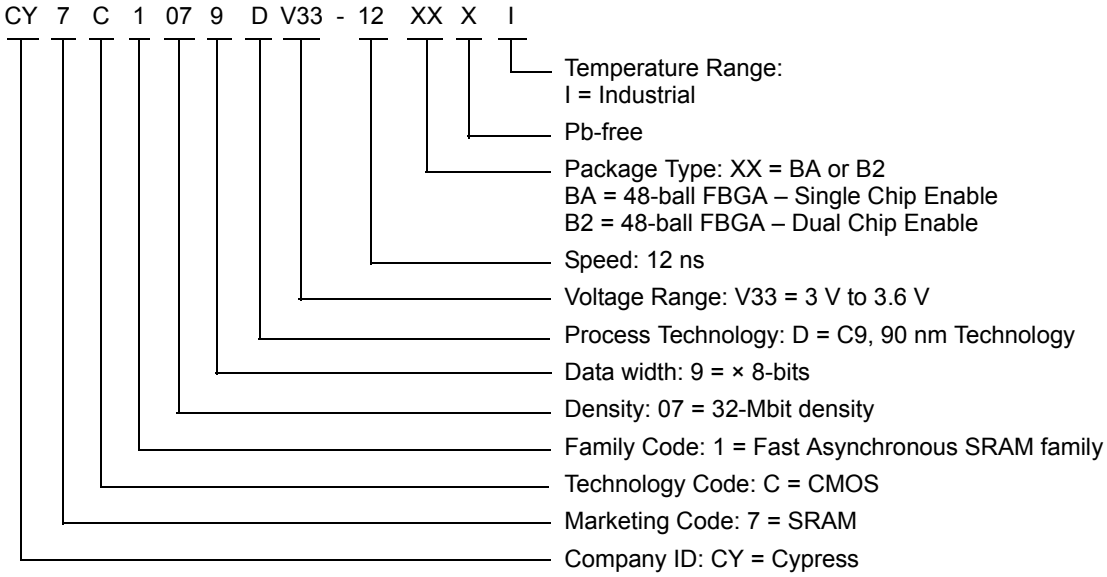
$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power Down	Standby (I_{SB})
X	L	X	X	High Z	Power Down	Standby (I_{SB})
L	H	L	H	Data Out	Read All Bits	Active (I_{CC})
L	H	X	L	Data In	Write All Bits	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1079DV33-12BAXI	51-85191	48-ball FBGA (8 × 9.5 × 1.2 mm) (Pb-free) [24]	Industrial

Contact sales for part availability.

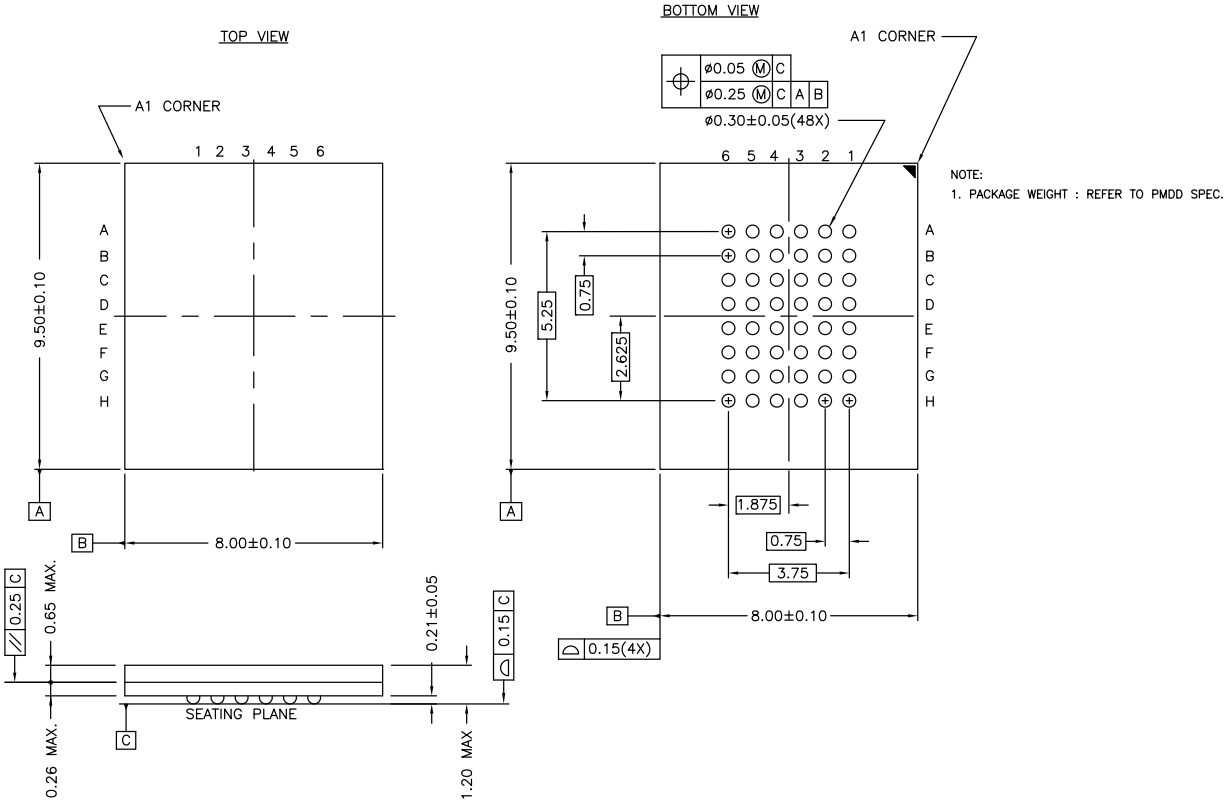
Ordering Code Definitions



Notes
24. This BGA package is offered with single chip enable.
25. This BGA package is offered with dual chip enable.

Package Diagrams

Figure 9. 48-ball FBGA (8 × 9.5 × 1.2 mm) BA48J Package Outline, 51-85191



51-85191 *C

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FPBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1079DV33, 32-Mbit (4 M × 8) Static RAM Document Number: 001-50282				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2711136	05/29/2009	VKN / PYRS	New data sheet.
*A	2759408	09/03/2009	VKN / AESA	Removed 10 ns speed bin related information across the document. Updated Thermal Resistance: Marked thermal specs as “TBD”. Updated AC Switching Characteristics: Changed maximum value of t_{DOE}, t_{HZOE}, t_{HZCE}, t_{HZWE} parameters from 6 ns to 7 ns. Updated Ordering Information: Added -12B2XI part (Dual CE option)
*B	2813370	11/23/2009	VKN	Updated DC Electrical Characteristics: Changed maximum value of I_{CC} parameter from 225 mA to 250 mA.
*C	3132969	01/11/2011	PRAS	Added Ordering Code Definitions under Ordering Information. Updated Package Diagrams. Added Acronyms and Units of Measure. Changed all instances of IO to I/O. Updated in new template.
*D	3232668	04/18/2011	PRAS	Changed status from Preliminary to Final. Updated Pin Configuration (Figure 2). Updated Thermal Resistance.
*E	4434923	07/09/2014	VINI	Updated Package Diagrams: spec 51-85191 – Changed revision from *A to *C. Updated in new template. Completing Sunset Review.
*F	4582593	11/28/2014	VINI	Added related documentation hyperlink in page 1. Removed missing part number CY7C1079DV33-12B2XI in Ordering Information.

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