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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY62146EV30 MoBL

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62146DV30
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in a Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin TSOP II Packages

Functional Description

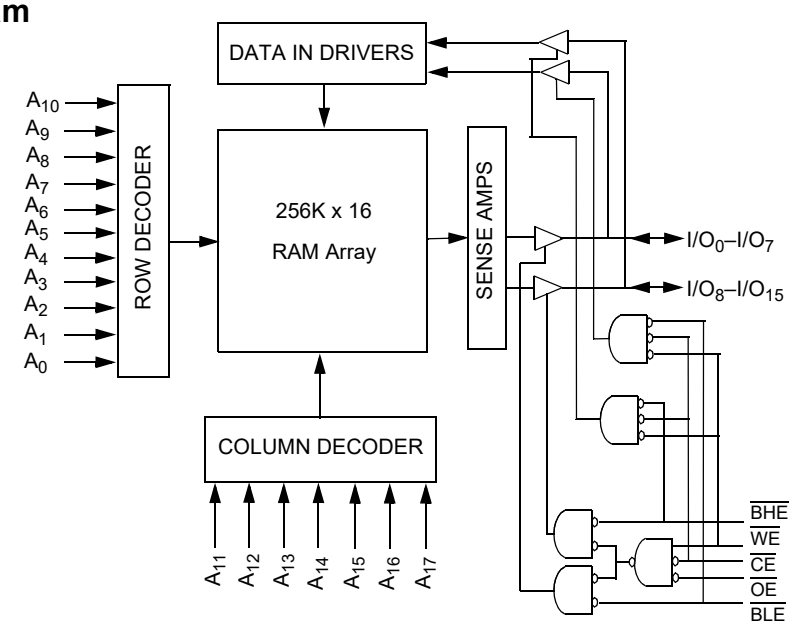
The CY62146EV30 is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features an advanced circuit design designed to provide an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 80 percent when addresses are not toggling.The device can also be put into standby mode reducing power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout [1, 2]

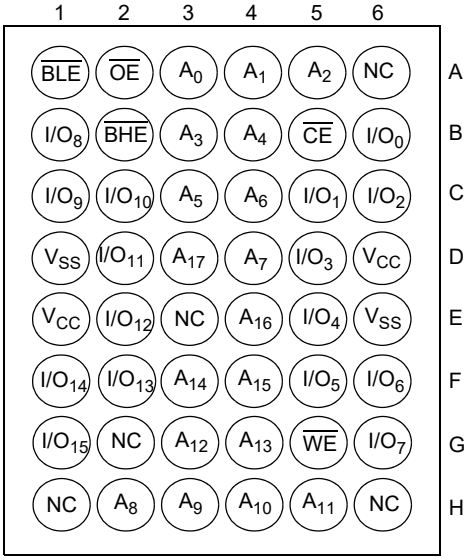
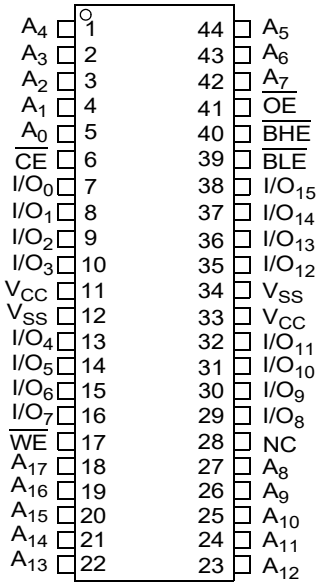


Figure 2. 44-pin TSOP II pinout [1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [3]	Max		Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62146EV30LL	Industrial/ Automotive-A	2.2	3.0	3.6	45	3.5	6	15	20	2.5	7

Notes
1. NC pins are not connected on the die.
2. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8Mb, 16Mb and 32Mb respectively.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.3 V to + 3.9 V (V_{CCmax} + 0.3 V)

DC voltage applied to outputs in High-Z state [4, 5] ..... –0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

DC input voltage [4, 5] ..... –0.3 V to 3.9 V ($V_{CC\ max}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [6]
CY62146EV30	Industrial/ Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial/Automotive-A)			Unit
				Min	Typ [7]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input high voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	$V_{CC} = V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	15	20	mA
		f = 1 MHz		–	3.5	6	
I_{SB1}	Automatic CE power down current – CMOS inputs	$\overline{CE}$ > V_{CC} – 0.2 V, V_{IN} > V_{CC} – 0.2 V or V_{IN} < 0.2 V, f = f_{max} (Address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	2.5	7	µA
I_{SB2} [8]	Automatic CE power down current – CMOS inputs	$\overline{CE} \geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	2.5	7	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{cc} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

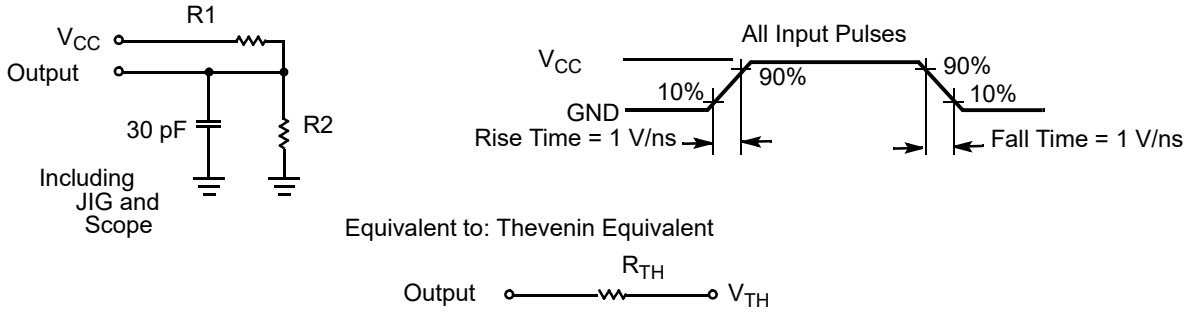
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	VFBGA	TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	42.10	55.52	°C/W
Θ_{JC}	Thermal resistance (junction to case)		23.45	16.03	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameter	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
9. Tested initially and after any design or process changes that may affect these parameters.

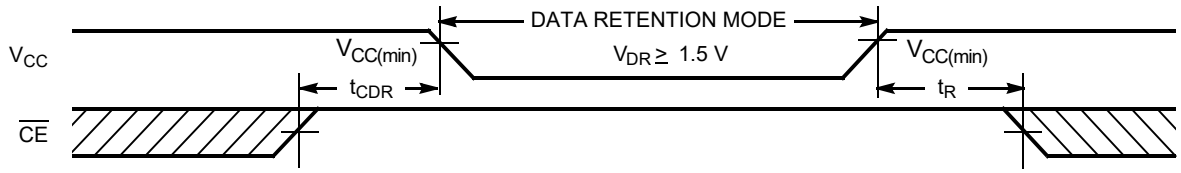
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial/ Automotive-A	–	3	8.8	µA
t_{CDR} [12]	Chip deselect to data retention time	–		0	–	–	ns
t_R [13]	Operation recovery time	–		45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industrial/Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z [16]	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z [16, 17]	–	18	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [16]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 3 on page 5.
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write
19. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) [20, 21]

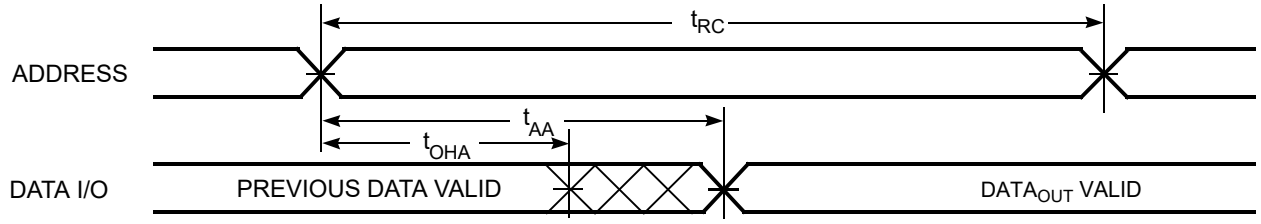
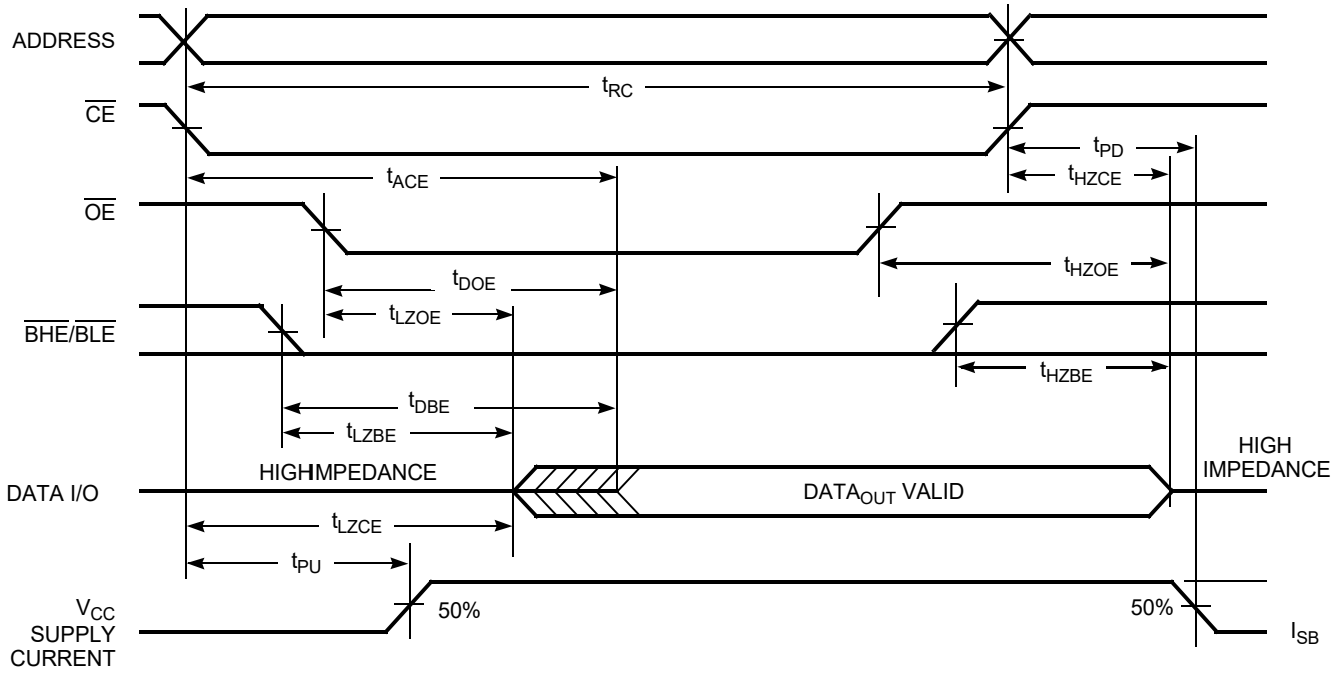


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [23, 24, 25]

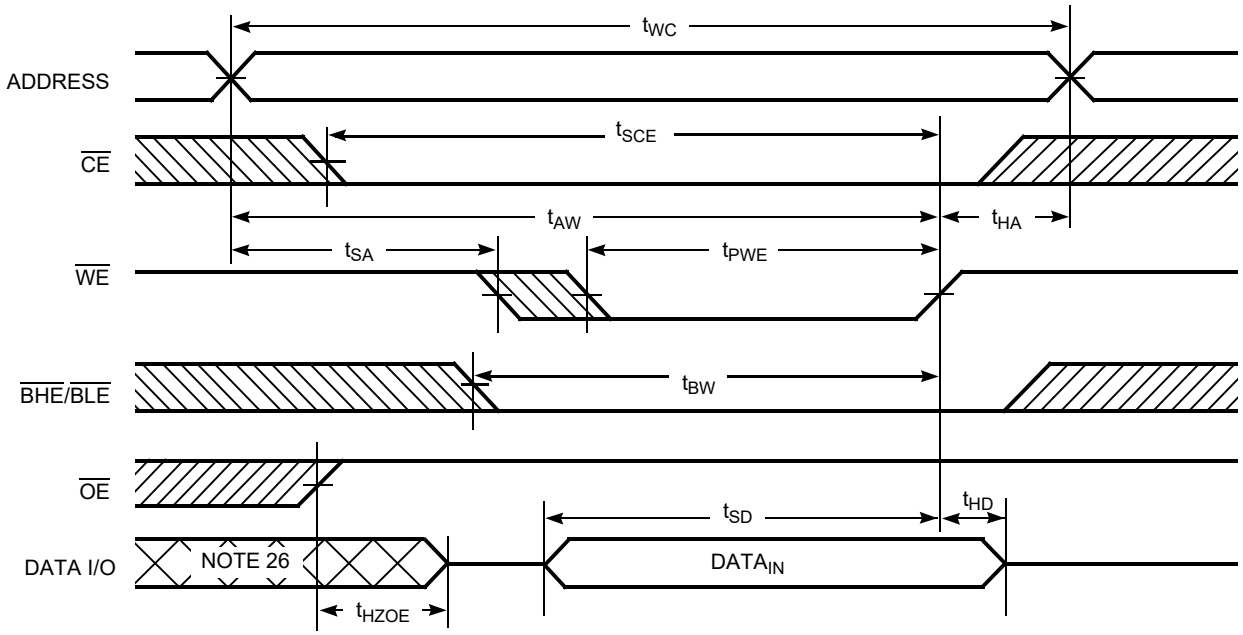
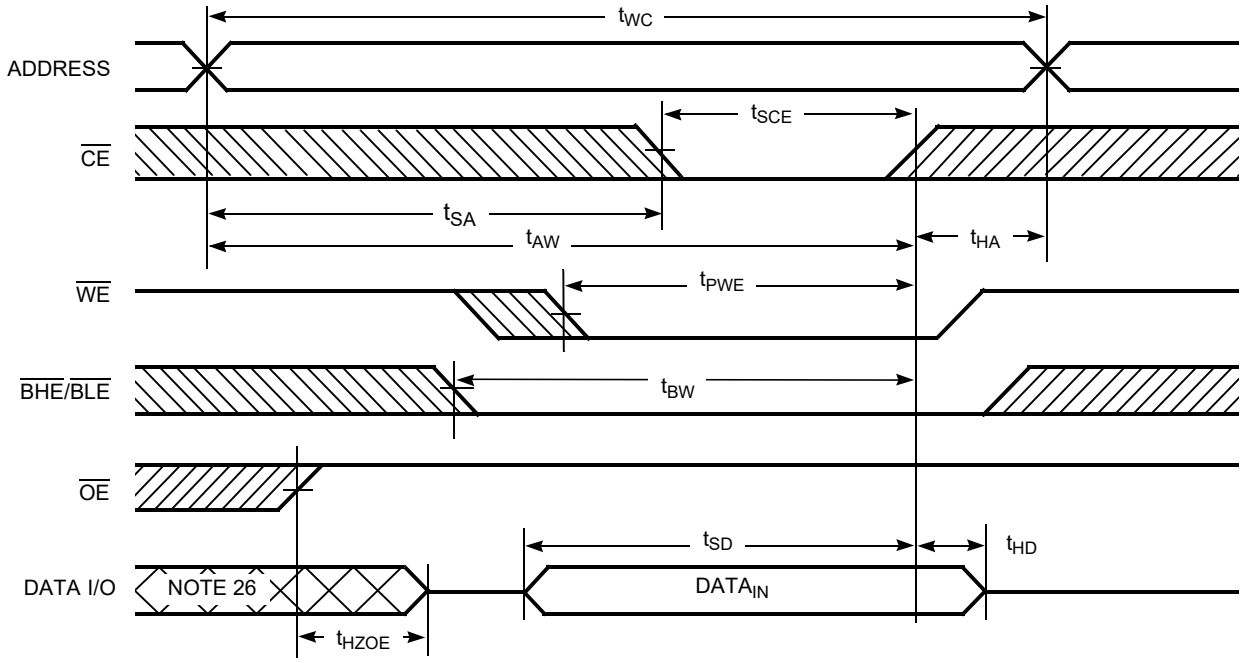


Figure 8. Write Cycle No. 2 ($\overline{CE}$ Controlled) [23, 24, 25]



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (WE Controlled, OE LOW) [27, 28]

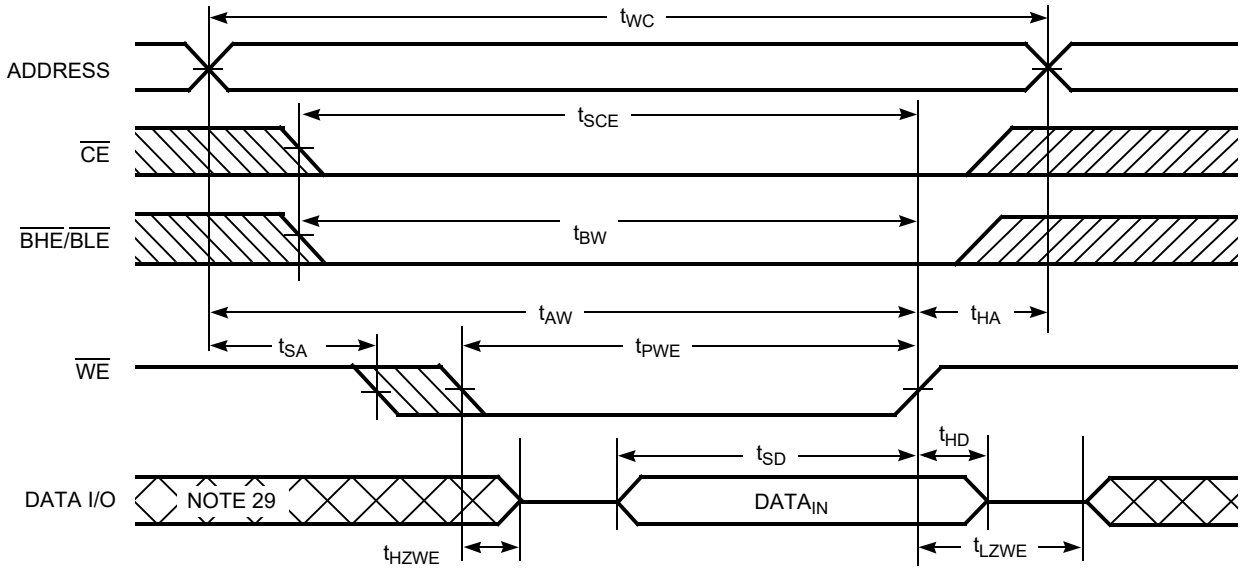
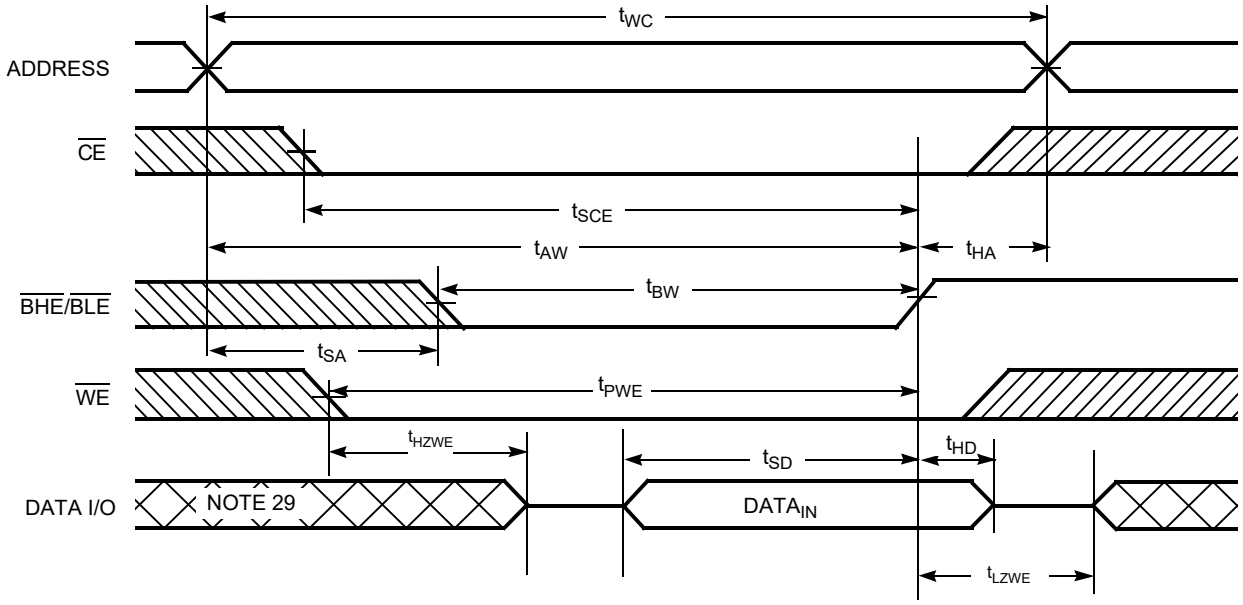


Figure 10. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [27]



Notes
27. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high impedance state.
28. The minimum write pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be sum of t_{HZWE} and t_{SD}.
29. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE}$ [30]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

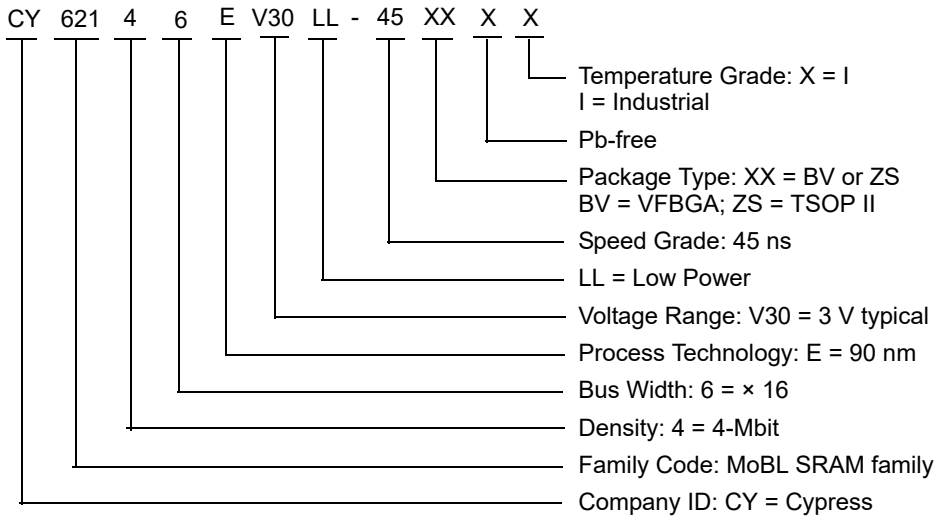
Note
30. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62146EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

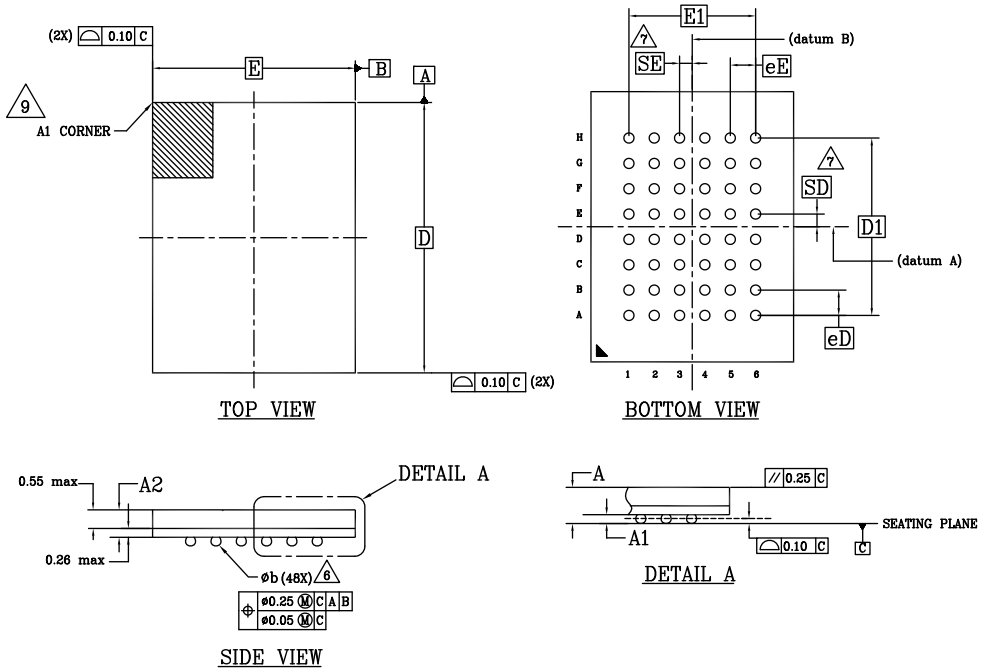
Please contact your local Cypress sales representative for availability of other parts

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

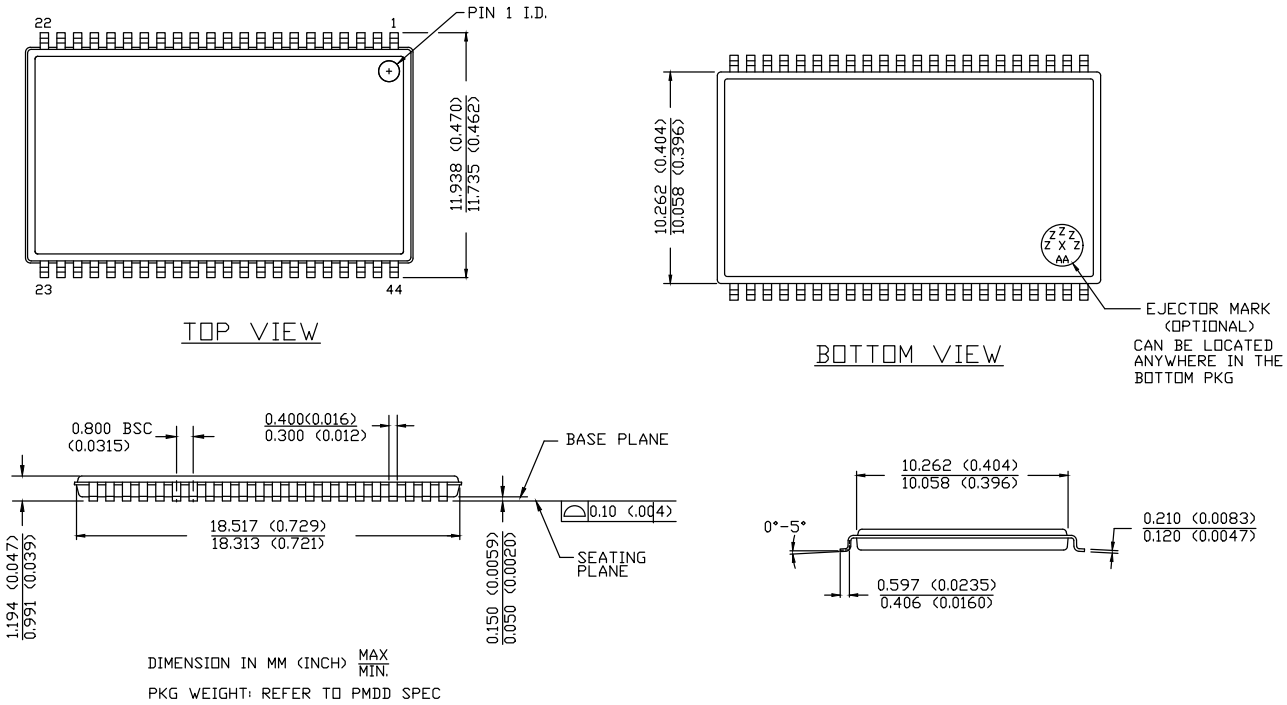
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Package Diagrams (continued)

Figure 12. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



51-85087 *F

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{CE}$	Chip Enable
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Gird Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146EV30 MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 38-05567			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	223225	05/05/2004	New data sheet.
*A	247373	07/28/2004	Changed status from Advance Information to Preliminary. Updated Operating Range: Updated Note 6 (Replaced “100 µs wait time” with “200 µs wait time”). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.0 µA to 2.5 µA. Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bin. Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE}, t_{HZBE}, and t_{HZWE} parameters from 12 ns to 15 ns corresponding 35 ns speed bin and from 15 ns to 18 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns corresponding to 35 ns speed bin and from 15 ns to 22 ns corresponding to 45 ns speed bin. Changed maximum value of t_{DBE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed minimum value of t_{SCE} and t_{BW} parameters from 25 to 30 ns corresponding to 35 ns speed bin and from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin and from 20 ns to 22 ns corresponding to 45 ns speed bin. Removed Note “If both Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are toggled together then this value is 6 ns min. Otherwise this value is 3 ns min.” and its reference in t_{LZBE} parameter. Updated Ordering Information: Updated part numbers.
*B	414807	12/16/2005	Changed status from Preliminary to Final. Removed “L” version of CY62146EV30 part in all instances across the document. Removed 35 ns speed bin related information in all instances across the document. Changed the address of Cypress Semiconductor Corporation in Page 1 from “3901 North First Street” to “198 Champion Court”. Updated Pin Configurations: Updated Figure 1 (Replaced DNU with NC corresponding to ball E3). Removed Note “DNU pins have to be left floating or tied to V_{SS} to ensure proper application.” and its reference. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 12 mA to 15 mA corresponding to 45 ns speed bin and Test Condition “f = f_{max}”. Changed typical value of I_{CC} parameter from 1.5 mA to 2 mA corresponding to 45 ns speed bin and Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2 mA to 2.5 mA corresponding to 45 ns speed bin and Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} parameter from 0.7 µA to 1 µA corresponding to 45 ns speed bin. Changed maximum value of I_{SB1} parameter from 2.5 µA to 7 µA corresponding to 45 ns speed bin. Changed typical value of I_{SB2} parameter from 0.7 µA to 1 µA corresponding to 45 ns speed bin. Changed maximum value of I_{SB2} parameter from 2.5 µA to 7 µA corresponding to 45 ns speed bin. Updated AC Test Loads and Waveforms: Updated Figure 3 (Replaced 50 pF with 30 pF).

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Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*B (cont.)	414807	12/16/2005	Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 2.5 µA to 7 µA. Added typical value of I_{CCDR} parameter. Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZCE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZBE} parameter from 6 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZWE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Updated Ordering Information: Updated part numbers. Removed “Package Name” column. Added “Package Diagram” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *B to *D. Updated to new template.
*C	925501	04/09/2007	Updated Electrical Characteristics: Added Note 8 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 11 and referred the same note in I_{CCDR} parameter. Updated Switching Characteristics: Added Note 15 and referred the same note in “Parameter” column.
*D	2678796	03/25/2009	Added Automotive-A Temperature Range related information in all instances across the document. Completing Sunset Review.
*E	2944332	06/04/2010	Updated Truth Table: Added Note 30 and referred the same note in “$\overline{CE}$” column. Updated Package Diagrams: spec 51-85150 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *A to *C. Updated to new template.
*F	3109050	12/13/2010	Changed all Table Footnotes to Notes in all instances across the document. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagrams: spec 51-85150 – Changed revision from *E to *F.
*G	3302915	07/14/2011	Updated Functional Description: Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.” at the end. Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions. Added Units of Measure. Updated to new template.

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Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*H	3961126	04/10/2013	Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *H. spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.
*I	4101995	08/22/2013	Updated Switching Characteristics: Updated Note 15. Updated to new template.
*J	4348752	04/16/2014	Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 28 and referred the same note in Figure 9 (for t_{PWE} parameter in $\overline{WE}$ Controlled, $\overline{OE}$ LOW Write Cycle). Completing Sunset Review.
*K	4576526	11/21/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*L	5233278	04/21/2016	Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Updated all values in “VFBGA” and “TSOP II” columns. Updated to new template. Completing Sunset Review.
*M	6029183	01/12/2018	Updated Ordering Information: Updated part numbers. Updated to new template.
*N	6560465	04/29/2019	Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I. Updated to new template. Completing Sunset Review.
*O	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to “f = 1 MHz”. Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to “f = 1 MHz”. Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition “f = 1 MHz”. Changed typical value of I_{SB1} parameter from 1 µA to 2.5 µA. Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 0.8 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagrams: spec 51-85087 – Changed revision from *E to *F. Updated to new template.

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