NCP6951B

Camera PMIC with Flash LED Driver

The NCP6951B integrated circuit is part of the ON Semiconductor mini power management IC family. It is optimized to supply battery powered portable application sub−systems such as camera function, microprocessors... etc. This device integrates one high efficiency 600 mA Step−down DCDC converter with DVS (Dynamic Voltage Scaling), 5 low dropout (LDO) voltage regulators and a 1.5 A Flash LED driver in WLCSP24 package.

Features

- One Flash LED Driver:
  - Adaptive boost supply or bypass mode depending on V_{in} and V_{flash} conditions
  - Programmable flash current from 100 mA to 1.6 A by 100 mA steps
  - Programmable safety and inhibit timer to limit the flash duration and protect the application
- One DCDC Converter:
  - Peak efficiency 96%
  - Programmable output voltage from 0.8 V to 2.3 V by 50 mV steps
  - 600 mA output current capability
- Five Low Noise − Low Dropout Regulators
  - Programmable output voltage from 1.7 V to 3.3 V for LDOs 1,2,3
  - Programmable output voltage from 1.2 V to 2.85 V for LDO 4 & 5
  - 200 mA output current capability: LDO's 1, 2, 3 & 4
  - 300 mA output current capability: LDO 5
  - 45 μVrms low output noise
- Control
  - 400 kHz / 3.4 MHz I^2C control interface
  - Hardware enable pin
  - Customizable power up sequencer
- Extended Input Voltage Range 2.5 V to 5.5 V
  - Support of newest battery technologies
- Optimized Power Efficiency
  - 82 μA very low quiescent current at no load
  - Dynamic voltage scaling on DCDC converter
  - Regulators can be supplied from DCDC converter output
- Small Footprint
  - Package WLCSP24 2.57 x 1.65 mm^2
  - DCDC converter runs at 3.0 MHz using a 1 μH inductor and 10 μF capacitor or 2.2 μH inductor and 4.7 μF capacitor

Typical Applications

- Cellular Phones
- Digital Cameras
- Personal Digital Assistant and Portable Media Player
- GPS

ON Semiconductor®

www.onsemi.com

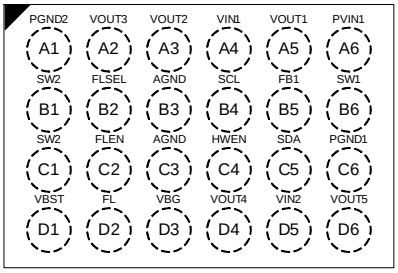
WLCSP24
CASE 567JA

MARKING DIAGRAM*

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

*Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 34 of this data sheet.

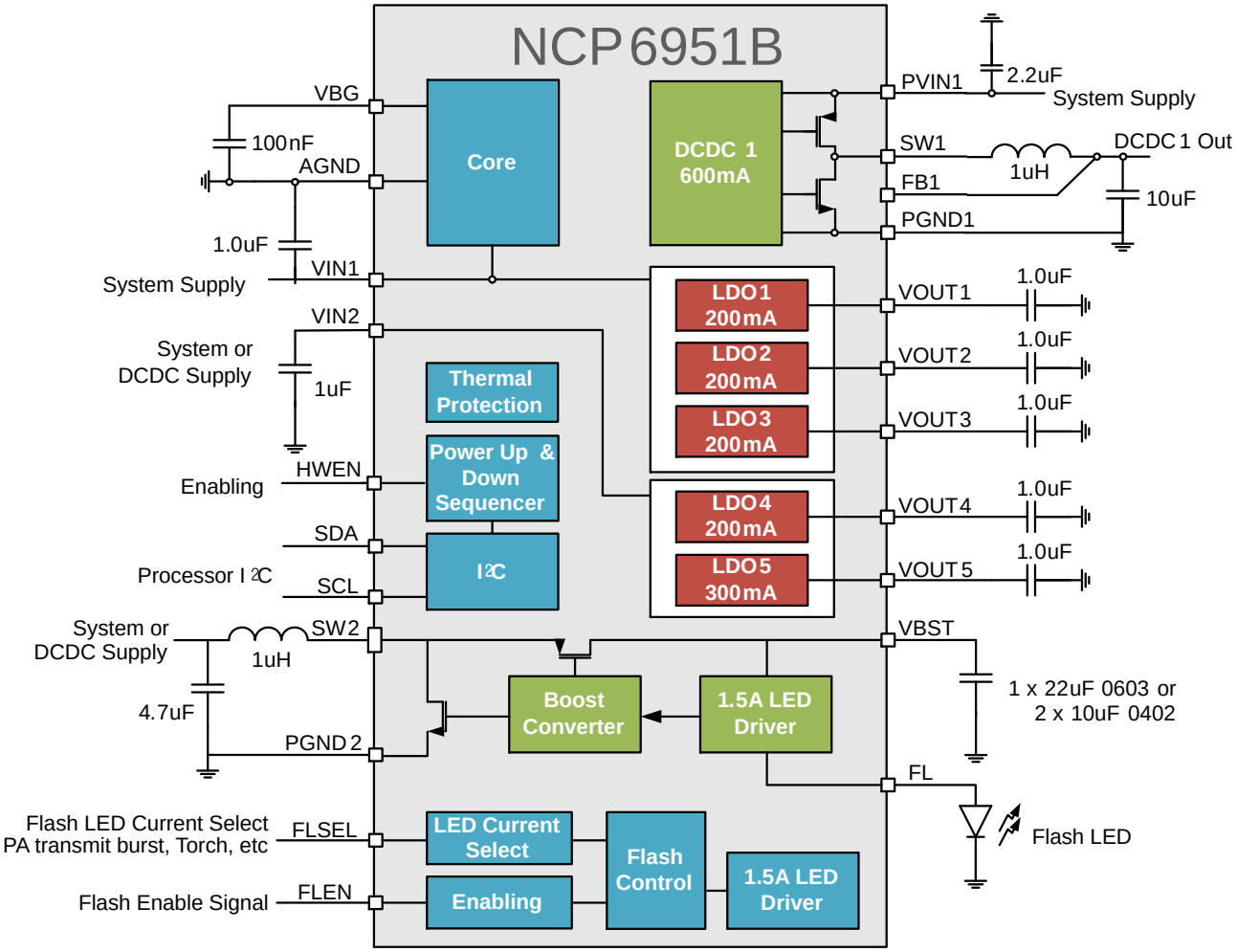


Figure 1. Functional Block Diagram

Table 1. PIN OUT DESCRIPTION

Pin	Name	Type	Description
POWER			
A4	VIN1	Power Input	Analog Supply. This pin is the device analog, digital and LDO 1, 2 & 3 supply. A 1.0 μF ceramic capacitor or larger must bypass this input to ground. This capacitor should be placed as close a possible to this pin.
D3	VBG	Analog Input	Reference Voltage. A 0.1 μF ceramic capacitor must bypass this pin to the ground
B3, C3	AGND	Analog Ground	Analog Ground. Analog and digital modules ground. Must be connected to the system ground.
CONTROL AND SERIAL INTERFACE			
C4	HWEN	Digital Input	Hardware Enable. Active high will enable the part; there is internal pull down resistor on this pin.
B4	SCL	Digital Input	I^2C interface **Clock**
C5	SDA	Digital Input/Output	I^2C interface **Data**
DCDC CONVERTER			
A6	PVIN1	Power Input	DCDC Power Supply. This pin must be decoupled to ground by a 2.2 μF ceramic capacitor. This capacitor should be placed as close a possible to this pin .
B6	SW1	Power Output	DCDC Switch Power. This pin connects power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
B5	FB1	Analog Input	DCDC Feedback Voltage. Must be connected to the output capacitor. This is the input to the error amplifier.
C6	PGND1	Power Ground	DCDC Power Ground. This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane is recommended.
LDO REGULATORS			
A4	VIN1	Power Input	LDO 1, 2 & 3 Power and Core supply (see Power table)
D5	VIN2	Power Input	LDO 4 & 5 Power Supply. This pin requires a 1 μF decoupling capacitor.
A5	VOUT1	Power Output	LDO 1 Output Power. This pin requires a 1 μF decoupling capacitor.
A3	VOUT2	Power Output	LDO 2 Output Power. This pin requires a 1 μF decoupling capacitor.
A2	VOUT3	Power Output	LDO 3 Output Power. This pin requires a 1 μF decoupling capacitor.
D4	VOUT4	Power Output	LDO 4 Output Power. This pin requires a 1 μF decoupling capacitor.
D6	VOUT5	Power Output	LDO 5 Output Power. This pin requires a 1 μF decoupling capacitor.
FLASH LED DRIVER			
D1	VBST	Power Output	Flash Led Driver Boost Output. This pin is the output of the boost converter. It requires a 10 μF decoupling capacitor.
B1, C1	SW2	Power Output	Flash Led Driver Switch Power. This pin connects power transistors to one end of the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information.
A1	PGND2	Power Ground	Flash Led Driver Power Ground. This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane is recommended.
D2	FL	Power Output	Flash Led Driver Output Power. This pin is the output of the current source of the flash LED driver. It needs a flash led to connect.
B2	FLSEL	Logic Input	Flash Led Driver Select Pin. Active high will select the reduced flash level.
C2	FLEN	Logic Input	Flash Led Driver Enable Pin. Active high will enable the flash mode.

Table 2. MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Analog and power pins: AVIN, PVIN, SW, VIN1, VIN2, VOUT1, VOUT2, VOUT3, VOUT4, VOUT5, FB, VBG Pins		V_A	−0.3 to + 6.0	V
Digital pins: SCL, SDA, HWEN Pin:	Input Voltage Input Current	V_{DG} I_{DG}	−0.3 to V_A +0.3 ≤ 6.0 10	V mA
Storage Temperature Range		T_{STG}	−65 to + 150	°C
Maximum Junction Temperature		T_{JMAX}	−40 to +150	°C
Moisture Sensitivity (Note 1)		MSL	Level 1	−
Human Body Model (HBM) ESD Rating (Note 2)		ESD_{HBM}	2000	V
Charged Device Model (CDM) ESD Rating (Note 2)		ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
2. This device series contains ESD protection and passes the following ratings:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114
   Charged Device Model (CDM) per JEDEC standard: JESD22−C101.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN1} PV_{IN}	Core Power Supply, DCDC power supply and LDOs 1, 2 & 3		2.5		5.5	V
V_{IN2}	LDOs 4 & 5 Input Voltage range		1.7		5.5	V
T_A	Ambient Temperature Range		−40	25	+ 85	°C
T_J	Junction Temperature Range (Note 6)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Case		−	80	−	°C/W
P_D	Power Dissipation Rating (Note 4)	T_A = 25°C	−	1250	−	mW
		T_A = 85°C	−	500	−	mW
L	Inductor for DCDC converter (Note 4)		1		2.2	μH
Co	Output Capacitor for DCDC Converter (Note 4)			10		μF
	Output Capacitors for LDO (Note 4)		0.65	1		μF
C_{BG}	Output Capacitors for V_{BG}			100		nF
Cpvin	Input Capacitor for DCDC Converter (Note 4)			2.2		μF
Cvin1	Input Capacitor for Vin1 (Note 4)			1		μF
Cvin2	Input Capacitor for Vin2 (Note 4)			1		μF
V_{FL}	LED Voltage	Lowest torch setting I_{FL} = 1 A I_{FL} = 1 A	2.0 2.8 3.3		 4.5 4.9	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
4. Refer to the Application Information section of this data sheet for more details.
5. The $R_{\theta CA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a NCP6951EVB board. It is a multilayer board with 1−ounce internal power and ground planes and 2−ounce copper traces on top and bottom of the board.
6. The maximum power dissipation (P_D) is dependent by input voltage, maximum output current and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}$$

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. PVIN = V_{IN1} = V_{IN2} = 3.6 V (Unless otherwise noted). DCDC Output Voltage = 1.2V, LDO1, 2 & 4= 2.8 V, LDO 3 & 5 = 1.8 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 9).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: Pins VIN1, VIN2, PVIN						
I_Q	Operating quiescent current	DCDC on – no load – no switching LDOs off T_A = up to +85°C	−	32	−	μA
		DCDC on – no load – no switching LDOs on – no load T_A = up to +85°C	−	80	−	
		DCDC Off LDOs on – no load T_A = up to +85°C	−	55	−	
I_{SLEEP}	Product sleep mode current	HWEN on All DCDC and LDOs off V_{IN} = 2.5 V to 5.5 V T_A = up to +85°C	−	6.0	−	μA
I_{OFF}	Product off current	HWEN off I^2C interface disabled V_{IN} = 2.5 V to 5.5 V T_A = up to +85°C	−	0.7	−	μA
DCDC CONVERTER						
PV_{IN}	Input Voltage Range		2.5	−	5.5	V
I_{OUTMAX}	Maximum Output Current		0.6	−	−	A
Δ_{VOUT}	Output Voltage DC Error	Io=300 mA, PWM mode (Note 9)	−1	0	1	%
DC_{OUT}	DCDC Output Voltage	Programmable 50 mV steps (Note 9)	0.8		2.3	V
F_{SW}	Switching Frequency		2.7	3	3.3	MHz
R_{ONHS}	P−Channel MOSFET ON Resistance	From PVIN1 to SW1 pins, Pvin1 = 3.6 V	−	185	−	mΩ
R_{ONLS}	N−Channel MOSFET ON Resistance	From SW1 to PGND1 pins, Pvin1 = 3.6 V	−	335	−	mΩ
I_{PK}	Peak Inductor Current	Open loop 2.5 V ≤ PV_{IN} ≤ 5.5 V	1.0	1.35	1.7	A
	Load Regulation	I_{OUT} from 300 mA to I_{OUTMAX}	−	−0.5	−	%/A
	Line Regulation	I_{OUT} = 100 mA 2.5 V ≤ V_{IN} ≤ 5.5 V	−	0	−	%/V
D	Maximum Duty Cycle		−	100	−	%
t_{START}	Soft−Start Time	From HWEN to 90% of Output Voltage (Note 10)	−	128		μs
$R_{DISDCDC}$	DCDC Active Output Discharge		−	7.0	−	Ω
LDO1, LDO2, LDO3						
V_{IN1}	LDO1, LDO2, LDO3 Input Voltage Range		2.5	−	5.5	V
$I_{OUTMAX1,2,3}$	Maximum Output Current		200	−	−	mA
$I_{LIM1,2,3}$	Output Current Limitation	(Note 9)	−	−	500	mA
$I_{SC1,2,3}$	Short Circuit Protection		−	130	−	mA
$V_{out1,2,3}$	Output Voltage	Programmable, see table. (Note 9)	1.7		3.3	V

7. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
8. Refer to the Application Information section of this data sheet for more details.
9. Guaranteed by design and characterized.
10. Tested in production at V_{OUT} = 2.0 V.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. PVIN = V_{IN1} = V_{IN2} = 3.6 V (Unless otherwise noted). DCDC Output Voltage = 1.2V, LDO1, 2 & 4= 2.8 V, LDO 3 & 5 = 1.8 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 9).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO1, LDO2, LDO3						
t_{START1}	Soft−Start Time	From HWEN to 90% of Output Voltage (Note 10)	−	128		μs
$\Delta V_{OUT1,2,3}$	Output Voltage Accuracy DC	$I_{OUT1,2,3}$ = 200 mA	−2	V_{NOM}	+2	%
	Load Regulation	$I_{OUT1,2,3}$ = 0 mA to 200 mA	−	0.4	−	%
	Line Regulation	V_{IN1} = (Vout + Drop) to 5.5 V $V_{OUT1,2}$ = 2.8 V, V_{OUT3} = 1.8 V $I_{OUT1,2,3}$ = 200 mA	−	0.3	−	%
V_{DROP}	Dropout Voltage	$I_{OUT1,2,3}$ = 200 mA, V_{OUT} = 3.3 V − 2%		135		mV
		$I_{OUT1,2,3}$ = 200 mA, V_{OUT} = 2.8 V − 2%	−	170	270	
PSRR	Ripple Rejection	F = 1 kHz, 100 mV peak to peak $V_{OUT1,2}$ = 2.8 V, V_{OUT3} = 1.8 V $I_{OUT1,2,3}$ = 5 mA	−	−70	−	dB
		F = 10 kHz, 100 mV peak to peak $V_{OUT1,2}$ = 2.8 V, V_{OUT3} = 1.8 V $I_{OUT1,2,3}$ = 5 mA	−	−60	−	
Noise		10 Hz → 100 kHz, 5 mA $V_{OUT1,2,3}$ = 2.8 V	−	45	−	μV
$R_{DISLDO1,2,3}$	LDO Active Output Discharge		−	15	−	Ω
LDO4 and LDO5						
V_{IN2}	LDO4 and LDO5 Input Voltage		1.7	−	5.5	V
$I_{OUTMAX4}$	Maximum Output Current		200	−	−	mA
$I_{OUTMAX5}$	Maximum Output Current		300	−	−	mA
I_{LIM4}	Output Current Limitation	(Note 9)	−	−	500	mA
I_{LIM5}	Output Current Limitation	(Note 9)	−	−	600	mA
I_{SC4}	Short Circuit Protection		−	130	−	mA
I_{SC5}	Short Circuit Protection		−	180	−	mA
$V_{out4,5}$	LDO 4&5 Output voltage	Programmable, see table. (Note 9)	1.2	−	2.85	V
t_{START2}	Soft−Start Time	Time from I^2C command ACK to 90% of Output Voltage.	−	128		μs
ΔV_{OUT4}	Output Voltage Accuracy	I_{OUT4} = 200 mA	−2	V_{NOM}	+2	%
ΔV_{OUT5}	Output Voltage Accuracy	I_{OUT5} = 300 mA	−2	V_{NOM}	+2	%
	Load Regulation	I_{OUT4} = 0 mA to 200 mA I_{OUT5} = 0 mA to 300 mA	−	0.4	−	%
	Line Regulation	V_{IN2} = (Vout + Drop) to 5.5 V V_{OUT4} = 2.8 V, V_{OUT5} = 1.8 V I_{OUT4} = 200 mA, I_{OUT5} = 300 mA	−	0.3	−	%

7. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
8. Refer to the Application Information section of this data sheet for more details.
9. Guaranteed by design and characterized.
10. Tested in production at V_{OUT} = 2.0 V.

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO4 and LDO5						
V_{DROP}	Dropout Voltage	I_{OUT4} = 200 mA V_{OUT4} = 2.8 V − 2%	−	170	270	mV
		I_{OUT5} = 300 mA V_{OUT5} = 2.8 V − 2%	−	120	220	
		I_{OUT5} = 300 mA V_{OUT5} = 1.8 V − 2%		250		
PSRR	Ripple Rejection	F = 1 kHz, 100 mV peak to peak $I_{OUT4=}$ 5 mA, $I_{OUT5=}$ 5 mA	−	−70	−	dB
		F = 10 kHz, 100 mV peak to peak $I_{OUT4,5=}$ 5 mA	−	−60	−	
Noise		10 Hz → 100 kHz, 5 mA $V_{OUT4,5}$ = 2.8 V	−	45	−	μV
$R_{DISLDO4,5}$	LDO 4&5 Active Output Discharge		−	15	−	Ω
FLASH LED DRIVER						
V_{IN}	Input Voltage	Pass through mode Boost mode	2.8 2.8		5.5 4.5	V
$UVLO_L$	UVLO low threshold	I^2C programmable with 150 mV steps (Note 9)	2.75		3.2	V
$UVLO_H$	UVLO high threshold	I^2C programmable with 150 mV steps (Note 9)	2.9		3.35	V
$UVLO_{acc}$	UVLO threshold accuracy		−50		50	mV
V_{BST}	Boost output voltage	(Note 9)	3.0		5.0	V
$V_{BST} - V_{FL}$	Driver headroom				350	mV
I_{FL}	Flash Current	I^2C programmable with 100 mA steps (Note 9)	100		1600	mA
I_{FLLOW}	Reduced Current	I^2C programmable with 100 mA steps (Note 9)	100		1600	mA
I_{TORCH}	Torch Current	I^2C programmable with 33 mA steps (Note 9)	33		533	mA
I_{FLACC}	Flash Current Accuracy	I_{FL} = 300 mA			8	%
$I_{TORCHACC}$	Torch Current Accuracy	I_{TORCH} = 100 mA			10	%
	Flash Current Slope	Ramp up or down		100/16		mA/μs
	Torch Current Slope	Ramp up or down		33/16		mA/μs
	PA Burst Blanking Speed	From flash to reduced setting		10		μs
F_{SW}	Boost Switching Frequency		1.8	2	2.2	MHz
R_{ON_H}	High−Side MOSFET ON Resistance			70		mΩ
R_{ON_L}	Low−Side MOSFET ON Resistance			60		mΩ
$I_{LIM-BOOST}$		I^2C programmable with 600 mA steps (Note 9)	1.8		3.6	A
I_{CCFL}	Short Circuit Detect Threshold			1.2		V

7. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
8. Refer to the Application Information section of this data sheet for more details.
9. Guaranteed by design and characterized.
10. Tested in production at V_{OUT} = 2.0 V.

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_J up to +125°C unless otherwise specified. PVIN = V_{IN1} = V_{IN2} = 3.6 V (Unless otherwise noted). DCDC Output Voltage = 1.2V, LDO1, 2 & 4= 2.8 V, LDO 3 & 5 = 1.8 V, Typical values are referenced to T_J = + 25°C and default configuration (Note 9).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HWEN, FLSEL, FLEN						
V_{IH}	High level input Voltage Threshold		1.1	−	−	V
V_{IL}	Low level Voltage Threshold		−	−	0.4	V
I_{PD}	Logic Pins Pull−down (input bias current)			0.1	1	μA
I^2C						
V_{I2C}	Voltage at SCL and SDA line		1.7	−	5.0	V
V_{I2CIL}	SCL, SDA low input voltage	SCL, SDA pin (Note 7)	−	−	0.5	V
V_{I2CIH}	SCL, SDA high input voltage	SCL, SDA pin (Note 7)	$0.8xV_{I^2C}$	−	−	V
V_{I2COL}	SCL, SDA low output voltage	I_{SINK} = 3 mA	−	−	0.4	V
F_{SCL}	I^2C clock frequency		−	−	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} rising	−	−	2.5	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} falling	60	−	200	mV
T_{SD}	Thermal Shut Down Protection		−	150	−	°C
$T_{WARNING}$	Warning Rising Edge		−	135	−	°C
T_{SDH}	Thermal Shut Down Hysteresis		−	15	−	°C

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9. Guaranteed by design and characterized.
10. Tested in production at V_{OUT} = 2.0 V.

TYPICAL CHARACTERISTICS

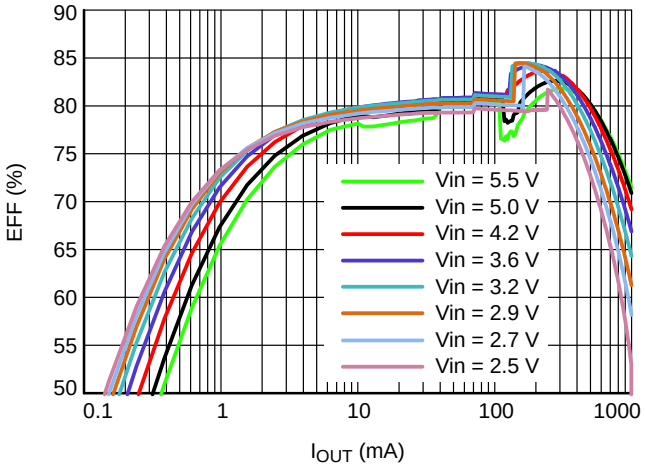


Figure 2. DCDC1 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 0.8 V

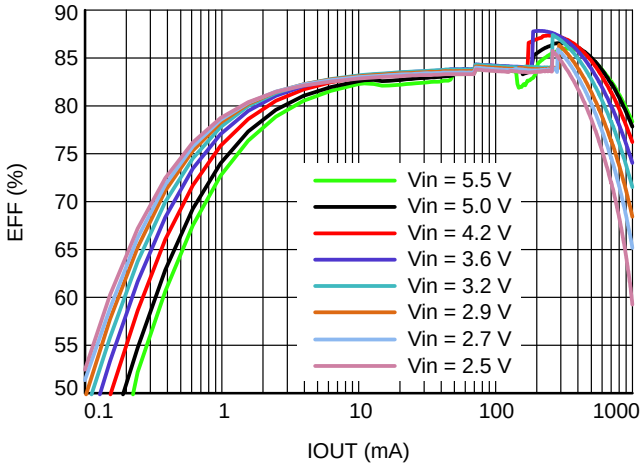


Figure 3. DCDC1 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 1.2 V

TYPICAL CHARACTERISTICS

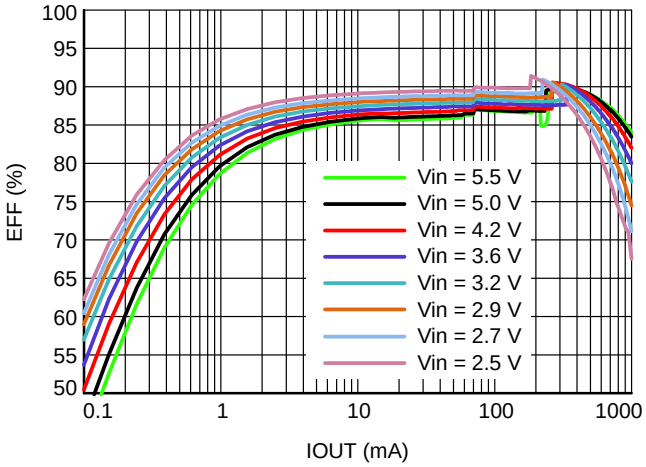


Figure 4. DCDC1 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 1.8 V

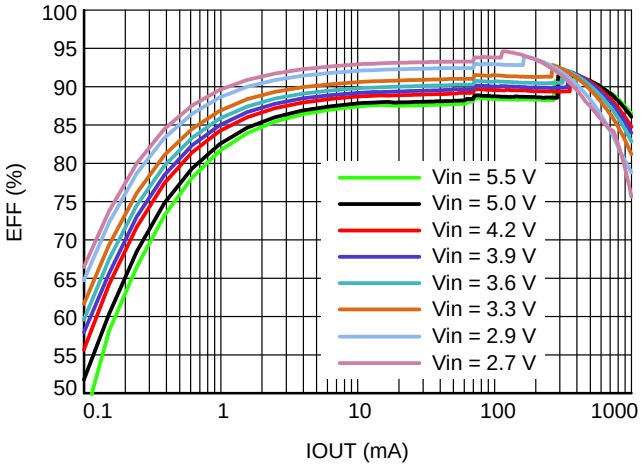


Figure 5. DCDC1 Efficiency vs. I_{OUT} (auto mode) V_{OUT} = 2.3 V

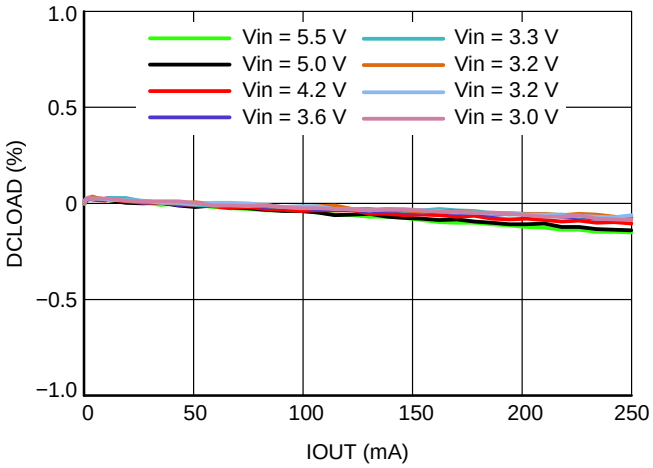


Figure 6. LDO1 Load Regulation (V_{OUT} = 2.8 V)

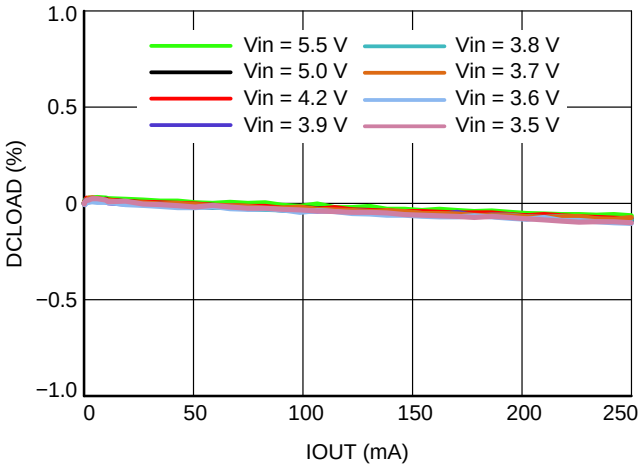


Figure 7. LDO1 Load Regulation (V_{OUT} = 3.3 V)

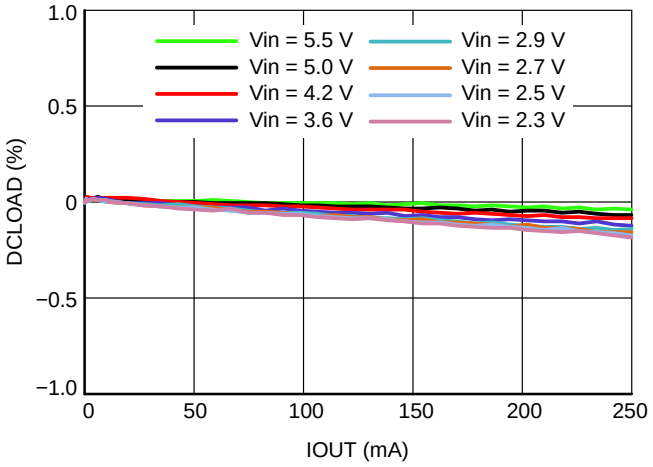


Figure 8. LDO1 Load Regulation (V_{OUT} = 1.8 V)

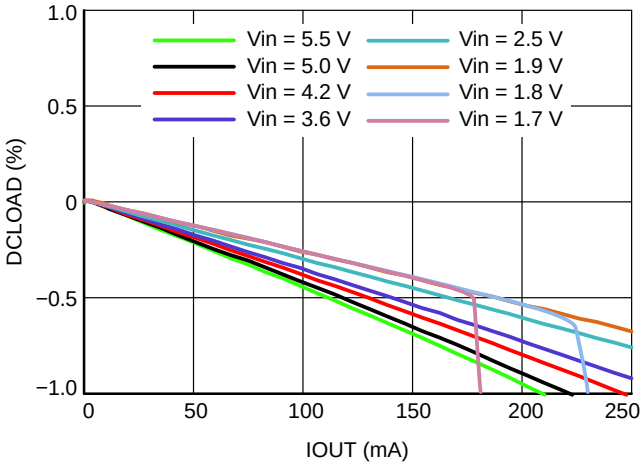


Figure 9. LDO1 Load Regulation (V_{OUT} = 1.2 V)

TYPICAL CHARACTERISTICS

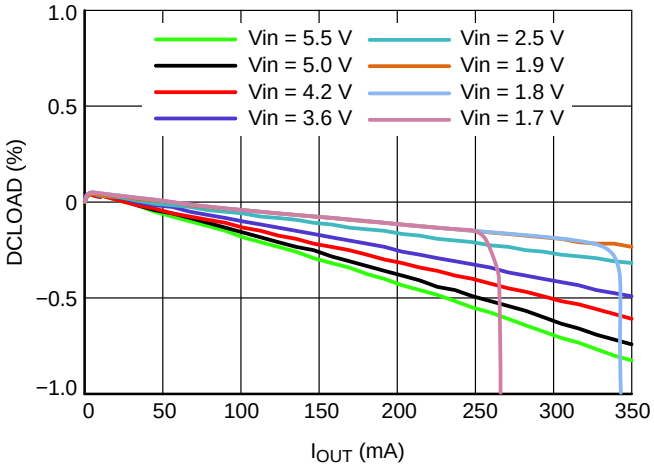


Figure 10. LDO5 Load Regulation (V_{OUT} = 1.2 V)

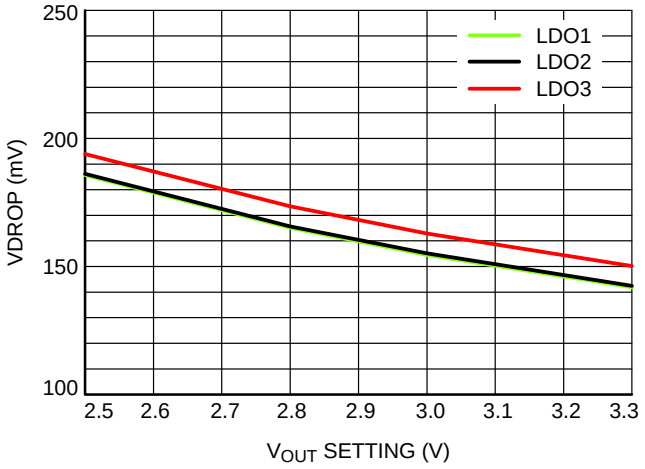


Figure 11. Dropout Voltage vs. V_{OUT}, LDO1, 2 & 3 (I_{OUT} = 200 mA)

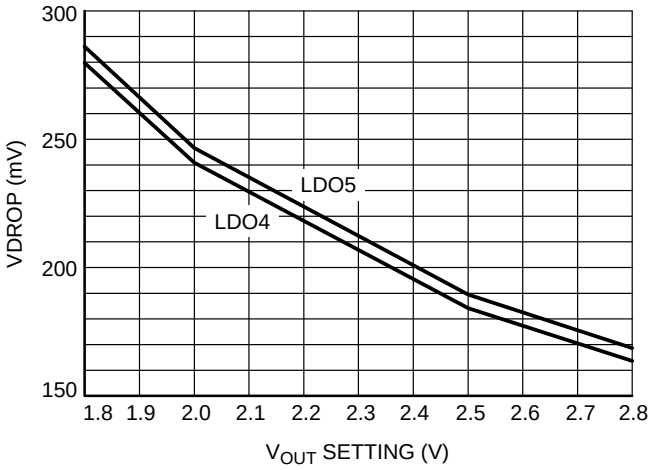


Figure 12. Dropout Voltage vs. V_{OUT}, LDO4 & 5 (I_{OUT} = 200 mA for LDO4 and 300 mA for LDO5)

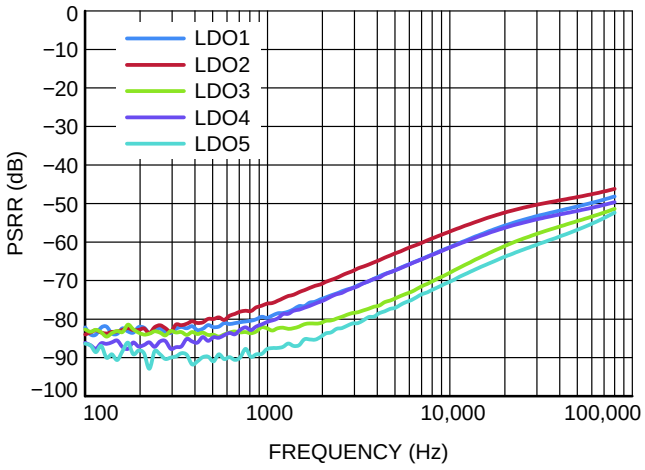


Figure 13. LDOx PSRR (V_{IN} = 3.6 V − V_{OUT} − 1.8 V − I_{OUT} = 5 mA)

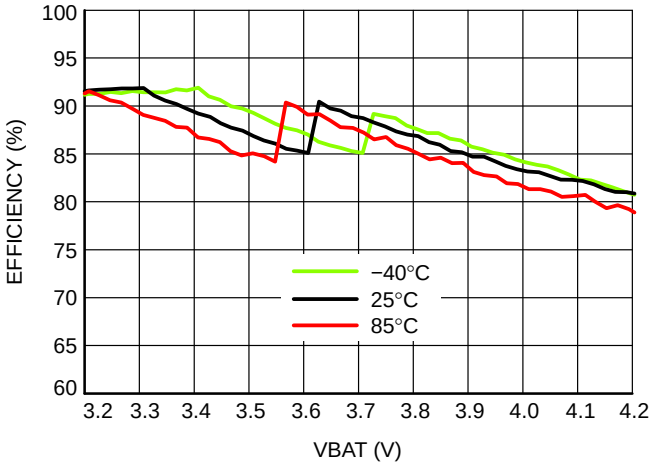


Figure 14. Flash LED Efficiency vs. Input Voltage (I_{FLASH} = 700 mA, V_{IN} Falling)

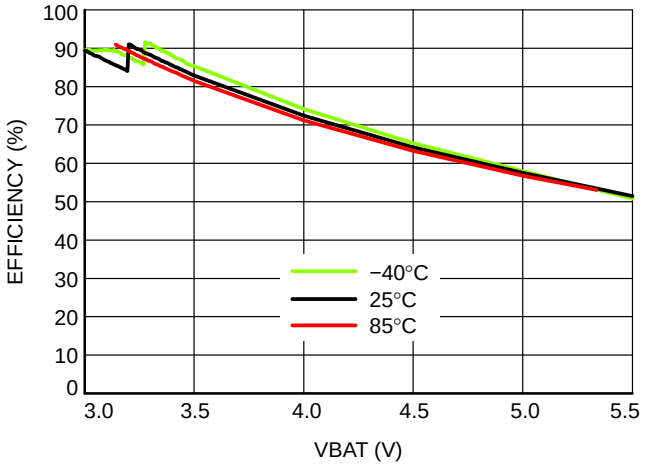


Figure 15. Torch LED Efficiency vs. Input Voltage (I_{TORCH} = 300 mA, V_{IN} Falling)

Detailed Description

The NCP6951B is optimized to supply the different sub systems of battery powered portable applications. The IC can be supplied directly from the latest technology single cell batteries such as Lithium−Polymer as well as from triple alkaline cells. Alternatively, the IC can be supplied from a pre−regulated supply rail in case of multi−cell or mains powered applications.

The output voltage range, current capabilities and performance of the switched mode DCDC converter are well suited to supply the different peripherals in the system as well as to supply processor cores. To reduce overall power consumption of the application, Dynamic Voltage Scaling (DVS) is supported on the DCDC converter. For PWM operation, the converter runs on a local 3 MHz clock. A low power PFM mode is provided that ensures that even at low loads high efficiency can be obtained. All the switching components are integrated including the compensation networks and synchronous rectifier. Small sized 1 μH inductor and 10 μF bypass capacitor are required for typical applications.

The general purpose low dropout regulators can be used to supply the lower power rails in the application. To improve on overall application standby current, the bias current of these regulators are made very low. The regulators have two separated input supply pin to be able to connect them independently to either the system supply voltage or to the output of the DCDC converter in the application. The regulators are bypassed with a small size 1.0 μF capacitor.

The IC is controlled through the I^2C interface that allows to program amongst others the output voltages of the different supply rails as well as to configure its behavior. In addition to this bus, a digital hardware enable control pin (HWEN) is provided.

Under Voltage Lockout

The core does not operate for voltages below the under voltage lockout (UVLO) threshold and all internal circuitry, both analog and digital, is held in reset.

NCP6951B functionality is guaranteed down to V_{UVLO} when the battery is falling. A hysteresis is implemented to avoid erratic on / off behavior of the IC. Due to its 200 mV hysteresis, when the battery is rising, re−start is guaranteed at 2.5 V.

Thermal Shutdown

Given the output power capabilities of the on chip step down converters and low drop out regulators the thermal capabilities of the device can be exceeded. A thermal protection circuit is therefore implemented to prevent the part from damage. This protection circuit is only activated when the core is in active mode (at least one output channel is enabled). During thermal shutdown, all outputs of NCP6951B are off.

When NCP6951B returns from thermal shutdown, it can re−start in two different configurations depending on REARM[7:6] bits ($09 register). If REARM[7:6] = 00 then NCP6951B re−starts with default register values, otherwise it re−starts with register values set prior to thermal shutdown.

In addition, a thermal warning is implemented which can inform the processor through an interrupt that NCP6951B is close to its thermal shutdown so that preventive action can be taken by software.

Active Output Discharge

By default, to prevent any disturbances on power−up sequence, output discharge is activated as soon as the input voltage is valid (upper than UVLO+ hyst).

After power up sequence and during ON state, output discharge can be independently enabled / disabled by appropriate settings in the DIS register (refer to the register definition section).

If a power down sequence, UVLO or thermal shutdown events occurs, the output discharge paths are activated until the next PUS and ON state.

When the IC is turned off when VIN1 drops down below UVLO threshold, no shut down sequence is expected, all supplies are disabled and outputs turn to high impedance.

Enabling

The HWEN pin controls the device start up. If HWEN is raised, this starts the power up sequencer (PUS). If HWEN is made low, device enters in shutdown mode and all regulators will be turned off with inverted PUS of power up.

A built−in pull−down resistor disables the device if this pin is left unconnected.

When HWEN is high, the different power rails can be independently enabled / disabled by writing the appropriate bit in the ENABLE register.

Power Up Sequence and HWEN

When enabling part with HWEN pin, the part will be set with the default configuration factory programmed in the registers, if no I^2C programming has been done as described in the below table.

Table 5. DEFAULT POWER UP SEQUENCER

Delay (in µs) from Tstart	Sequence	Default Assignment	Default Vprog	Default Mode and ON/OFF
128	To: 000	DCDC	1.20 V	Auto PFM/PWM OFF
256	T1: 001	LDO1	2.80 V	OFF
384	T2: 010	LDO2	2.80 V	OFF
512	T3: 011	LDO3	1.80 V	OFF
640	T4: 100	LDO4	2.80 V	OFF
768	T5: 101	LDO5	1.80 V	OFF

NOTE: Additional power sequence are available. Please contact your ON representative for further information.

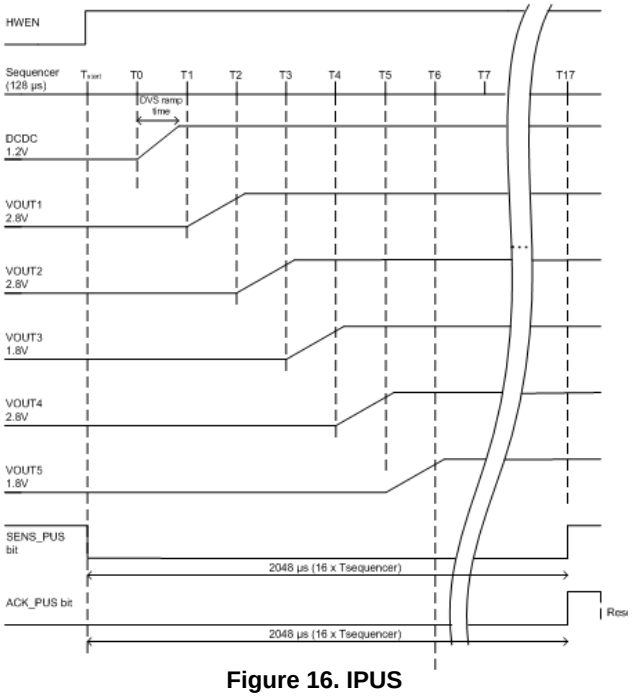


Figure 16. IPUS

The initial power up sequence (IPUS) is described in Figure 16.

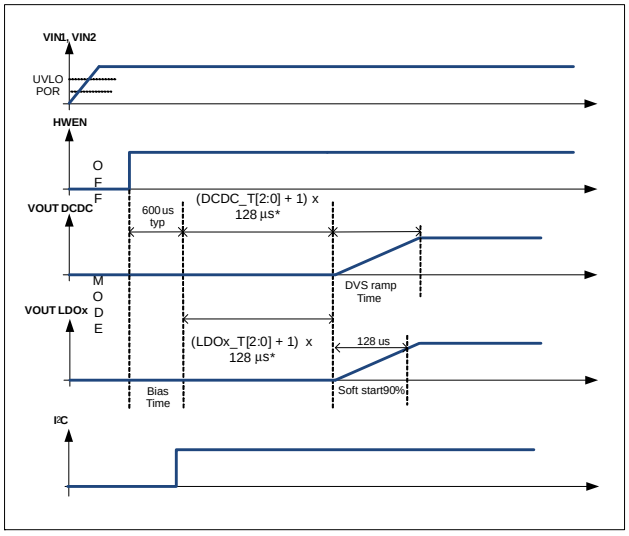


Figure 17. IPUS

In order to power up the circuit, the input voltage VIN1 has to rise above the VUVLO threshold. This triggers the internal core circuitry power up including:

- Internal references
- Core circuitry “Wake Up Time”
- DCDC “Bias Time”

These delays are internals and cannot be bypassed.

As the default configuration factory is programmed with disable state for the DCDC and LDOs, an I^2C access must be done at the end of the bias time to enable the supplies.

In addition a user programmable delay will also take place between end of Core circuitry turn on (Bias time) and Start up time: The *PowerSupplies_T*[2..0] bits of TIME register will set this user programmable delay with a 128 µs resolution (note: please contact your ON Semiconductor representative for additional resolution options). The output discharge of the DCDC and LDOs are done during this time slot. NOTE: During the Bias time, the I^2C interface is not active during the first 50 µs. Any I^2C request to the IC during this time period will result in a NACK reply.

However, I^2C registers can be read and written while HWEN pin is still low (except blanking time of 50 µs typical). By programming the appropriate registers (see registers description section), the power up sequence default can be modified and set upon requirements (please contact your ON Semiconductor representative for additional PUS options)

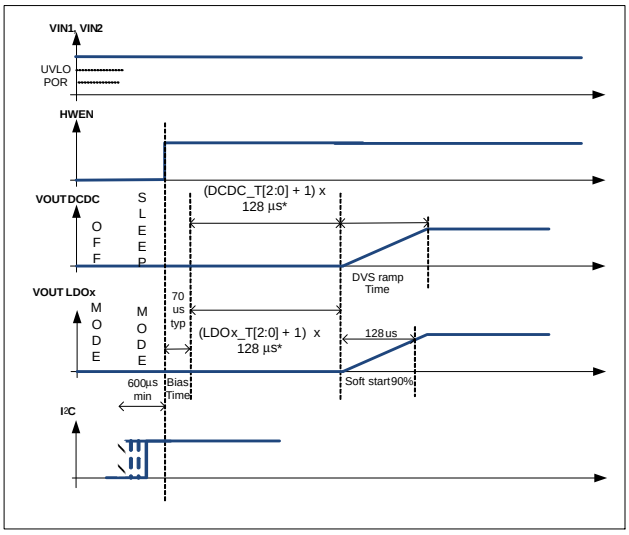


Figure 18. Sleep Mode PUS (SMPUS)

A third turn on sequence is also available by I^{2}C. Indeed each power supply can be turn off/on through I^{2}C register. In this case no biasing time is required except for DCDC bias time (32 µs typical).

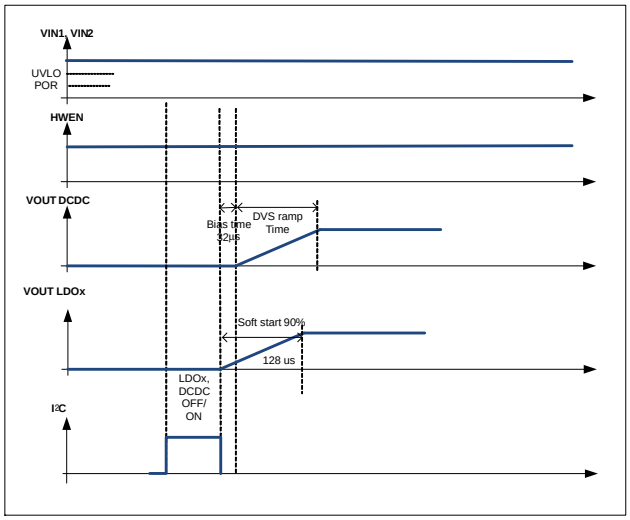


Figure 19. ON Mode PUS (OPUS)

Shutdown by HWEN

When HWEN is tied low, all supplies are disabled with reverted turn on sequence detailed in default Power Up Sequencer table. If different turn off sequence is required, a different programming can be done by I^{2}C.

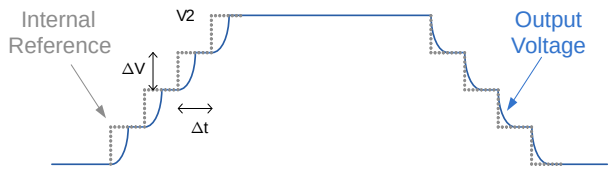


Figure 20. Dynamic Voltage Scaling Effect Timing

DCDC Converter

The converter can operate in two modes: PWM mode and PFM mode. In PWM mode the converter operates at a fixed frequency and adapts its duty cycle to regulate to the desired output voltage. The advantage of this mode is that the EMI noise is predictable. However, at lower loadings the efficiency is degraded. In PFM mode some switching pulses are skipped to control the output voltage. This allows maintaining high efficiency even at low loadings. In addition, no high frequency clock is required which provides additional current savings. The switchover point between both modes is chosen depending on the supply conditions such that highest efficiency is obtained over the entire load range.

The switch over between PWM/PFM modes can occur automatically but the switcher can be set in auto switching mode PFM / PWM by I^{2}C programming.

A soft start is provided to limit inrush currents when enabling the converters. The soft start consists of ramping gradually the reference to the switcher.

Additional current limitation is provided by a peak current limiter that monitors and limits the current through the inductor.

DCDC converter output voltage can be set by I^{2}C

MODEDCDC bit is used to program switcher mode control.

Table 6. MODEDCDC BIT DESCRIPTION

MODEDCDC	DCDC Mode Control
0	Mode is auto switching PFM / PWM (default)
1	Mode is PWM only

Dynamic Voltage Scaling (DVS)

Step down converters support dynamic voltage scaling (DVS). This means the output voltage can be reprogrammed based upon I^{2}C commands to provide the different voltages required by the processor. The change between set points is managed in a smooth manner without disturbing the operation of the processor.

When programming a higher voltage, the reference of the switcher and therefore the output is raised in 50 mV/ 2.67 µs (default) steps such that the dV/dt is controlled. When programming a lower voltage the output voltage will decrease based on the output capacitor value and the load. The DVS system makes sure that the voltage ramp down will not exceed the steps settings.

Figure 21. DVS Figure

Programmability

DCDC converter has two different output voltages programmed by default in the DCDC_V1 and V2 bank. The DCDC output voltage can be changed from V1 to V2 with the DCDC_V2/V1 bit in $08 register.

Table 7. DCDC_V2/1 BIT DESCRIPTION

DCDC_V2/1	Bit Description
0	Output voltage is set to DCDC_V2
1	Output voltage is set to DCDC_V1(Default)

The two DVS bits in register TIME determine ramp up time per each voltage step.

Table 8. DVS BIT DESCRIPTION

DVS [0]	Bit Description
0	2.67 μs per step (default)
1	10.67 μs per step

DCDC Step Down Converter and LDOs End of Turn On Sequence

To indicate the end of the power up sequence, a power good sense bit is available at the $0A address. (SEN_PG). Sense bit is set to 0 during power up sequence and 16 x digital clock (128's by default). The Power good sense bit is released to 1 after this sequence and trig ACK_PG interrupt. The interrupt is reset by a read or HWEN.

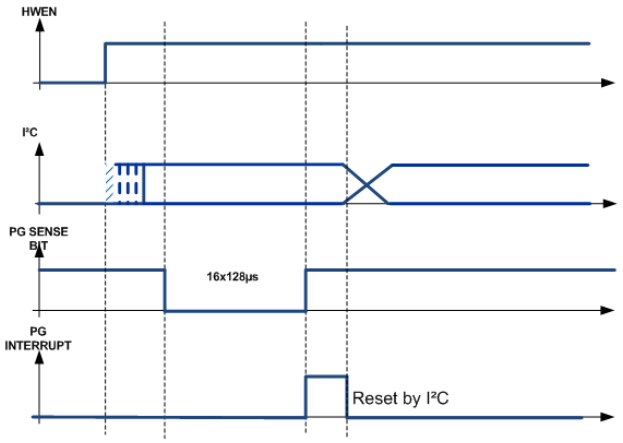


Figure 22. Power Good Behavior

Interrupt

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring). The interrupt sources include:

Table 9. INTERRUPT SOURCES

Register	$0B
UVLO	Under voltage threshold
PUS	End of power up sequence
WNRG	Thermal warning
TSD	Thermal shutdown

Individual bits generating interrupts will be set to 1 in the INT_ACK register (I^2C read only register), indicating the interrupt source. INT_ACK register is reset by an I^2C read. INT_SEN registers (read only registers) are real time indicators of interrupt sources.

Force Register Reset

The I^2C registers are reset when the part is in Off Mode:

- Vin<UVLO or
- I^2C and HWEN not present or
- Restart from TSD event (REARM_ TSD[7:6]=00, register $09)

Flash LED Driver

NCP6951B includes an adaptive boost converter with an high side current source allowing the use of a thermally grounded flash LED.

Flash LED driver has two mains operating modes: flash mode and torch mode which is controlled thru the I^2C interface and the FLEN and FLSEL pins.

Adaptive Boost − Bypass Converter

NCP6951B includes an adaptive boost−bypass converter to optimize the efficiency of the flash LED driver. The boost−bypass converter monitors the flash LED voltage and the battery voltage.

When $V_{BST} < V_{FL}$ + 250 mV, the adaptive boost−bypass converter operates in boost mode and regulates $V_{BST} = V_{FL}$ + 275 mV.

When $V_{BAT} \geq V_{FL}$ + 540 mV, the adaptive boost−bypass converter operates in bypass mode and $V_{BST} = V_{BAT}$.

Boost Mode

The adaptive boost−bypass converter implements an architecture allowing the device to operate in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

The adaptive boost−bypass converter operates in DCM in order to save power and improve efficiency at low loads by reducing the switching frequency. When current in the inductor becomes continuous, the controller automatically turns to CCM mode and goes back in DCM when current in the inductor is discontinuous.

Bypass Mode

The adaptive boost−bypass converter has been designed to manage conditions for which V_{BAT} becomes close to V_{FL} + 275 mV. In that case the adaptive boost−bypass converter enters automatically in bypass mode from boost mode. The V_{BST} voltage is the copy of the input voltage minus a dropout voltage resulting from the resistance of the internal P−MOSFET plus the inductor.

Timeout Description

NCP6951B includes 2 timers which help to prevent any damage to the part due to too high flash duration or too close consecutive flash.

The 3 bits SAFETY_TIMER[2:0] set a maximum flash duration from 32 ms to 1024 ms.

The 4 bits INHIBIT_TIMER[3:0] register set a minimum off time duration after the flash from 0 to 7680 ms.

When FLEN is going high, SAFETY_TIMER is started and the flash current source is turn off if FLEN pin is not pulling down before the end of the timer. The timer is reset when FLEN is going low.

After a flash pulse, the flash current source can remain disabled for a guaranteed off period and as such will ignore the state of the FLEN pin.

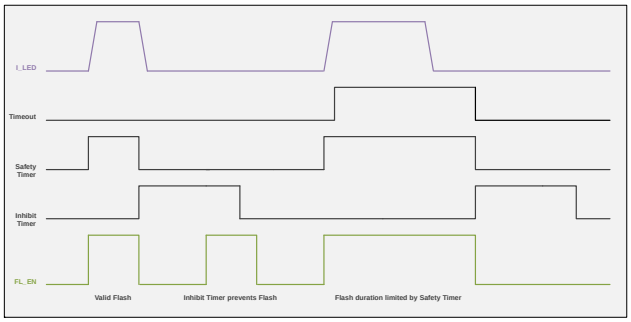


Figure 23. Battery Voltage Adaptive Mode Behavior

PA Burst Blanking

When the flash is enabled and the FLSEL pin being pulled high, the reduced flash LED current is selected. Normally the reduced LED current level is programmed much lower than the flash LED current so that FLSEL high selects the reduced level. A dedicated bit is available to invert the polarity of the FLSEL pin.

During PA burst blanking, the transition to the lower current is instantaneity. The transition to the higher current follow the ramp time set in the FLASH_SETTING register.

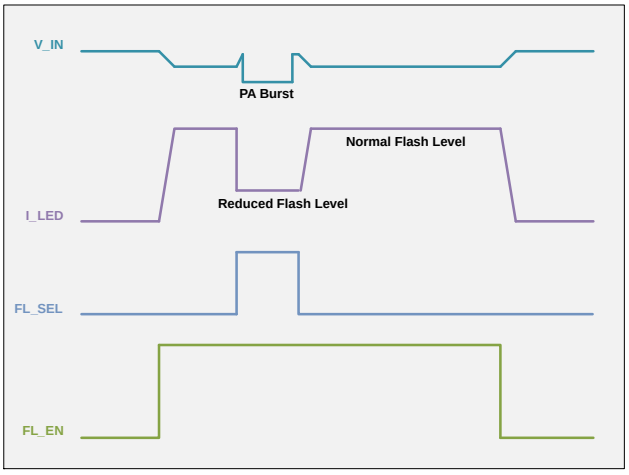


Figure 24. Battery Voltage Adaptive Mode Behavior

Low Battery Protection and Die Temperature Management in Flash Mode

The battery voltage is permanently monitored. 2 different behaviors can be set with the battery_voltage_mode bit.

Low Battery Voltage Adaptive mode:

2 thresholds can be programmed thru I^2C to reduce the flash current in case the battery voltage is too low.

When Vin goes below UVLO_High, the NCP6951B try to recover by decreasing the current down to I reduced, and then increase it up to the $I_{FL\ FAULT} - 1$.

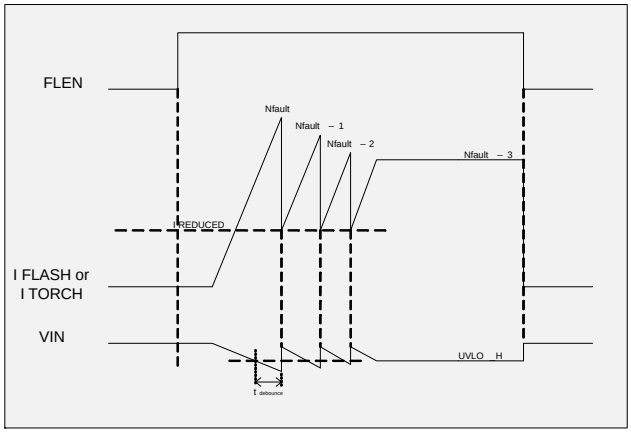


Figure 25. Battery Voltage Adaptive Mode Behavior

When Vin goes below UVLO low, flash current is stopped.

Low Battery Voltage Reduce mode:

2 thresholds can be programmed thru I^2C to reduce the flash current in case the battery voltage is too low.

When Vin goes below UVLO_High, I flash is decreased down to I reduced.

When Vin goes below UVLO low, flash current is stopped.

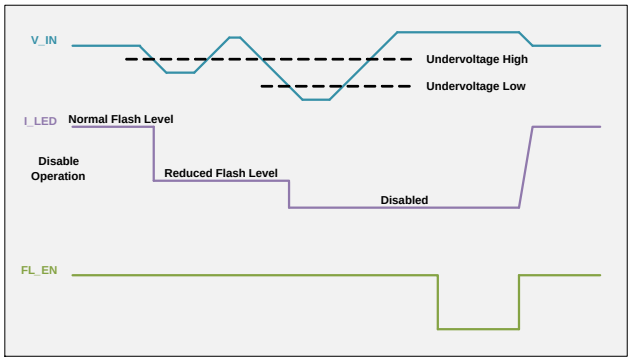


Figure 26. Battery Voltage Reduce Mode Behavior

The die temperature is also permanently monitored. And 2 different behaviors can also be set with the die_temp_mode bit.

Die Temperature Management Adaptative mode:

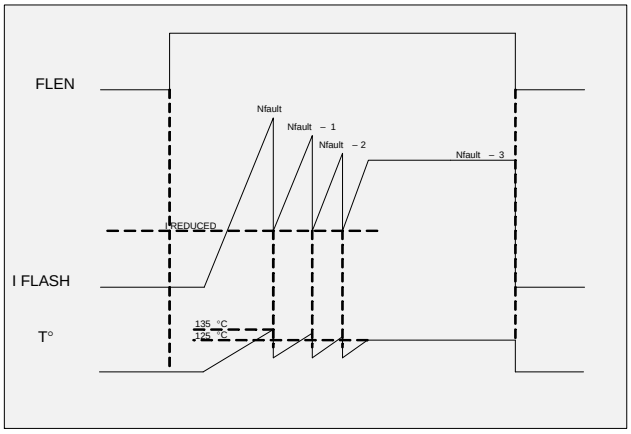


Figure 27. Die Temperature Adaptative Mode Behavior

Die Temperature Management Reduce mode:

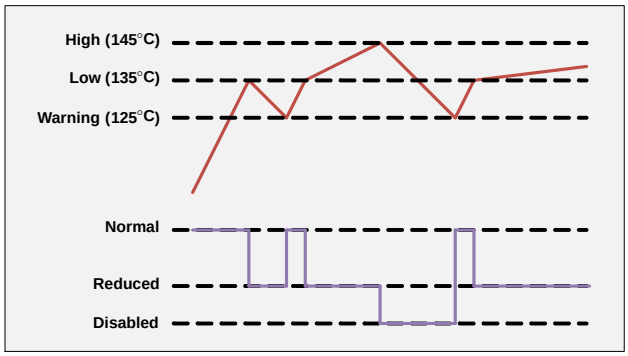


Figure 28. Die Temperature Reduce Mode Behavior

The following state machine describe the behavior of the part with the combination of the 4 monitoring modes:

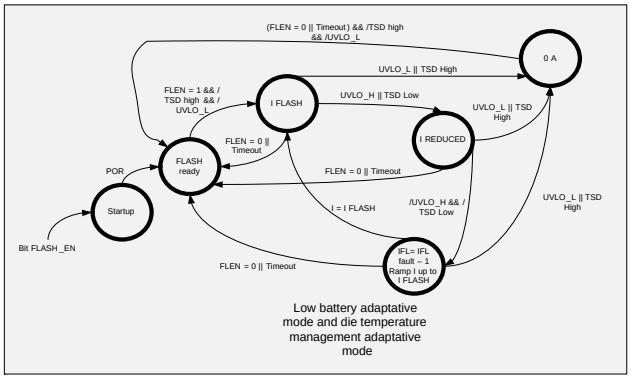


Figure 29. State Machine Battery Voltage and Die Temperature Adaptative Mode

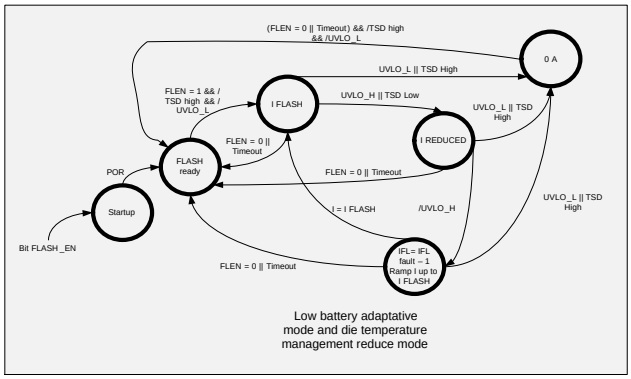


Figure 30. State Machine Battery Voltage Adaptative Mode and Die Temperature Reduce Mode

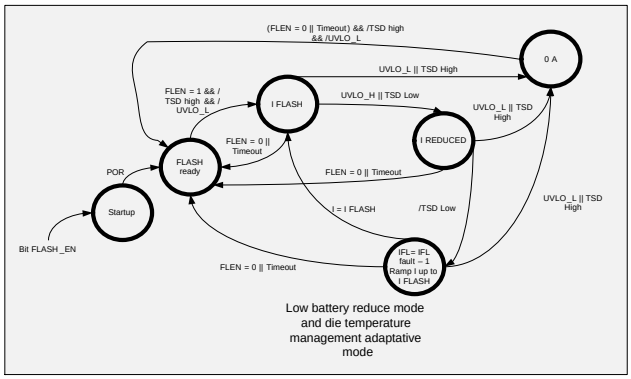


Figure 31. State Machine Battery Voltage Reduce Mode and Die Temperature Adaptative Mode

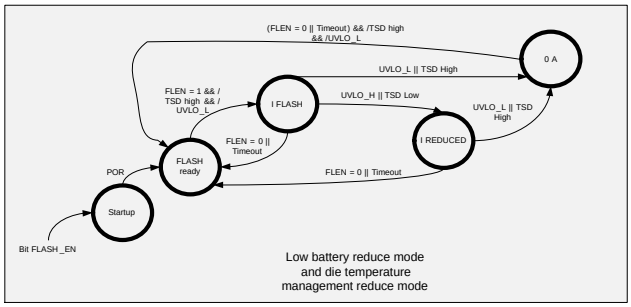


Figure 32. State Machine Battery Voltage Mode and Die Temperature Reduce Mode

Low Battery Protection in Torch Mode

In case of torch mode, when UVLO_L threshold is reached, the torch current is set to 0 mA and the UVLO flag is set. NCP6951B recovers its torch current when Vin reach UVLO_H if the TORCH_RETRY bit is set.

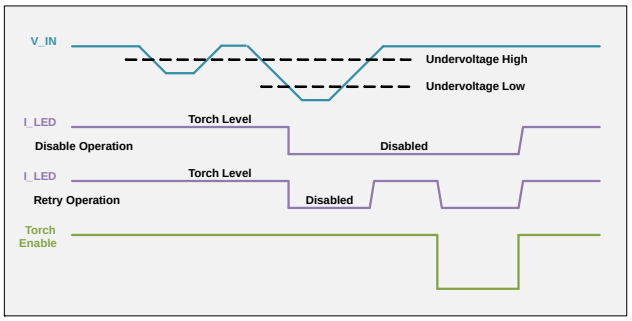


Figure 33. Battery Voltage Reduce Mode Behavior

Anti Red−eye Function

NCP6951B includes an anti red−eye function. Pre−flash level and number of pre−flash pulses can be set thru the RED_EYE register. The user has only to send the sequence with the FLEN pin. A time out can be activated (2 s) in case a FL_EN pulse is not sent after the first pulse to reset the function.

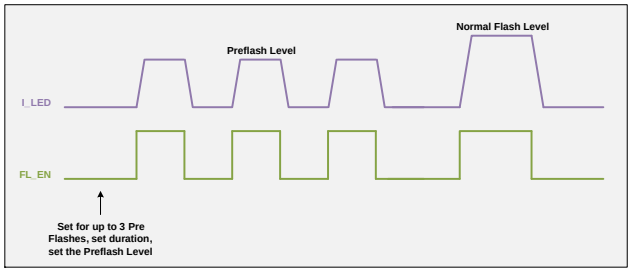


Figure 34. Anti Red−eye Behavior

I²C Compatible Interface

NCP6951B can support a subset of I²C protocol, below are detailed introduction for I²C programming.

I²C Communication Description

ON Semiconductor communication protocol is a subset of I²C protocol.

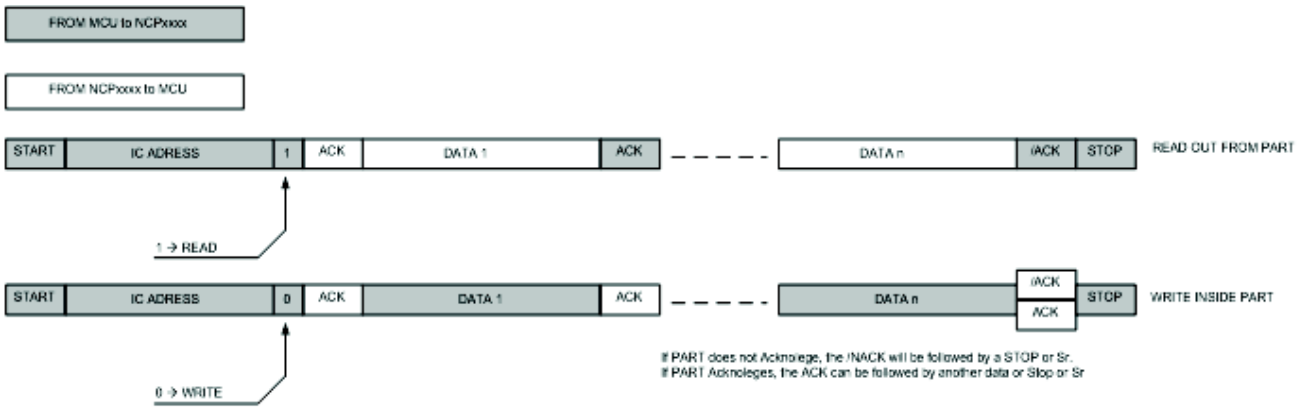


Figure 35. General Protocol Description

The first byte transmitted is the Chip address (with LSB bit sets to 1 for a read operation, or sets to 0 for a Write operation). Then the following data will be:

- In case of a Write operation, the register address (@REG) we want to write in followed by the data we will write in the chip. The writing process is incremental. So the first data will be written in @REG, the second one in @REG + 1... The data are optional.
- In case of read operation, the NCP6951B will output the data out from the last register that has been accessed by the last write operation. Like writing process, reading process is an incremental process.

Read Out from Part

The Master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has set:

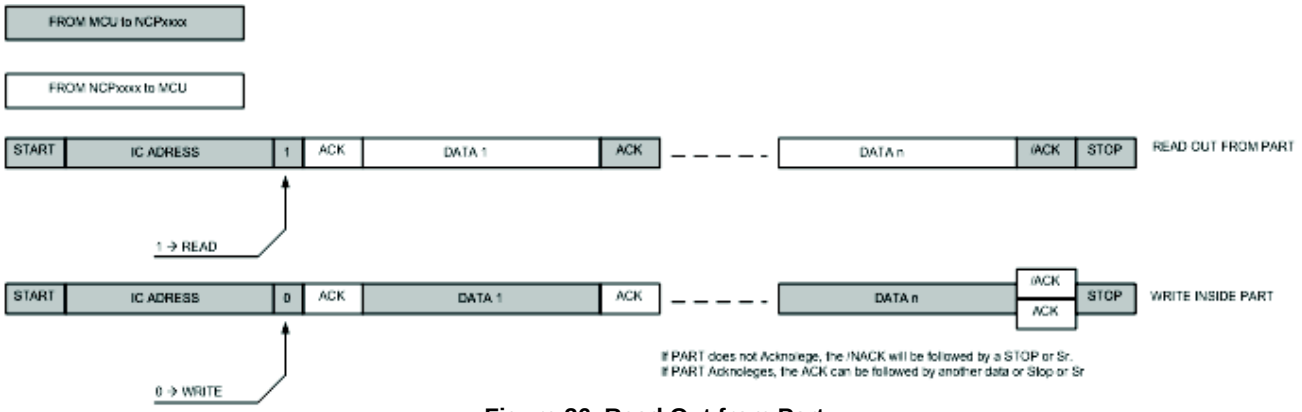


Figure 36. Read Out from Part

The first WRITE sequence will set the internal pointer on the register we want access to. Then the read transaction will start at the address the write transaction has initiated.

Transaction with Real Write then Read

1. With Stop Then Start

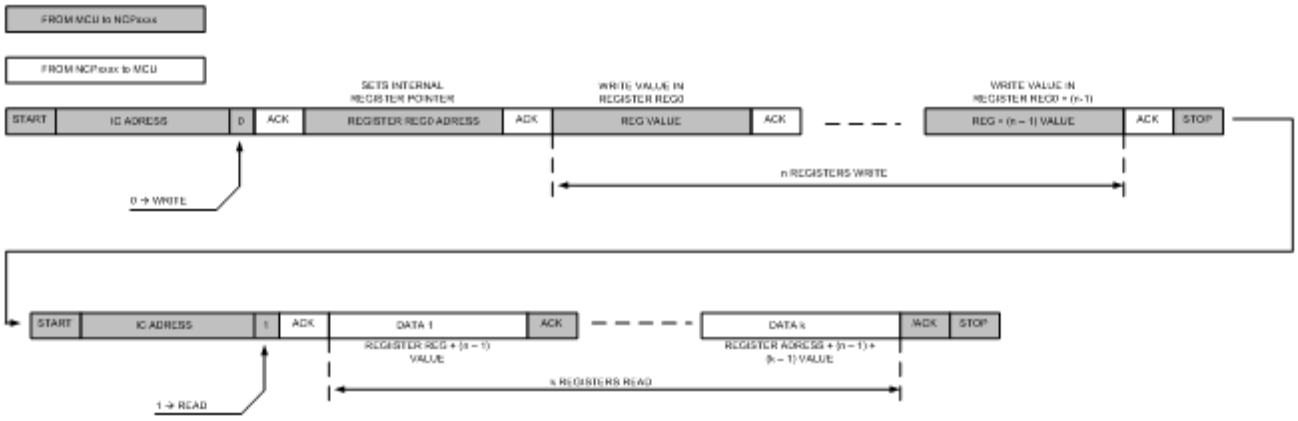


Figure 37. Write Followed by Read Transaction

Write in Part

Write operation will be achieved by only one transaction. After chip address, the MCU first data will be the internal register we want access to, then following data will be the data we want to write in Reg, Reg + 1, Reg + 2,..., Reg +n.

Write n Registers:

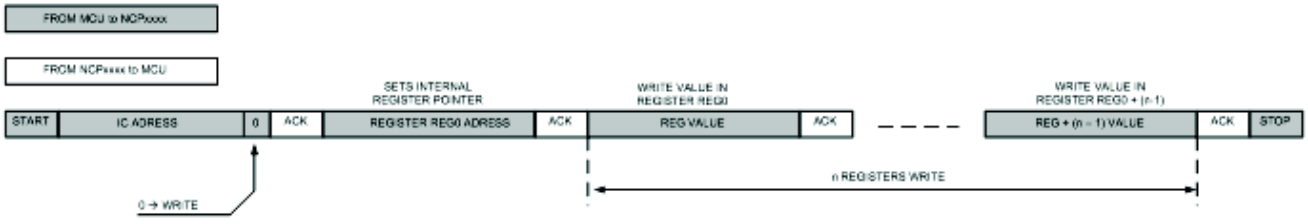


Figure 38. Write in N Registers

I²C Address

NCP6951B has fixed I²C but different I²C address (by default $10, 7 bit address, see below table A7~A1), NCP6951B supports 7−bit address only.

Table 10. NCP6951B I²C ADDRESS

I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
ADD0 (Default)	W $20 /R $21	0	0	1	0	0	0	0	X
ADDRESS	$10	0	0	1	0	0	0	0	−

Different default address is available upon request

Register Map

Following register map describes I²C registers.

Registers can be:

Reserved Address is reserved and register is not physically designed

Spare Address is reserved and register is physically designed

Table 11. REGISTERS SUMMARY

Address	Register Name	Type	Default	Function
$00	GENERAL_SETTINGS	RW	$00	DVS control Settings
$01	LDO1_SETTINGS	RW	$39	LDO1 register settings
$02	LDO2_SETTINGS	RW	$59	LDO2 register settings
$03	LDO3_SETTINGS	RW	$6C	LDO3 register settings
$04	LDO4_SETTINGS	RW	$9E	LDO4 register settings
$05	LDO5_SETTINGS	RW	$B1	LDO5 register settings
$06	DCDC_SETTINGS1	RW	$09	DCDC register settings 1
$07	DCDC_SETTINGS2	RW	$07	DCDC register settings 2
$08	ENABLE	RW	$80	Enable and DVS register settings
$09	PULLDOWN	RW	$3F	Active discharge and rearming register
$0A	STATUS	R	$04	Status or sense register
$0B	INTERRUPT_ACK	RC	$00	Interrupt register
$0C	FLASH_SETTING	RW	$1F	Flash current register
$0D	REDUCED_CURRENT	RW	$00	Reduced current register
$0E	TORCH_CURRENT	RW	$00	Torch current register
$0F	PROTECTION	RW	$20	Boost peak inductor current and UVLO register
$10	FLASH_TIMER	RW	$13	Safety timer register
$11	RED_EYE	RW	$43	Red eye register
$12	FLASH_CONFIGURATION	RW	$08	Flash configuration register
$13	FLASH_ENABLE	RW	$00	Flash enable register
$14	FLASH_STATUS	RC	$00	Flash status register
$15 to $FF	−	−	−	Reserved. Do not access to those registers

Details of the registers are in the following section.

Registers Description

Table 12. GENERAL_SETTINGS REGISTER

Name: GENERAL_SETTINGS				Address: $00			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	spare=0	DVS	spare=0	spare=0	spare=0	spare=0

Table 13. BIT DESCRIPTION OF GENERAL_SETTINGS REGISTER

Bit	Bit Description
DVS[0]	Ramp up time per voltage step

Table 14. LDO1_SETTINGS REGISTER

Name: LDO1_SETTINGS				Address: $01			
Type: RW				Default: $39			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO1_T [2:0]			LDO1_V[4:0]				

Table 15. BIT DESCRIPTION OF LDO1_SETTINGS REGISTER

Bit	Bit Description
LDO1_V[4:0]	LDO1 output voltage setting, refer to Table 17
LDO1_T[2:0]	LDO1 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO1 startup Delay time = (LDO1_T[2:0] + 1) * 128 μs

NOTE: 64 μs, 128 μs, 1ms, 2 ms OTP options (128 μs default value)

Table 16. LDO2_SETTINGS REGISTER

Name: LDO2_SETTINGS				Address: $02			
Type: RW				Default: $59			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO2_T [2:0]			LDO2_V[4:0]				

Table 17. BIT DESCRIPTION OF LDO2_SETTINGS REGISTER

Bit	Bit Description
LDO2_V[4:0]	LDO2 output voltage setting, refer to Table 17
LDO2_T[2:0]	LDO2 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO2 startup Delay time = (LDO2_T[2:0] + 1) * 128 μs

Table 18. LDO3_SETTINGS REGISTER

Name: LDO3_SETTINGS				Address: $03			
Type: RW				Default: $6C			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO3_T [2:0]			LDO3_V[4:0]				

Table 19. BIT DESCRIPTION OF LDO3_SETTINGS REGISTER

Bit	Bit Description
LDO3_V[4:0]	LDO3 output voltage setting, refer to Table 17
LDO3_T[2:0]	LDO3 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO3 startup Delay time = (LDO3_T[2:0] + 1) * 128 μs

Table 20. LDO1_V[4:0], LDO2_V[4:0], LDO3_V[4:0] SETTING TABLE

Register	Vout(V)	Register	Vout(V)	Register	Vout(V)	Register	Vout(V)
00000	1.70	01000	1.70	10000	2.10	11000	2.75
00001	1.70	01001	1.70	10001	2.20	11001	2.80
00010	1.70	01010	1.70	10010	2.30	11010	2.85
00011	1.70	01011	1.75	10011	2.40	11011	2.90
00100	1.70	01100	1.80	10100	2.50	11100	2.95
00101	1.70	01101	1.85	10101	2.60	11101	3.00
00110	1.70	01110	1.90	10110	2.65	11110	3.10
00111	1.70	01111	2.00	10111	2.70	11111	3.30

Table 21. LDO4_SETTINGS REGISTER

Name: LDO4_SETTINGS				Address: $04			
Type: RW				Default: $9E			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO4_T [2:0]			LDO4_V[4:0]				

Table 22. BIT DESCRIPTION OF LDO4_SETTINGS REGISTER

Bit	Bit Description
LDO4_V[4:0]	LDO4 output voltage setting, refer to Table 22
LDO4_T[2:0]	LDO4 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO4 startup Delay time = (LDO4_T[2:0] + 1) * 128 μs

Table 23. LDO5_SETTINGS REGISTER

Name: LDO5_SETTINGS				Address: $05			
Type: RW				Default: $B1			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LDO5_T [2:0]			LDO5_V[4:0]				

Table 24. BIT DESCRIPTION OF LDO5_SETTINGS REGISTER

Bit	Bit Description
LDO5_V[4:0]	LDO5 output voltage setting, refer to Table 22
LDO5_T[2:0]	LDO5 startup delay time setting (delay time between HWEN transitions from LOW to High and LDO5 startup Delay time = (LDO5_T[2:0] + 1) * 128 μs

Table 25. LDO4_V[4:0], LDO5_V[4:0] SETTING TABLE

Register	Vout(V)	Register	Vout(V)	Register	Vout(V)	Register	Vout(V)
00000	1.20	01000	1.35	10000	1.75	11000	2.40
00001	1.20	01001	1.40	10001	1.80	11001	2.50
00010	1.20	01010	1.45	10010	1.85	11010	2.60
00011	1.20	01011	1.50	10011	1.90	11011	2.65
00100	1.20	01100	1.55	10100	2.00	11100	2.70
00101	1.20	01101	1.60	10101	2.10	11101	2.75
00110	1.25	01110	1.65	10110	2.20	11110	2.80
00111	1.30	01111	1.70	10111	2.30	11111	2.85

Table 26. DCDC_SETTINGS1 REGISTER

Name: DCDC_SETTINGS1				Address: $06			
Type: RW				Default: $09			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DCDC_T[2:0]			DCDC_V1[4:0]				

Table 27. BIT DESCRIPTION OF DCDC_SETTINGS1 REGISTER

Bit	Bit Description
DCDC_V1[4:0]	DCDC output voltage setting 1, refer to Table 26
DCDC_T[2:0]	DCDC startup delay time setting (delay time between HWEN transitions from LOW to High and DCDC startup Delay time = (DCDC_T[2:0] + 1) * 128 μs

Table 28. DCDC_SETTINGS2 REGISTER

Name: DCDC_SETTINGS2				Address: $07			
Type: RW				Default: $07			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	MODEDCDC	DCDC_V2[4:0]				

Table 29. BIT DESCRIPTION OF DCDC_SETTINGS2 REGISTER

Bit	Bit Description
DCDC_V2[4:0]	DCDC output voltage setting 2, refer to Table 26
MODEDCDC	DCDC Operating Mode 0: Auto switching PFM / PWM (default) 1: Forced PWM

Table 30. DCDC_Vx[4:0] SETTING TABLE

DCDC_V1/2	Vout(V)	DCDC_V1/2	Vout(V)	DCDC_V1/2	Vout(V)	DCDC_V1/2	Vout(V)
00000	0.80V	01000	1.15V	10000	1.55V	11000	1.95V
00001	0.80V	01001 (V1)*	1.20V	10001	1.60V	11001	2.00V
00010	0.85V	01010	1.25V	10010	1.65V	11010	2.05V
00011	0.90V	01011	1.30V	10011	1.70V	11011	2.10V
00100	0.95V	01100	1.35V	10100	1.75V	11100	2.15V
00101	1.00V	01101	1.40V	10101	1.80V	11101	2.20V
00110	1.05V	01110	1.45V	10110	1.85V	11110	2.25V
00111	1.10V	01111 (V2)	1.50V	10111	1.90V	11111	2.30V

*Default value: V1

Table 31. ENABLE REGISTER

Name: ENABLE				Address: $08			
Type: RW				Default: $80			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DCDC_V2/V1	spare=0	DCDC_ EN	LDO5_ EN	LDO4_ EN	LDO3_ EN	LDO2_ EN	LDO1_ EN

Table 32. BIT DESCRIPTION OF ENABLE REGISTER

Bit	Bit Description
DCDC_V2/V1	DCDC output voltage setting 0: DCDC converter output voltage is set to DCDC_V2 1: DCDC converter output voltage is set to DCDC_V1
DCDC_ EN	DCDC Enabling 0: Disabled 1: Enabled
LDO5_ EN	LDO5 Enabling 0: Disabled 1: Enabled
LDO4_ EN	LDO4 Enabling 0: Disabled 1: Enabled
LDO3_ EN	LDO3 Enabling 0: Disabled 1: Enabled
LDO2_ EN	LDO2 Enabling 0: Disabled 1: Enabled
LDO1_ EN	LDO1 Enabling 0: Disabled 1: Enabled

Table 33. PULLDOWN REGISTER

Name: PULLDOWN				Address: $09			
Type: RW				Default: $3F			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
REARM_ TSD[7] REARM_TSD[7]	REARM_ TSD[6]	DCDC_ PULLDOWN	LDO5_ PULLDOWN	LDO4_ PULLDOWN	LDO3_ PULLDOWN	LDO2_ PULLDOWN	LDO1_ PULLDOWN

Table 34. BIT DESCRIPTION OF PULLDOWN REGISTER

Bit	Bit Description
REARM_ TSD[7:6]	Device Rearming after Thermal Shut Down 11: N/A 10: No re−arming after TSD 01: Re−arming active after TSD with no reset of I^2C registers: new power−up sequence is initiated with I^2C registers values. 00: Re−arming active after TSD with reset of I^2C registers: new power−up sequence is initiated with default I^2C registers values (default).
DCDC_ PULLDOWN	DCDC active output discharge 0: Disabled 1: Enabled
LDO5_ PULLDOWN	LDO5 active output discharge 0: Disabled 1: Enabled
LDO4_ PULLDOWN	LDO4 active output discharge 0: Disabled 1: Enabled
LDO3_ PULLDOWN	LDO3 active output discharge 0: Disabled 1: Enabled
LDO2_ PULLDOWN	LDO2 active output discharge 0: Disabled 1: Enabled
LDO1_ PULLDOWN	LDO1 active output discharge 0: Disabled 1: Enabled

Table 35. STATUS REGISTER

Name: STATUS				Address: $0A			
Type: R				Default: $04			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	spare=0	spare=0	SEN_UVLO	SEN_/PUS	SEN_TSD	SEN_WNRG

Table 36. BIT DESCRIPTION OF STATUS REGISTER

Bit	Bit Description
SEN_UVLO	UVLO sense 0: Input voltage is higher than (UVLO + hyst) threshold. 1: Input voltage is lower than (UVLO) threshold.
SEN_PUS	Power up sequence 0: Power up sequence on going 1: Power up sequence finished or HWEN is low
SEN_TSD	Thermal Shut Down sense 0: IC temperature is below TSD threshold 1: IC temperature is over TSD threshold
SEN_WNRG	Thermal warning sense 0: IC temperature is below Thermal Warning threshold 1: IC temperature is over Thermal Warning threshold

Table 37. INTERRUPT_ACK REGISTER

Name: INTERRUPT_ACK				Address: $0B			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
spare=0	spare=0	spare=0	spare=0	ACK_UVLO	ACK_PUS	ACK_TSD	ACK_WNRG

Table 38. BIT DESCRIPTION OF INTERRUPT_ACK REGISTER

Bit	Bit Description
ACK_UVLO	UVLO sense acknowledge 0: Cleared 1: SEN_UVLO Dual edge triggered interrupt
ACK_PUS	Power up sequence sense acknowledge 0: Cleared 1: SEN_PUS Rising edge triggered interrupt
ACK_TSD	Thermal Shut Down sense acknowledge 0: Cleared 1: SEN_TSD Dual edge triggered interrupt
ACK_WNRG	Thermal warning sense acknowledge 0: Cleared 1: SEN_WNRG Dual edge triggered interrupt

NOTE: SEN_PUS rising edge appears (16) x 128 μs (default) after HWEN rising edge.

Table 39. FLASH_SETTING REGISTER

Name: FLASH_CURRENT				Address: $0C			
Type: RW				Default: $1F			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	FLASH_TR[1:0]		FLASH_CURRENT[4:0]				

Table 40. BIT DESCRIPTION OF FLASH_SETTING REGISTER

Bit	Bit Description
FLASH_CURRENT[4:0]	Defines the flash current.
FLASH_TR[1:0]	Defines the flash ramp time.

Table 41. BIT DESCRIPTION OF FLASH_CURRENT[4:0]

Register Value	FLASH_CURRENT[4:0] (mA)	Register Value	FLASH_CURRENT[4:0] (mA)
00000	100	10000	800
00001	133	10001	900
00010	166	10010	1000
00011	200	10011	1100
00100	233	10100	1200
00101	266	10101	1300
00110	300	10110	1400
00111	333	10111	1500
01000	366	11000	1600
01001	400	11001	1600
01010	433	11010	1600
01011	466	11011	1600
01100	500	11100	1600
01101	533	11101	1600
01110	600	11110	1600
01111	700	11111	1600

Table 42. BIT DESCRIPTION OF FLASH_TR[1:0]

Register Value	FLASH_TR[1:0] (V)
00	100 mA / 16 μs
01	100 mA / 32 μs
10	100 mA / 64 μs
11	100 mA / 128 μs

Table 43. REDUCED_CURRENT REGISTER

Name: FLASH_CURRENT				Address: $0D			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	Spare = 0	Spare = 0	REDUCED_CURRENT[3:0]			

Table 44. BIT DESCRIPTION OF REDUCED_CURRENT REGISTER

Bit	Bit Description
REDUCED_CURRENT[3:0]	Defines the reduced current.

Table 45. BIT DESCRIPTION OF REDUCED_CURRENT[3:0]

Register Value	REDUCED_CURRENT[3:0] (mA)
0000	100
0001	200
0010	300
0011	400
0100	500
0101	600
0110	700
0111	800
1000	900
1001	1000
1010	1100
1011	1200
1100	1300
1101	1400
1110	1500
1111	1600

Table 46. TORCH_CURRENT REGISTER

Name: TORCH_CURRENT				Address: $0E			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	TORCH_TR[1:0]		TORCH_CURRENT[3:0]			

Table 47. BIT DESCRIPTION OF TORCH_CURRENT REGISTER

Bit	Bit Description
TORCH_CURRENT[3:0]	Defines the torch current.
TORCH_TR[1:0]	Defines the torch ramp time.

Table 48. BIT DESCRIPTION OF TORCH_TR[1:0]

Register Value	TORCH_TR[1:0] (V)
00	33 mA / 64 μs
01	33 mA / 128 μs
10	33 mA / 256 μs
11	33 mA / 512 μs

Table 49. BIT DESCRIPTION OF TORCH_CURRENT[3:0]

Register Value	TORCH_CURRENT[3:0] (mA)
0000	33
0001	66
0010	100
0011	133
0100	166
0101	200
0110	233
0111	266
1000	300
1001	333
1010	366
1011	400
1100	433
1101	466
1110	500
1111	533

Table 50. PROTECTION REGISTER

Name: UVLO				Address: $0F			
Type: RW				Default: $20			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	ILIM[1:0]		UVLO_HIGH[1:0]		UVLO_LOW[1:0]	

Table 51. BIT DESCRIPTION OF PROTECTION REGISTER

Bit	Bit Description
UVLO_LOW[1:0]	Defines the UVLO low threshold.
UVLO_HIGH[1:0]	Defines the UVLO high threshold.
ILIM_CURRENT[1:0]	Defines the boost peak inductor current.

Table 52. BIT DESCRIPTION OF UVLO_LOW[1:0]

Register Value	UVLO_LOW[1:0] (V)
00	2.75
01	2.9
10	3.05
11	3.2

Table 53. BIT DESCRIPTION OF UVLO_HIGH[1:0]

Register Value	UVLO_HIGH[1:0] (V)
00	2.9
01	3.05
10	3.2
11	3.35

Table 54. BIT DESCRIPTION OF ILIM_CURRENT[1:0]

Register Value	ILIM[2:0] (A)
00	1.8
01	2.4
10	3.0
11	3.6

Table 55. FLASH_TIMER REGISTER

Name: SAFETY_TIMER				Address: $10			
Type: RW				Default: $13			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	INHIBIT_TIMER[3:0]			SAFETY_TIMER[2:0]			

Table 56. BIT DESCRIPTION OF FLASH_TIMER REGISTER

Bit	Bit Description
SAFETY_TIMER[2:0]	Defines the safety timing. (maximum flash duration)
INHIBIT_TIMER[3:0]	Defines the inhibit timing. (off duration after a flash)

Table 57. BIT DESCRIPTION OF SAFETY_TIMER[4:0]

Bit[2:0]	SAFETY_TIMER (ms)
$0	32
$1	64
$2	128
$3	256
$4	512
$5	1024

Table 58. BIT DESCRIPTION OF INHIBIT_TIMER[4:0]

Bit[3:0]	INHIBIT_TIMER(ms)
$00	512
$01	1024
$02	1536
$03	2048
$04	2560
$05	3072
$06	3584
$07	4096
$08	4608
$09	5120
$0A	5632
$0B	6144
$0C	6656
$0D	7168
$0E	7680
$0F	8192

Table 59. RED_EYE REGISTER

Name: RED_EYE				Address: $11			
Type: RW				Default: $43			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	RED_EYE_TIMEOUT	PRE_FLASH_CURRENT[3:0]				PRE_FLASH_COUNT[1:0]	

Table 60. BIT DESCRIPTION OF RED_EYE REGISTER

Bit	Bit Description
PRE_FLASH_COUNT[1:0]	Set the number of preflash pulses.
PRE_FLASH_CURRENT[3:0]	Set the preflash current.
RED_EYE_TIMEOUT	Activate or disactivate the timeout protection (2 s) between each pulses of the red eye functionality (preflash and flash pulses)

Table 61. BIT DESCRIPTION OF PRE_FLASH_COUNT[1:0]

Register Value	PRE_FLASH_COUNT
00	0
01	1
10	2
11	3

Table 62. BIT DESCRIPTION OF PRE_FLASH_CURRENT[3:0]

Register Value	PRE_FLASH_CURRENT[3:0] (mA)
0000	100
0001	200
0010	300
0011	400
0100	500
0101	600
0110	700
0111	800
1000	900
1001	1000
1010	1100
1011	1200
1100	1300
1101	1400
1110	1500
1111	1600

Table 63. FLASH_CONFIGURATION REGISTER

Name: FLASH_ENABLE				Address: $12			
Type: RW				Default: $08			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	Spare =0	Spare = 0	FLSEL_POL	TORCH_RETRY	BAT_V_SEL	DIE_TEMP_SEL

Table 64. BIT DESCRIPTION OF FLASH_CONFIGURATION REGISTER

Bit	Bit Description
DIE_TEMP_SEL	Select the low battery voltage mode. (0 = reduce mode, 1 = adaptative mode)
BAT_V_SEL	Select the die temperature monitoring mode. (0 = reduce mode, 1 = adaptative mode)
TORCH_RETRY	Enable the retry operation for the torch low battery monitoring function.
FLSEL_POL	Select the polarity of the FLSEL pin (0 = active low, 1 = active high)

Table 65. FLASH_ENABLE REGISTER

Name: FLASH_ENABLE				Address: $13			
Type: RW				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	Spare = 0	RED_EYE_EN	INHIBIT_EN	SAFETY_EN	TORCH_EN	FLASH_EN

Table 66. BIT DESCRIPTION OF FLASH_ENABLE REGISTER

Bit	Bit Description
FLASH_EN	Enable the flash mode. (flash is turn on when FLEN pin goes high)
TORCH_EN	Enable the torch mode.
SAFETY_EN	Enable the safety timer functionality.
INHIBIT_EN	Enable the inhibit timer functionality.

Table 67. FLASH_STATUS REGISTER

Name: FLASH_STATUS				Address: $14			
Type: RC				Default: $00			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TORCH_UVLO	FLASH_DIE_TEMP	FLASH_PA_BURST	FLASH_UVLO	FLASH_OVP	FLASH_SC	FLASH_TSD	FLASH_TIMEOUT

Table 68. BIT DESCRIPTION OF FLASH_STATUS REGISTER

Bit	Bit Description
FLASH_TIMEOUT	Indicates a flash timeout event.
FLASH_TSD	Indicates a flash TSD fault.
FLASH_SC	Indicates a short circuit fault.
FLASH_OVP	Indicates an OVP fault.
FLASH_UVLO	Indicates a flash UVLO event.
FLASH_PA_BURST	Indicates a PA burst blanking event.
FLASH_DIE_TEMP	Indicates a Flash TSD warning event.
TORCH_UVLO	Indicates a torch UVLO_L event.

Application Information

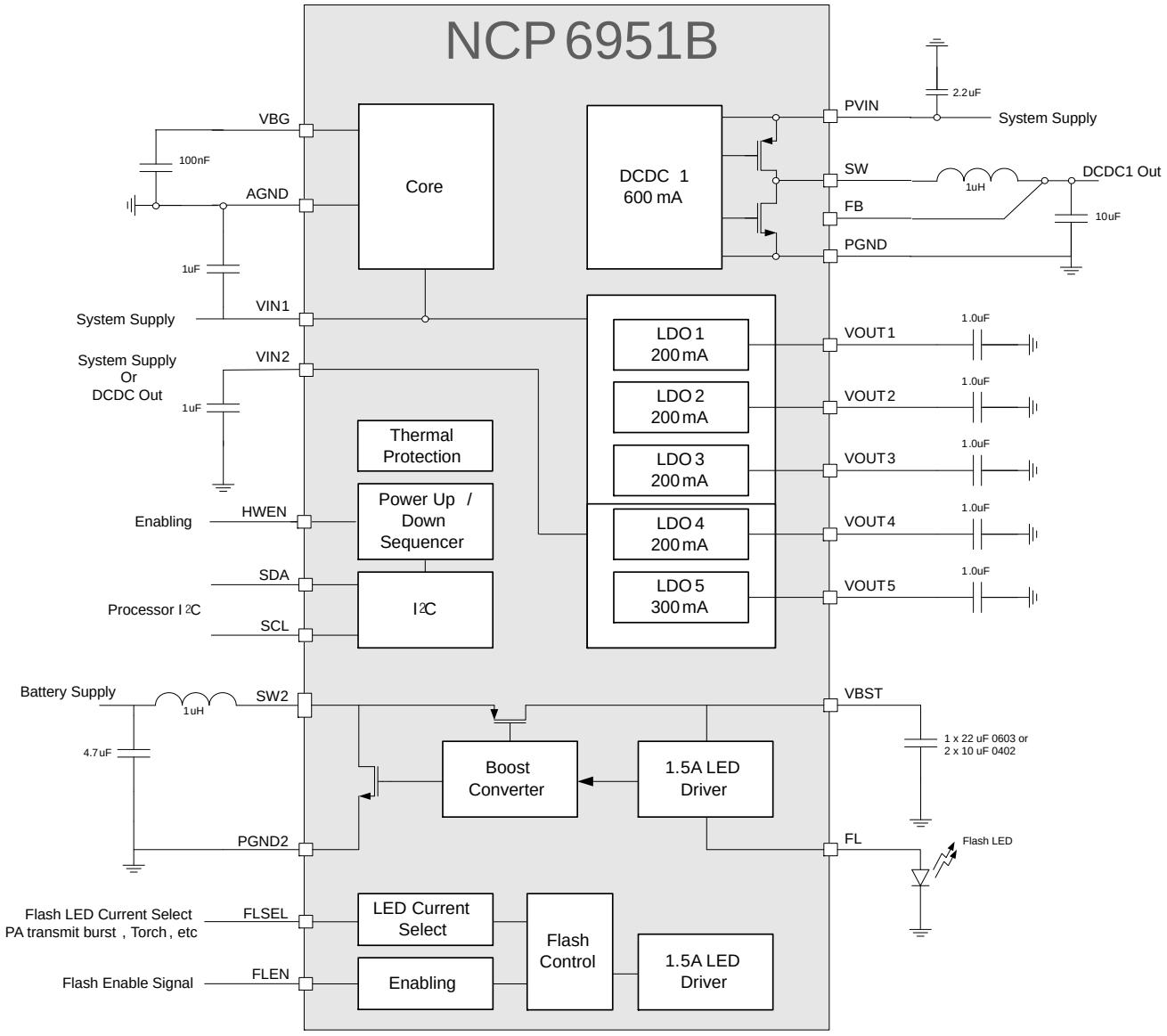


Figure 39. Typical Application Schematic

Inductor Selection

NCP6951B DCDC converters typically use 1 μH inductor. Use of different values can be considered to optimize operation in specific conditions. The inductor parameters directly related to device performances are saturation current, DC resistance and inductance value. The inductor ripple current (ΔIL) decreases with higher inductance.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \quad \text{(eq. 1)}$$

$$I_{LMAX} = I_{OMAX} + \frac{\Delta I_L}{2} \quad \text{(eq. 2)}$$

With:

- Fsw = Switching Frequency (Typical 3 MHz)
- L = Inductor value
- ΔI_L = Peak−To−Peak inductor ripple current
- I_{LMAX} = Maximum Inductor Current

To achieve better efficiency, ultra low DC resistance inductor should be selected.

The saturation current of the inductor should be higher than the I_{LMAX} calculated with the above equations.

Table 69. INDUCTOR L = 1.0 μH

Supplier	Part #	Size (mm) (L x l x T)	DC Rated Current (A)	DCR Max at 25°C (mΩ)
TOKO	DFE201610R−1R0M	2.0 x 1.6 x 1.0	2.2	66
TOKO	DFE252012R−1R0M	2.5 x 2.0 x 1.2	3.4	38
TOKO	DFE252012P−1R0M	2.5 x 2.0 x 1.2	3.8	35
MURATA	LQH44PN−1R0NP0	4.0 x 3.5 x 1.8	2.5	36
MURATA	LQM2HPN−1R0MG0	2.5 x 2.0 x 1.0	1.6	69
TOKO	FDSD0412−H−1R0M	4.2 x 4.2 x 1.2	4.7	37

Output Capacitor Selection for DC to DC converters

Selecting the proper output capacitor is based on the desired output ripple voltage. NCP6951B DCDC converters typically use 10 μF output capacitor. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode can be estimated by:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_{IN}}}{L \times F_{SW}} \times \left(\frac{1}{2 \times \pi \times C_O \times f} + ESR \right) \quad \text{(eq. 3)}$$

Table 70. RECOMMENDED OUTPUT CAPACITOR FOR DC TO DC CONVERTERS

Manufacturer	Part Number	Case Size	Height Typ. [mm]	C [μF]
MURATA	GRM188R60J106ME47	0603	0.8	10
MURATA	GRM188R60J226MEA0	0603	0.8	22
TDK	C1608X5R0C106K/M	0603	0.8	10
TDK	C1005X5R0J106M050BC	0402	0.5	10
TDK	C1608X5R0J226M080AC	0603	0.8	22

Input Capacitor Selection for DC to DC Converters

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is 1/2 of maximum output current. A low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to PVIN1 and PVIN2 pins.

Table 71. RECOMMENDED INPUT CAPACITOR FOR DC TO DC CONVERTERS

Supplier	Part Number	Case Size	Height Typ. [mm]	C [uF]
MURATA	GRM188R60J475KE	0603	0.8	4.7
MURATA	GRM188R60J106ME	0603	0.8	10
TDK	C1608X5R0C475K/M	0603	0.8	4.7
TDK	C1608X5R0C106K/M	0603	0.8	10

Output Capacitor for LDOs

For stability reason, a typical 1 μF ceramic output capacitor is suitable for LDOs. The LDO output capacitor should be placed as close as possible to the NCP6951B output pin.

Input Capacitor for LDOs

NCP6951B LDOs do not require specific input capacitors. However, a typical 1 μF ceramic capacitor placed close to LDOs' input is helpful for load transient.

Power input of LDO can be connected to main power supply. However, for optimum efficiency and lower NCP6951B thermal dissipation, the lowest voltage available in the system is preferred. Input voltage of each LDO should always be higher than V_{OUT} + $V_{LDODROP}$ (V_{DROP}, LDO dropout voltage at maximum current).

Capacitor DC Bias Characteristics

Real capacitance of ceramic capacitor changes versus DC voltage. Special care should be taken to DC bias effect in order to make sure that the real capacitor value is always higher than the minimum allowable capacitor value specified.

PCB Layout Recommendation

The high speed operation of the NCP6951B demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device, any high current copper trace which see high frequency switching should be optimized. Therefore, use short and wide traces for power current paths and for power ground tracks, power plane and ground plane are recommended if possible.

Both the inductor and input/output capacitor of each DC to DC converters are in the high frequency switching path where current flow may be discontinuous. These components should be placed as close to NCP6951B as possible to reduce parasitic inductance connection. Also it is important to minimize the area of the switching nodes and use the ground plane under them to minimize cross−talk to sensitive signals and ICs. It's suggested to keep as complete of a ground plane under NCP6951B as possible.

PGND and AGND pin connection must be connected to the ground plane. Care should be taken to avoid noise interference between PGND and AGND.

It is always good practice to keep the sensitive tracks such as feedback connection (FB1 / FB2) away from switching signal connections (SW1 / SW2) by laying the tracks on the other side or inner layers of PCB.

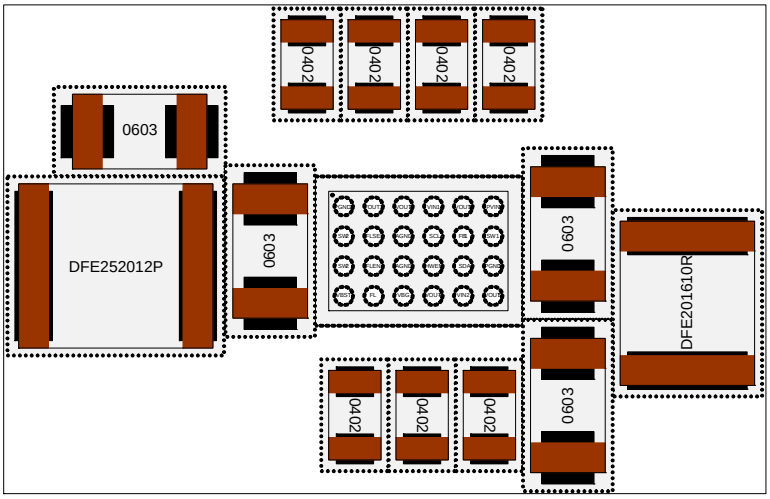


Figure 40. Recommended PCB Components Placement

Thermal Considerations

Careful attention must be paid to the power dissipation of the NCP6951B. The power dissipation is a function of efficiency and output power. Hence, increasing the output power requires better components selection. Care should be taken of LDO V_{DROP}, the larger it is, the higher dissipation it will bring to NCP6951B. Keep a large copper plane under and close to NCP6951B is helpful for thermal dissipation.

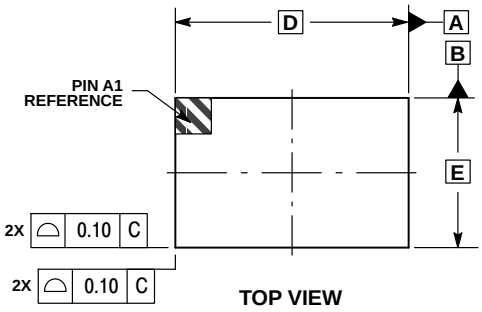
Table 72. ORDERING INFORMATIONS

Device	Marking	Package	Shipping†
NCP6951BFCCT1G	6951B	WLCSP24 (Pb−Free)	3000 / Tape & Reel

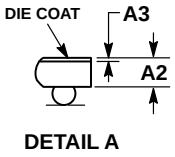
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WLCSP24, 2.57x1.65
CASE 567JA
ISSUE C



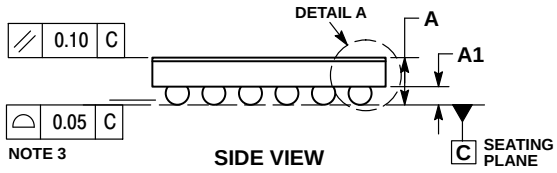
TOP VIEW



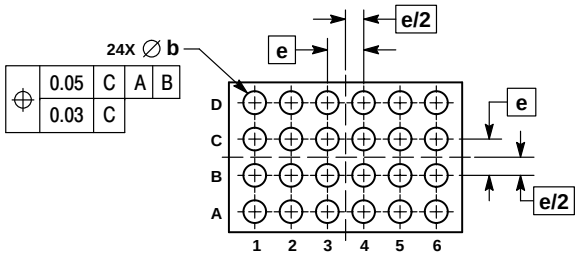
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.17	0.23
A2	0.36 REF	
A3	0.02 REF	
b	0.24	0.29
D	2.57 BSC	
E	1.65 BSC	
e	0.40 BSC	

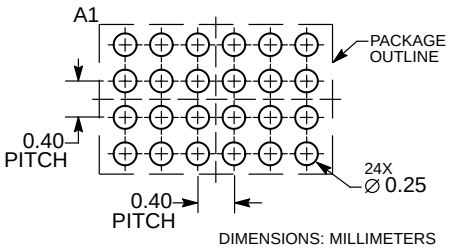


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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