DAC5681/81z/82z EVM

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1 Overview

1.1 Purpose

The DAC5681/81z/82z EVM provides a platform for evaluating the DAC5681, DAC5681z and DAC5682z family of 16-bit, 1GSPS digital-to-analog converters (DAC) under various signal, reference, and supply conditions. The evaluation module allows designers using the DAC5682z to analyze either a transformer-coupled output from the DAC or an RF-modulated output using Texas Instruments TRF3703 analog quadrature modulator. The DAC5681 and DAC5681z options only allow the use of a transformer-coupled output. Use this document with the EVM schematic diagram and the corresponding device datasheet (DAC5681 - SLLS864, DAC5681z - SLLS865A, and DAC5682z - SLLS853B).

1.2 EVM Basic Functions

Digital inputs to the DAC can be provided with LVDS level signals up to 1 GSPS through a SEMTEK connector compatible with various pattern generation solutions. The analog outputs from the DAC are available via SMA connectors. Because of its flexible design the analog outputs of the DAC device can be configured to drive a 50-Ω terminated cable using a 4:1 or 1:1 impedance ratio transformer, or single-ended referred to AVDD. The EVM also allows for an option to use Texas Instrument's TRF3703 analog quadrature modulator to mix the DAC outputs to RF. This option is only available when using the DAC5682z.

The EVM also includes a Texas Instrument's CDCM7005 clock distribution device to clock the system. The CDCM7005 can be used in conjunction with an on-board VCXO for full PLL functionality or with an external signal source in which case the CDCM7005 functions as a buffer.

Power connections to the EVM are via banana jack sockets. In addition to the internal bandgap reference provided by the DAC devices, the EVM allows an external reference to be provided to the DAC.

The DAC5681/81z/82z EVM allows the user to program the DAC and CDCM7005 registers through a USB port. The interface allows read and write access to all the DAC registers and write-only access to the CDCM7005 registers.

1.3 Power Requirements

The DAC5681/81z/82z EVM requires 1.8-Vdc and 3.3-Vdc supplies for normal operation. An additional 5-Vdc supply is required to power up the TRF3703 for RF measurements.

1.3.1 Voltage Limits

CAUTION

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

2 Software Installation

The DAC5681/81z/82z EVM comes with a software package that allows the user to configure the DAC and CDCM7005 registers, save and load register settings to/from text files, and visualize the data path through the DAC. Communication with the EVM is achieved through a USB port on the host PC. Once the software is installed, the GUI is accessible from *Start > All Programs > Texas Instruments DACs > DAC5682z EVM Control*.

2.1 Minimum Requirements

Before installing the software, verify that the PC meets the following requirements:

- Microsoft Windows™ 2000 or later operating system
- 1024 x 768 screen resolution for optimal viewing
- USB 1.1 or later compatible input port

Other configurations may work; however, they remain untested.

2.2 Installing the EVM Control Software

Double-click the setup.exe file located on the installation CD. The EVM Installation Wizard will open (Figure 1).

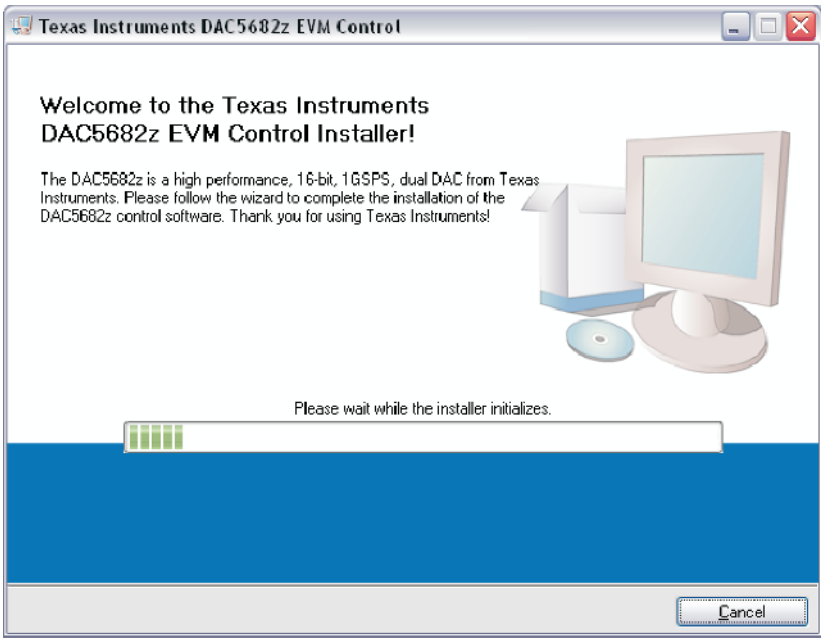


Figure 1. EVM Installation Wizard

2.3 Installing the DAC5681/81z/82z EVM Instrument Drivers

As part of the Install Wizard, the EVM instrument drivers are installed automatically. Because the USB device driver is unsigned by Windows, the warning in Figure 2 appears. Press *Continue Anyway* to complete the installation.

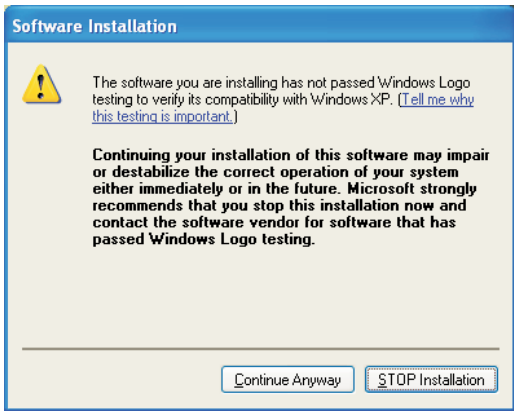


Figure 2. Windows USB Driver Warning

To finalize the installation, the Installation Wizard asks the user to restart the computer. The system must be rebooted prior to running the software.

2.4 Installing the DAC5681/81z/82z EVM Hardware

After installing the EVM control software and drivers, connect the DAC5681/81z/82z EVM to a spare USB port of the host PC. If this is the first time connecting to the device, the Windows Found New Hardware Wizard guides you through the final setup steps. If the Hardware Wizard does not start, ensure that the cable is connected properly.

Instruct the Hardware Wizard to find the software automatically. If Windows is unable to find the drivers automatically, point it to the DAC5682 program folder. The default folder is *C:\Program Files\Texas Instruments\DAC5682z\DAC5682z Drivers*. A warning indicating that the drivers are unsigned by Windows appears. Press *Continue Anyway* to complete the setup.

To verify a complete installation, open Windows Hardware Device Manager and observe that the DAC5682 EVM is listed under the USB controllers list as shown in Figure 2.

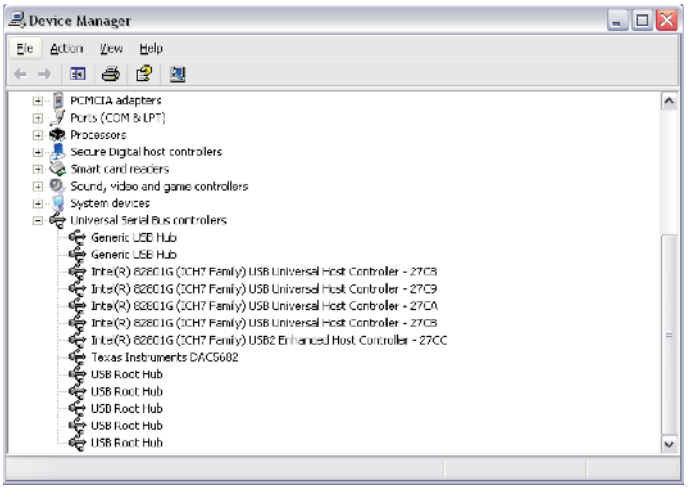


Figure 3. Hardware Device Manager

3 DAC5681/81z/82z EVM Description

The DAC5681/81z/82z EVM provides a robust and flexible evaluation system for the 16-bit, 1GSPS DAC5681/DAC5681z/DAC5682z DAC family. In addition to the DAC, the EVM includes a CDCM7005 for clock distribution and in the DAC5682z option a TRF3703 analog quadrature modulator path for RF measurements. For a complete hardware description, consult the schematics and layout sections at the end of this guide. See the DAC5681, DAC5681z, DAC5682z, CDCM7005, and TRF3703 data sheets for more information on each device.

3.1 Texas Instruments Components on the DAC5681/81z/82z EVM

A basic radio system block diagram is shown in Figure 4. The dashed-line box illustrates where the EVM fits in the system.

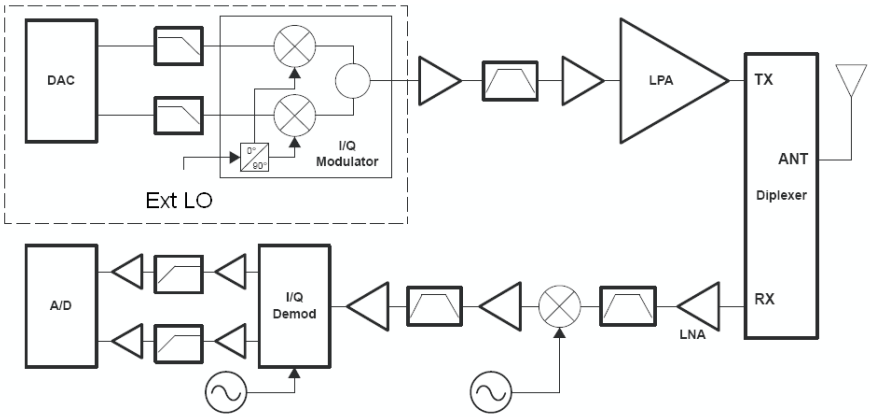


Figure 4. Basic Radio System

The block diagram of the DAC5682z EVM option is shown in Figure 5. As illustrated on the block diagram, the DAC5682z EVM option includes three Texas Instruments components that make the entire solution an excellent choice for radio systems.

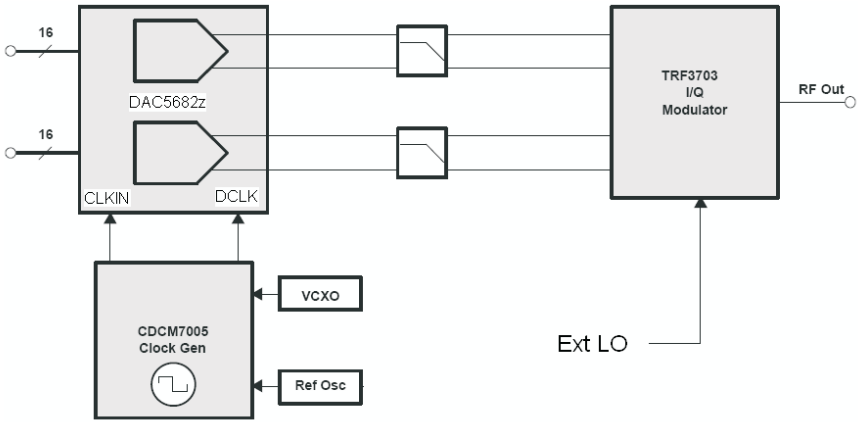


Figure 5. DAC5682z Option Block Diagram

3.1.1 DAC5681/81z/82z

The DAC5681/81z/82z is a family of high-performance, 16-bit, 1.0-GSPS DACs with wideband LVDS data input and internal voltage reference. The family integrates a wideband LVDS port with on-chip termination. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control fot the LVDS input data clock.

The DAC5681and DAC5681z are single-channel devices while the DAC5682z supports two-channels. The DAC5681z and DAC5682z include 2x/4x interpolation filters and on-board clock multiplier with superior phase noise performance. Each interpolation FIR is configurable in either Low-Pass or High-Pass mode, allowing selection of a higher order output spectral image.

The DAC5682z is the only member of the family that allows a complex output. An optional Fs/4 coarse mixer in complex mode provides coarse frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. An external RF quadrature modulator then performs the final single sideband up-conversion.

3.1.2 CDCM7005

The CDCM7005 is a high-performance, low-phase noise and low-skew clock synchronizer that synchronizes a VCXO (voltage-controlled crystal oscillator) or VCO (voltage-controlled oscillator) frequency to a reference clock. The CDCM7005 is used to generate and synchronize the clock outputs to the system. The device has five outputs which can be configured to LVPECL or LVCMOS levels and can be divided down by 1, 2, 3, 4, 6, 8, and 16. The divide by 16 can be replaced with a divide by 4 or 8 with a 90° phase shift.

3.1.3 TRF3703

The TRF3703 is a very-low-noise direct quadrature modulator, capable of converting complex modulated signals from baseband or IF directly up to RF-based on the LO frequency.

4 DAC5681/81Z/82z EVM Hardware Description

The DAC5681/81z/82z EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The demonstration board comes with the following factory-set configuration:

- No VCXO installed. CDCM7005 in buffer mode which requires an input single-ended clock signal to SMA connector J6.
- On the DAC5682z EVM outputs are set by default to drive the TRF3703. The DAC5681 and DAC5681z output is connected to J3.
- The converter is set to operate with internal reference. Jumper JP8 EXTLO is installed between pins 2 and 3.
- Full-scale output current set to 20mA through RBIAS resistor R18.

4.1 Jumper Settings

The DAC5681/81z/82z EVM has onboard jumpers that allow the user to modify the board configuration. Table 1 explains the functionality of the jumpers.

Table 1. Jumper List

Jumper	Label	Function	Condition	Default
JP8	EXTLO	Internal (GND) or external (3.3V) voltage reference	GND	Pin 2-3
JP10	VFUSE	Factory use only. Connect to 1.8VDD for normal operation.	1.8 VDD	Pin 1-2
JP12	CDC_PD	Low active power down of CDCM7005	3.3 VCLK	Pin 1-2
JP13	VCXOB	Choose internal VCXO or external VCXO INB	External VCXO	Pin 2-3
JP14	VCXO_P	Choose internal VCXO or external VCXO positive input	External VCXO	Pin 2-3
JP15	VCXO_N	Choose CDCM7005 or external VBB	CDCM7005	Pin 1-2
JP16	REF_CLK	Choose internal 10-MHz ref or external ref	Internal Ref	Pin 2-3
JP17	+3.3V_IN	Main or TP3 3.3 voltage source for CDCM7005 and USB	Main	Pin 1-2
JP19	+3.3VCLK	VCXO power down	3.3 VCLK	Pin 1-2

4.2 Input/Output Connectors

Table 2 lists the input and output connectors on the EVM.

Table 2. Input and Output Connectors

Reference Designator	Label	Connector Type	Description
J1	IOUTB2	SMA	DACB transformer output. Optional IOUTB2 output. Not populated on DAC5681/81z.
J2	IOUTB1	SMA	Optional IOUTB1 output. Not populated on DAC5681/81z.
J3	IOUTA2	SMA	DACA transformer output. Optional IOUTA2 output.
J4	IOUTA1	SMA	Optional IOUTA1 output.
J5		SEMTEK	Input LVDS data to DAC. Output clock to data source.
J6	EXT_VCXO_P	SMA	External main clock input.
J7	EXT_VCXO_N	SMA	External VCXO negative connection. Not required.
J8	Y2A_CLK	SMA	Optional CDCM7005 clock output.
J9	EXT_REF_CLK	SMA	External reference clock input.
J10	Y2B_CLK	SMA	Optional CDCM7005 clock output.
J13	USB_CONN	USB	USB connector for software communication.
J14/J15	+1.8V_IN	Banana Plug	+1.8V connection pair.
J16	RFOUT	SMA	RF output from TRF3703.
J17/J18	+3.3V_IN	Banana Plug	+3.3V connection pair.
J19/J20	+5VA_IN	Banana Plug	+5V connection pair. Required only for RF measurements.
J23	RF_LO_IN	SMA	TRF3703 LO source input. Not populated on DAC5681/81z.

4.3 USB Interface

The DAC5681/81z/82z EVM has a 4-pin USB port connector that interfaces to a USB 1.1 (or later) compliant USB port. Programming of the CDCM7005 and DAC is accomplished through this port.

4.4 Power Management

The DAC5681/81z/82z EVM requires 1.8-V and 3.3-V supplies for normal operation. An additional 5-V supply is required supply power up the TRF3073 for RF measurements.

4.5 Input Connector

The DAC5681/81z/82z EVM accepts LVDS inputs through a SEMTEK connector. These inputs drive DCLK, SYNC and D15-D0 LVDS pairs on the DAC device. An LVDS clock signal from the CDCM7005 is also output through this connector. This output clock is useful for synchronization with the pattern generation source.

Table 3. Input Connector

Pin	Description	Pin	Description
47	D15P	101	D7P
49	D15N	103	D7N
53	D14P	107	D6P
55	D14N	109	D6N
59	D13P	113	D5P
61	D13N	115	D5N
65	D12P	119	D4P

Table 3. Input Connector (continued)

Pin	Description	Pin	Description
67	D12N	121	D4N
71	D11P	125	D3P
73	D11N	127	D3N
77	D10P	131	D2P
79	D10N	133	D2N
83	D9P	137	D1P
85	D9N	139	D1N
89	D8P	143	D0P
91	D8N	145	D0N
95	DCLKP	155	SYNCP
97	DCLKN	157	SYNCN
96	Synchronizing Positive LVDS output clock	161,162,163,164,165,166,167,168,169,170,171,172	GND
98	Synchronizing Negative LVDS output clock	All others	Unused

4.6 Clock Configuration

The CDCM7005 requires a VCXO or external clock source to derive its output clock signals.

4.6.1 Buffer Mode

The DAC5681/81z/82z EVM does not come populated with a VCXO and requires an external sine wave source with a 1-Vrms, 0-V offset on SMA J6. Under this setup, the CDCM7005 operates as a buffer. To select this mode, the following changes need to be made:

1. JP13 and JP14 need to be set in position 2-3.
2. If a VCXO is installed, it is recommended to disable it by removing jumper JP19.

4.6.2 PLL Mode

A VCXO can be installed in U6 to operate the CDCM7005 as a PLL. The following changes need to be made:

1. JP13 and JP14 need to be in the 1-2 position.
2. Install jumper JP19.
3. A frequency reference (internal or external) needs to be provided.

4.7 Output Configurations

The DAC5681 and DAC5681z options are configured such that the single DAC output drives a a doubly terminated 50-Ω cable using a 4:1 impedance ratio transformer with the center tap of the transformer connected to +3.3 V. The output signal is found at SMA connector J3.

The DAC5682z EVM option has a resistor network that can be configured such that the DAC outputs are routed to the TRF3703 for an RF measurement or routed to the transformer path for a DAC measurement. The default setup on the board is for RF output.

4.7.1 DAC Outputs

To configure the DAC5682z EVM to evaluate the DAC outputs, the following changes need to be done to the board:

1. R137, R153, R155 and R156 need to be uninstalled

2. R109, R134, R135 and R136 need to be installed

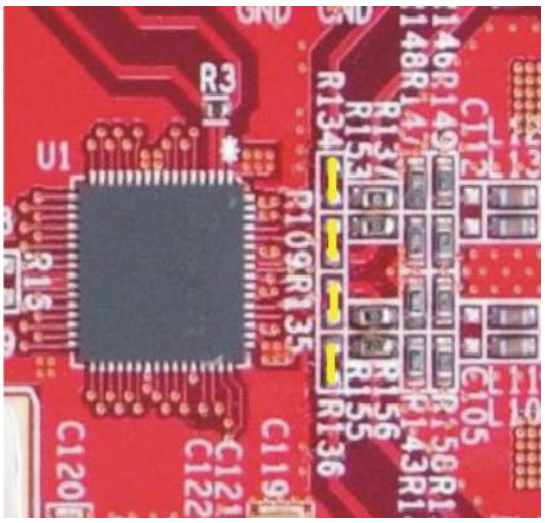


Figure 6. DAC5682Z DAC Output Resistor Configuration

If the board is configured for DAC outputs, the TRF3703 modulator is not used and the 5-Vdc supply is unnecessary. The DAC outputs in this setup are in J1 and J3.

4.7.2 RF Output

To configure the DAC5682z EVM to evaluate the RF output (default setup), the following changes need to be done to the board:

1. R137, R153, R155 and R156 need to be installed
2. R109, R134, R135 and R136 need to be uninstalled

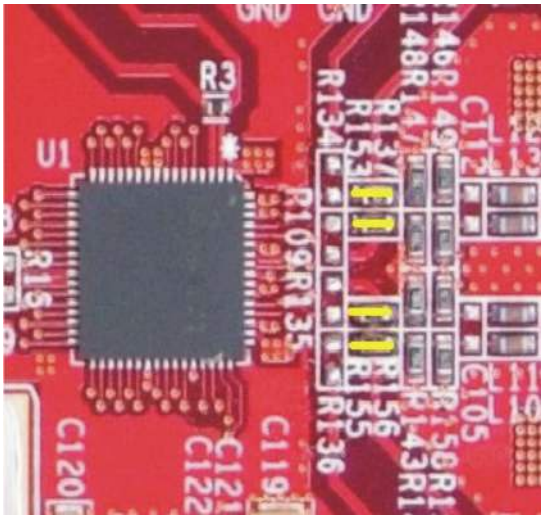


Figure 7. DAC5682z RF Output Resistor Configuration

If the board is configured for RF output, the 5-Vdc must be applied to power up the modulator. The output in this setup is in J16.

4.7.2.1 TRF3703 LO Source

The DAC5682z EVM requires an external local oscillator (LO) source to drive the onboard TRF3703 modulator. This external LO input needs to be connected to the SMA connector J23. The signal level of the LO source must comply with the requirements in the TRF3703 data sheet (SLWS184), but typically an LO power around 6-to-8 dBm is adequate.

4.7.2.2 DAC-to-Modulator Interface

The TRF3703 quadrature modulator requires a common-mode dc voltage of approximately 3.3 V. In order to use the dc-offset adjustment capabilities of the DAC5682z for carrier suppression, it is imperative to maintain a dc path from the DAC output to the modulator input. The common-mode voltage for the modulator is maintained with a passive resistor network that is designed to provide the proper operation point for the DAC5682z and the TRF3703 modulator.

The DAC5682z EVM is configured with enough pads to provide a specific fifth-order differential passive LC filter. By default, it is only populated with a simple LC low-pass filter to attenuate the higher clock harmonics. The 3-dB corner of this filter is approximately 300 MHz.

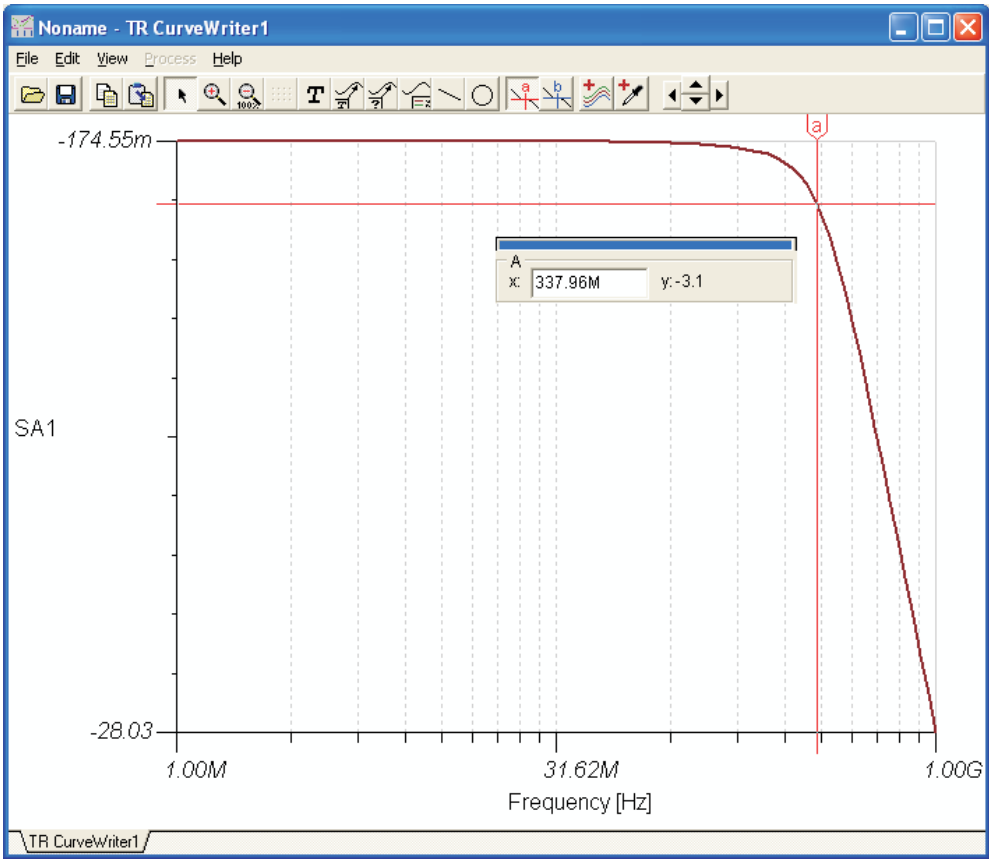


Figure 8. Response of Default Baseband Filter

The DAC5682z EVM also includes a pi pad network on the modulator output to provide some matching or filtering, if desired. In its default state, the pad is not used and a series capacitor is used on the RF output.

4.8 Reference Operation

The DAC5681/81z/82z full-scale output current is set by applying an external resistor (R18) between the BIASJ pin of the device and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying this resistor. The full-scale output current, IOUTFS, is defined as follows:

$$IOUT_{FS} = 16 \times \left(\frac{V_{EXTIO}}{R18} \right)$$

where V_{EXTIO} is the voltage at pin EXTIO. This voltage is 1.2 V when using the internally provided bandgap reference voltage source. The internal reference can be disabled and overridden by an external reference by connecting a voltage source to EXTIO and connecting EXTLO to +3.3 VA (JP8 EXTLO connected between pins 1 and 2). The specified range for external reference voltages must be observed.

5 DAC5681/81z/82z EVM Software

The EVM Control Software is started by accessing the Windows **start** → **All Programs** → **Texas Instruments DACs** cascading menus.

The DAC EVM application helps you to:

- Configure the DAC and CDCM7005 registers.
- Save and load these register settings using text files.
- Visualize the data path through the DAC
- Download a pattern to a TSW3100 Pattern Generator System (link to TSW3100 EVM folder).

5.1 Software Functionality Overview

This section provides you an overview of the software settings and functionality for the entire DAC Graphical User Interface. The software has five groups of settings that help you modify the functionality of the active panels. You can switch between these settings by selecting one of the **Menu** items described in Table 4.

Table 4. Software Main Menu Selections

Menu Item	Top Panel	Bottom Panel	Section Example Screen Functionality Reference
EVM Home	EVM and DAC serial information. EVM communication status	not applicable	Section 5.2 Figure 9 Table 6
DAC5682z Diagram	DAC Register Configuration	DAC data path under the current register settings	Section 5.3 Figure 10 Table 7
Register Config	DAC Register Configuration	CDCM7005 Register Configuration	Section 5.4 Figure 11 Table 8
TSW3100 Config	DAC Register Configuration	TSW3100 Configuration Pattern Generator display	Section 5.5 Figure 12 Table 9
Help	DAC Register Configuration	DAC data path and help window	Section 5.6

The DAC software interface controls are divided into areas. The functionality of these areas is described in Section 5.2 through Section 5.6.

Table 5. Software Area Descriptions

Area	Description
Menu	Switch between the main functionality settings described in Table 4.
DAC5682Z Home	Displays DAC part serial information and EVM status.
USB and Readback buttons	Reset the USB port to begin a new data session. Disable DAC read capabilities (simulation mode).
DAC5682z Register Table	Displays DAC register settings in binary and hexadecimal formats.

Table 5. Software Area Descriptions (continued)

Area	Description
DAC5682z Register Configuration	Read/Write DAC register configuration.
CDCM7005 Register Configuration	Write CDCM7005 register configuration (no read capability)
DAC5682z Diagram	Graphical representation of the DAC data path under current register configuration.
TSW3100 Configuration	Controls TSW3100 pattern generation system (See TSW3100 User's Guide SLLU101 for more information)
Help	Information about specific DAC register configuration GUI controls

Figure 9 through Figure 12 displays some of the Menu software areas.

5.2 EVM Home Area

The EVM Home Area includes these GUI controls:

- **Menu**—switches between the major functionality listed in Table 4 and displayed in Figure 9.
- **Home**—displays DAC part information and EVM status.
- **USB/Readback**—reset the USB port to begin a new data session. Disable DAC read capabilities (simulation mode).
- **DAC5682z Register Table**—displays DAC register settings in binary and hexadecimal formats (Figure 10 - **Regs**).

Note: The numbers on Figure 9 through Figure 12 correspond to the numbered graphical user interface subareas **(X)**, described in each table for the DAC EVM software functionality.

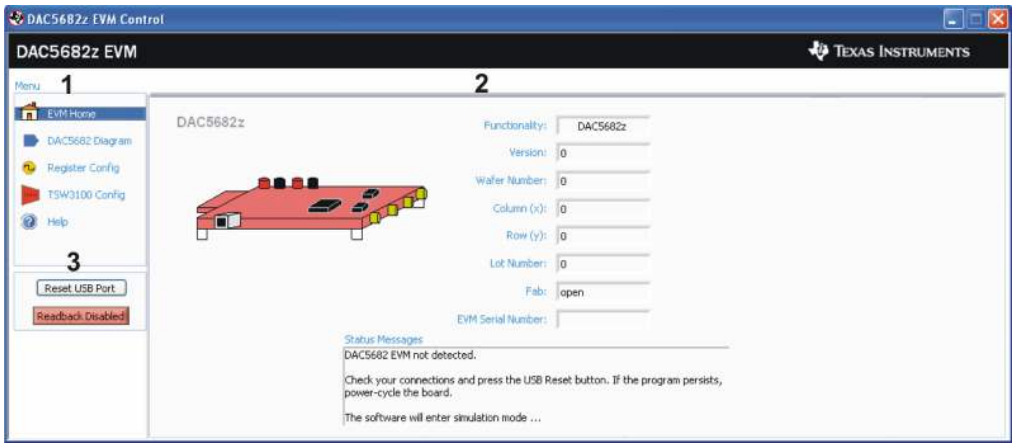


Figure 9. EVM Home Displaying EVM Status Settings

Table 6. EVM Home Software Functionality

Subarea Name	Input Output	Description
Menu Area (1)		
EVM Home	Input	DAC EVM Home area - part number information and EVM status messages
DAC5682z Diagram	Input	DAC Register Configuration and DAC5682z Diagram areas
Register Config	Input .	DAC and CDCM7005 Register Configuration areas
TSW3100 Config	Input	DAC Register Configuration and TSW3100 Configuration areas
Help	Input	Help area
DAC5682z EVM Home Area (2)		
Functionality	Output	DAC device
Version	Output	Chip version
Wafer number	Output	DAC wafer number
Column (x)	Output	DAC column position
Row (y)	Output	DAC row position
Lot Number	Output	DAC lot number
Fab	Output	Fabrication facility where the DAC was manufactured
EVM Serial Number	Output	Serial number for this EVM
Status Messages	Output	Displays the status of the communication session.
USB / Readback Area (3)		
Reset USB Port	Input	Begins a new USB session. Click this button if you see a status error message.
Readback	Input/Output	Disables DAC register reads (simulation mode)
DAC5682z Register Table Area (See Figure 10, Figure 11, and Figure 12)		
Register Table	Output	Displays the DAC register configuration in binary and hexadecimal formats for all menu settings.

5.3 DAC Register Configuration and Block Diagram

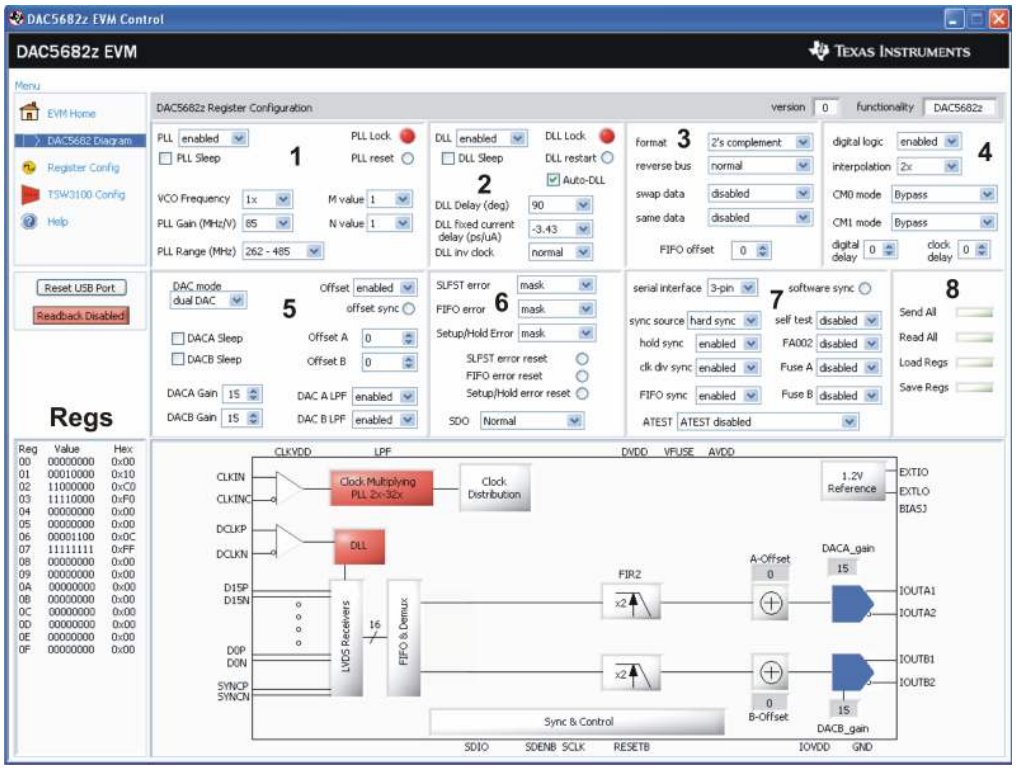


Figure 10. DAC Block Diagram and Register Configuration Settings

Table 7. DAC Register Configuration Software Functionality

Subarea Name	Input Output	Description of Functionality (GUI Setting)
PLL Settings (1)		
PLL	Input/Output	Phased-locked Loop (PLL) is bypassed (*disabled*)
PLL Sleep	Input/Output	PLL is put into sleep mode (*selected*)
PLL Lock	Output	Internal PLL is locked (*Green*)
PLL Reset	Input/Output	PLL loop filter is pulled down to 0V (*set*). Toggle to restart the PLL if an over-speed lock-up occurs.
VCO Frequency	Input/Output	PLL clock output is one-half the PLL VCO frequency (*2x*). Runs the VCO at twice the needed clock frequency to reduce phase noise for lower input clock rates.
PLL Gain (MHz/V)	Input/Output	Adjust the PLL Voltage Controlled Oscillator (VCO) gain.
PLL Range (MHz)	Input/Output	Sets the PLL VCO frequency range.
M value	Input/Output	M portion of the M/N divider of the PLL.
N value	Input/Output	N portion of the M/N divider of the PLL. This value should be chosen to divide down the input CLK_{IN} to maintain a maximum PFD of 160 MHz.
DLL Settings (2)		
DLL	Input/Output	Delay lock loop (DLL) is bypassed and LVDS data source provides correct setup and hold timing (*disabled*)
DLL Sleep	Input/Output	DLL is put into sleep mode (*selected*)
Auto-DLL	Input	DLL is restarted automatically when DLL settings change, so there is no need to press the DLL restart control (*selected*).
DLL Lock	Output	Internal DLL is locked (*Green*)
DLL restart	Input/Output	Restarts the DLL manually
DLL Delay (deg.)	Input/Output	Manually adjust the DLL delay ± from the DLL fixed current delay.

Table 7. DAC Register Configuration Software Functionality (continued)

Subarea Name	Input Output	Description of Functionality (GUI Setting)
DLL fixed current delay (ps/μA)	Input/Output	Adjusts the DLL delay line bias current. Used in conjunction with the DLL inv clock to select appropriate delay range for a given DCLK frequency
DLL inv clock	Input/Output	Inverts the internal DLL clock to force convergence to a different solution. Used when the DLL delay adjustment has exceeded the limits of its range.
Input Settings (3)		
format	Input/Output	Select *2's complement* or *offset binary* format.
reverse bus	Input/Output	Reverses the LVDS input data bus so that the MSB to LSB order is swapped (*enabled*)
swap data	Input/Output	A/B data paths are swapped prior to routing to the DACA and DACB outputs (*enabled*)
same data	Input/Output	Data routed to DACA is also routed to DACB (*enabled*)
FIFO offset	Input/Output	Sets the FIFO's output pointer location, allowing the input pointer to be shifted –4 to +3 positions upon SYNC. Default offset is *0* and is updated upon each sync event.
Digital Settings (4)		
digital logic	Input/Output	Uses the interpolation filters (*enabled*)
interpolation	Input/Output	Selects the interpolation rate.
CM0 mode	Input/Output	Determines the mode of FIR0 and CMIX0 blocks. Since CMIX0 is located between FIR0 and FIR1, its output is half-rate. Settings apply to both A and B channels.
CM1 mode	Input/Output	Determines the mode of FIR1 and final CMIX1 blocks. Settings apply to both A and B channels.
digital delay	Input/Output	DAC data delay adjustment (0–3 periods of the DAC clock). Used to adjust system level output timing. The same delay is applied to both DACA and DACB data paths.
clock delay	Input/Output	Changes the number of buffers that the input clock goes through. This allows some adjustment of the setup/hold of the handoff between the receivers and the digital section.
DAC Settings (5)		
DAC mode	Input/Output	Selects *dual DAC* mode or *single DAC* mode. Used to select input interleaved data (*dual DAC*).
DACA Sleep	Input/Output	DACA is put into sleep mode (*selected*)
DACB Sleep	Input/Output	DACB is put into sleep mode (*selected*). DACB is not automatically set into sleep mode when configured for single DAC mode. Use this control with *single DAC* mode to get the lowest power configuration for DACA output only.
DACA Gain	Input/Output	Scales the DACA output current in 16 equal steps.
DACB Gain	Input/Output	Scales the DACB output current in 16 equal steps.
Offset	Input/Output	Offset A and Offset B values are summed into the DACA and DACB data paths (*enabled*). Provides a system-level offset adjustment capability that is independent of the input data.
offset sync	Input/Output	Transfers the Offset A and Offset B values to the registers used in the DACA and DACB offset calculations. This control is enabled automatically for any change in the Offset A or Offset B values.
Offset A	Input/Output	Offset adjustment value for the A data path.
Offset B	Input/Output	Offset adjustment value for the B data path.
DAC A LPF	Input/Output	95 kHz low pass filter corner on the DACA current source bias (*enabled*). Uses a 472 Hz filter corner (*disabled*).
DAC B LPF	Input/Output	95 kHz low pass filter corner on the DACB current source bias (*enabled*). Uses a 472 Hz filter corner (*disabled*).
Error Settings (6)		
SLFST Error	Input/Output	Masks out SLFTST Errors.
FIFO Error	Input/Output	Masks out FIFO Errors.
Setup/Hold Error	Input/Output	Masks out Setup/Hold Errors.
SLFST error reset	Input/Output	Asserted when the Digital Self Test (SLFTST) fails. Clear to reset a SLFST error.
FIFO error reset	Input/Output	Asserted when the FIFO pointers overrun each other, causing a sample to be missed. Clear to reset a FIFO error.
Setup/Hold error reset	Input/Output	Any received data pattern other than 0xAAAA or 0x5555 causes this bit to be set. Clear to reset a Setup/Hold error.
SDO	Input/Output	Selects the signal polarity on the SDO pin (*normal* or *inverted*)
SYNC Settings (7)		
serial interface	Input/Output	Selects *3-pin* or *4-pin* serial interface mode.

Table 7. DAC Register Configuration Software Functionality (continued)

Subarea Name	Input Output	Description of Functionality (GUI Setting)
sync source	Input/Output	Selects the synchronization signal source. If *soft sync* is selected the software sync control is used as the only synchronization input and the LVDS external SYNC input pins (*hard sync*) are ignored.
software sync	Input/Output	Substitute for the LVDS external SYNC input pins for both synchronization and transmit enable control.
hold sync	Input/Output	Enables the sync to the FIFO output HOLD block.
clk div sync	Input/Output	Enables the clock divider sync.
FIFO sync	Input/Output	Enables the FIFO offset sync.
self test	Input/Output	Enables a Digital Self Test (SLFTST) of the core logic.
FA002	Input/Output	Keep *disabled*. Used only for factory test purposes.
Fuse A	Input/Output	Keep *disabled*. Used only for factory test purposes.
Fuse B	Input/Output	Keep *disabled*. Used only for factory test purposes.
ATEST	Input/Output	Keep *disabled*. Used only for factory test purposes.
SEND/SAVE Button Settings (8)		
Send All	Input	Writes all registers to the DAC device.
Read All	Input	Reads all registers from the DAC device. It is rarely necessary to use this as the registers are read every time a DAC control changes.
Load Regs	Input	Loads a DAC register configuration from a text file. Files need to consist of a single column with the register values in hexadecimal format.
Save Regs	Input	Saves a DAC register configuration to a text file.

5.4 CDCM7005 Register Configuration

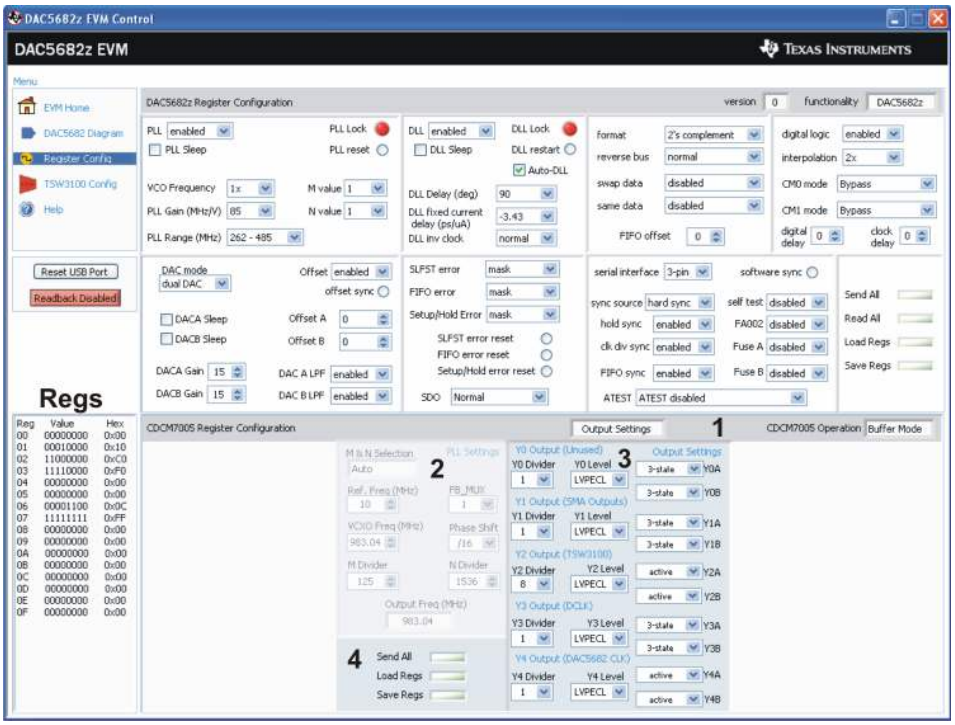


Figure 11. The CDCM7005 and DAC5682 Register Configuration Settings

Table 8. CDCM7005 Register Configuration Software Functionality

Subarea Name	Input Output	Description
General Settings (1)		
Output Settings	Input	Switches the display between the CDCM7005 *output settings* and advanced settings.
CDCM7005 Operation	Input	Select *Buffer Mode* when there is no VCXO installed or the VCXO is enabled. In this case the CDCM7005 operates as a buffer. Select *PLL Mode* when a VCXO is being used by the CDCM7005.
PLL Settings (2)		
M & N Selection	Input	(*Auto*) M and N divider values are calculated automatically based on Reference and VCXO frequencies.
Ref. Freq. (MHz)	Input	Frequency of the reference oscillator given to the CDCM7005.
VCXO Freq. (MHz)	Input	Frequency of the VCXO used.
M Divider	Input/Output	M divider value.
N Divider	Input/Output	N divider value.
FB_MUX	Input/Output	Feedback MUX select.
Phase Shift	Input	Phase shift select.
Output Freq (MHz)	Output	Output frequency of the CDCM7005 based on the Reference and VCXO frequencies, and M and N values. If Output Freq differs from VCXO Freq, Output Freq displays using a red text.
Output Settings (3)		
Y0-Y4 Dividers	Input	Selects the output dividers of the CDCM7005 outputs.
Y0-Y4 Levels	Input	Selects between CMOS or LVPECL levels of the CDCM7005 outputs.
Y0-Y4 States	Input	Selects the operating state of the CDCM7005 outputs.
SEND/SAVE Button Settings (4)		
Send All	Input	Writes all registers to the DCDM7005 device.
Load Regs	Input	Loads a DCDM7005 register configuration from a text file. Files need to consist of a single column with the register values in hexadecimal format.
Save Regs	Input	Saves a DCDM7005 register configuration to a text file.
Advanced Settings (not shown)		
Advanced Registers		Input CDCM7005 advanced registers. See the CDCM7005 data sheet (SCAS793) for more information about these registers.

5.5 TSW3100 Configuration and Pattern Generation

The TSW3100 can be loaded with a custom pattern file using the GUI options. For further details on the file format of the custom pattern, see the TSW3100 Users Guide (SLLU101).

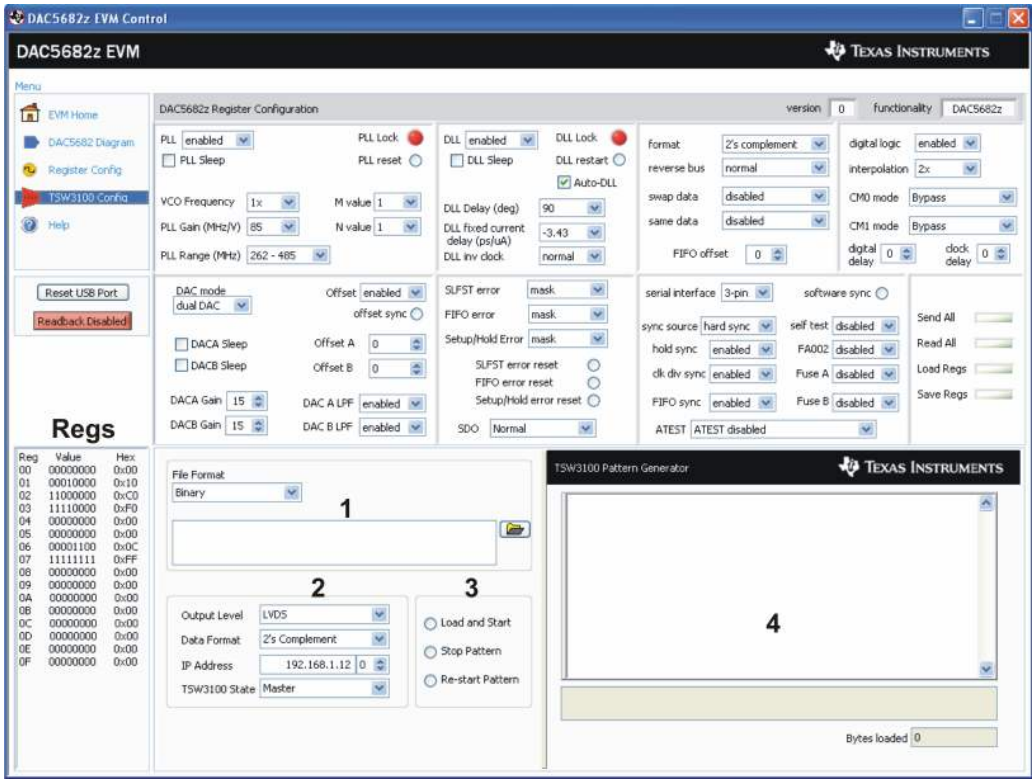


Figure 12. TSW3100 Pattern Generator and DAC Register Configuration Settings

Table 9. TSW3100 Configuration and Pattern Generation Functionality

Subarea Name	Input Output	Description
Pattern Selection (1)		
File Format	Input	Selects *Binary* and 16-bit signed *Integer* format. If Binary is selected, the file must comply with the requirements described on the TSW3100 (SLLU101) documentation. If integer format is selected, the file must consist of a single column for a real signal or two columns for a two-channel or complex signal.
Browse Button	Input	Navigate to the folder containing the input pattern file name. Select the file to use.
Output Mode (2)		
Column Delimiter	Input	Column separator used in the two-channel or complex integer input file. (Not displayed)
Output Level	Input	*LVDS* or *CMOS* outputs. Only *LVDS* is available for the DAC5682z.
Data Format	Input	*2's complement* or *offset binary* format.
IP Address	Input	Specify final digit (1, 2, 3, or 4) of the IP address for the TSW3100 pattern generator.
TSW3100 State	Input	*Master* or *Slave* mode. The default state is *Master* mode. See TSW3100 (SLLU101) documentation for more information.
Command Buttons (3)		
Load and Start	Input	Load a pattern file and start the TSW3100.
Stop Pattern	Input	Stop the pattern transfer.
Re-start Pattern	Input	Re-start the pattern. A pattern must be loaded in memory for this command to work.
Pattern Generation Results (4)		
Command	Output	Shows sequence of commands sent to the TSW3100.

Table 9. TSW3100 Configuration and Pattern Generation Functionality (continued)

Subarea Name	Input Output	Description
Status	Output	Status of the TSW3100 transaction.
Bytes loaded	Output	Number of bytes loaded to the TSW3100.

5.6 Help

When you select the the **Help** menu item, the DAC Diagram screen (Figure 10) and a detached, pop-up Help text window display. As you move the cursor over the DAC Diagram GUI controls, the context-sensitive help text changes in the pop-up window.

6 DAC5681/81z/82z Initial Power Up and Test

6.1 Test Setup Block Diagram

The recommended test setup for the EVM is shown in Figure 13. In this setup the Texas Instruments TSW3100 pattern generator solution is used to supply the LVDS input data.

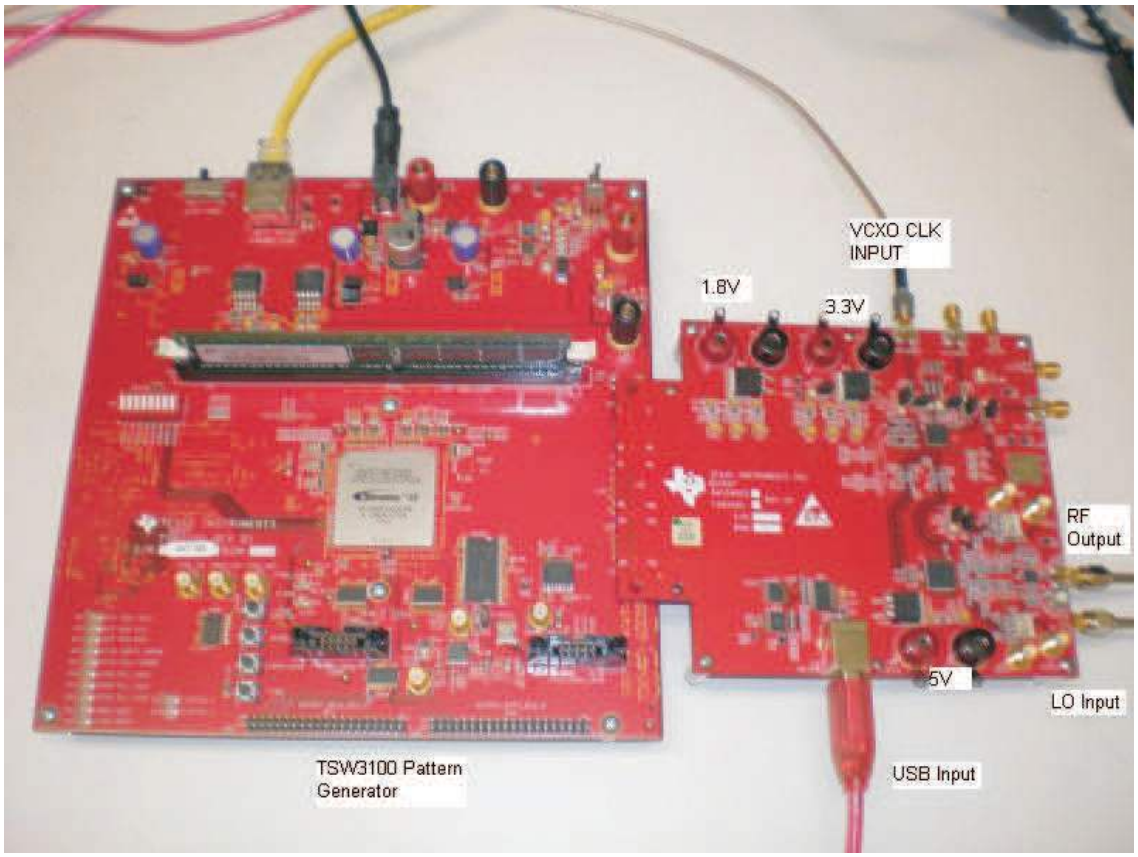


Figure 13. DAC5682z EVM Driven by TSW3100 Pattern Generator

6.2 Test Equipment

The test equipment listed below is required to evaluate the EVM. Other equipment may be substituted, however results may vary due to instrument limitations.

- Power supplies—1.8 V (DAC digital), 3.3 V (DAC analog), and 5 V (RF modulator)
- Spectrum Analyzer—Rhode & Schwarz FSU, FSQ, or equivalent. This is necessary to measure the noise floor ACPR greater than 70 dBm with the noise correction option.
- Pattern generator—TSW3100 using LVDS mode, or some other LVDS capable generator.
- Oscilloscope—probe clock and data lines for troubleshooting.
- Digital volt meter—verify signal levels.

6.3 Calibration

To measure the proper output power, the insertion loss of the analyzer cable must be calibrated. Measure a calibrated 0 dBm source to see how much loss is in the cable at the frequency of interest.

6.4 Typical Performance Measurements

The DAC5681, DAC5681z and DAC5682z measurements at the transformer outputs J1 and J3 will have better performance than the RF output at low output frequencies. The RF output is typically limited by the performance of the RF parts. In this case the DAC output at 0 IF or low IF is several dB better than the noise floor of the modulator output at J16.

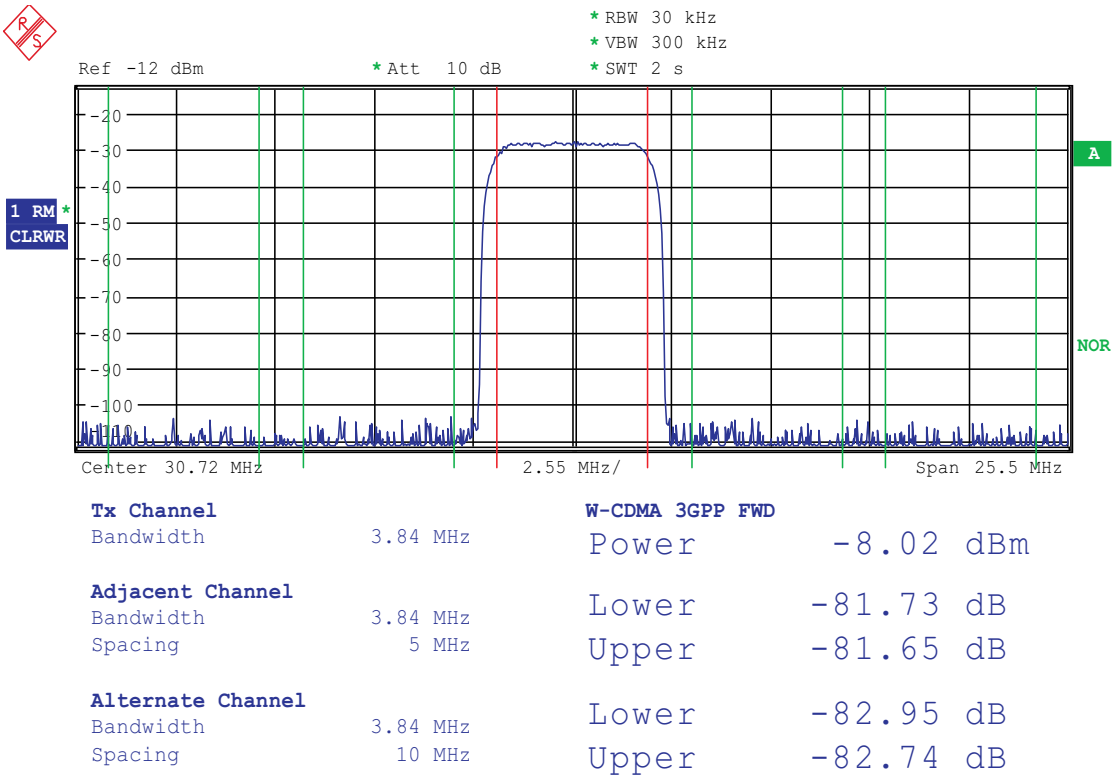


Figure 14. DAC5681/81z/82z EVM Transformer Output With a Low IF at 30.72 MHz

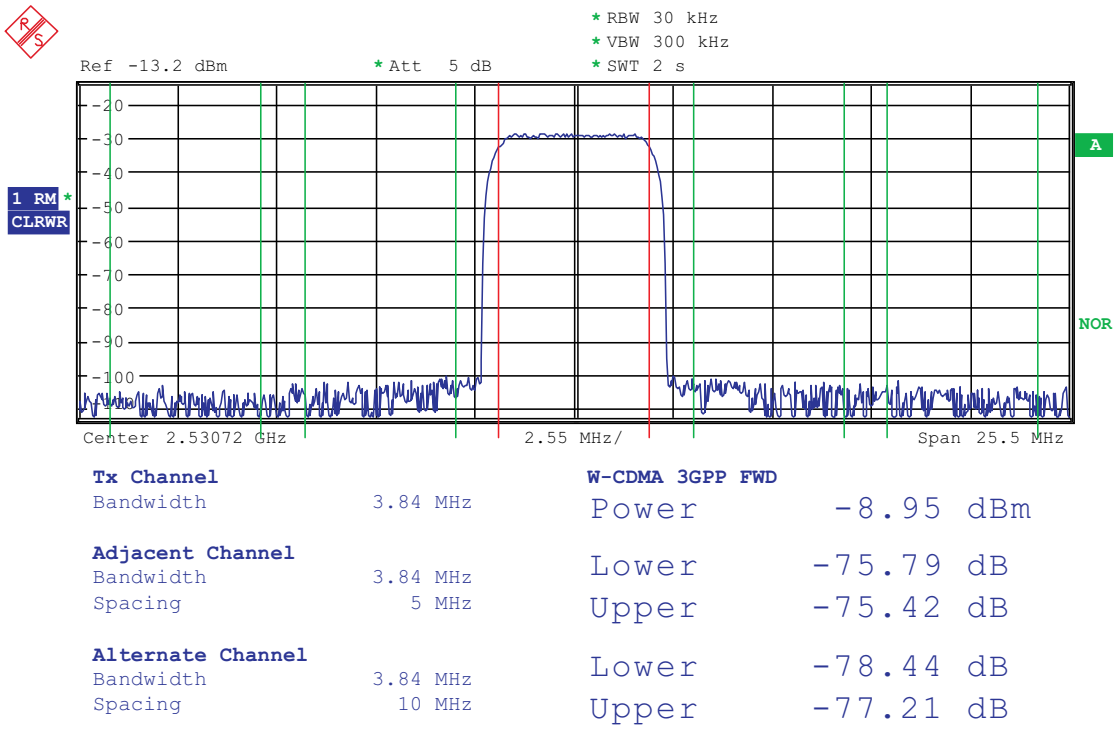


Figure 15. DAC5682z EVM output at RF LO + low IF of 30.72M (6 dB lower than DAC output)

6.5 DAC5681/81z/82z Test Procedure

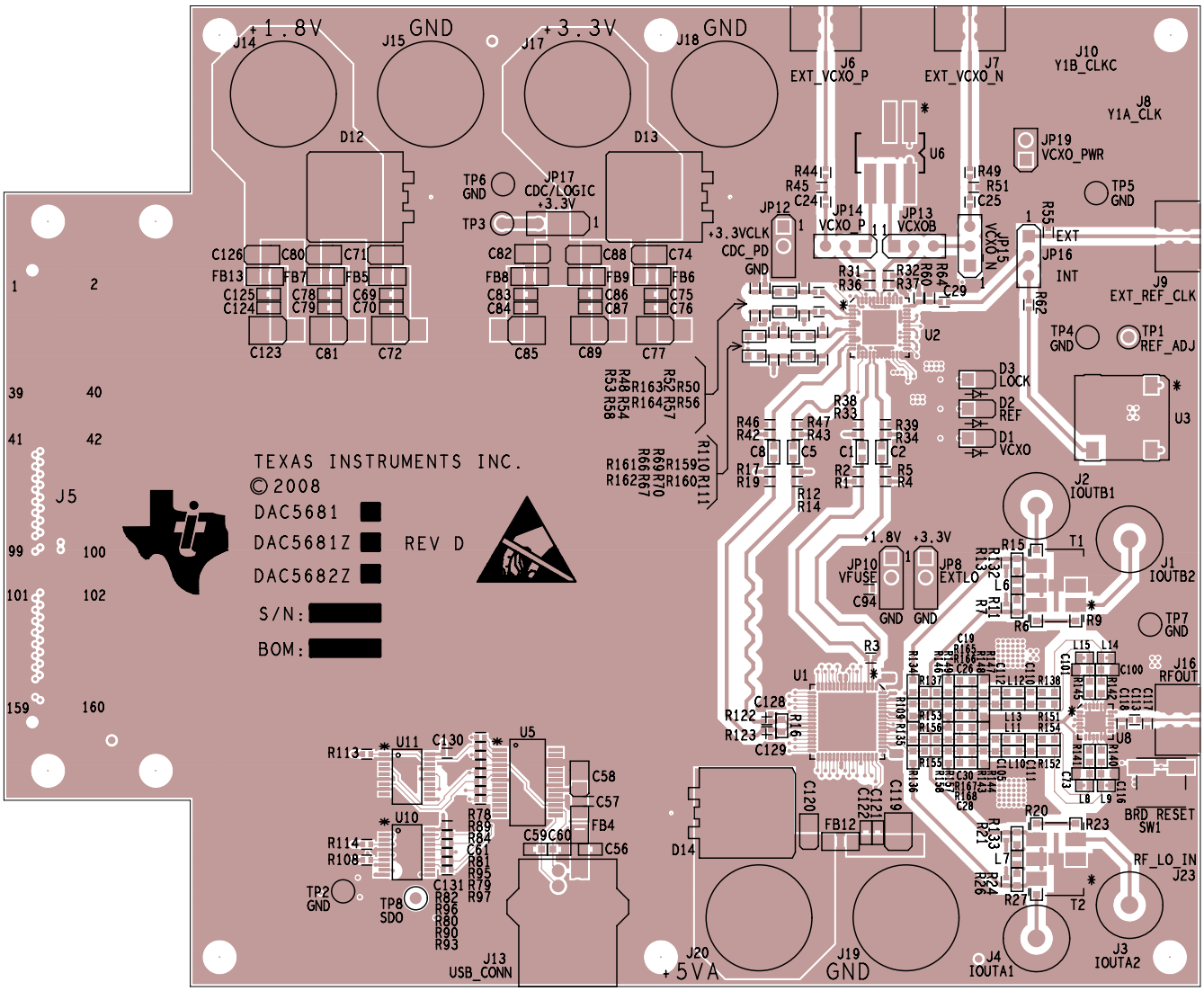
The steps described in this section show how to connect and configure the DAC5681/81z/82z EVM for evaluation under the default settings.

1. Connect the DAC5681/81z/82z EVM SEMTEK connector to a digital test pattern generator that supports this interface such as Texas Instruments TSW3100.
2. Connect the 1.8-V (J14/J15) and 3.3-V (J17/J18) power supplies. If using the modulator the 5-V (J19/J20) supply also needs to be connected. Ensure that each supply is not drawing more than 1-A of current.
3. Provide a single-ended, 1-Vrms, 0-V, offset sine-wave signal to the EVM EXT_VCXO_P (J6) SMA connector. LED D1 should illuminate indicating that a signal has been detected. If not, verify that the correct signal is being provided.
4. If testing at RF (DAC5682z EVM option) provide a 6-dBm LO signal to the RF_LO_IN (J23) SMA connector.
5. Connect one end of the supplied USB cable to an available USB port on the host PC. Connect the other end of the cable to J13 on the EVM.
6. Open the DAC5682z EVM software. The DAC software detects if the USB port is active and if it is capable of reading the EVM serial number. The **EVM Home** menu (Figure 9 and Table 6) of the DAC8652z GUI software provides this status information.
7. Program the CDCM7005 and DAC registers as necessary. An example configuration file is included under the installation folder: *C:\Program Files\Texas Instruments\DAC5682z\DAC5682z Configuration Files*
8. Program and run the pattern generator. If using the TSW3100, see the user's guide for more information on how to set up a digital pattern.
9. Analyze the DAC or RF output using an spectrum analyzer.

7 PC Board Layouts, Bill of Materials and Schematics

This section contains the PC-board layouts, bill of materials and schematics for the DAC5681/81z/82z EVM.

7.1 Board Layouts



TEXAS INSTRUMENTS
DAC5682Z EVM
REV D
LAYER 1 (TOP SIDE)
SILKSCREEN TOP

Figure 16. Silkscreen (top)

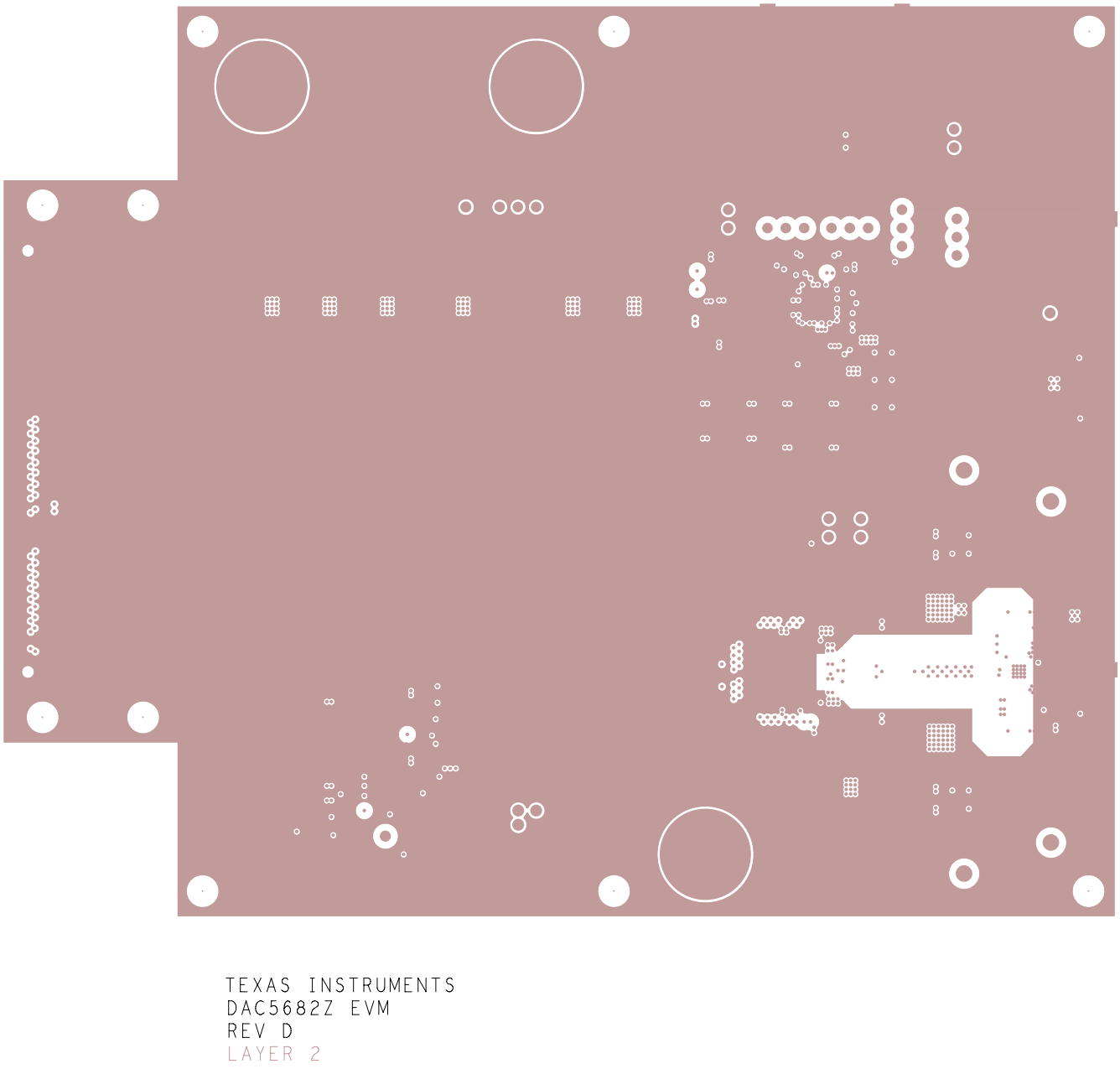


Figure 17. Layer 2

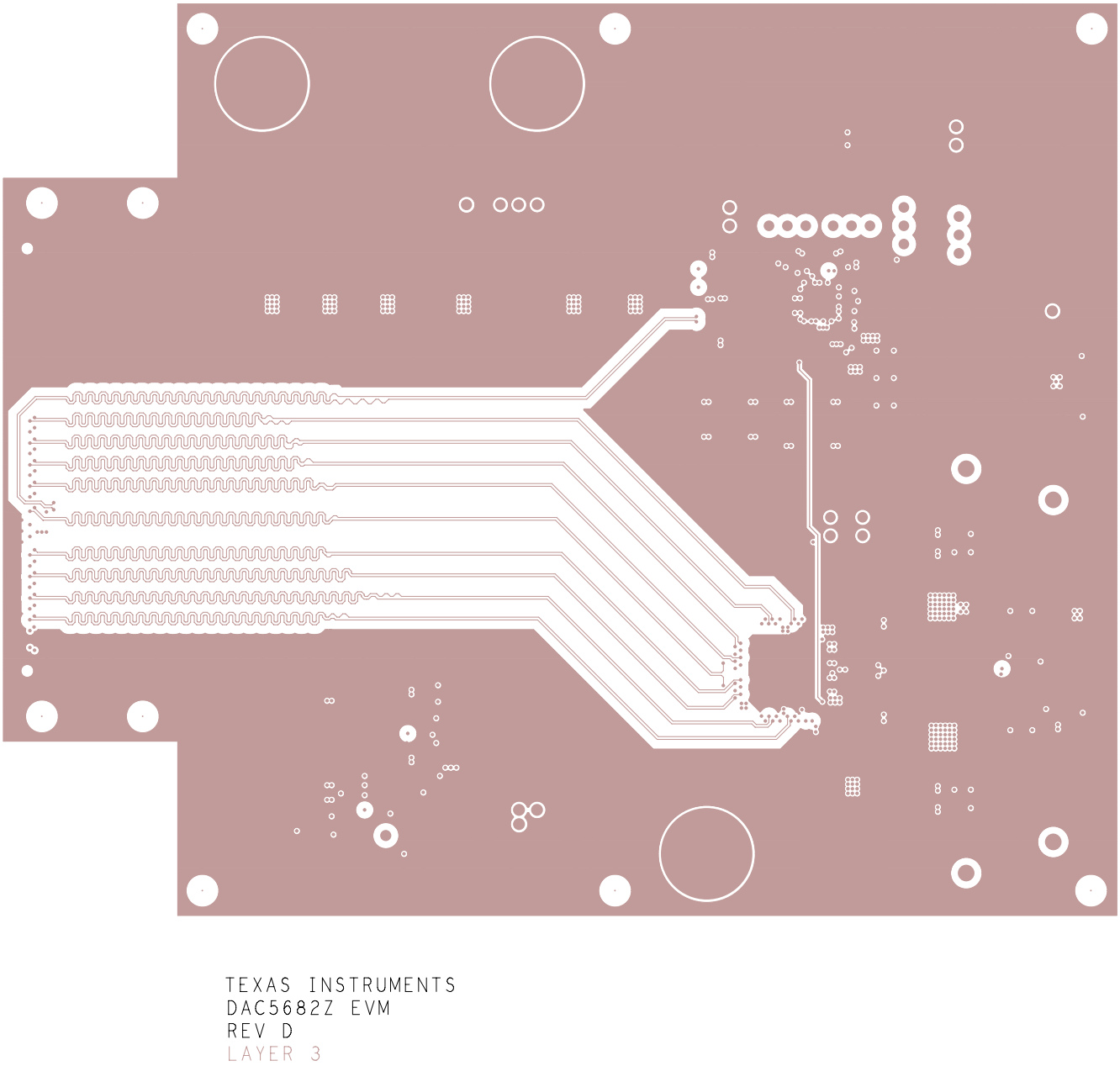


Figure 18. Layer 3

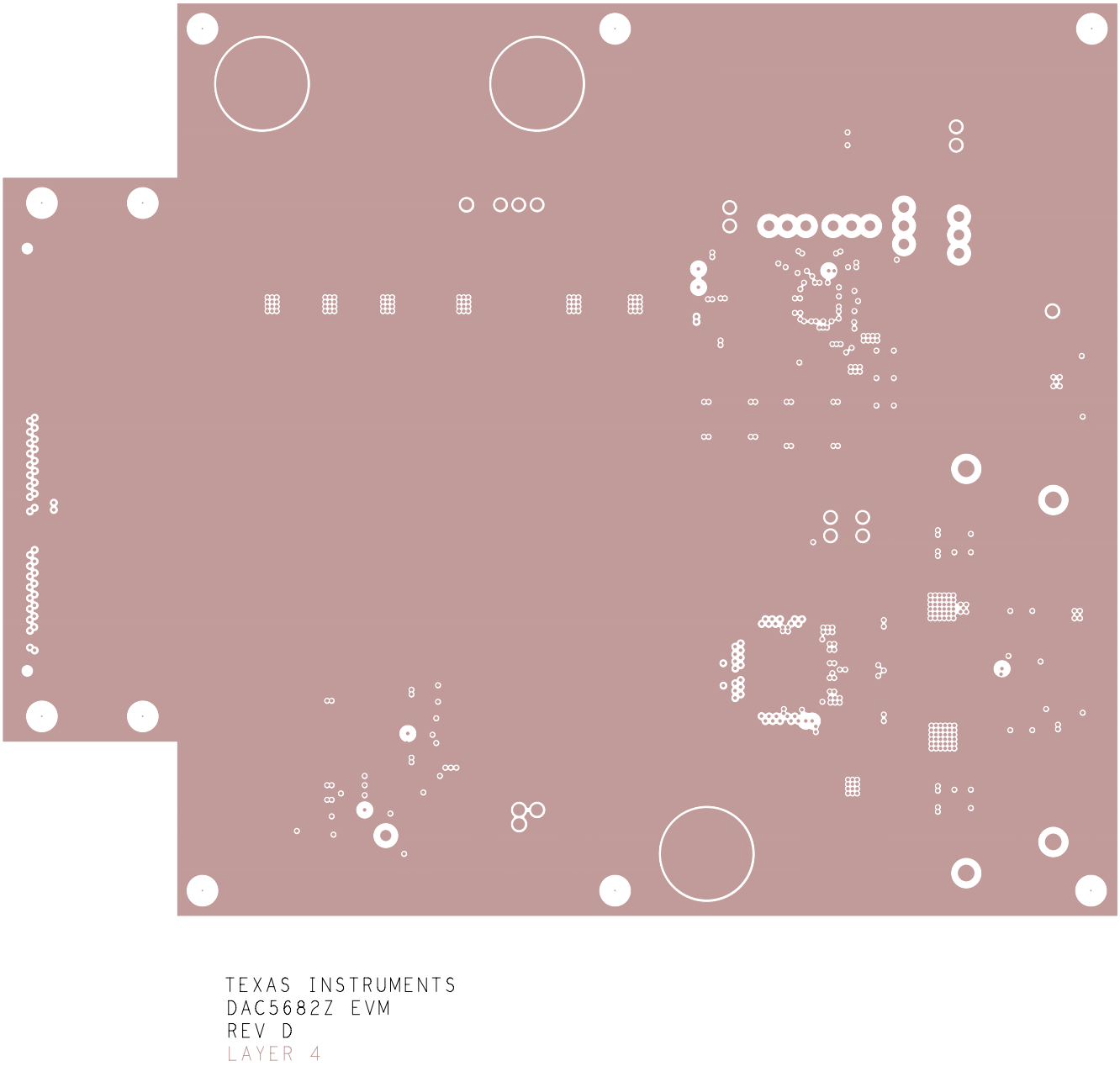


Figure 19. Layer 4

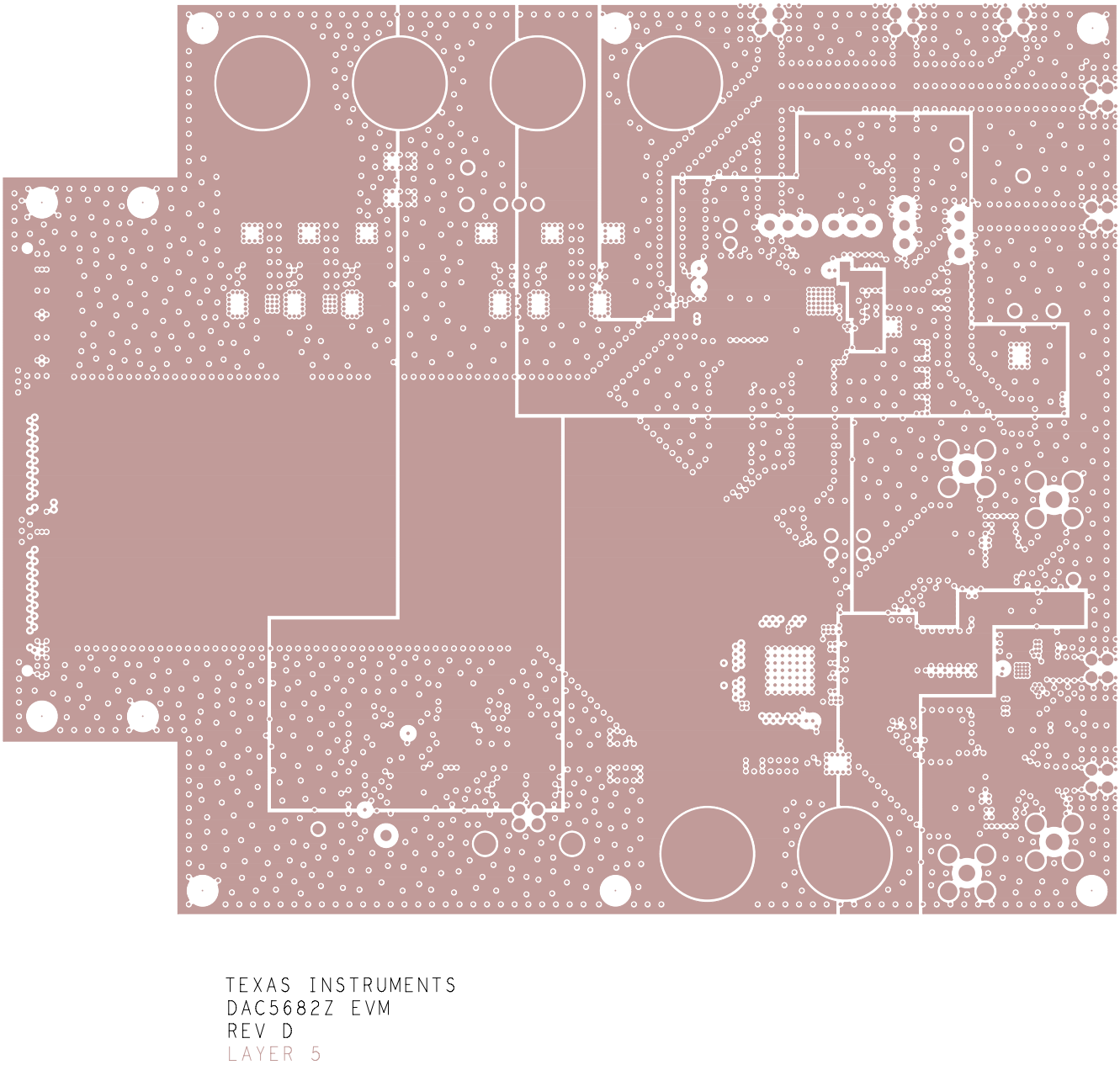


Figure 20. Layer 5

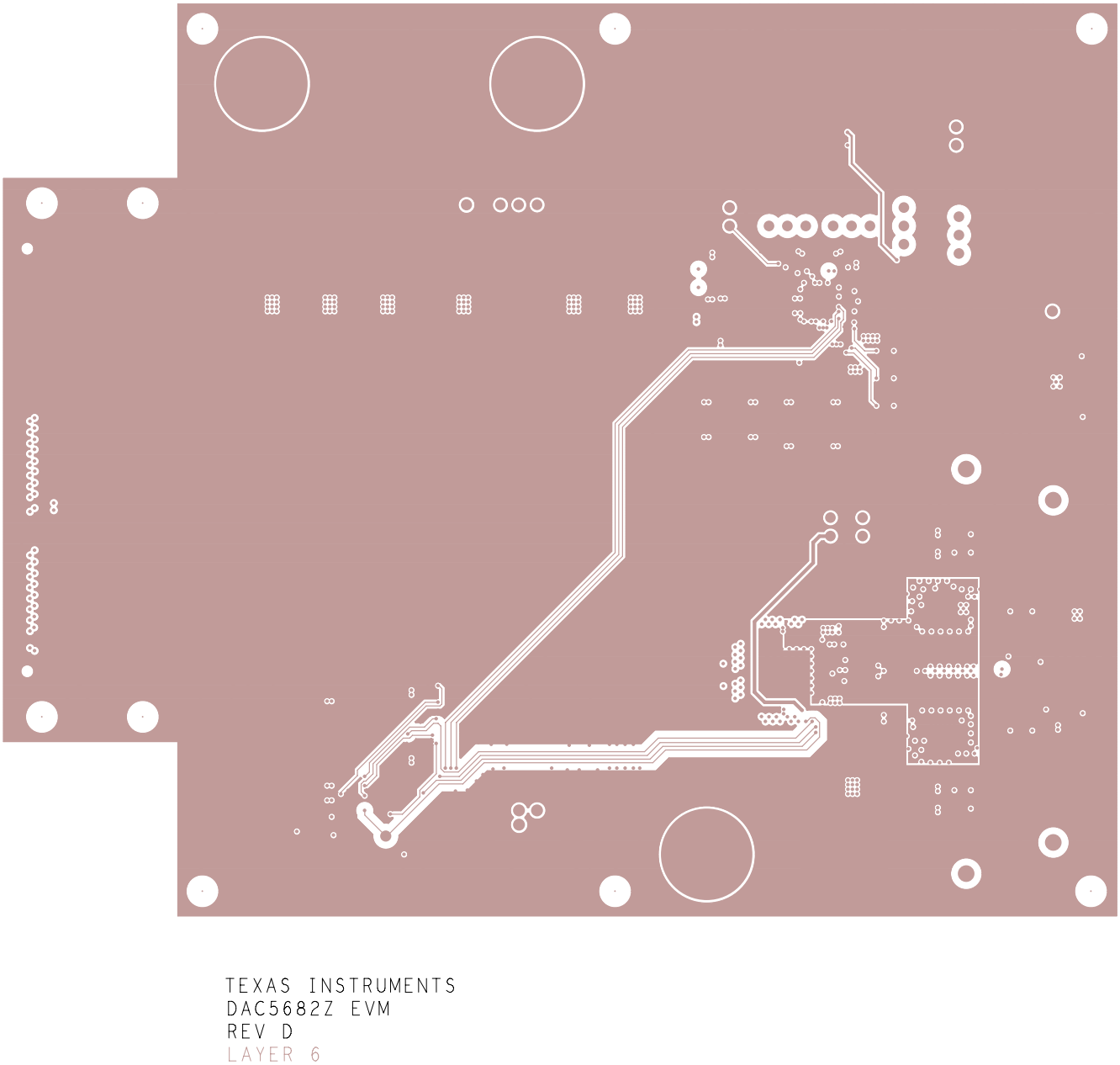


Figure 21. Layer 6

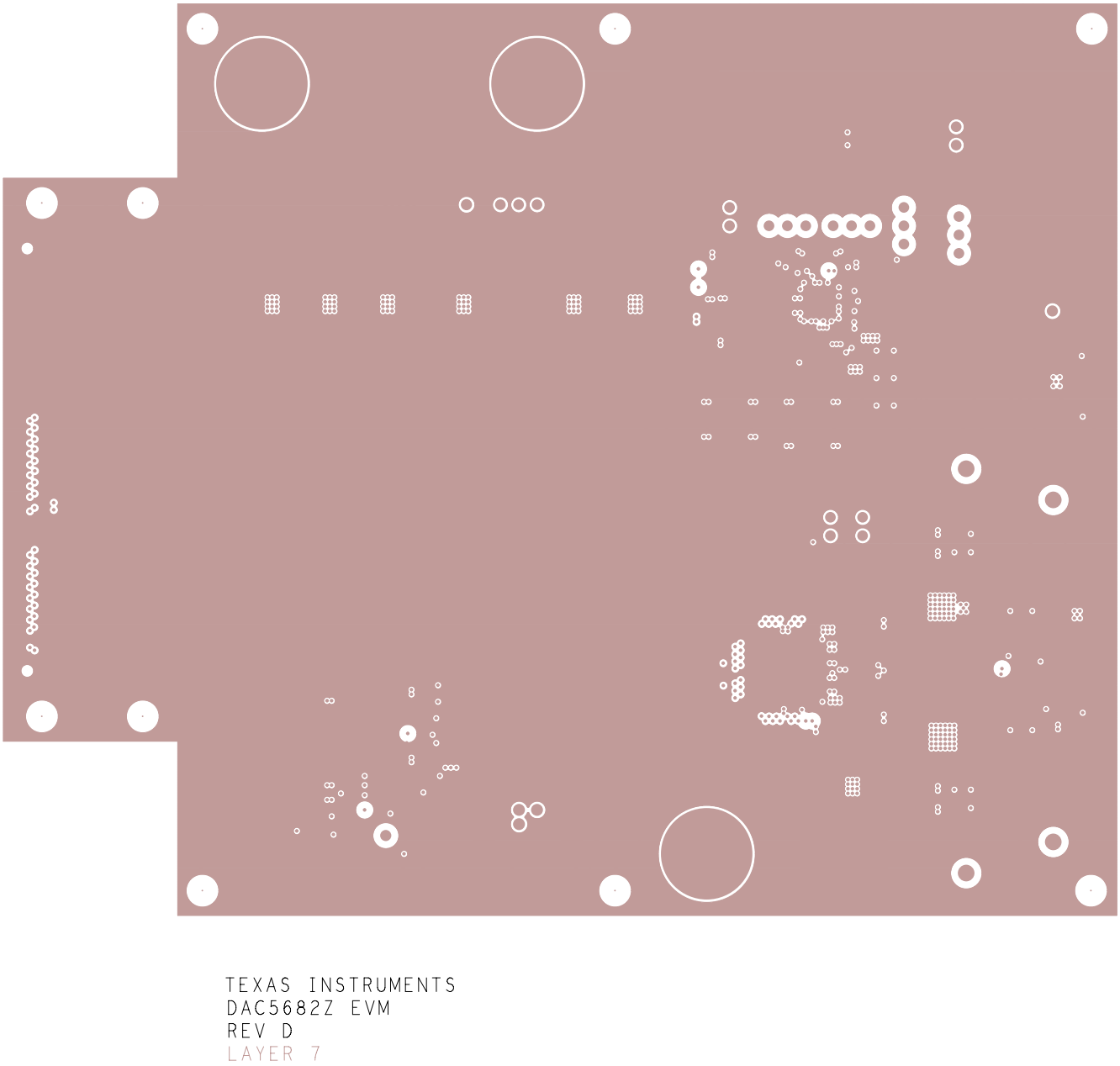


Figure 22. Layer 7

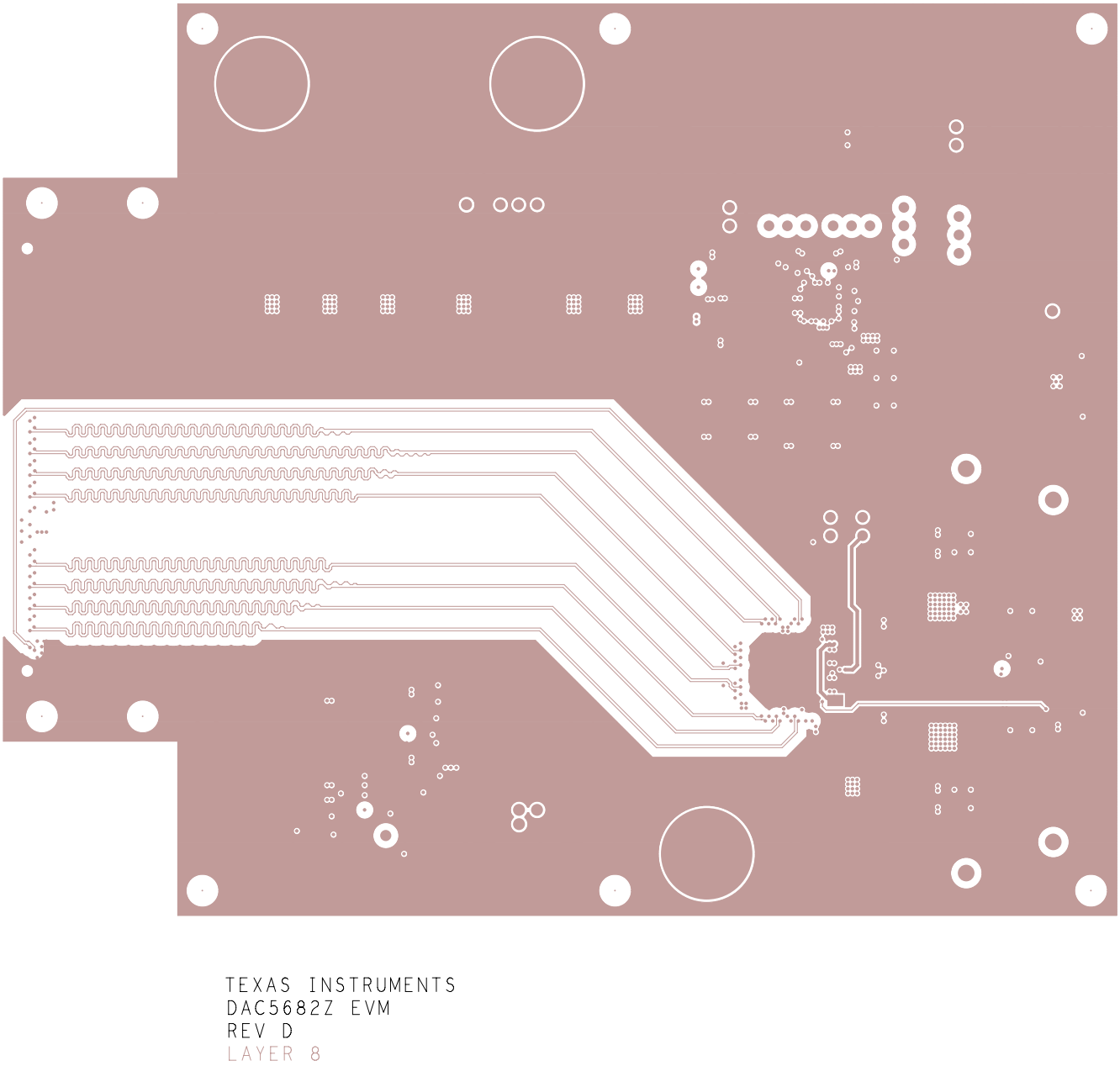


Figure 23. Layer 8

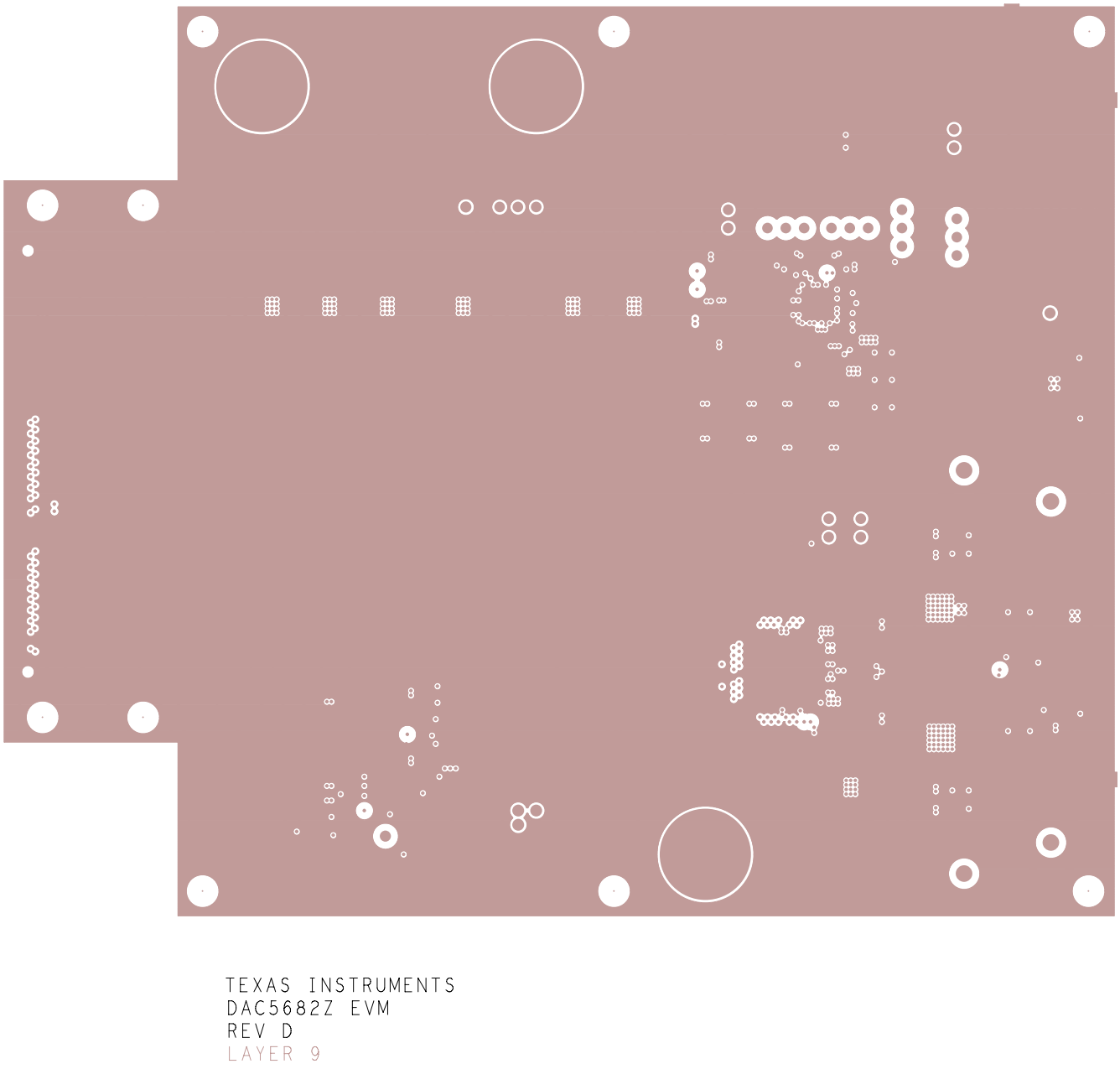
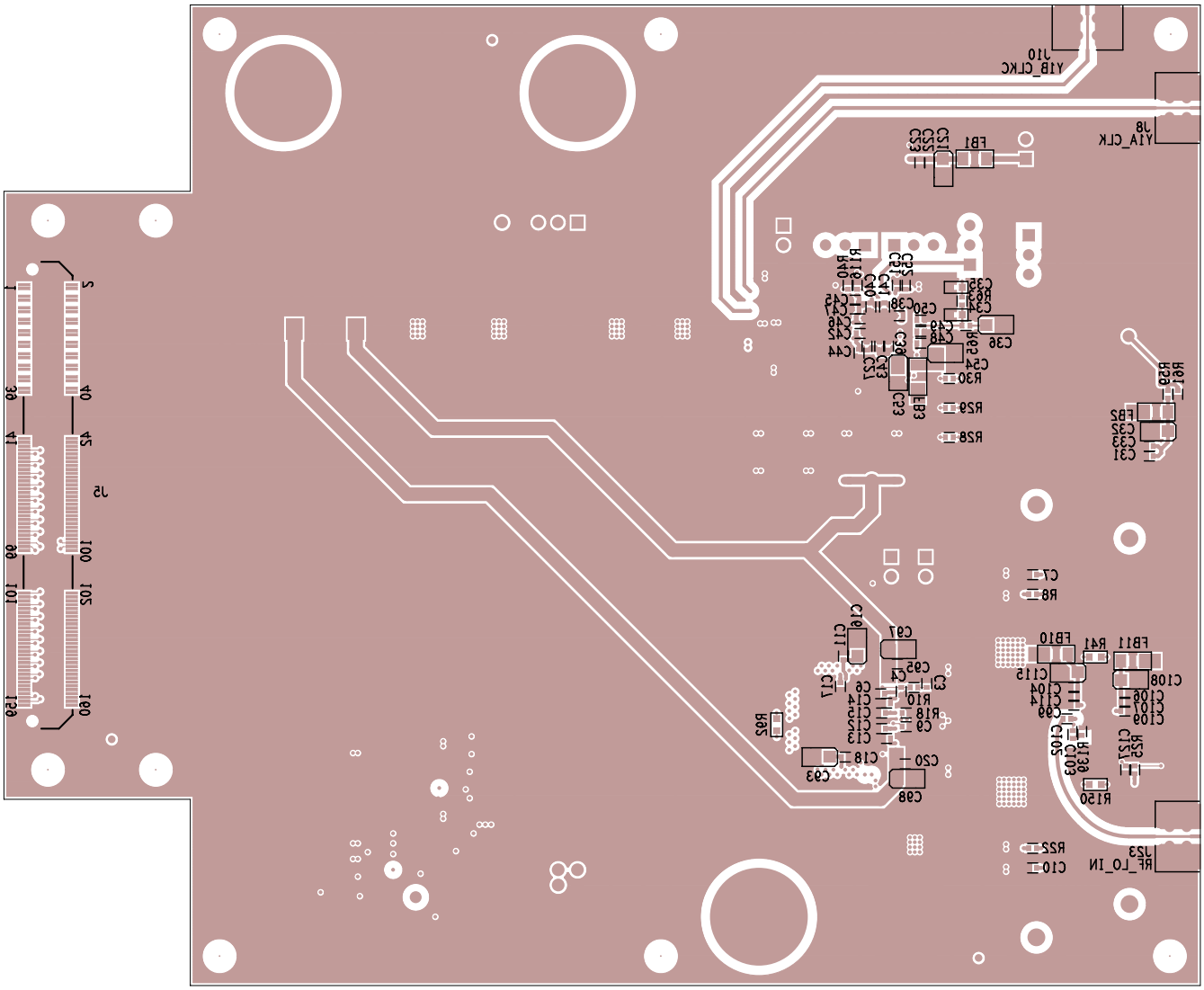


Figure 24. Layer 9



TEXAS INSTRUMENTS
DAC5682Z EVM
REV D
LAYER 10 (BOTTOM SIDE)
SILKSCREEN BOTTOM

Figure 25. Screen (Bottom)

7.2 Bill of Materials

QTY.	Part Reference	Value	PCB Footprint	MFR. Name	MFR. Part Number	Note
12	C1 C2 C5 C8 C56 C70 C76 C79 C84 C87 C121 C124	0.01 µF	0603	Panasonic	ECJ-1VB1C103K	
1	C3	0.15 µF	0402	Murata	GRM36X5R154K10H520	
6	C4 C29 C48 C104 C106 C127	1000 pF	0402	Panasonic	ECJ-0EB1E102K	
38	C6 C7 C9-C15 C17 C18 C20 C23-C25 C27 C33 C38-C47 C50-C52 C57 C61 C94 C95 C107 C114 C130 C131	0.1 µF	0402	Panasonic	ECJ-0EB1C104K	
16	C16 C21 C32 C36 C53 C54 C71 C74 C80 C82 C88 C93 C97 C98 C120 C126	10 µF	tant_a	Kermet	T494A106M016AS	
0	C19 C26 C28 C30	0.01 µF	0603	Panasonic	ECJ-1VB1C103K_DNI	DNI
1	C22	560 pF	0402	Panasonic	ECJ-0EB1H561K	
2	C31 C113	100 pF	0402	Panasonic	ECJ-0EB1E101K	
8	C34 C69 C75 C78 C83 C86 C122 C125	1 µF	0603	Panasonic	ECJ-1V41E105M	
1	C35	0.47 µF	0603	Murata	GRM188R71C474KA88D	
3	C49 C128 C129	0.01 µF	0402	Panasonic	ECJ-0EB1E103K	
3	C58 C108 C115	4.7 µF	tant_a	AVX	TAJA475K020R	
2	C59 C60	47 pF	0603	Panasonic	ECJ-1VC1H470J	
7	C72 C77 C81 C85 C89 C119 C123	47 µF	tant_b	Kemet	T494B476M010AS	
0	C73 C100 C101 C116	4.7 pF	0603	Panasonic	ECJ-1VC1H047C_DNI	DNI
2	C99 C109	3.3 pF	0402	Murata	GRM1555C1H3R3CZ01D	
2	C102 C103	22 pF	0402	Panasonic	ECJ-0EC1H220J	
0	C105 C112	2.2 pF	0603	AVX	06035A2R2CAT2A_DNI	DNI
2	C110 C111	2.7 pF	0603	AVX	06035A2R7CAT2A	
0	C117 C118	0.01 µF	0402	Panasonic	ECJ-0EB1E103K_DNI	DNI
3	D1-D3	LED green	LED_0805	Panasonic	LNJ306G5UUX	
3	D12-D14	MBRB2515L	DIODE_MBRB2515L	ON Semiconductor	MBRB2515LT4G	
13	FB1-FB13	68 Ω at 100 MHz	1206	Panasonic	EXC-ML32A680U	
4	J1-J4	SMA_PCB_THVT	SMA_THVT_312x312	Johnson Components	142-0701-201	
7	J6-J10 J16 J23	SMA_END_JACK_RND	SMA_SMEL_218x247_096	Johnson Components	142-0761-801	
1	J13	USB_B_S_F_B_TH	CON_THRT_USB_B_F	SAMTEC	USB-B-S-F-B-TH	
3	J14 J17 J20	BANANA_JACK_RED	CON_THVT_BANANA_JACK_250DIA	SPC Technology	845-R	
3	J15 J18 J19	BANANA_JACK_BLK	CON_THVT_BANANA_JACK_250DIA	SPC Technology	845-B	
1	J5	ASP-122952-01	CON_SMVT_160POS_ASP_122952	SAMTEC	ASP-122952-01	
4	JP8 JP13 JP14 JP16	Jumper_1x3_100_430L	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.230	(SHUNT 2-3)
4	JP10 JP12 JP15 JP17	Jumper_1x3_100_430L	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.230	(SHUNT 1-2)
1	JP19	Jumper_1x2_100_430L	HDR_THVT_1x2_100_M	SAMTEC	HMTSW-102-07-G-S-.230	
0	L6 L7	56 nH	IND_0603	Panasonic	ELJ-RE56NJF3_DNI	DNI
4	L8 L9 L14 L15	10 nH	IND_0603	Coilcraft	0603CS-10NXLU	
4	L10-L13	68 nH	0603	Coilcraft	0603CS-68NXJL	
0	R1 R2 R4 R5 R12 R14 R17 R19	1K	0402	Panasonic	ERJ-2RKF1001X_DNI	DNI
10	R3 R7 R13 R21 R26 R80 R82 R90 R93 R96	100	0402	Panasonic	ERJ-2RKF1000X	
0	R6 R9 R15 R20 R23 R27 R109 R134-R136	0	0603	Panasonic	ERJ-3GEY0R00V_DNI	DNI
5	R8 R22 R44 R49 R62	0	0402	Panasonic	ERJ-2GE0R00X	
1	R10	93.1	0402	Panasonic	ERJ-2RKF93R1X	
0	R11 R24 R132 R133	60.4	0603	Yageo	RC0603FR-0760R4L_DNI	DNI
0	R16	100	0603	Panasonic	ERJ-3EKF1000V_DNI	DNI
1	R18	953	0402	Panasonic	ERJ-2RKF9530X	
1	R25	1K	0402	Panasonic	ERJ-2RKF1001X	
3	R28-R30	750	0402	Panasonic	ERJ-2RKF7500X	
8	R31-R34 R42 R43 R66 R67	130	0402	Panasonic	ERJ-2RKF1300X	

QTY.	Part Reference	Value	PCB Footprint	MFR. Name	MFR. Part Number	Note
8	R36-R39 R46 R47 R69 R70	82.5	0402	Panasonic	ERJ-2RKF82R5X	
2	R40 R116	150	0402	Panasonic	ERJ-2RKF1500X	
2	R41 R150	90.9	0603	Panasonic	ERJ-3EKF90R9V	
0	R45 R51 R122 R123	0	0402	Panasonic	ERJ-2GE0R00X_DNI	DNI
0	R48 R54	130	0402	Panasonic	ERJ-2RKF1300X_DNI	DNI
9	R50 R56 R78 R79 R81 R84 R89 R95 R97	22.1	0402	Panasonic	ERJ-2RKF22R1X	
0	R52 R57 R110 R111	150	0402	Panasonic	ERJ-2RKF1500X_DNI	DNI
0	R53 R58	82.5	0402	Panasonic	ERJ-2RKF82R5X_DNI	DNI
0	R55	49.9	0402	Panasonic	ERJ-2RKF49R9X_DNI	DNI
7	R59-R61 R64 R108 R113 R114	10K	0402	Panasonic	ERJ-2RKF1002X	
1	R63	162	0402	Panasonic	ERJ-2RKF1620X	
1	R65	4.75K	0402	Panasonic	ERJ-2RKF4751X	
1	R92	100	0603	Panasonic	ERJ-3EKF1000V	
18	R137 R140-R142 R145 R153 R155 R156 R159-R168	0	0603	Panasonic	ERJ-3GEY0R00V	
4	R138 R151 R152 R154	60.4	0603	Yageo	RC0603FR-0760R4L	
1	R139	49.9	0402	Panasonic	ERJ-2RKF49R9X	
4	R143 R144 R147 R148	634	0603	Yageo	RC0603FR-07634RL	
4	R146 R149 R157 R158	115	0603	Yageo	RC0603FR-07115RL	
1	SW1	SW RESET	SW_SMVT_RESET	C&K	KT11P3JM	
2	T1 T2	ADT4-1T	TFMR_6_250x340_100	Mini-Circuits	ADT4-1T	
8	TP1-TP8	Testloop_Black	TP_THVT_060_RND	Components Corporation	TP-105-01-00	
1	U1	DAC5681/81Z/82Z	QFN_64_360x360_0p50mm_pwrpad	Texas Instruments	DAC5681,81Z,82Z	TI
1	U2	CDCM7005	QFN_48_281x281_0p50mm_pwrpad	Texas Instruments	CDCM7005RGZT	TI
1	U3	OSC-VECTRON	OSC_4_SM_460x386	Vectron	VTD3-J0BC-10M000	TI
1	U5	FT245RL	SSOP_28_413x220_26	FTDI Chip	FT245RL	
0	U6	2115-491.52MHZ	VCXO_6	Toyocom	TCO-2111-491.52_DNI	DNI
1	U8	TRF3703-33	QFN_24_163x163_0p50mm_pwrpad	Texas Instruments	TRF3703-33IRGET	TI
1	U10	SN74AHC541PW	TSSOP_20_260x177_26	Texas Instruments	SN74AHC541PW	TI
1	U11	SN74HC241PW	TSSOP_20_260x177_26	Texas Instruments	SN74HC241PW	TI
4	Z_SCREW1-Z_SCREW4	SCREW PANHEAD 4-40 x 3/8		Building Fasteners	PMS 440 0038 PH	SCREW FOR STANDOFF
8	Z_SH-H1-Z_SH-H6 Z_SH-H9 Z_SH-H10	SHUNT-HEADER		Keltron	MJ-5.97-G	SHUNT FOR HEADER
4	Z_STANDOFF1-Z_STANDOFF4	STANDOFF ALUM HEX 4-40 x 0.500		Keystone	2203	STANDOFF

Notes:

1. DNI = DO NOT INSTALL
2. SHUNT 2-3
3. SHUNT 1-2
4. SCREW FOR STANDOFF
5. SHUNT FOR HEADER
6. STANDOFF

7.3 Schematics

The DAC5681/81z/82z schematics are appended to the end of this document.

NOTES:

1) DNI = DO NOT INSTALL

2) FOR DAC5681/81Z OPTION:

SHEET 1
R109,R134,R135,R136 ARE INSTALLED
R7 AND R13 = 0 OHMS
R8,C7,T1,J1,J2 = DNI

SHEET 6
ALL COMPONENTS ARE DNI

U1
DAC5681/81Z/82Z

ADT4-1T

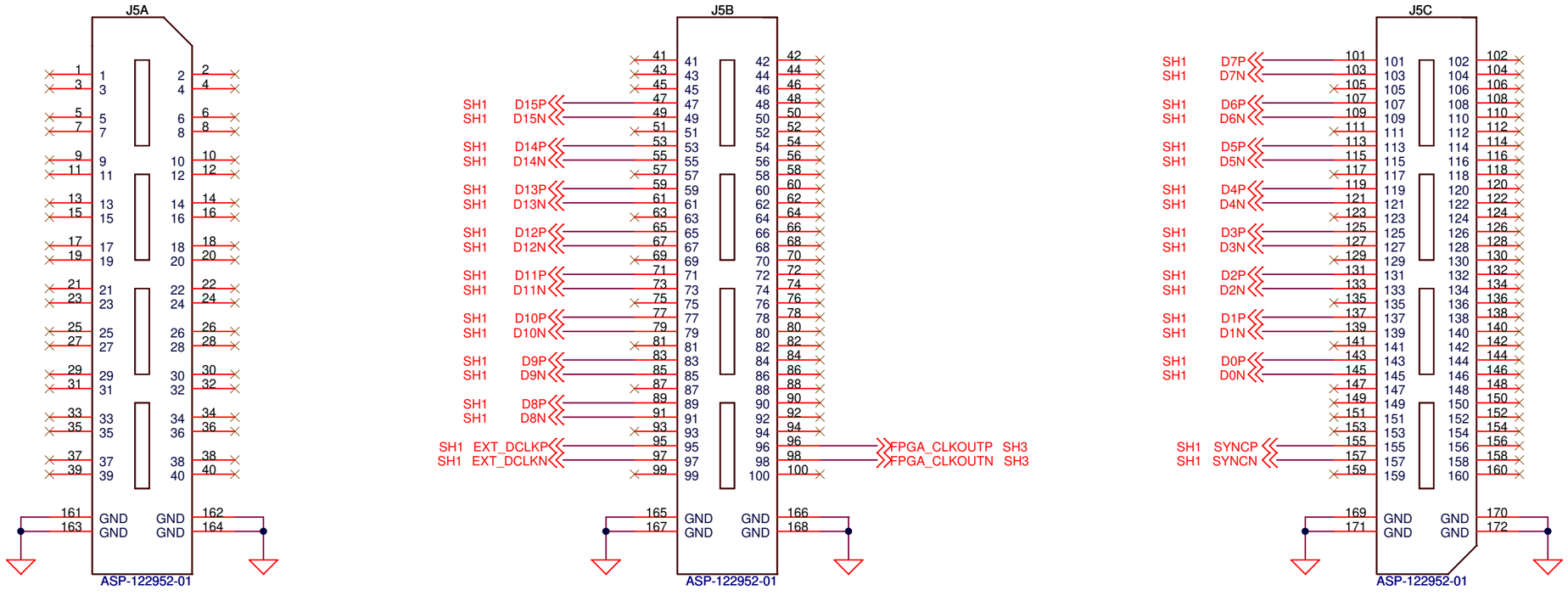
(SHUNT 2-3)

(SHUNT 1-2)

SW RESET

TEXAS INSTRUMENTS

Title: DAC5682Z EVM		
Size: B	Document Number: DAC	Rev: D
Date: Wednesday, August 06, 2008	Sheet 1 of 6	



TEXAS INSTRUMENTS

Title	DAC5682Z EVM	
Size: B	Document Number: INTERFACE CONTROL	Rev: D
Date: Monday, August 04, 2008	Sheet 2 of 6	

NOTES:

1) DNI = DO NOT INSTALL

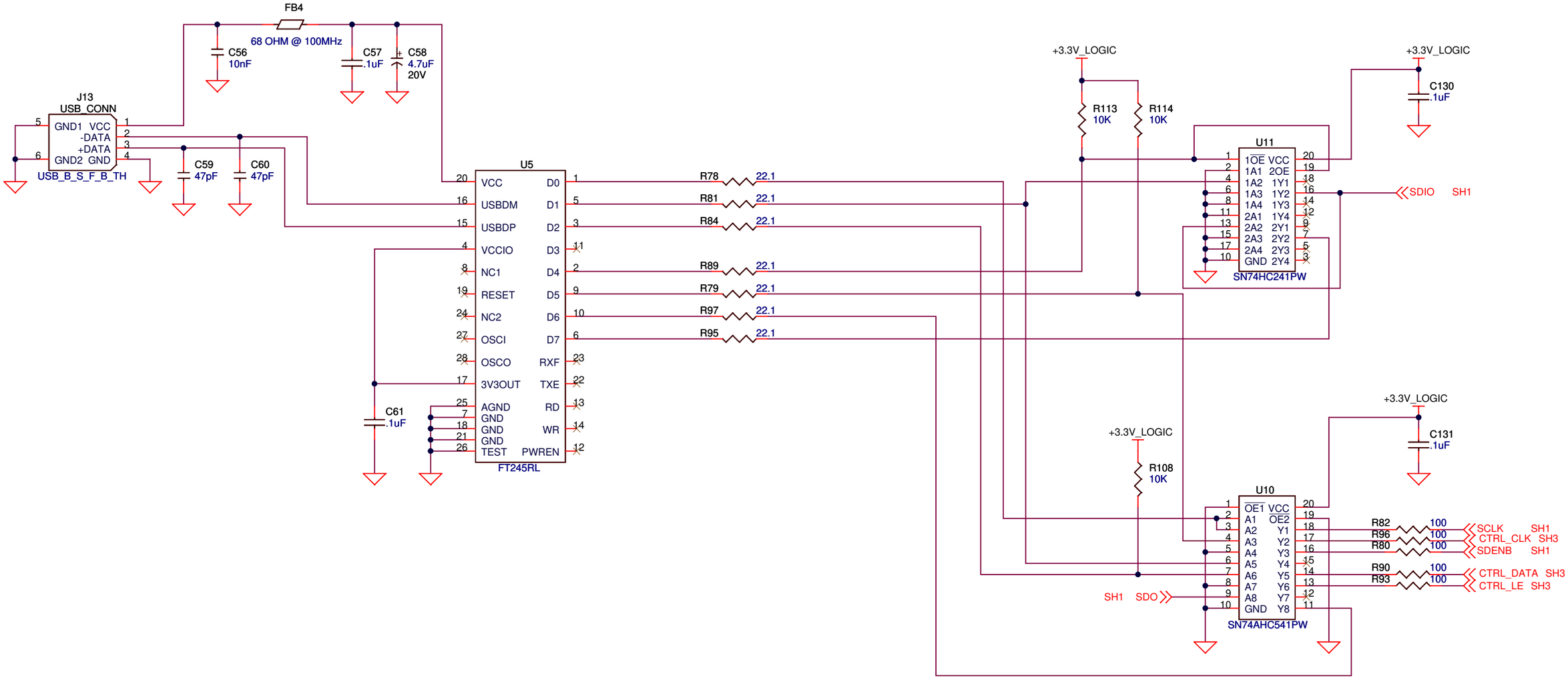
+3.3VCLK
JP19
+3.3VCLK
FB1
68 OHM @ 100MHz
C21 10uF 10V
C22 560pF 10% 50V
C23 .1uF 10% 16V
V_CTRL
U6
V_CTRL VCC
NC OUTB
GND OUT
2115-491.52MHZ
DNI
+3.3VCLK
R31 130
R32 130
R36 82.5
R37 82.5
JP13 VCXOB
(SHUNT 2-3)
JP14 VCXO_P
(SHUNT 2-3)
JP15 VCXO_N
(SHUNT 1-2)
J6 EXT_VCXO_P
R44 0
R45 0 DNI
C24 .1uF
J7 EXT_VCXO_N
R49 0
R51 0 DNI
C25 .1uF
J9 EXT_REF_CLK
R55 49.9 DNI
TP1 REF_ADJ
R59 10K
R61 10K
+3.3VCLK
FB2
68 OHM @ 100MHz
C32 10uF 10V
C31 100pF
C33 .1uF
U3
REF OUT
VDD GND
OSC-VECTRON
R62 0
JP16 REF_CLK
(SHUNT 2-3)
C29 1000pF 25V 10%
+3.3VCLK
R60 10K
R64 10K
R116 150
R40 150
+3.3VCLK
AVCC
+3.3VCLK
C27 .1uF 10% 16V
+3.3VCLK
U2
VCC Y0B Y0A VCC VCC VCXO_IN VCXO_INB VCC VBB AVCC AVCC
SEC_REF PRI_REF REF_SEL NC VCC_CP AVCC CP_OUT AVCC CTRL_LE CTRL_CLK AVCC
CDCM7005
/PD VCC Y4A Y4B VCC VCC Y3A Y3B VCC VCC Y2A Y2B VCC /RESET or /HOLD VCC Y1A Y1B VCC VCC VCC VCC
STATUS_VCXO or I_REF_CP
STATUS_REF or PRI_SEC_CLK
GND PWRPAD
PLL_LOCK CTRL_DATA
CTRL_DATA SH4
CTRL_CLK SH4
CTRL_LE SH4
+3.3VCLK
JP12 CDC_PD
(SHUNT 1-2)
RESET SH1,4
R110 150 DNI
R111 150 DNI
R63 162
V_CTRL
R65 4.75K
C36 22uF 20% 10V
C34 1uF 20% 25V
C35 .47uF 10% 16V
R28 750 VCXO D1 LED green
R29 750 REF D2 LED green
R30 750 LOCK D3 LED green
+3.3VCLK
R33 130
R34 130
R38 82.5
R39 82.5
CLKINC SH1
CLKIN SH1
+3.3VCLK
R42 130
R43 130
R46 82.5
R47 82.5
INT_DCLKN SH1
INT_DCLKP SH1
+3.3VCLK
R66 130
R67 130
R159 0
R161 0
R160 0
R162 0
FPGA_CLKOUTN SH2
FPGA_CLKOUTP SH2
R69 82.5
R70 82.5
+3.3VCLK
R48 130 DNI
R50 22.1
R163 0
R52 150 DNI
R53 82.5 DNI
J8 Y2A_CLK
+3.3VCLK
R54 130 DNI
R56 22.1
R164 0
R57 150 DNI
R58 82.5 DNI
J10 Y2B_CLKC
+3.3VCLK
C53 10uF 10V
C38 .1uF
C39 .1uF
C40 .1uF
C41 .1uF
C42 .1uF
C43 .1uF
C44 .1uF
C45 .1uF
C46 .1uF
C47 .1uF
FB3
68 ohm @ 100MHz
C48 .001uF
C49 .01uF
C50 .1uF
C51 .1uF
C52 .1uF
AVCC
C54 10uF 10V

TEXAS INSTRUMENTS

Title: DAC5682Z EVM

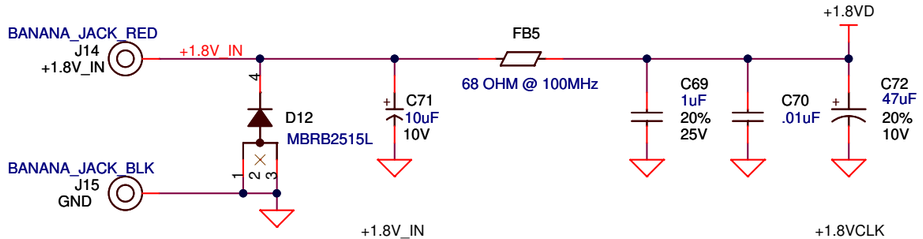
Size	Document Number	Rev
B	CDC	D

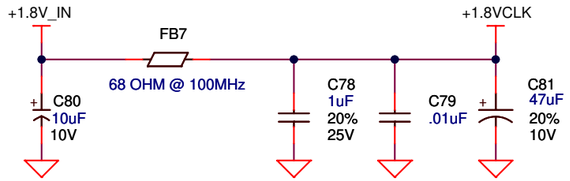
Date: Wednesday, August 06, 2008 Sheet 3 of 6

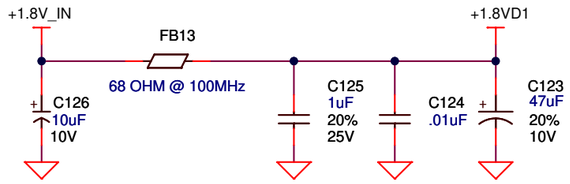


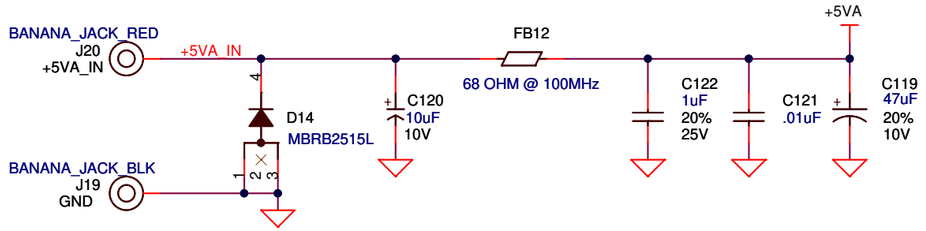
TEXAS INSTRUMENTS

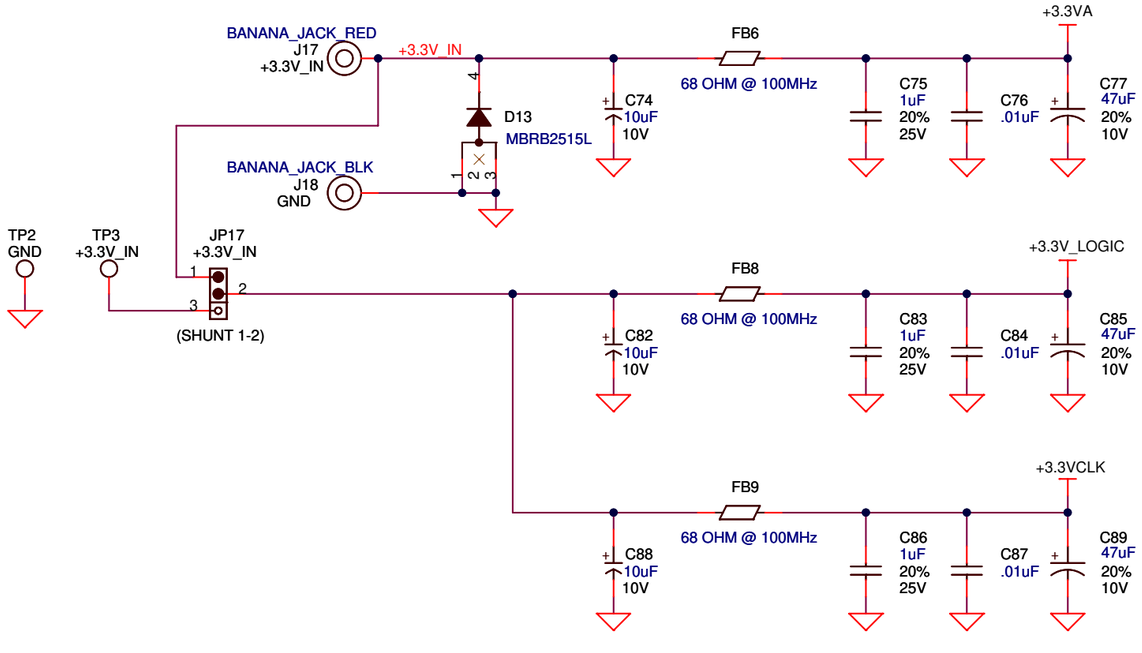
Title	DAC5682Z EVM	
Size: B	Document Number: USB INTERFACE	Rev: D
Date: Wednesday, August 06, 2008	Sheet 4 of 6	

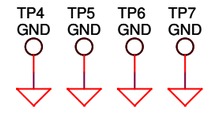


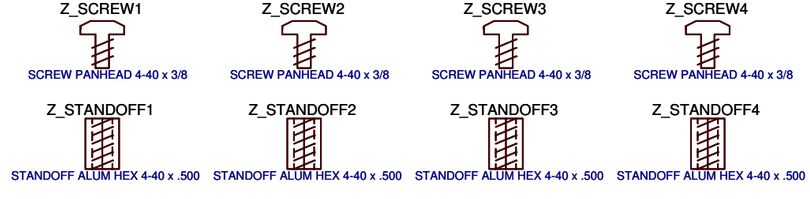












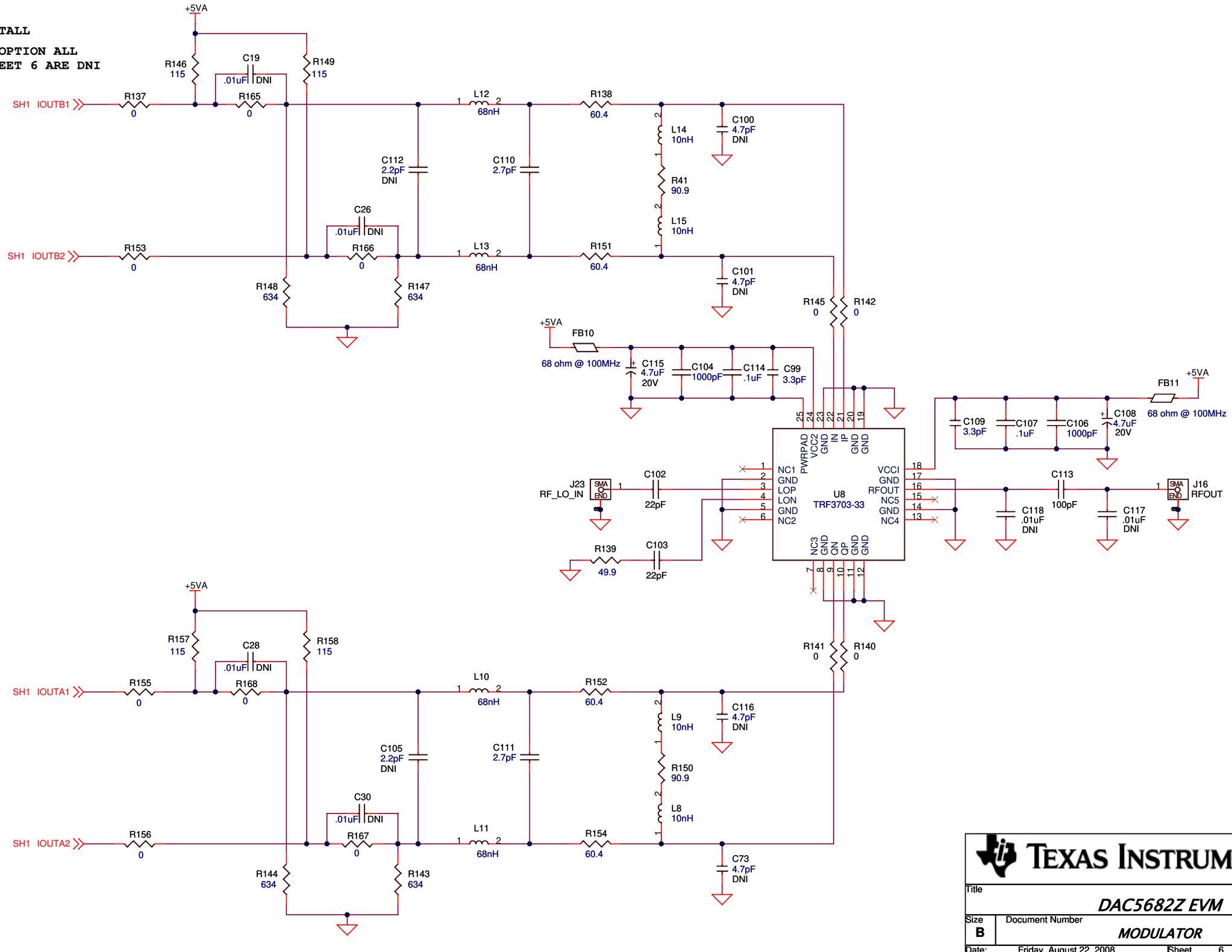
TEXAS INSTRUMENTS

Title	DAC5682Z EVM	
Size: B	Document Number: POWER DISTRIBUTION	Rev: D
Date: Monday, August 04, 2008	Sheet 5 of 6	

NOTES:

1) DNI = DO NOT INSTALL

2) FOR DAC5681/81Z OPTION ALL COMPONENTS ON SHEET 6 ARE DNI



TEXAS INSTRUMENTS

Title	DAC5682Z EVM	
Size: B	Document Number: MODULATOR	Rev: D
Date: Friday, August 22, 2008	Sheet 6 of 6	

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