MP8843

6V, 3A, Synchronous, Step-Down Switcher with I²C Interface

The Future of Analog IC Technology

DESCRIPTION

The MP8843 is a highly integrated, high-frequency, synchronous, step-down switcher with an I²C control interface. The MP8843 can support up to 3A of current from a wide 2.6V-to-6V input supply range with excellent load and line regulation.

Constant-on-time (COT) control provides a fast transient response, high light-load efficiency, and eases loop stabilization.

The I²C interface allows for communication interface speed up to 3.4Mbps. It controls the output voltage from 0.6V to 1.1V on the fly with 3.9mV voltage steps. This interface also controls the output voltage transition slew rate and allows the power-save mode selection to meet different application requirements.

Protection features include internal soft start (SS), over-current protection (OCP), and over-temperature protection (OTP).

The MP8843 requires a minimal number of readily available, standard, external components and is available in an ultra-small QFN-12 (2mmx2mm) package.

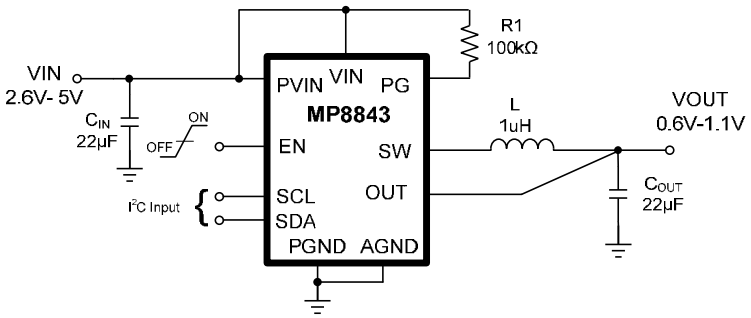
FEATURES

- Wide Input Range from 2.6V to 6V
- Up to 3A of Continuous Current
- 55mΩ and 35mΩ Internal Power MOSFET
- High-Speed I²C Communication Interface up to 3.4MHz
- I²C Programmable Output Voltage from 0.6V to 1.1V for Direct V_{OUT} Sense
- V_{OUT} Range Extendable by Adding External Feedback Resistor
- Programmable Switching Frequency from 1MHz to 2MHz
- Programmable Voltage Transition Slew Rate
- I²C Selectable Power Save Mode
- External and I²C-Controlled Power Good Indicator
- Internal Soft Start (SS)
- Short-Circuit Protection (SCP) with Latch-Off
- Thermal Shutdown
- Available in a QFN-12 (2mmx2mm) Package

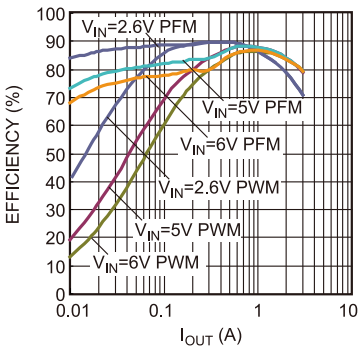
APPLICATIONS

Small/Handheld Devices
Storage Drives
Portable Instruments
Battery-Powered Devices

TYPICAL APPLICATION



Efficiency vs. Load



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8843GG	QFN-12 (2mmx2mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP8843GG–Z)

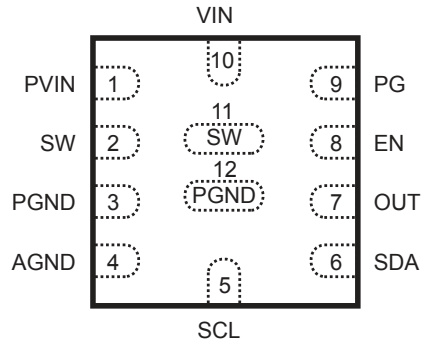
TOP MARKING

BLY
LLL

BL: Product code of MP8843GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-12 (2mmx2mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +6.5V
V_{SW}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (7V for <10ns and 9V for <5ns)
All other pins .....-0.3V to +6.5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
QFN-12 (2mmx2mm)..... 1.7W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.6V to 6V
Output voltage (V_{OUT}).....0.6V to 1.1V
Operating junction temp..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-12 (2mmx2mm) .....70..... 15.....°C/W

NOTES:

Exceeding these ratings may damage the device.

The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

The device is not guaranteed to function outside of its operating conditions.

Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.6		6	V
Quiescent current	I_Q	V_{EN} = 1.8V, no switching, PFM mode		60		µA
		Io = 0A, switching, PWM mode(5)		7		mA
Shutdown current	I_S	V_{EN} = GND, T_J = 25°C			1	µA
Internal reference voltage	V_{REF}	T_J = 25°C	0.594	0.6	0.606	V
	V_{REF}		0.591	0.6	0.609	V
Lowest output voltage	V_{LOW}	Register = 00h, T_J = 25°C	0.594	0.6	0.606	V
Highest output voltage	V_{HIGH}	Register = 7Fh, T_J = 25°C	1.089	1.1	1.111	V
Output voltage step	V_{STEP}			3.9		mV
High-side switch on resistance	R_{HSON}			55		mΩ
Low-side switch on resistance	R_{LSON}			35		mΩ
UVLO rising threshold	V_{UVLOR}			2.35	2.55	V
UVLO hysteresis	V_{UVLOHY}			170		mV
VIN over-voltage	V_{OVP}			6.3		V
VIN over-voltage hysteresis	V_{OVPHY}			250		mV
Switching frequency	f_{SW}		1		2	MHz
Minimum on time(5)	T_{MINON}			50		ns
Minimum off time	T_{MINOFF}			90		ns
Switch leakage	I_{SW}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = 25°C		1	2	µA
EN logic high	V_{ENL}		1.2			V
EN logic low	V_{ENH}				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2		µA
PG rising threshold	V_{PGH}	V_{OUT} refer to I²C setting target voltage, V_{OUT} from 80% to 100%		85		$\%V_{TARGET}$
PG falling threshold	V_{PGFTH}	V_{OUT} refer to I²C setting target voltage, V_{OUT} from 100% to 120%		115		$\%V_{TARGET}$
PG hysteresis	V_{PGHY}			20		mV
PG pull-down voltage	V_{PGL}	I_{sink} = 2mA			0.4	V
PG delay	T_{PGd}	PG_DELAY = 0		30		µs
	T_{PGd}	PG_DELAY = 1		17		ms
High-side switch peak current limit (source)(5)	I_{peak}		3.6	4.8	6	A
Low-side switch valley current limit (source)(5)	I_{valley}			3.6		A

ELECTRICAL CHARACTERISTICS *(CONTINUED)*

V_{IN} = 3.6V, T_J = -40°C to +125°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start time	T_{SS-ON}	Vo = 0.9V		1		ms
Thermal warning(6)				140		°C
Thermal shutdown(6)				160		°C
DAC resolution(6)				7		bits

NOTES:
Guaranteed by engineering sample characterization.
Guaranteed by design.

I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}	V_{IN} = 2.6V - 6V		0.4		0.4	V
High-level input voltage	V_{IH}	V_{IN} = 2.6V - 6V	1.4		1.4		V
Low-level output voltage (open drain) at 3mA sink current	V_{OL}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	$0.2V_{CC}$	0	$0.2V_{CC}$	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL = 3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50	-	50	-	kΩ
SCLH current source pull-up current	I_{cs}	SCLH output levels between $0.3V_{CC}$ and $0.7V_{CC}$	2	6	2	6	mA
SCLH or SCL signal rise time	T_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
SCLH or SCL signal fall time	T_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
SDAH signal rise time	T_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
SDAH signal fall time	T_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Spike pulse width requiring input filter suppression	T_{SP}		0	10	0	50	ns
I/O pin input current	I_i	Input voltage between $0.1V_{CC}$ and $0.9V_{CC}$	-	10	-10	+10	μA
I/O pin capacitance	C_i		-	10	-	10	pF

I²C PORT SIGNAL CHARACTERISTICS

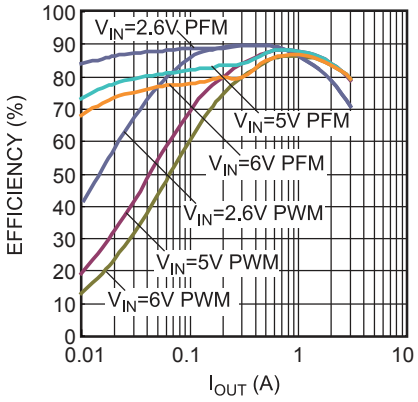
Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCL}		0	3.4	0	0.4	MHz
Set-up time for repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time for repeated start condition	$T_{HD;STA}$		160	-	600	-	ns
SCL clock low period	T_{LOW}		160	-	1300	-	ns
SCL clock high period	T_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
SCLH signal rise time	T_{rCL}		10	40	20x0.1Cb	300	ns
SCLH signal rise time after a repeated start condition and an acknowledge bit	T_{rCL1}		10	80	20x0.1Cb	300	ns
SCLH signal fall time	T_{fCL}		10	40	20x0.1Cb	300	ns
SDAH signal rise time	T_{fDA}		10	80	20x0.1Cb	300	ns
SDAH signal fall time	T_{fDA}		10	80	20x0.1Cb	300	ns
Stop condition set-up time	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between stop and start condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Bus line capacitive load	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF
Low-level noise margin	V_{nL}	For each connected device	-	$0.1V_{CC}$	$0.1V_{CC}$	-	V
High-level noise margin	V_{nH}	For each connected device	-	$0.2V_{CC}$	$0.2V_{CC}$	-	V

NOTE:
Vcc is the I²C bus voltage, 1.5V to 2.5V range.

TYPICAL PERFORMANCE CHARACTERISTICS

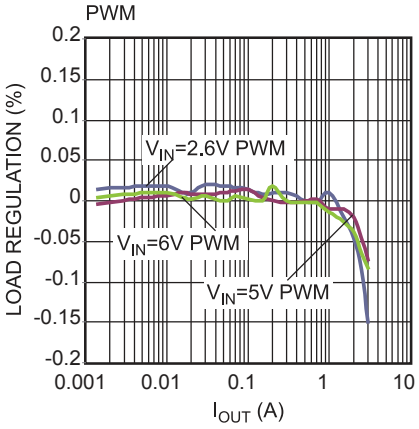
V_{IN} = 5V, V_{OUT} = 0.9V, L = 1µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load



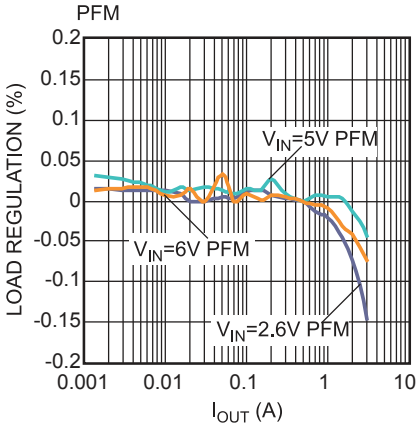
Load Regulation

PWM



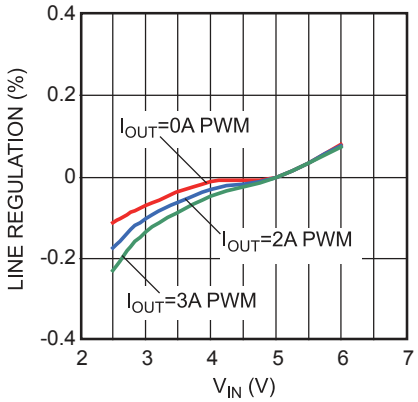
Load Regulation

PFM

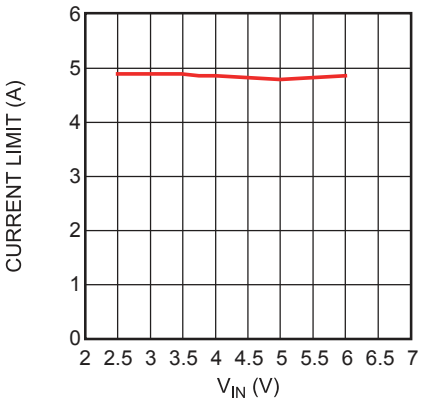


Line Regulation

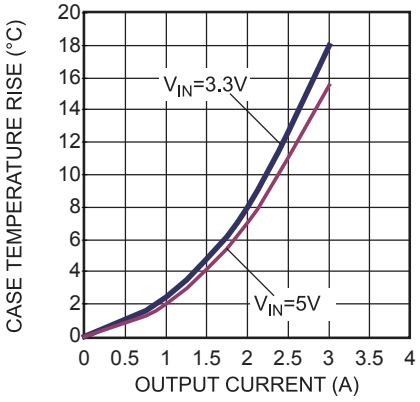
PWM



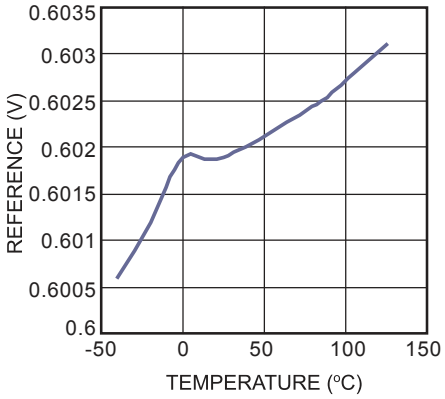
Current Limit vs. Input Voltage



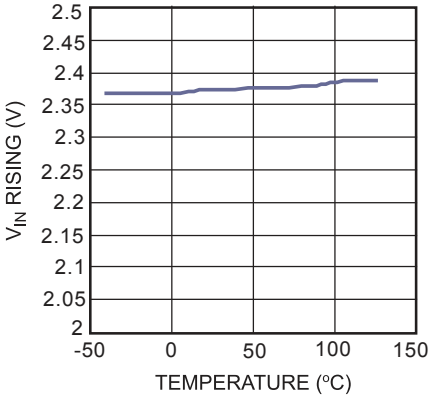
Thermal Rise vs. Load



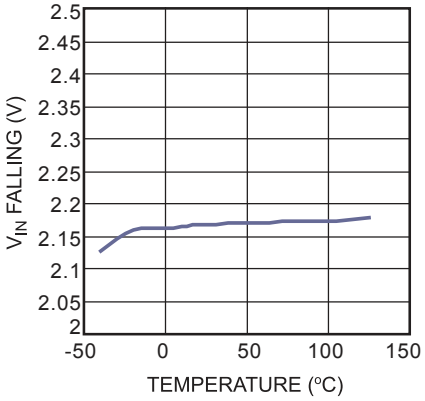
Reference vs. Temperature



V_{IN} Rising vs.Temperature



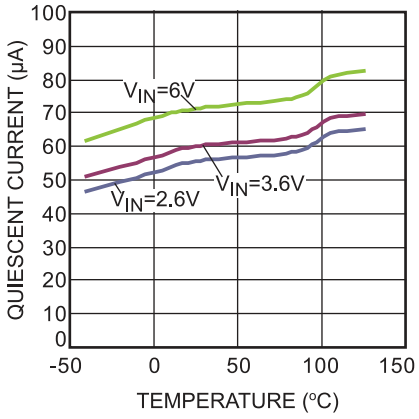
V_{IN} Falling vs. Temperature



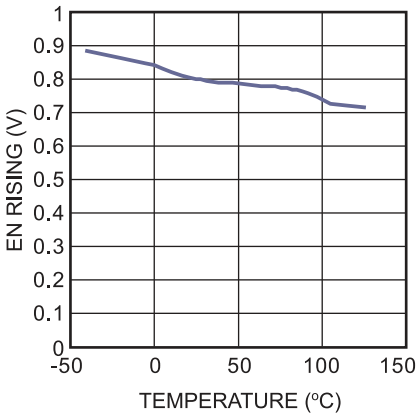
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.9V, L = 1µH, T_A = 25°C, unless otherwise noted.

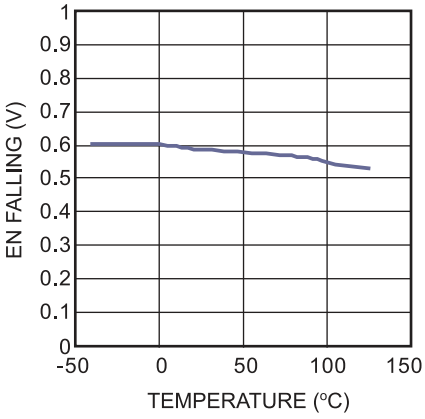
IQ_PFM vs. Temperature



EN Rising vs. Temperature



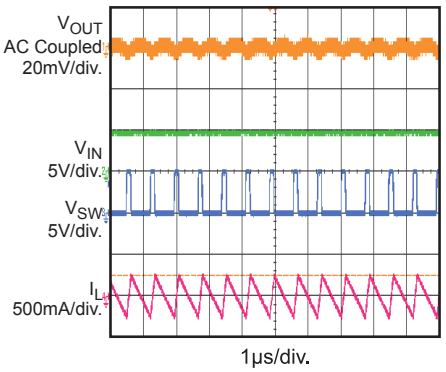
EN Falling vs. Temperature



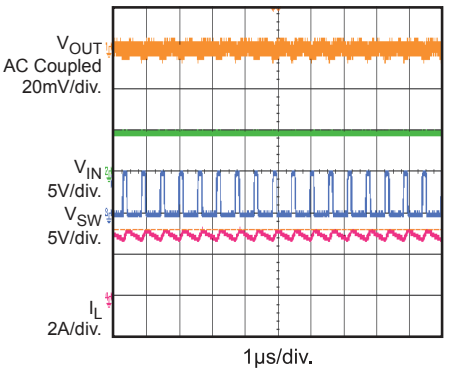
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.9V, L = 1µH, T_A = 25°C, unless otherwise noted.

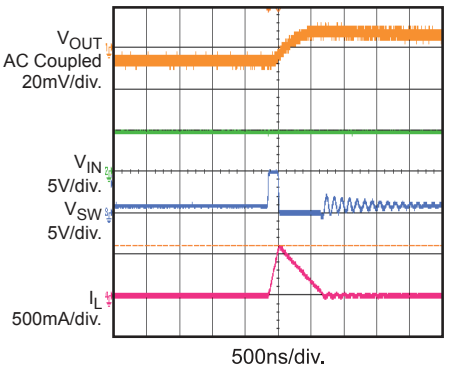
Steady State
PWM I_{OUT}=0A



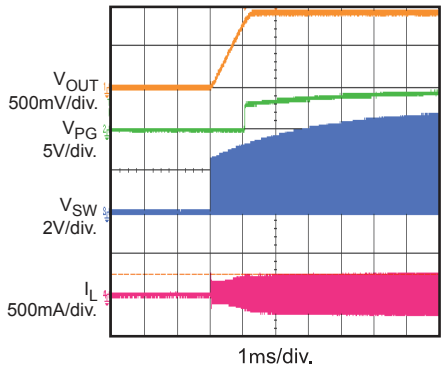
Steady State
PWM I_{OUT}=3A



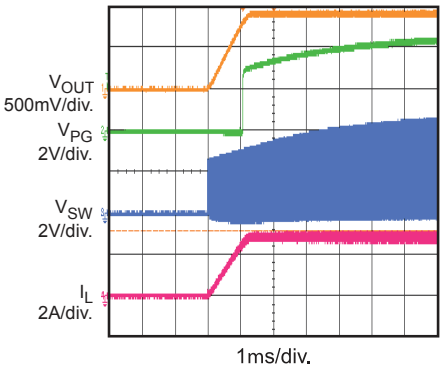
Steady State
PFM I_{OUT}=0A



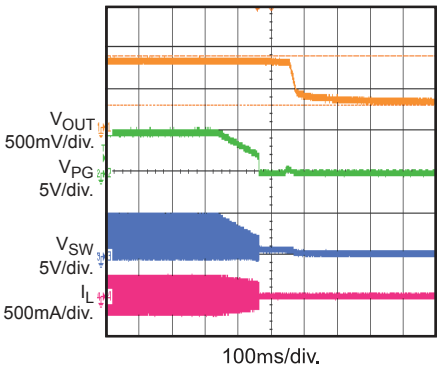
VIN Start-Up
PWM I_{OUT}=0A



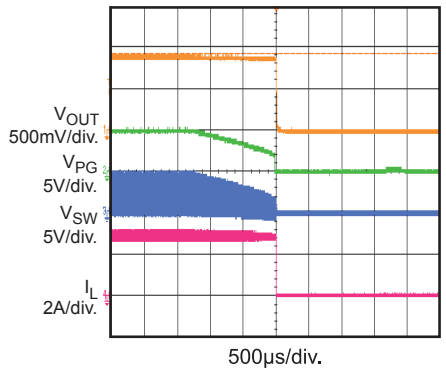
VIN Start-Up
PWM I_{OUT}=3A



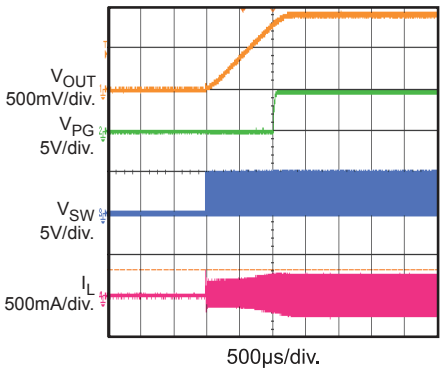
VIN Shutdown
PWM I_{OUT}=0A



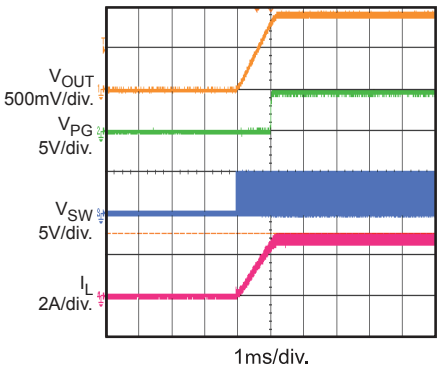
VIN Shutdown
PWM I_{OUT}=3A



EN Start-Up
PWM I_{OUT}=0A



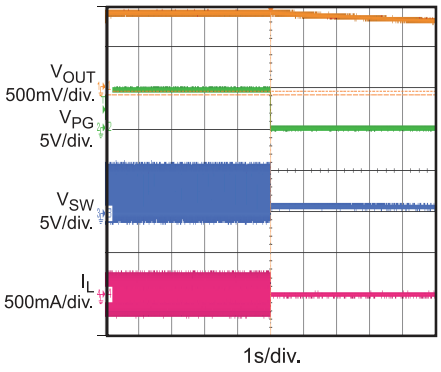
EN Start-Up
PWM I_{OUT}=3A



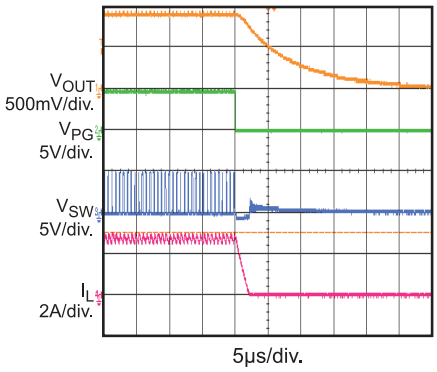
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.9V, L = 1µH, T_A = 25°C, unless otherwise noted.

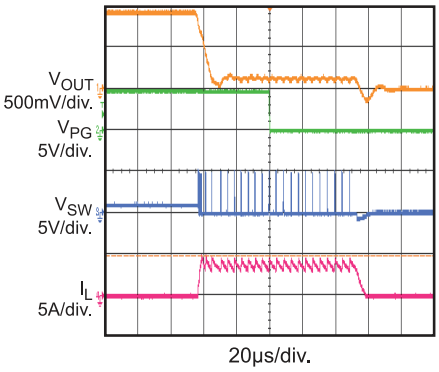
EN Shutdown
PWM I_{OUT}=0A



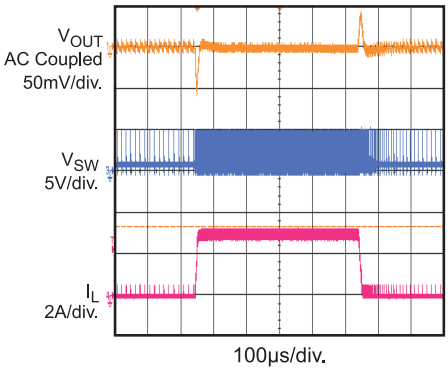
EN Shutdown
PWM I_{OUT}=3A



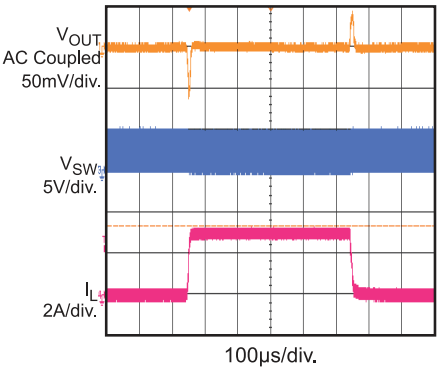
SCP
PFM



Load Transient
PFM I_{OUT}=0A to 3A



Load Transient
PWM I_{OUT}=0A to 3A



PIN FUNCTIONS

QFN-12 Pin #	Name	Description
1	PVIN	**Supply voltage to power FETs.** PVIN requires a capacitor to prevent voltage spikes from damaging the device. Connect the capacitor return to PGND directly. PVIN connects to VIN internally.
2, 11	SW	**Switch output.**
3, 12	PGND	**Power ground.**
4	AGND	**Analog ground.** AGND is the low-noise ground for the controller circuitry.
5	SCL	**I²C serial clock.** SCL provides the clock for the serial interface.
6	SDA	**I²C serial data.** SDA is an I²C pin that receives clocked serial data from the host and sends clocked serial data to the host. SDA is at high impedance except when transmitting.
7	OUT	**Output sense.** OUT senses the output voltage directly to program the output voltage from 0.6V to 1.1V. Sense the output voltage through an external feedback resistor to extend the output voltage range.
8	EN	**On/off control.** The MP8843 is enabled when EN is high.
9	PG	**Power good indicator.** The output of PG is an open drain with an internal pull-up resistor to VIN. When PG can detect both the positive and negative excursion of V_O from the reference, PG is pulled up to VIN when the output is within 85%~115% of regulation voltage. Otherwise, PG is low.
10	VIN	**Supply voltage to internal control circuitry.** VIN connects to PVIN internally.

BLOCK DIAGRAM

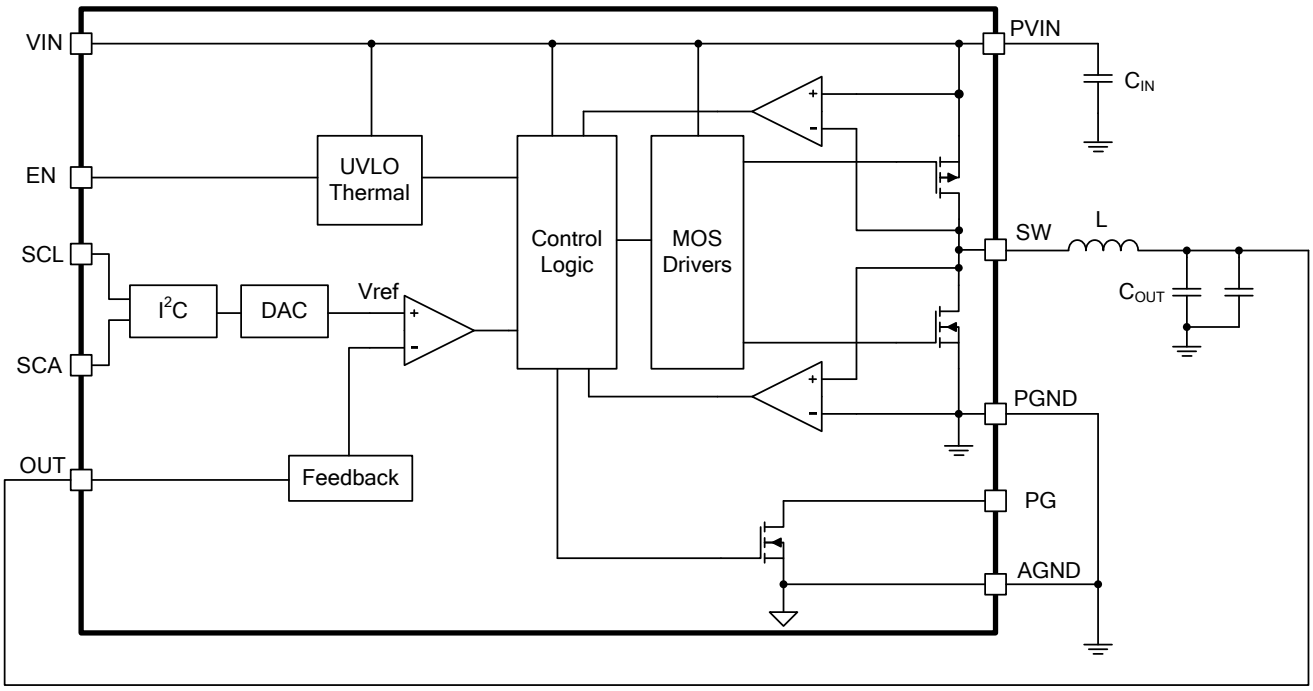


Figure 1: Functional Block Diagram

OPERATION

Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	EN	Output reference						
01	SysCntlreg1	R/W	Switching frequency			Reserved	PG_DELAY	PG_LOHI	V_{IN}_OVP	Mode
02	SysCntlreg2	R/W	Reserved		Go	Out_Dis	Reserved	Slew rate		
03	ID1	R	Vendor ID (0001)				Die ID			
04	ID2	R	Reserved				Die rev			
05	Status	R	OT	UVLO	OVP	V_O_OV	Vo_UV	PGOOD	OTW	EN state

Default Value of Register

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	1	1	0	0	1	1	0	1
01	SysCntlreg1	R/W	0	1	0	1	0	1	1	1
02	SysCntlreg2	R/W	1	1	0	0	0	1	1	0
03	ID1	R	0	0	0	1	0	0	0	1
04	ID2	R	0	0	0	0	0	0	0	0
05	Status	R	NA	NA	NA	NA	NA	NA	NA	NA

Register Description

1. Reg00 VSEL

NAME	BITS	DESCRIPTION
EN	D7	I^2C control enable. When EN is low, the converter is off. When EN is high, the EN bit takes over.
Output reference	D[6:0]	For direct output voltage sense, refer to Figure 4. Set the output voltage from 0.6V to 1.1V, per Table 1. For output sense through the feedback resistor network, refer to Figure 6 and the Extending the Output Voltage Range section on page 19.

Table 1: Output Voltage Chart

D[6:0]	V_{OUT}	D[6:0]	V_{OUT}	D[6:0]	V_{OUT}	D[6:0]	V_{OUT}
000 0000	0.6000	010 0000	0.7260	100 0000	0.8520	110 0000	0.9780
000 0001	0.6039	010 0001	0.7299	100 0001	0.8559	110 0001	0.9819
000 0010	0.6079	010 0010	0.7339	100 0010	0.8598	110 0010	0.9858
000 0011	0.6118	010 0011	0.7378	100 0011	0.8638	110 0011	0.9898
000 0100	0.6157	010 0100	0.7417	100 0100	0.8677	110 0100	0.9937
000 0101	0.6197	010 0101	0.7457	100 0101	0.8717	110 0101	0.9976
000 0110	0.6236	010 0110	0.7496	100 0110	0.8756	110 0110	1.0016
000 0111	0.6276	010 0111	0.7535	100 0111	0.8795	110 0111	1.0055
000 1000	0.6315	010 1000	0.7575	100 1000	0.8835	110 1000	1.0094
000 1001	0.6354	010 1001	0.7614	100 1001	0.8874	110 1001	1.0134
000 1010	0.6394	010 1010	0.7654	100 1010	0.8913	110 1010	1.0173
000 1011	0.6433	010 1011	0.7693	100 1011	0.8953	110 1011	1.0213
000 1100	0.6472	010 1100	0.7732	100 1100	0.8992	110 1100	1.0252
000 1101	0.6512	010 1101	0.7772	100 1101	0.9031	110 1101	1.0291
000 1110	0.6551	010 1110	0.7811	100 1110	0.9071	110 1110	1.0331
000 1111	0.6591	010 1111	0.7850	100 1111	0.9110	110 1111	1.0370
001 0000	0.6630	011 0000	0.7890	101 0000	0.9150	111 0000	1.0409
001 0001	0.6669	011 0001	0.7929	101 0001	0.9189	111 0001	1.0449
001 0010	0.6709	011 0010	0.7968	101 0010	0.9228	111 0010	1.0488
001 0011	0.6748	011 0011	0.8008	101 0011	0.9268	111 0011	1.0528
001 0100	0.6787	011 0100	0.8047	101 0100	0.9307	111 0100	1.0567
001 0101	0.6827	011 0101	0.8087	101 0101	0.9346	111 0101	1.0606
001 0110	0.6866	011 0110	0.8126	101 0110	0.9386	111 0110	1.0646
001 0111	0.6906	011 0111	0.8165	101 0111	0.9425	111 0111	1.0685
001 1000	0.6945	011 1000	0.8205	101 1000	0.9465	111 1000	1.0724
001 1001	0.6984	011 1001	0.8244	101 1001	0.9504	111 1001	1.0764
001 1010	0.7024	011 1010	0.8283	101 1010	0.9543	111 1010	1.0803
001 1011	0.7063	011 1011	0.8323	101 1011	0.9583	111 1011	1.0843
001 1100	0.7102	011 1100	0.8362	101 1100	0.9622	111 1100	1.0882
001 1101	0.7142	011 1101	0.8402	101 1101	0.9661	111 1101	1.0921
001 1110	0.7181	011 1110	0.8441	101 1110	0.9701	111 1110	1.0961
001 1111	0.7220	011 1111	0.8480	101 1111	0.9740	111 1111	1.1000

2. Reg01 SysCntlreg1

<table>
<tr><th>NAME</th><th>BITS</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="5">Switching frequency</td><td rowspan="5">D[7:5]</td><td>D[7:5]</td><td>Switching frequency</td><td>D[7:5]</td><td>Switching frequency</td></tr>
<tr><td>000</td><td>—</td><td>100</td><td>1.25MHz</td></tr>
<tr><td>001</td><td>2MHz</td><td>101</td><td>1.11MHz</td></tr>
<tr><td>010</td><td>1.67MHz (default)</td><td>110</td><td>1MHz</td></tr>
<tr><td>011</td><td>—</td><td>111</td><td>—</td></tr>
<tr><td>Reserved</td><td>D4</td><td colspan="4">Reserved.</td></tr>
<tr><td>PG_DELAY</td><td>D3</td><td colspan="4">A “0” disables the PG delay. A “1” enables the 17ms delay.</td></tr>
<tr><td>PG_LOHI</td><td>D2</td><td colspan="4">A “0” sets PG to sense only a negative voltage excursion of V_{OUT} from the reference. High (default) sets PG to detect both a positive and negative excursion of V_{OUT} from the reference.</td></tr>
<tr><td>V_{IN}_OVP</td><td>D1</td><td colspan="4">A “0” disables the VIN OVP function. The converter continues operating. High (default) turns off the converter when VIN reaches 6.3V.</td></tr>
<tr><td>Mode</td><td>D0</td><td colspan="4">A “0” enables PFM mode; high disables PFM mode.</td></tr>
</table>

3. Reg02 SysCntlreg2

NAME	BITS	DESCRIPTION			
Reserved	D[7:6]	Reserved.			
Go	D5	Write this bit to "1" to start a V_{OUT} transition regardless of its initial value.			
Out_Dis	D4	A "0" disables the output discharge. The output voltage is discharged by a load. High enables an internal pull-down.			
Reserved	D3	Reserved.			
Slew rate	D[2:0]	D[2:0]	Slew rate	D[2:0]	Slew rate
		000	64mV/μs	100	4mV/μs
		001	32mV/μs	101	2mV/μs
		010	16mV/μs	110	1mV/μs (default)
		011	8mV/μs	111	0.5mV/μs

4. Reg03 ID1

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	Vendor ID [0001].
Die ID	D[3:0]	IC type.

5. Reg04 ID2

NAME	BITS	DESCRIPTION
Reserved	D[7:4]	Reserved.
Die Rev	D[3:0]	Die revision.

6. Reg05 Status

NAME	BITS	DESCRIPTION
OT	D7	When the bit is high, the IC is in thermal shutdown.
UVLO	D6	When the bit is high, V_{IN} is less than the UVLO threshold.
OVP	D5	When the bit is high, V_{IN} is greater than the OVP threshold.
Vo_OV	D4	When the bit is high, a voltage higher than 115% of the regulation voltage is presented.
Vo_UV	D3	When the bit is high, a voltage lower than 85% of the regulation voltage is presented.
PGOOD	D2	When the bit is high, the output is in regulation. Otherwise, the output voltage is out of the regulation window.
OTW	D1	When the junction temperature exceeds 140°C, the bit goes high.
EN State	D0	When the bit is high, the MOSFET driver is enabled.

Operation Status

FAULT CONDITION	PG	REGULATION	LATCH-OFF	STATUS BIT
Current limit	High	On	No	
V_{IN} under-voltage	Low	Off	NA	UVLO
V_{IN} over-voltage(7)	Low	Off	No	OVP
V_O under-voltage	Low	Off	**Yes**	Vo_UV
V_O over-voltage (>115% of target output)(8)	Low	On	No	Vo_OV
Thermal warning	Low	On	No	OTW
Thermal shutdown	Low	Off	**Yes**	OT

NOTES:
The part turns off when V_{IN}_OVP is high and V_{IN} reaches 6.3V.
The PG is low when PG_LOHI is written to 1.

OPERATION

The MP8843 is a low-voltage, 3A, synchronous, step-down converter with a controllable I²C interface. The MP8843 uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over the entire input range. Because it does not require compensation, it has a simple design procedure.

The MP8843 integrates an I²C-compatible interface that allows transfers up to 3.4Mbps. This communication interface can scale the voltage dynamically with voltage steps as small as 3.9mV with an output voltage range of 0.6V to 1.1V. The interface can also control the voltage transition slew rate.

Constant-on-Time (COT) Control

Compared to the fixed-frequency PWM control, COT control simplifies the control loop and speeds up the transient response. The MP8843 uses input voltage feed-forward to maintain a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$\tau_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{f_{sw}} \quad (1)$$

To prevent inductor current runaway during the load transient, the MP8843 has a fixed minimum off time of 90ns. This minimum off time does not affect steady-state operation in any way.

Light-Load Operation

Under light-load conditions, the MP8843's I²C interface uses power save mode. When the MODE bit is "0," the MP8843 enters power save mode and uses a proprietary control scheme to save power and improve efficiency. The MP8843 turns off the low-side switch when the inductor current begins to reverse. Then the MP8843 works in discontinuous conduction mode (DCM).

Enable (EN)

When the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.35V), the MP8843 can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MP8843. There is an internal 1MΩ resistor from EN to ground.

Soft Start (SS)

The MP8843 has a built-in soft start (SS) that ramps up the output voltage at a controlled slew rate to prevent an overshoot at start-up. The soft-start time is about 1ms, typically, when V_{OUT} is 0.9V.

Power Good (PG) Indictor

The MP8843 uses an open drain for the power good (PG) indicator. When PG is able to detect both the positive and negative excursion of V_{OUT} from the reference, PG is pulled up to VIN by the external resistor when the OUT voltage is within 85%~115% of the regulation voltage. Otherwise, the internal MOSFET pulls PG to ground. If PG is only able to detect a negative voltage excursion of V_{OUT} from the reference, PG is pulled up to VIN when the OUT voltage is higher than 115% of regulation voltage. The MOSFET has a maximum $R_{DS(ON)}$ of less than 200Ω.

Current Limit

The MP8843 has a 4.8A high-side switch current limit. When the high-side switch reaches its current limit, the MP8843 turns off the high-side switch until the low-side current drops to 3.8A. This prevents the inductor current from continuing to rise and damaging components. If the over-current status is continuous, the output voltage falls and may trigger short-circuit protection.

Short Circuit

The MP8843 monitors the output voltage through OUT to detect an under-voltage condition. The MP8843 enters a latch-off protection mode when an output short occurs. Only an EN or VIN restart can turn the MP8843 on again.

I²C Interface

The MP8843 can communicate with the core via the I²C for smart design. The GUI control interface is shown in Figure 2. The installation process and usage can be found in the MP8843 software guide.

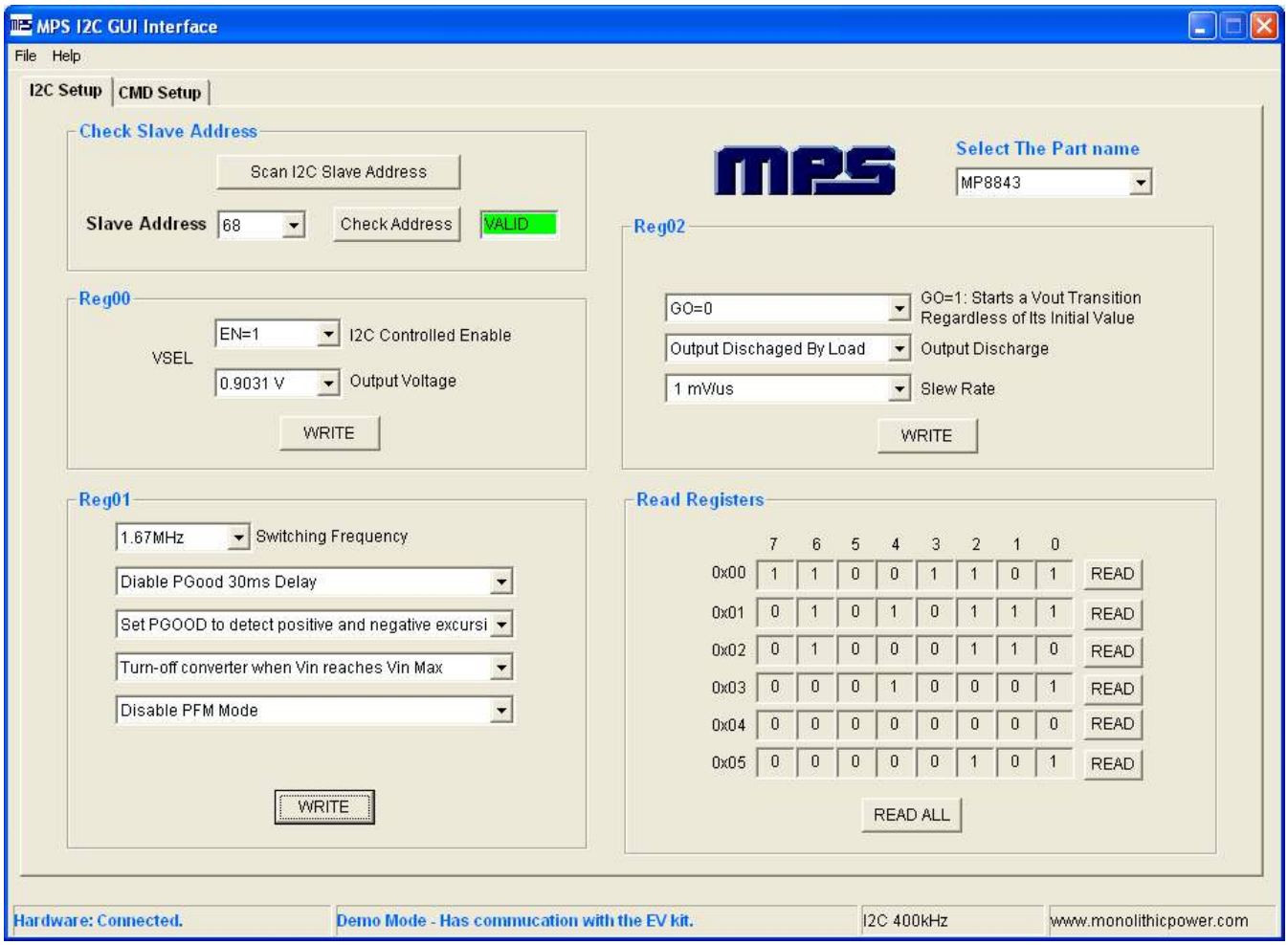


Figure 2: MP8843 Control Interface

I²C Address

The I²C slave address of the MP8843 is 0xD0H / 0xD1H. If another slave address is needed, please contact the factory.

Table 2: I²C Slave Address

Hex	A7	A6	A5	A4	A3	A2	A1	A0
W 0xD0	1	1	0	1	0	0	0	R/
R 0XD1	1	1	0	1	0	0	0	W
Address	0x68							

I²C Enable

The MP8843's EN can start up and shut down the convertor. The I²C's EN can also control the convertor. The Reg00 VSEL D7 bit is I²C-control enabled. When writing D7 = 0, the convertor is off. When writing D7 = 1, the convertor is on. Both the external EN and I²C EN can control the converter. The converter works only when both EN pins are high.

Output Voltage Select

The MP8843 output voltage is I²C programmable. There is no need to set feedback resistors to obtain a different output voltage. The default output voltage is 0.9031V, but can be set from 0.6V to 1.1V in 3.9mV steps by the I²C. Change the output voltage with the following steps:

1. Write the Go bit (Reg02 SyCntlreg2 [D5]) to 1. This action means the output voltage can be set to another value that is not the default Vo voltage.
2. Write the output reference bit (Reg00 VSEL [D6:D0]). The output voltage can be changed according to Table 1.

Switching Frequency

The default switching frequency of the MP8843 is 1.67MHz. However, the frequency can also be changed based on the application. By writing the switching frequency bits (Reg01 SysCntlreg1 [D7:D5], the switching frequency can be programmed as one of five possible values. Their corresponding data can be found in Reg01 SysCntlreg1.

The SW has some jitter with low VIN and a heavy load if the frequency is set to 2MHz. This is because a low VIN and a high frequency make the internal ramp ripple small. The internal noise becomes larger under heavy-load conditions. This produces little jitter on SW while V_{OUT} is still in regulation. The jitter is found in the conditions shown in Figure 3.

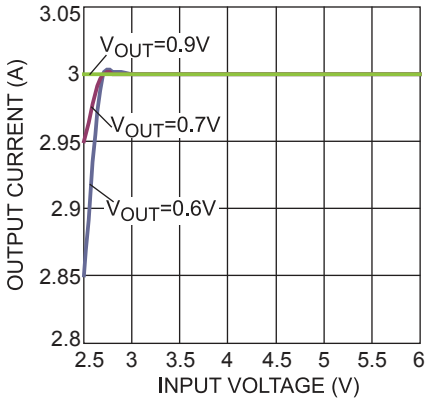


Figure 3: Max I_{OUT} for a Certain Input Voltage

For example, the SW has little jitter when V_{IN} is 2.5V, V_{OUT} is 0.7V and the output current is bigger than 2.95A.

Power Good Configuration

The MP8843 has an option to use the PG_LOHI function. This function can be written with the PG_LOHI bit (Reg01 SysCntlreg1 [D2]). The default value is 1. PGOOD can sense both a positive and negative excursion of V_{OUT} from the reference. If writing this bit to 0, PGOOD can only sense a negative voltage excursion of V_{OUT} from the reference.

Input Over-Voltage Protection (OVP)

The MP8843 has an option to use the VIN OVP function. This function can be written through the VIN_OVP bit (Reg01 SysCntlreg1 [D1]). When set as the default value 1, the VIN OVP function is enabled. When the VIN voltage is higher than 6.3V, the converter is disabled. After VIN recovers to 6.05V, the converter restarts. If the VIN_OVP bit is set to 0, VIN OVP is disabled. The converter should not stop, even if VIN exceeds its safe range.

Pulse Frequency Modulation (PFM) Mode Selection

The MP8843 uses forced continuous conduction mode (CCM) and pulse frequency modulation (PFM) mode. Writing the MODE bit (Reg01 SysCntlreg1 [D0]) can change the work mode. When the MODE bit is set to the default value 1, forced CCM is selected. Considering high efficiency at light load, PFM mode is recommended. Set this bit to 0 to enable PFM mode.

Output Discharge

The MP8843 has an output discharge function. Write the Out-Dis bit (Reg02 SysCntlreg2 [D4]) to change the output discharge mode. The default value is 0 and discharges V_{OUT} by its load when EN is low. Writing D4 = 1 can enable the function, and then the output voltage can be discharged by the internal pull-down resistance.

Output Voltage Transition Slew Rate

When the output voltage transitions from a low voltage to a high voltage, or from a high voltage to a low voltage, the transition slew rate can be different.

There are eight possible selection values. Through writing the slew rate bits (Reg02 SysCntlreg2 [D2:D0]), the transition slew rate can be set as one possible value based on the application. The internal reference follows the set slew rate, but the output voltage slew rate does not always follow the internal reference. Considering the output capacitor and inductor, the actual output voltage slew rate should be slower.

APPLICATION INFORMATION

Extending the Output Voltage Range

The MP8843 can extend the output voltage range more than 1.1V by the external feedback resistor network. The extended output range ratio (Vo_max divided by Vo_min) is not more than 1.8 (equal to 1.1V/0.6V).

The output voltage is determined by the external feedback resistor networks (R4 and R5) and the internal reference voltage (REF) (see Figure 6). The internal reference is controlled by the I²C and the initial V_{REF} is 0.9V. V_{OUT_REAL} and V_{STEP_REAL} can be calculated with Equation (2) and Equation (3):

$$V_{OUT\_REAL} = V_{REF} * (1+\frac{R4}{R5}) \quad (2)$$

$$V_{STEP\_REAL} = 3.9mV * (1+\frac{R4}{R5}) \quad (3)$$

For example, if V_{REF} = 0.9V, R4 = 18k, and R5 = 57.6k, then $V_{OUT\_DEFAULT}$ = 1.18V, V_{OUT_MIN} = 0.79V, V_{OUT_MAX} = 1.44V, and V_{STEP_REAL} = 5.1mV.

Generally, the sum of R4 and R5 is not more than 100k. The I²C's programmable feature still works with an external feedback resistor. Only the output voltage needs to multiply the same ratio, as shown in Equation (2) and Equation (3). The internal V_{OUT} range is 0.6 - 1.1V, and the output voltage range can be deduced by Equation (2). The recommended maximum V_{OUT} is less than 1.8V in application.

Considering the efficiency and load regulation, the recommended inductor DCR is lower than 15mΩ in the external feedback resistor network application.

The real switching frequency increases with the extended output voltage range circuit. The switching frequency can be estimated with Equation (4):

$$F_{SW\_REAL} = (1+\frac{R4}{R5}) * F_{SW\_INTERNAL} \quad (4)$$

For example, if V_{REF} = 0.9V, R4 = 18K, R5 = 57.6k, and $F_{SW\_INTERNAL}$ = 1.67MHz, then the estimated F_{SW_REAL} = 2.19MHz.

With the external feedback network, the output discharge capability decreases correspondingly because of the upper feedback resistor network.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. For higher output voltages, a 47µF capacitor may be needed for increased system stability.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_C = I_{LOAD}\sqrt{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2V_{OUT}, shown in Equation (6):

$$I_C = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e.: 0.1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

An output capacitor (C_{OUT}) is required to maintain the DC output voltage. Low ESR ceramic capacitors can be used to keep the output ripple low. Generally, a 22μF output ceramic capacitor is sufficient for most cases. In higher output voltage conditions, a 47μF capacitor may be required for system stability. A larger output capacitor can result in a smaller output voltage ripple. When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Proper layout of the switching power supplies is critical for proper operation, especially for the high-switching converter. If the layout is not carefully done, the regulator could show poor line or load regulation and stability issues. For best results, refer to Figure 4 and follow the guidelines below.

1. Place the high-speed, step-down regulator, and input capacitor as close to the IC pins as possible.
2. Ensure that the two ends of the capacitor are connected to VIN and GND directly if the 0805 size ceramic capacitor is used.

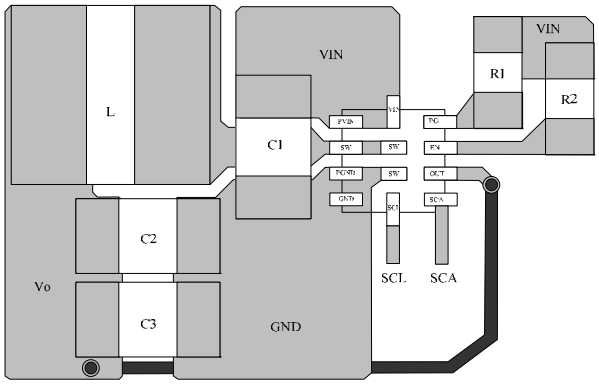


Figure 4: Recommended Layout

Design Example

Table 3 is a design example following the application guidelines for the specifications below:

Table 3: Design Example

V_{IN}	5V
V_O	0.9V
I_O	3A

The detailed application schematic is shown in Figure 5. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

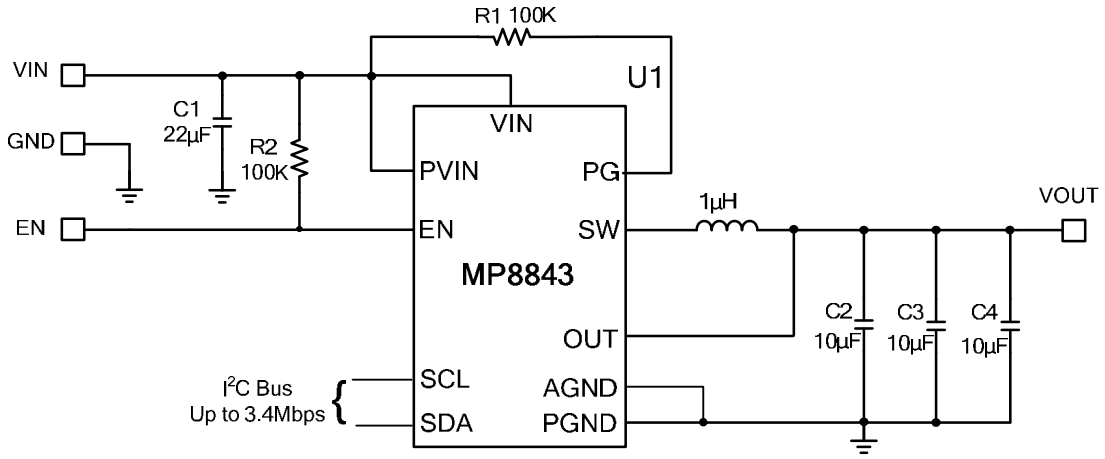


Figure 5: V_{OUT} Range Adjusted from 0.6V to 1.1V

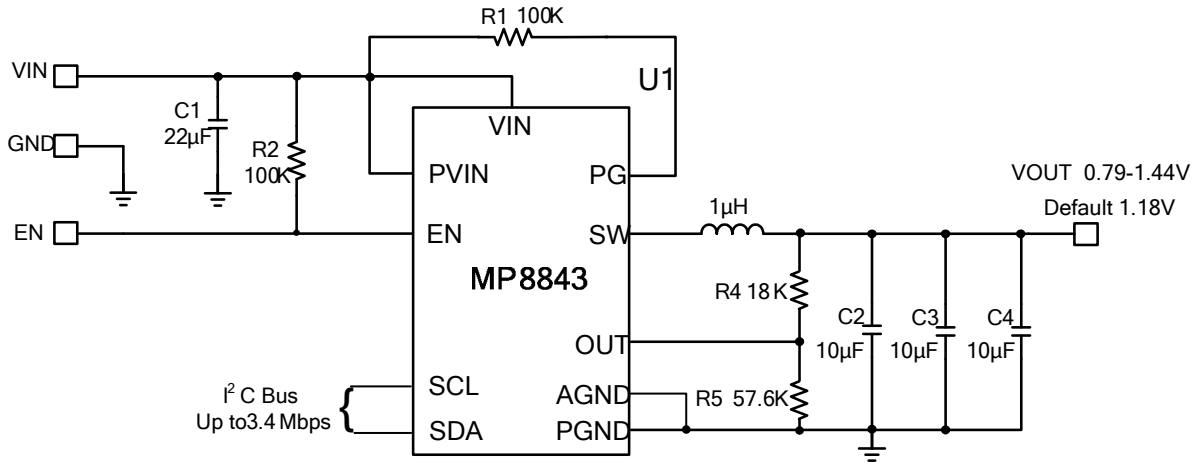


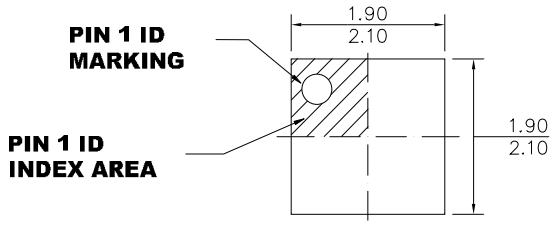
Figure 6: V_{OUT} Range Extended by External Feedback Resistor Network

NOTE:

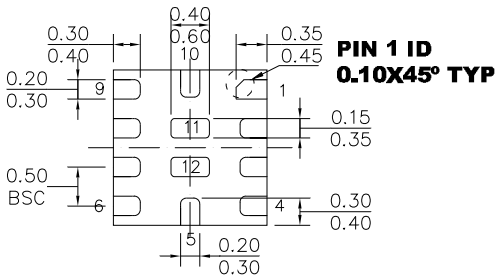
For other default V_{OUT} settings, fix R4 at first and calculate R5 based on the formula $V_{OUT} = 0.9V\frac{R4+R5}{R5}$.

PACKAGE INFORMATION

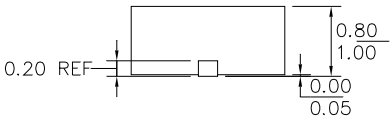
QFN-12 (2mmx2mm)



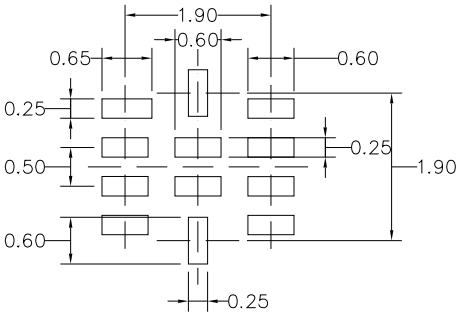
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.