EVALUATION KIT AVAILABLE

19-5945 Rev 0; 6/11

MAX1454

Precision Sensor Signal Conditioner with Overvoltage Protection

General Description

The MAX1454 is a highly integrated analog sensor signal conditioner targeted for automotive applications. The device provides amplification, calibration, and temperature compensation to enable an overall performance approaching the inherent repeatability of the sensor. The fully analog signal path introduces no quantization noise in the output signal while enabling digitally controlled trimming of the output. Offset and span are calibrated with integrated 16-bit DACs, allowing sensors to be truly interchangeable.

The device architecture includes a programmable sensor excitation, a 32-step programmable-gain amplifier (PGA), a 2K x 8 bits internal flash memory, four 16-bit DACs, and an on-chip temperature sensor. In addition to offset and span compensation, the device provides a unique temperature-compensation method for offset TC and FSO TC to provide a remarkable degree of flexibility while minimizing manufacturing costs.

The device is packaged in a 16-pin TSSOP and covers the automotive AEC-Q100 Grade 1 temperature range of -40°C to +125°C.

Applications

Pressure Sensors

Strain Gauges

Pressure Calibrators and Controllers

Resistive Element Sensors

Humidity Sensors

Benefits and Features

- **Complete Signal Conditioning in a Single IC Package**
  - **Provides Amplification, Calibration, and Temperature Compensation**
  - **Accommodates Sensor Output Sensitivities from 1mV/V to 200mV/V**
  - **Overvoltage Protection to 45V**
  - **Reverse-Voltage Protection to 45V**
- **High-Precision Compensation Reduces Downstream Circuit Complexity**
  - **Fully Analog Signal Path**
  - **16-Bit Offset and Span-Calibration Resolution**
  - **On-Chip Lookup Table Supports Multipoint Calibration Temperature Correction**
- **Supports Both Current and Voltage-Bridge Excitation**
- **Fast 85µs Step Response**
- **Sensor Fault Detection**
- **Simple PCB Layout**
- **Single-Pin Digital Programming**
- **No External Trim Components Required**

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maxim-ic.com/MAX1454.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V_{DD}, V_{DDF} .....-0.3V to +3.0V
V_{DDX}.....-45V to +45V
All Other Pins..... -0.3V to Min (V_{DDX} + 0.3V, 6V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 11.1mW/°C above +70°C) ...888.9mW

Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....90°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....27°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DDX} = 5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
External Supply Voltage	V_{DDX}		3.0	5.0	5.5	V
External Supply Current	I_{DDX}	(Note 3)		2.5	3	mA
Oscillator Frequency	f_{OSC}		0.85	1	1.15	MHz
LDO Regulator Output Voltage	V_{DD}	Not to be loaded by external circuitry, must be connected to a 0.1µF capacitor to GND	2.375	2.5	2.625	V
Power-On-Reset Threshold	V_{POR}	Referred to V_{DDX} pin		2.4		V
External Supply Voltage-Ramp Rate		(Note 4)	1			V/ms
ANALOG INPUT						
Input Impedance	R_{IN}			1		MΩ
Input-Referred Offset-Temperature Coefficient		(Notes 5, 6)		±1		µV/°C
Input-Referred Adjustable-Offset Range		Offset TC = 0 at gain = 44 (Note 7)	-150		+150	mV
Nonlinearity of Signal Path		Percent of 4V span, no load, IRO[3:0] = 0000bin, source impedance = 5kΩ, V_{OUT} = 0.5V to 4.5V; measured at V_{OUT} = [0.5V, 2.5V, 4.5V] at a gain of 112		0.01		%
Common-Mode Rejection Ratio	CMRR	Specified for common-mode voltages between GND and V_{DDX}		90		dB
Input-Referred Adjustable FSO		(Note 8)	1		200	mV/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDX} = 5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG OUTPUT							
Differential Signal Gain		Selectable in 32 steps			6 to 2048		V/V
		PGA[4:0] = 00000bin		5.5	6	6.5	
		PGA[4:0] = 00101bin		12.5	14	15.5	
		PGA[4:0] = 01010bin		40	44	48	
		PGA[4:0] = 01100bin		58	64	70	
		PGA[4:0] = 01101bin		72	80	88	
		PGA[4:0] = 01110bin		86	96	106	
		PGA[4:0] = 01111bin		101	112	123	
		PGA[4:0] = 10000bin		130	144	158	
		PGA[4:0] = 10110bin		374	416	458	
		PGA[4:0] = 11100bin		1037	1152	1267	
		PGA[4:0] = 11111bin		1823	2048	2253	
Output-Voltage Swing		No load		V_{GND} + 0.02		V_{DDX} - 0.32	V
Output-Voltage Low		I_{OUT} = 1mA sinking, T_A = T_{MIN} to T_{MAX}				0.25	V
Output-Voltage High		I_{OUT} = 1mA sourcing, T_A = T_{MIN} to T_{MAX}		V_{DDX} - 0.55			V
Output Current Drive Capability		Maintain DC output to 2mV error compared to no load case (Note 4)		±1			mA
Output Source Current Limit						8	mA
Output Sink Current Limit				-8			mA
Output Impedance at DC		V_{OUT} = 2.5V			0.2		Ω
Output Offset Ratio	ΔV_{OUT}/ ΔOffset DAC			0.9		1.2	V/V
Output Offset TC Ratio	ΔV_{OUT}/ ΔOffset TC DAC			0.9		1.2	V/V
Step Response (63% Final Value)					85		µs
Maximum Capacitive Load					0.01		µF
Noise at Output Pin		DC to 1kHz, source impedance = 5kΩ	Gain = 36		0.5		mV_{RMS}
			Gain = 256		1.5		
			Gain = 512		3		
			Gain = 1024		6		
			Gain = 2048		12		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDX} = 5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BRIDGE DRIVE						
Bridge Current	I_{BDR}		0.1		2.5	mA
Current-Mirror Ratio	AA	CMRATIO[1:0] = 00	4.8	6	7.2	A/A
		CMRATIO[1:0] = 01	9.6	12	14.4	
		CMRATIO[1:0] = 10	14.4	18	21.6	
		CMRATIO[1:0] = 11	24	30	36	
Maximum Bridge Load Capacitance		Voltage excitation mode (Note 4)	1			nF
FSO DAC Code Range		(Note 4)	0x4000		0xC000	Hex
Output Voltage Range	V_{BDR}	(Note 4)	0.75		V_{DDX} - 0.75	V
DIGITAL-TO-ANALOG CONVERTERS (DACs)						
DAC Resolution				16		Bits
Offset DAC Bit Weight	$\Delta V_{OUT}/\Delta Code$	DAC reference = V_{DDX} = 5V		76		µV/bit
Offset TC DAC Bit Weight	$\Delta V_{OUT}/\Delta Code$	DAC reference = V_{BDR} = 2.5V		38		µV/bit
FSO DAC Bit Weight	$\Delta V_{BDR}/\Delta Code$	DAC reference = V_{DDX} = 5V		76		µV/bit
FSO TC DAC Bit Weight	$\Delta V_{BDR}/\Delta Code$	DAC reference = V_{BDR} = 2.5V		38		µV/bit
COARSE-OFFSET DAC						
IRO DAC Resolution		Including sign		5		Bits
IRO DAC Bit Weight	$\Delta V_{OUT}/\Delta Code$	Input referred, DAC reference = V_{DDX} = 5V (Note 9)		3.7		mV/bit
INTERNAL RESISTORS						
OUT/DIO Pullup Resistance	R_{PULLUP}			100		kΩ
Current Source Reference Resistor	R_{ISRC}			10		kΩ
Current Source Reference Resistor Temperature Coefficient	TCR_{ISRC}			600		ppm/°C
FLASH MEMORY						
Endurance		(Notes 4, 10)	10,000			Cycles
Retention		T_A = +85°C (Note 4)	10			Years
Page Erase Time		(Notes 4, 11)			32	ms
Mass Erase Time		(Notes 4, 11)			32	ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDX} = 5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Current		(Note 4)			8	mA
Program/Erase Current		(Note 4)			7	mA
TEMPERATURE-TO-DIGITAL CONVERTER						
Temperature ADC Resolution				8		Bits
Offset				±3		LSB
Gain				1.5		°C/Bit
Nonlinearity				±0.5		LSB
Lowest Digital Output				0x00		hex
Highest Digital Output				0xAF		hex
DIGITAL INPUT (OUT/DIO)						
Input Low Voltage	V_{IL}		0		V_{DDX}/3	V
Input High Voltage	V_{IH}		V_{DDX} x 2/3		V_{DDX}	V
OVERVOLTAGE PROTECTION						
Overvoltage-Protection Threshold			5.53	5.75	6.0	V
FAULT DETECTION						
IN+/IN- Low Comparator Threshold				0.2 x V_{BDR}		V
IN+/IN- High Comparator Threshold				0.8 x V_{BDR}		V
Detection-Threshold Accuracy				±25		mV
Comparator Hysteresis				20		mV
Output Clip Level During Fault Conditions		I_{OUT} = 1mA sinking		150	250	mV

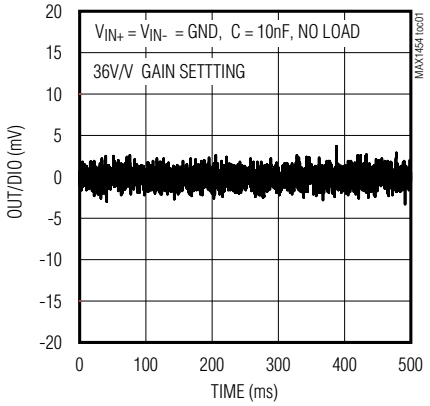
Note 2: All units are production tested at T_A = +25°C and +125°C. Specifications over temperature are guaranteed by design.
Note 3: Excludes sensor or load current. Analog mode with voltage excitation on BDR pin, FSODAC = 0x8000.
Note 4: Specification is guaranteed by design.
Note 5: All electronics temperature errors are compensated together with sensor errors.
Note 6: The sensor and the device must be at the same temperature during calibration and use.
Note 7: This is the maximum allowable sensor offset.
Note 8: This is the sensor's sensitivity normalized to its drive voltage, assuming a desired full-span output of V_{DDX} - 1V and a nominal bridge voltage of V_{DDX}/2.
Note 9: Bit weight is ratiometric to V_{DDX}.
Note 10: Programming of the flash memory at room temperature is recommended.
Note 11: No commands can be executed until the erase operation has completed. During erase operations, all commands sent to the device are ignored.

Typical Operating Characteristics

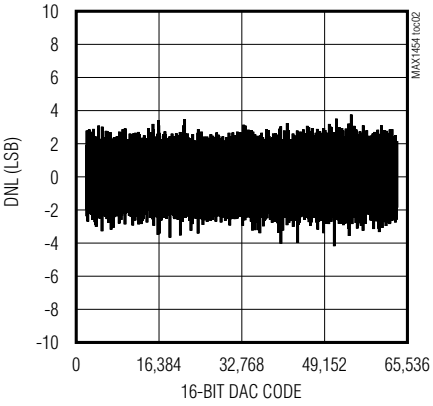
(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

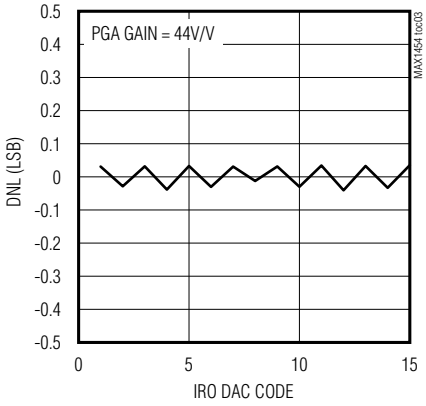
OUTPUT NOISE



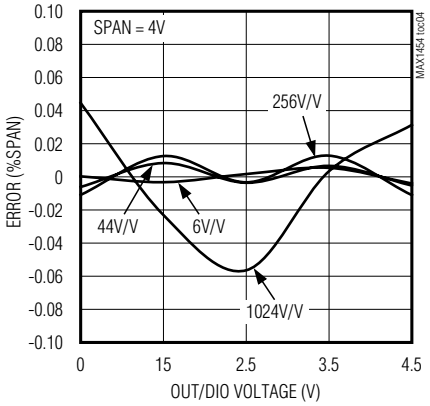
16-BIT DAC DIFFERENTIAL NONLINEARITY



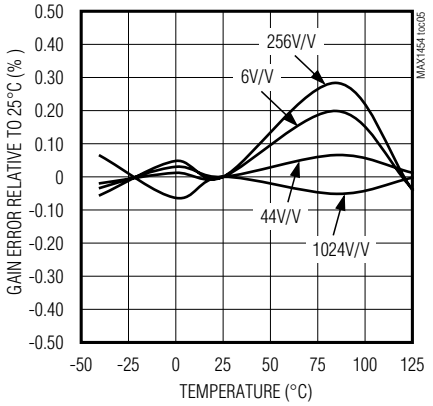
IRO DAC DIFFERENTIAL NONLINEARITY



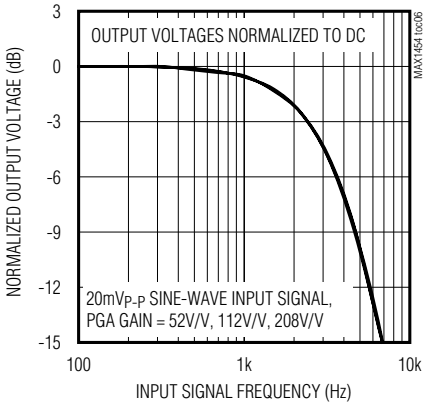
SIGNAL-PATH NONLINEARITY



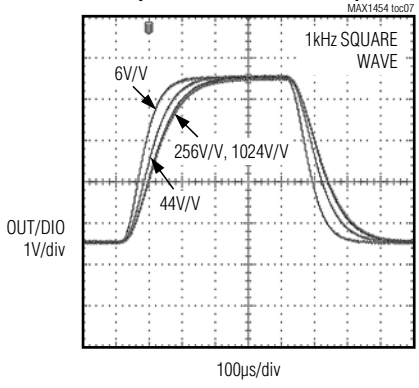
SIGNAL-PATH GAIN DEVIATION vs. TEMPERATURE



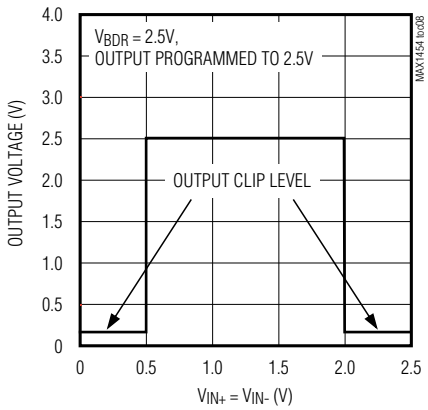
OUTPUT VOLTAGE vs. INPUT SIGNAL FREQUENCY



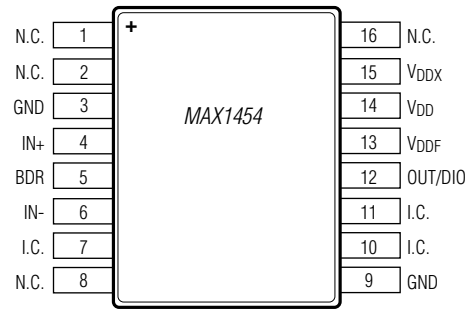
STEP RESPONSE (VARIOUS GAIN SETTINGS)



OUTPUT VOLTAGE vs. INPUT VOLTAGE (FAULT DETECTION ENABLED)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 2, 8, 16	N.C.	No Connection. Not internally connected.
3, 9	GND	Ground
4	IN+	Positive Bridge Input. IN+ can be swapped to IN- by Configuration Register 1.
5	BDR	Bridge Drive
6	IN-	Negative Bridge Input. IN- can be swapped to IN+ by Configuration Register 1.
7, 10, 11	I.C.	Internally Connected. Connect I.C. to GND.
12	OUT/DIO	Analog Output and Digital I/O (Multiplexed)
13	V_{DDF}	Flash Memory Supply Voltage. Connect V_{DDF} to V_{DD}.
14	V_{DD}	Regulated Supply Voltage. Requires a 0.1µF capacitor from V_{DD} to GND.
15	V_{DDX}	External Supply Voltage. Bypass to GND with a 0.1µF capacitor.

Detailed Description

The MAX1454 is a highly integrated analog sensor signal conditioner targeted for automotive applications. The device provides amplification, calibration, and temperature compensation to enable an overall performance approaching the inherent repeatability of the sensor. The fully analog signal path introduces no quantization noise in the output signal while enabling digitally controlled calibration of offset and span with integrated 16-bit DACs, allowing sensors to be truly interchangeable.

The device architecture includes a programmable sensor excitation, a 32-step PGA, a 2K x 8 bits internal flash memory, four 16-bit DACs, and an on-chip temperature sensor. In addition to offset and span compensation, the device provides a unique temperature-compensation method for offset TC and FSO TC, which was developed to provide a remarkable degree of flexibility while minimizing manufacturing costs.

The device uses four 16-bit DACs (offset, FSO, offset TC, and FSO TC) with coefficients ranging from 0x0000 to 0xFFFF. The offset DAC and FSO DAC are referenced to V_{DDX} (76µV resolution when V_{DDX} = 5V). The offset TC DAC and FSO TC DAC are referenced to the bridge voltage (38µV resolution when bridge voltage is 2.5V).

The user can select from one to 110 temperature points to compensate their sensor. This allows the latitude to compensate a sensor with a simple 1st-order linear correction or to match an unusual temperature curve. Programming up to 110 independent 16-bit flash memory locations corrects performance in 1.5°C temperature increments, over a range of -40°C to +125°C. For sensors that exhibit a characteristic temperature performance, a select number of calibration points can be used with a number of preset values that define the temperature curve. For full temperature compensation, the sensor and the device must be at the same temperature. In cases where the sensor is at a different temperature than the device, the device can use the sensor excitation voltage to provide 1st-order temperature compensation.

The single-pin, multiplexed, serial digital input/output (DIO) communication architecture, and the ability to time-share its activity with the sensor's output signal, enables output sensing and calibration programming on a single line.

The device allows complete calibration and sensor verification to be performed at a single test station. Once calibration coefficients have been stored in the device, the customer can retest to verify performance as part of a regular QA audit, or to generate final test data on individual sensors.

The device (Figure 1) provides an analog amplification path for the sensor signal. It also uses an analog architecture for 1st-order temperature correction. A digitally controlled analog path is then used for nonlinear temperature correction. Calibration and correction is achieved by varying the offset and gain of a PGA, and by varying the sensor bridge excitation current or voltage. The PGA utilizes a switched-capacitor CMOS

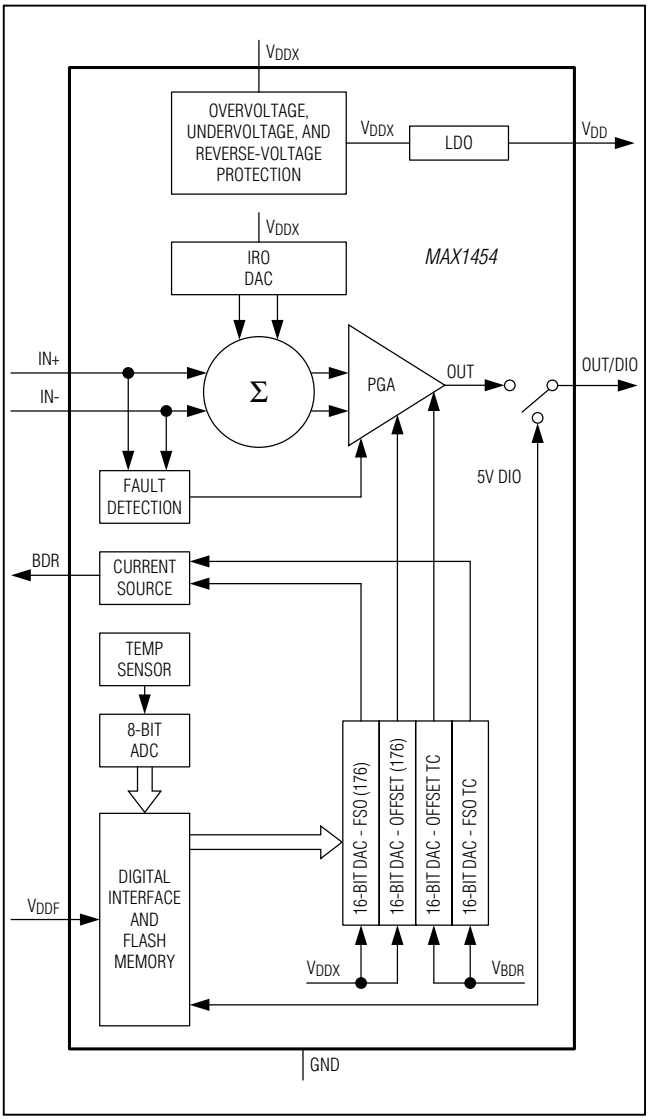


Figure 1. Functional Diagram

technology, with an input-referred offset-trimming range of more than ±150mV. The PGA provides gain values from 6V/V to 2048V/V in 32 steps.

The device includes an internal 2K x 8-bit flash memory to store calibration coefficients and user data. The internal memory contains the following information as 16-bit-wide words:

- Configuration Register 1 (CONFIG1)
- Configuration Register 2 (CONFIG2)
- Offset calibration coefficient (ODAC) table
- Offset Temperature Coefficient register (OTCDAC)
- Full-span output calibration coefficient (FSODAC) table
- FSO Temperature Coefficient register (FSOTCDAC)
- Power-Up Configuration register (PWRUPCFG)
- 256 bytes (2048 bits) uncommitted for customer programming of manufacturing data (e.g., serial number and date)

Offset Correction

Initial offset correction is accomplished at the input stage of the signal-gain amplifiers by a coarse offset setting. Final offset correction occurs through the use of a temperature-indexed lookup table with 176 16-bit entries. The on-chip temperature sensor provides a unique 16-bit offset-trim value from the table with an indexing resolution of approximately 1.5°C, from -40°C to +125°C. Every 4ms (programmable through the CONFIG2 register), the on-chip temperature sensor provides indexing into the offset lookup table in flash memory, with the resulting value transferred to the offset DAC register. The resulting voltage is fed into a summing junction at the PGA output, compensating the sensor offset with a resolution of ±76µV (±0.0019% FSO). If the offset TC DAC is set to zero, then the maximum temperature error is typically one degree of temperature drift of the sensor, given the offset DAC has corrected the sensor at every 1.5°C.

FSO Correction

Two functional blocks control the FSO gain calibration. First, a coarse gain is set by digitally selecting the gain of the PGA. Second, FSO DAC (and FSO TC DAC in current excitation mode) sets the sensor bridge current or voltage with the digital input obtained from the flash memory. FSO correction occurs through the use of a temperature-indexed lookup table with 176 16-bit entries. The on-chip temperature sensor provides a unique FSO trim from the table with one 16-bit value at every 1.5°C, from -40°C to +125°C.

Linear and Nonlinear Temperature Compensation

In most applications, the device and the sensor are at the same temperature, and coefficients in the offset and FSO lookup table correct both linear and nonlinear temperature errors to an accuracy approaching the sensor's repeatability error. In these applications, the offset TC DAC and FSO TC DACs should be set to nominal values.

In applications where the sensor and the device are at different temperatures, the FSO and offset DAC lookup tables cannot be used. Writing 16-bit calibration coefficients into the offset TC and FSO TC registers compensates 1st-order temperature errors. The piezoresistive sensor is powered by a current source, resulting in a temperature-dependent bridge voltage due to the sensor's temperature coefficient of resistance (TCR). The reference inputs of the offset TC DAC and FSO TC DAC are connected to the bridge voltage, causing their outputs to change as a function of temperature. When properly programmed, they provide 1st-order temperature compensation of the input signal. Only two test temperatures are required for linear temperature compensation.

The device uses a 10kΩ internal feedback resistor (R_{ISRC}) for FSO temperature compensation. Since the required feedback resistor value is sensor dependent, the device offers the ability to adjust the current-mirror ratio (CMRATIO) of the bridge driver. By selecting one of four CMRATIO settings in the CONFIG1 register, the bridge driver's feedback loop can be optimized for silicon piezoresistive sensors typically ranging from 2kΩ to 10kΩ.

Internal Temperature Sensor/ADC

The signal conditioner uses an internal temperature sensor to generate an 8-bit temperature index. An ADC converts the integrated temperature-sensor output to an 8-bit value every 4ms (programmable through the CONFIG2 register). This digitized value is then transferred into the temperature index register.

The typical transfer function for the temperature index is as follows:

TEMPINDEX = 0.6561 x temperature (°C) + 53.6

where TEMPINDEX is truncated to an 8-bit integer value. Typical values for the temperature index register are given in Table 13.

This index determines which FSO and offset DAC settings get loaded from the flash memory. The temperature-indexing boundaries are outside of the specified *Absolute Maximum Ratings* to eliminate indexing wrap-around errors. The minimum indexing value is 0x00, corresponding to approximately -82°C. All temperatures below this value generate the index 0x00. The maximum indexing value is 0xAF, corresponding to approximately +185°C. All temperatures higher than +185°C generate the index 0xAF.

Overvoltage, Undervoltage, Reverse-Voltage Protection

Overvoltage protection shuts down the device when the supply voltage is typically above 5.75V. A power-on reset prevents erroneous operation with supply voltages below 2.4V. Reverse voltage protects the device from negative voltages due to transients, reverse battery, etc. These protections allow the device to withstand any supply voltage from -45V to +45V.

Sensor Fault Detection

When enabled, the fault-detection circuitry on the device detects faults on the sensor inputs (IN+ and IN-). If either one of the sensor inputs is below the input low threshold (20% of V_{BDR}) or above the input high threshold (80% of V_{BDR}), a fault signal is asserted internally. If the part is in analog mode, the internal fault signal causes the voltage on the OUT/DIO pin to clip to a fixed DC level (typically 150mV). Enable or disable fault detection through the CONFIG2 register, bit 6 (ENFDET).

Internal Calibration Registers (ICRs)

The device has six 16-bit ICRs (ODAC, FSODAC, OTCDAC, FSOTCDAC, CONFIG1, and CONFIG2) that are loaded from flash memory, or loaded from the serial digital interface when in the digital programming mode. Data can be loaded into the ICRs under two different modes of operations (fixed analog operation and calibration operation).

Fixed Analog Operation

- The device has been calibrated.
- Power is applied to the device.
- The power-on-reset functions have completed.
- The digital listening mode times out and the device goes into the fixed analog mode.
- The internal temperature sensor stores the 8-bit TEMPINDEX value.
- Registers CONFIG1, CONFIG2, ODAC, FSODAC, OTCDAC, and FSOTCDAC are loaded from flash memory.
- After each time the DAC refresh timer reaches its set time period, the internal-temperature ADC updates the 8-bit TEMPINDEX value and the ODAC and FSODAC registers are refreshed from the temperature-indexed flash memory locations.

Calibration Operation (Registers Updated by Serial Communications)

- Power is applied to the device.
- The power-on-reset functions have completed.
- The digital listening mode detects serial communication.
- The registers can then be loaded from the serial digital interface by use of serial commands. See the *Serial-Interface Command Format* section.
- (Optionally) After calibration, the device can be set to run in fixed analog operation using a software command. Note that the configuration and DAC registers refresh from flash memory upon entering fixed analog mode.

Internal Flash Memory

The internal flash memory is organized as a 2K by 8-bit memory. It is divided into four pages with 512 bytes per page. Each page can be individually erased. The memory structure is arranged as shown in Table 1. The lookup tables for ODAC and FSODAC are also shown, with the respective TEMPINDEX pointer. The ODAC table occupies a segment from address 0x000 to address 0x15F, and the FSODAC table occupies a segment from 0x200 to 0x35F.

The flash memory is configured as an 8-bit wide array so each of the 16-bit registers is stored as two 8-bit quantities. The configuration registers and the FSOTCDAC and OTCDAC registers are loaded from the preassigned locations in the flash memory. The ODAC and FSODAC registers are loaded from memory lookup tables using an index pointer that is a function of temperature.

Maxim programs all flash memory locations to 0xFF, except for the reserved locations, 0x400 and 0x401. Values stored at 0x400 and 0x401 should be kept at the factory-programmed defaults.

Table 1. Flash Memory Address Map

PAGE	LOW-BYTE ADDRESS (hex)	HIGH-BYTE ADDRESS (hex)	TEMPINDEX[7:0] (hex)	CONTENTS
0	000	001	00	ODAC lookup table
	002	003	01	
	:	:	:	
	15C	15D	AE	
	15E	15F	AF to FF	
	160	161	—	CONFIG1
	162	163	—	CONFIG2
	164	165	—	Reserved
	166	167	—	OTCDAC
	168	169	—	Reserved
	16A	16B	—	FSOTCDAC
	16C	16D	—	PWRUPCFG
	16E	16F	—	Reserved
	:	:		
	17E	17F		
	180	181	—	128 general-purpose user bytes
	:	:		
	1FE	1FF		
1	200	201	00	FSODAC lookup table
	202	203	01	
	:	:	:	
	35C	35D	AE	
	35E	35F	AF to FF	
	360	361	—	Reserved
	:	:		
	37E	37F		
	380	381	—	128 general-purpose user bytes
	:	:		
	3FE	3FF		
2	400	401	—	Reserved*
	402	403		Reserved
	:	:		
	5FE	5FF		
3	600	601	—	Reserved
	:	:		
	7FE	7FF		

**Do not change values stored at locations 0x400 and 0x401 from the factory defaults.*

Communications Protocol

The DIO serial interface is used for asynchronous serial data communications between the device and a host calibration test system. The device automatically detects the baud rate of the host computer when the host transmits the initialization sequence. Baud rates between 4800bps and 38,400bps can be detected and used regardless of the internal oscillator frequency setting. Data format is always 1 start bit, 8 data bits, 1 stop bit, and no parity. Communications are only allowed when the device is in digital mode.

Initialization Sequence

Sending the initialization sequence shown below enables the device to establish the baud rate that initializes the serial port. The initialization sequence is 1 byte transmission of 01hex, as follows: 11111111**0**10000000**1**11111111. The first start bit **0** initiates the baud-rate synchronization sequence. The 8 data bits 01hex (LSB first) follow this and then the stop bit, which is indicated above as a **1**, terminates the baud-rate synchronization sequence. This initialization sequence on OUT/DIO should occur after a period of 2ms after stable power is applied to the device. This allows time for the power-on-reset function to complete.

Serial-Interface Command Format

All communication commands into the device follow a defined format utilizing an interface register set (IRS). The IRS is an 8-bit command that contains both an interface register set data (IRSD) nibble (4 bits) and an interface register set address (IRSA) nibble (4 bits). All internal calibration registers and flash memory locations are accessed for read and write through this interface register set. The IRS byte command is structured as follows:

IRS[7:0] = IRSD[3:0], IRSA[3:0]

where:

IRSA[3:0] is the 4-bit interface register set address and indicates which register receives the data nibble IRSD[3:0];

IRSA[0] is the first bit on the serial interface after the start bit;

IRSD[3:0] is the 4-bit interface register set data;

IRSD[0] is the 5th bit received on the serial interface after the start bit

The IRSA address decoding is shown in Table 14.

Special Command Sequences

A special command register to internal logic (CRIL[3:0]) causes execution of special command sequences within the device. These command sequences are listed as CRIL command codes, as shown in Table 15.

Write Examples

A 16-bit write to any of the internal calibration registers is performed as follows:

1) Write the 16 data bits to DHR[15:0] using 4 byte accesses into the interface register set.
2) Write the address of the target internal calibration register to ICRA[3:0].
3) Write the load internal calibration register (LdICR) command to CRIL[3:0]. When a LdICR command is issued to the CRIL register, the calibration register loaded depends on the address in the internal calibration register address (ICRA). Table 16 specifies which calibration register is decoded.

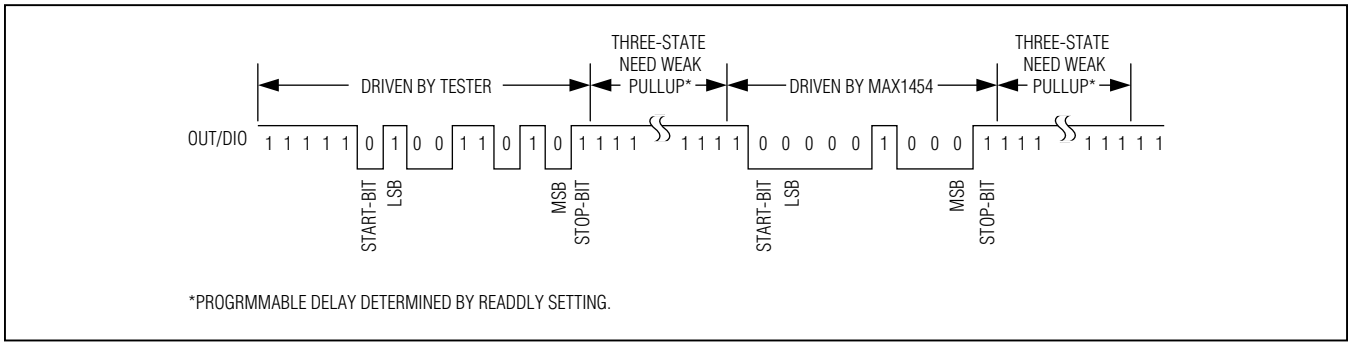


Figure 2. OUT/DIO Output Data Format

Erasing and Writing the Flash Memory

The internal flash memory needs to be erased (bytes set to FFhex) prior to programming the desired contents.

The internal flash memory can be entirely erased with the ERASE command, or partially erased with the PageErase command (see Table 15). It is necessary to wait 32ms after issuing the ERASE or PageErase command before sending the next command.

After the memory has been erased (value of every byte = FFhex), the user can program its contents using the following procedure:

1) Write the 8 data bits to DHR[7:0] using 2 byte accesses into the interface register set.
2) Write the address of the target internal memory location to IEEA[10:0] using 3 byte accesses into the interface register set.
3) Write the flash memory write command (EEPW) to CRIL[3:0].

Caution: It is not recommended to change values of flash memory locations 0x400 and 0x401. Changing the values at these locations (through a memory write or page/total erasure) can cause the device to lose its factory trim settings, which can affect device performance.

Multiplexed Analog and Serial Digital Output

When an RdIRS command is written to CRIL[3:0], OUT/DIO is configured as a digital output and the contents of the register designated by IRSP[3:0] are sent out as a byte framed by a start bit. Once the tester finishes sending the RdIRS command, it must three-state its connection to OUT/DIO to allow the device to drive the OUT/DIO line. The device three-states OUT/DIO high for a programmable number of byte times (determined by READDLY[1:0]) and then sends out the data byte (with a start and stop bit). The sequence is shown in Figure 2.

The data returned on an RdIRS command depends on the address in IRSP. Table 17 defines what is returned for the various addresses.

When an RdAlg command is written to CRIL[3:0] the analog signal designated by ALOC[4:0] is asserted on the OUT/DIO pin. The duration of the analog signal is determined by ATIM[3:0], after which the pin reverts to a digital I/O. The host computer or calibration system must three-state its connection to OUT/DIO after asserting the stop bit. Do not load the OUT/DIO line when reading nonbuffered internal signals.

The analog output sequence is shown in Figure 3. The digital serial interface and analog output are internally multiplexed onto OUT/DIO. The duration of the analog signal is controlled by ATIM[3:0], as given in Table 18.

The analog signal driven onto the OUT/DIO pin is determined by the value in the ALOC register. The signals are specified in Table 19.

Burst Mode Operation

The device supports burst mode operation for reading/writing blocks of data from/to flash memory addresses 0x000 to 0x3FF. Addresses 0x400 and 0x401 cannot be accessed with burst mode. First, program the starting address of the flash memory into IEEA[10:0]. Next, enable burst mode by writing a 1 to the burst mode enable bit (BURSTEN). In burst mode, an internal counter is used to increment the memory address with every read/write operation. With the 0-to-1 transition of BURSTEN, the memory address stored in IEEA[10:0] is latched into the internal counter as the starting address. Once the burst enable is high, the internal counter takes precedence over the memory address bits. All the memory read/write operations happen on the address indicated by the internal counter.

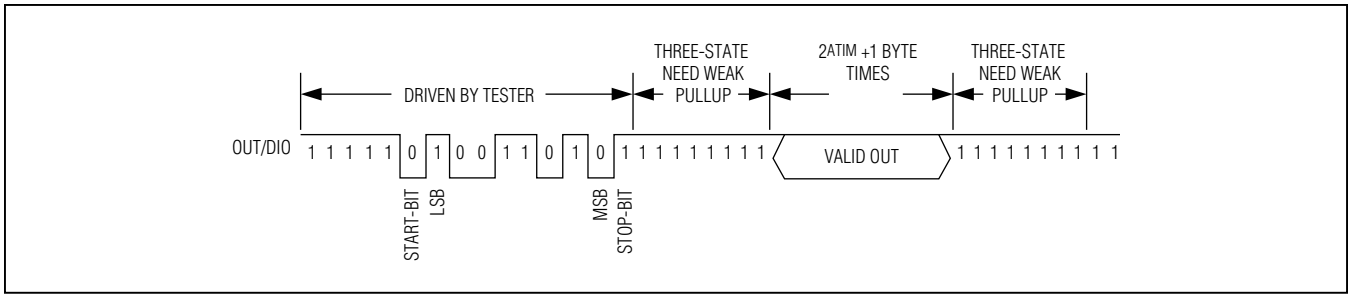


Figure 3. Analog Output Timing

To write to a flash memory location in burst mode, the user simply writes DHR[3:0], followed by DHR[7:4]. Since the internal counter keeps track of the memory address, there is no need to send address information to the part. After DHR[7:4] is written, a write command to the flash memory is automatically generated, the data in DHR[7:0] is written to the memory, and the address counter is incremented. If the user wishes to skip certain memory locations, first exit burst mode (by writing a 0 to BURSTEN), then program a new starting address. The user can now reenable burst mode again.

During burst read operations, the device waits for a read command before sending out data whose address is derived from the internal counter. To start burst read mode, first program the flash memory address into IEEA[10:0]. Next, write a 1 to BURSTEN to enable burst mode. The IRSP register must then be programmed to 0 (through an IRSA = 8 command). Then, send the flash memory read (RdEEP) CRIL command to initiate an internal read; the device sends the contents of the flash memory out of the DIO/OUT pin through the serial interface. Similar to the burst write operation, the burst read operation does not skip memory locations. To skip memory locations, first write a zero to BURSTEN to end burst mode. Next, change the memory address bits using the corresponding command bytes. Once the desired starting address is loaded, reenable burst mode to resume burst reading.

Always disable burst mode (IRSD = 0000 when IRSA = 1101) after burst reading/writing all the locations. This is necessary to continue in digital programming mode after all the burst read/writes are complete.

Note: Use burst mode to program a maximum of 1024 locations. Care must be taken to avoid additional writes to prevent unintentionally rewriting locations. The internal address counter wraps around to address 0x000 after reaching address 0x3FF.

Register Map

Table 2. Registers

REGISTER	DESCRIPTION
CONFIG1	Configuration Register 1
CONFIG2	Configuration Register 2
ODAC	Offset DAC
OTCDAC	Offset Temperature Coefficient DAC
FSODAC	Full-Span Output DAC
FSOTCDAC	Full-Span Output Temperature Coefficient DAC
PWRUPCFG	Power-Up Configuration

Table 3. Configuration Register 1 (CONFIG1[15:0])

BIT	NAME	DESCRIPTION
15:11	PGA[4:0]	Programmable-gain amplifier setting
10	PGA Sign	Logic 1 inverts IN- and IN+ polarity
9	IRO Sign	Logic 1 for positive input-referred offset (IRO), logic 0 for negative input-referred offset (IRO)
8:5	IRO[3:0]	Input-referred coarse-offset adjustment
4:3	CMRATIO[1:0]	Bridge driver current-mirror ratio
2	Reserved	Set to logic 0
1	ODAC Sign	Logic 1 for positive offset DAC output, logic 0 for negative offset DAC output
0	OTCDAC Sign	Logic 1 for positive offset TC DAC output, logic 0 for negative offset TC DAC output

Table 4. Configuration Register 2 (CONFIG2[15:0])

BIT	NAME	DESCRIPTION
15:7	Reserved	Reserved. Set to logic 0.
6	ENFDET	Enable fault-detection circuitry. Logic 1 enables fault detection.
5:4	REFRATE[1:0]	DAC register refresh rate during fixed analog mode
3	ENPULLUP	Enable internal pullup resistor on OUT/DIO pin. Logic 1 enables pullup.
2:1	READDLY[1:0]	Number of byte times the part waits before responding to read requests
0	EXCIMODE	Logic 1 for voltage excitation mode, logic 0 for current excitation mode

Table 5. Power-Up Configuration Register (PWRUPCFG[15:0])

BIT	NAME	DESCRIPTION
15:7	Reserved	Reserved. Set to logic 0.
6:3	DIGMODETIME[3:0]	Number of ms the part waits to receive a control word before switching to analog mode
2:0	CTRLREP[2:0]	Number of repetitions of the control word required to switch the part into digital mode

Table 6. PGA Setting (PGA[4:0])

PGA[4:0]	PGA GAIN (V/V)	PGA[4:0]	PGA GAIN (V/V)
00000	6	10000	144
00001	7	10001	176
00010	9	10010	208
00011	11	10011	256
00100	12	10100	288
00101	14	10101	352
00110	18	10110	416
00111	22	10111	512
01000	28	11000	576
01001	36	11001	704
01010	44	11010	832
01011	52	11011	1024
01100	64	11100	1152
01101	80	11101	1408
01110	96	11110	1664
01111	112	11111	2048

Table 7. Input-Referred Offset Setting (IRO Sign, IRO[3:0])

IRO SIGN	IRO[3:0]	INPUT-REFERRED OFFSET CORRECTION AS % OF V_{DDX}	INPUT-REFERRED OFFSET CORRECTION AT V_{DDX} = 5V DC (mV)	IRO SIGN	IRO[3:0]	INPUT-REFERRED OFFSET CORRECTION AS % OF V_{DDX}	INPUT-REFERRED OFFSET CORRECTION AT V_{DDX} = 5V DC (mV)
1	1111	1.11	55.5	0	0000	0	0
1	1110	1.04	51.8	0	0001	-0.07	-3.7
1	1101	0.96	48.1	0	0010	-0.15	-7.4
1	1100	0.89	44.4	0	0011	-0.22	-11.1
1	1011	0.81	40.7	0	0100	-0.30	-14.8
1	1010	0.74	37	0	0101	-0.37	-18.5
1	1001	0.67	33.3	0	0110	-0.44	-22.2
1	1000	0.59	29.6	0	0111	-0.52	-25.9
1	0111	0.52	25.9	0	1000	-0.59	-29.6
1	0110	0.44	22.2	0	1001	-0.67	-33.3
1	0101	0.37	18.5	0	1010	-0.74	-37
1	0100	0.30	14.8	0	1011	-0.81	-40.7
1	0011	0.22	11.1	0	1100	-0.89	-44.4
1	0010	0.15	7.4	0	1101	-0.96	-48.1
1	0001	0.07	3.7	0	1110	-1.04	-51.8
1	0000	0	0	0	1111	-1.11	-55.5

Table 8. Bridge Driver Current-Mirror Ratio Setting (CMRATIO[1:0])

CMRATIO[1:0]	CURRENT-MIRROR RATIO	BRIDGE RESISTANCE (kΩ)
00	6	10
01	12	5
10	18	3.33
11	30	2

Table 9. DAC Refresh Rate (REFRATE[1:0])

REFRATE[1:0]	UPDATE INTERVAL (ms)
00	4.096
01	16.384
10	65.536
11	131.072

Table 10. Wait Time for Read Requests (READDLY[1:0])*

READDLY[1:0]	RESPONSE DELAY IN BYTE TIMES (8-BIT TIME)
00	1 byte time (i.e., (1 x 8)/baud rate)
01	2 byte times
10	4 byte times
11	8 byte times

**The selected delay time is applied before and after the requested byte is read.*

Table 11. DIGMODETIME Setting* (DIGMODETIME[3:0])

DIGMODETIME[3:0]	DESCRIPTION
0000	Part stays in digital mode for 1ms after power-up (for each repetition of the control word)
0001	2ms wait
0010	3ms wait
0011	4ms wait
0100	5ms wait
0101	8ms wait
0110	10ms wait
0111	15ms wait
1000	20ms wait
1001	25ms wait
1010 to 1111	30ms wait**

**Wait times specified are based on a typical oscillator frequency of 1MHz. Wait times are proportional to the oscillation frequency. Actual wait times depend on the factory-trimmed oscillator frequency.*

***Parts ship with a DIGMODETIME setting of 1111.*

Table 12. CTRLREP Setting (CTRLREP[2:0])

CTRLREP[2:0]	DESCRIPTION
000	1 control word expected
001	1 control word expected
010	2 control words expected
011	3 control words expected
100	4 control words expected
101	5 control words expected
110	6 control words expected
111	Part powers up in digital mode*

**Parts ship with a CTRLREP setting of 111.*

Table 13. Temperature Index Typical Values

TEMPERATURE	TEMPINDEX[7:0]	
(°C)	DECIMAL	HEXADECIMAL
-40	27	1B
+25	70	46
+85	109	6D
+125	136	88

Table 14. IRSA Decoding (IRSA[3:0])

IRSA[3:0]	DESCRIPTION
0000	Write IRSD[3:0] to DHR[3:0] (data hold register).
0001	Write IRSD[3:0] to DHR[7:4] (data hold register).
0010	Write IRSD[3:0] to DHR[11:8] (data hold register).
0011	Write IRSD[3:0] to DHR[15:12] (data hold register).
0100	Reserved.
0101	Reserved.
0110	Write IRSD[3:0] to ICRA[3:0] or IEEA[3:0] (internal calibration register address or internal flash memory address nibble 0).
0111	Write IRSD[3:0] to IEEA[7:4] (internal flash memory address nibble 1).
1000	Write IRSD[3:0] to IRSP[3:0] or IEEA[10:8] (interface register set pointer where IRSP[2:0] is IEEA[10:8]).
1001	Write IRSD[3:0] to CRIL[3:0] (command register to internal logic).
1010	Write IRSD[3:0] to ATIM[3:0] (analog timeout value on read).
1011	Write IRSD[3:0] to ALOC[3:0] (analog location).
1100	Write IRSD[0] to ALOC[4] (analog location).
1101	Write IRSD[0] to the burst mode enable bit (BURSTEN). See the *Burst Mode Operation* section for details regarding read/write operations in this mode. Logic 1 enables burst mode.
1100 to 1111	Reserved.

Table 15. CRIL Command Codes (CRIL[3:0])

CRIL[3:0]	NAME	DESCRIPTION
0000	LdICR	Load internal calibration register at address given in ICRA with data from DHR[15:0].
0001	EEPW	Flash memory write of 8 data bits from DHR[7:0] to address location pointed by IEEA[10:0].
0010	ERASE	Erase all flash memory (all bytes equal FFhex).
0011	RdICR	Read internal calibration register as pointed to by ICRA and load data into DHR[15:0].
0100	RdEEP	Read internal flash memory location pointed by IEEA[10:0] and load data into DHR[7:0].
0101	RdIRS	Read interface register set pointer IRSP[3:0] and output the multiplexed digital signal onto OUT/DIO (see Table 17).
0110	RdAlg	Output the multiplexed analog signal (i.e., test mux output) onto OUT/DIO. The duration (in byte times) that the signal is asserted onto the pin is specified by ATIM[3:0] (Table 18) and the analog location is specified by ALOC[4:0] (Table 19).
0111	PageErase	Erases the page of the flash memory as pointed by IEEA[10:9]. There are 512 bytes per page.
1000	SwToANA	Switch to fixed analog mode.
1001 to 1110	Reserved	Reserved.
1111	RELEARN	Relearn the baud rate.

Table 16. ICRA Decoding (ICRA[3:0])

IRCA[3:0]	NAME	DESCRIPTION
0000	CONFIG1	Configuration Register 1
0001	CONFIG2	Configuration Register 2
0010	ODAC	Offset DAC
0011	OTCDAC	Offset Temperature Coefficient DAC
0100	FSODAC	Full-Span Output DAC
0101	FSOTCDAC	Full-Span Output Temperature Coefficient DAC
0110	PWRUPCFG	Power-Up Configuration
0111 to 1111	Reserved	Reserved (do not write to these locations)

Table 17. IRSP Decoding (IRSP[3:0])

IRSP[3:0]	RETURNED VALUE	IRSP[3:0]	RETURNED VALUE
0000	DHR[7:0]	0110	IEED[7:0] flash memory data byte
0001	DHR[15:8]	0111	TEMPINDEX[7:0]
0010	0bin, IEEA[10:8], ICRA[3:0] concatenated	1000	BitClock[7:0]
0011	CRIL[3:0], IRSP[3:0] concatenated	1001	00bin, BURSTEN, ALOC[4:0] concatenated
0100	0000bin, ATIM[3:0] concatenated	1010 to 1110	Reserved
0101	IEEA[7:0] flash memory address byte	1111	11001010 (CAhex) (this can be used to test communication)

Table 18. ATIM Definition (ATIM[3:0])

ATIM[3:0]	DURATION OF ANALOG SIGNAL SPECIFIED IN BYTE TIMES (8-BIT TIME)	ATIM[3:0]	DURATION OF ANALOG SIGNAL SPECIFIED IN BYTE TIMES (8-BIT TIME)
0000	2^0 + 1 = 2 byte times (i.e., (2 x 8)/baud rate)	0111	2^7 + 1 = 129 byte times
0001	2^1+ 1 = 3 byte times	1000	2^8 + 1 = 257 byte times
0010	2^2 + 1 = 5 byte times	1001	2^9 + 1 = 513 byte times
0011	2^3+ 1 = 9 byte times	1010	2^{10} + 1 = 1025 byte times
0100	2^4 + 1 = 17 byte times	1011	2^{11} + 1 = 2049 byte times
0101	2^5 + 1 = 33 byte times	1100	2^{12} + 1 = 4097 byte times
0110	2^6 + 1 = 65 byte times	1101	2^{13} + 1 = 8193 byte times
		1110 or 1111	2^{14} + 1 = 16,385 byte times

Table 19. ALOC Definition (ALOC[4:0])

ALOC[4:0]	NAME	DESCRIPTION
BUFFERED OUTPUTS		
00000	OUT	PGA output
00001	BDR1	Bridge drive voltage
00010	V_{ISRC}	Bridge drive current-setting voltage (see the *Detailed Block Diagram*)
00011	V_{DD}	Internal regulated supply
00100	AGND	Internal analog ground; approximately 1/2 of V_{DD}
00101	$V_{DUALDAC}$	Full-scale output plus full-scale output TC DAC (see the *Detailed Block Diagram*)
00110	V_{ODAC}	Offset DAC (see the *Detailed Block Diagram*)
00111	V_{OTCDAC}	Offset TC DAC (see the *Detailed Block Diagram*)
01000	V_{REF}	Bandgap voltage reference (nominally 1.25V)
01001	Reserved	Reserved
01010	Reserved	Reserved
01011	REFD3BUF	Ratiometric reference; approximately 1/3 of V_{DDX}
01100	Reserved	Reserved
01101	Reserved	Reserved
01110	IN+	Sensor's positive input
01111	IN-	Sensor's negative input
NONBUFFERED OUTPUTS		
10000	BDR2	Bridge drive voltage
10001	V_{DDI}	Internal positive supply
10010	GND	Internal ground
10011 to 11101	Reserved	Reserved
SPECIAL-PURPOSE OUTPUTS		
11110	CLIPLVL	Output clip level during fault conditions (buffered output)
11111	Hi-Z	High-impedance state on OUT/DIO

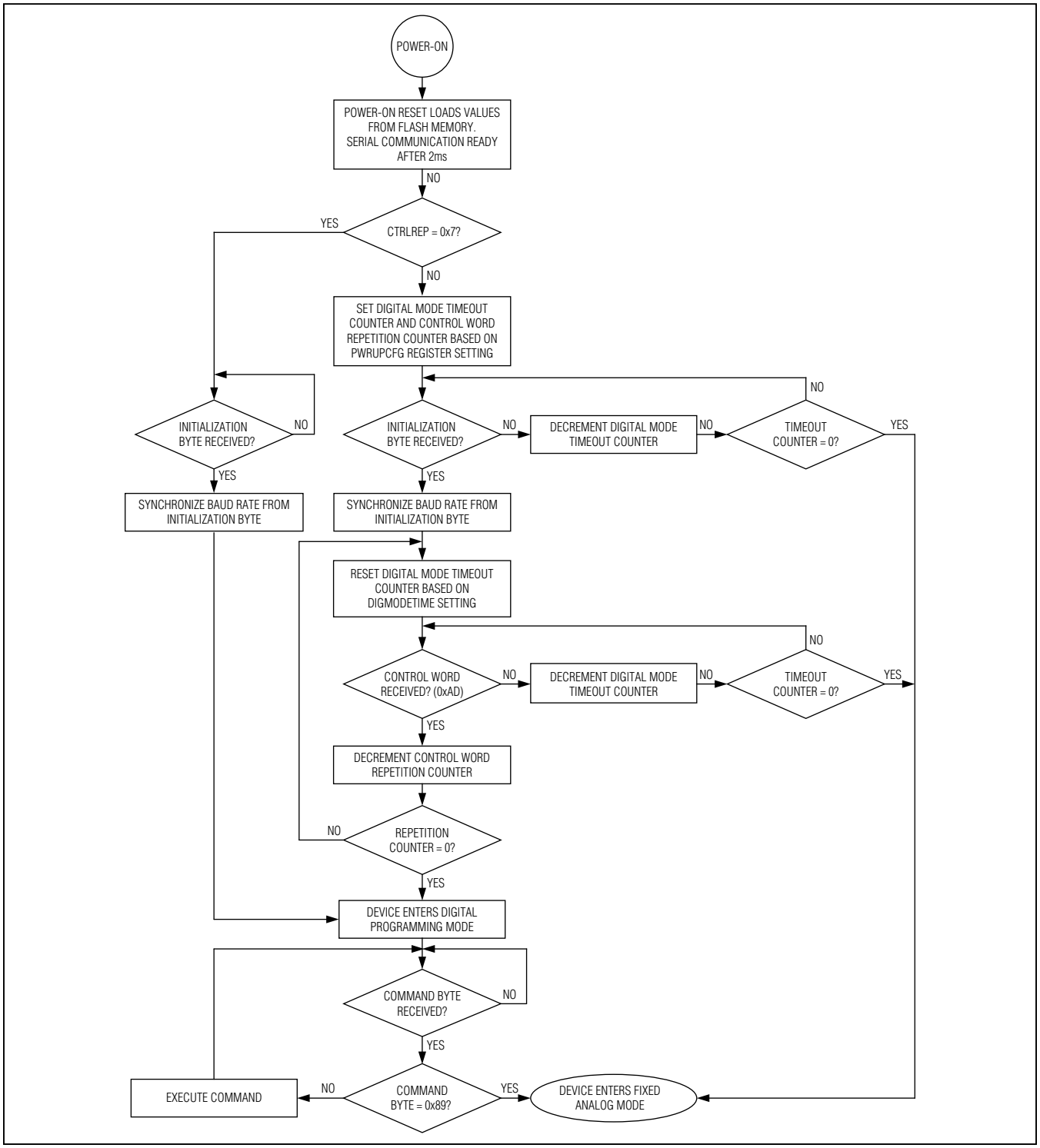


Figure 4. Power-Up Flow Chart

Power-Up Control Sequence

The device uses a power-up state machine to determine whether the device should switch to the fixed analog mode, or enable the digital programming mode (Figure 4).

At power-up, the device loads the PWRUPCFG register to establish a wait time (Table 11), and the number of control words (Table 12) required to enter the digital programming mode. If the wait time expires, the device automatically switches to the fixed analog mode. However, if the interface receives the correct number of control words within the established wait times, the device enters the digital programming mode. A serial command enables the device to switch into the fixed analog mode after the part has been programmed.

Note: Setting CTRLREP[2:0] to 111 in the PWRUPCFG flash memory location forces the part into the digital programming mode without the need for control words (an initialization byte is still required). By default, parts shipped from the factory are programmed to start in the digital programming mode.

Sensor Compensation Overview

The device compensates for sensor offset, FSO, and temperature errors by loading the internal calibration registers with the compensation values. These compensation values can be loaded to registers directly through the serial digital interface during calibration, or loaded automatically from flash memory at power-on. During the calibration process, the device is configured, tested, and compensation values are calculated and stored in the internal flash memory. Once programmed, after each power-up, the device autoloads the registers from flash memory and is ready for use without further configuration.

Compensation requires an examination of the sensor performance over the operating pressure and temperature range. A minimum of two test temperatures and two test pressures (zero and full scale) are required to correct the linear component of temperature error to achieve pressure calibration. For higher temperature accuracy, more test temperatures must be used. A typical compensation procedure can be summarized in the following sections.

Initialize the Device

Initialize the device registers with known values (e.g., compensation coefficients of a similar device) or determine values for IRO, PGA gain, FSO DAC, and offset DAC based on sensor parameters (offset, sensitivity, bridge resistance, etc). Select a current-mirror ratio value corresponding to the sensor in use. Initialization is an important step to ensure that the device output remains in range over the full operating conditions. When the device is initialized successfully, the excitation voltage is within the normal range, and the output voltage is around the desired offset value (when zero pressure is applied).

Characterize the Sensor at Test Temperatures

1) Set the temperature to the first test temperature point and allow the system to reach equilibrium.
2) By changing the FSO DAC through an iterative process, set the bridge voltage to a value that produces the desired output span. Change the offset DAC as necessary.
3) Once the desired output span is achieved, change the offset DAC to produce the final offset.
4) Record the values of TEMPINDEX, FSODAC, and ODAC. The device flash memory can be used to store the information.
5) Change the temperature to the next value and repeat this procedure to determine a unique value for the TEMPINDEX, FSODAC, and ODAC at every test temperature.

Calculate Compensation Coefficients

1) **FSO Lookup Table:** Using a fitting function, fit the FSODAC and TEMPINDEX values obtained during the characterization step and generate an array of 176 elements (FSODAC vs. TEMPINDEX array, where $0 \leq$ TEMPINDEX ≤ 175).
2) **Offset Lookup Table:** Using a fitting function, fit the ODAC and TEMPINDEX values obtained during the characterization step and generate an array of 176 elements (ODAC vs. TEMPINDEX array).

Program Flash Memory and Final Test

1) Program the device by writing to the ODAC and FSODAC lookup tables, and the OTCDAC, FSOTCDAC, CONFIG1, CONFIG2, PWRUPCFG, and user data locations in flash memory.
2) While the sensor is still at the last test temperature point, perform a final test to verify the compensation accuracy.

Applications Information

Typical Ratiometric Operating Circuit

Ratiometric output configuration provides an output that is proportional to the power-supply voltage. This output can then be applied to a ratiometric ADC to produce a digital value independent of supply voltage. Ratiometricity is an important consideration for battery-operated instruments, automotive, and some industrial applications.

The device provides a high-performance ratiometric output with a minimum number of external components (Figure 5). These external components include the following:

- Supply bypass capacitor (V_{DDX})
- 0.1µF output capacitor (V_{DD})
- Optional output capacitor (OUT/DIO)

Typical Nonratiometric Operating Circuit (6V DC < V_{PWR} < 40V DC)

Nonratiometric output configuration enables the sensor power to vary over a wide range. A high-performance voltage reference, such as the MAX15006B, is incorporated in the circuit to provide a stable supply and reference for device operation. A typical nonratiometric circuit is shown in Figure 6. Nonratiometric operation is valuable when a wide range of input voltage is to be expected and the system ADC or readout device does not enable ratiometric operation.

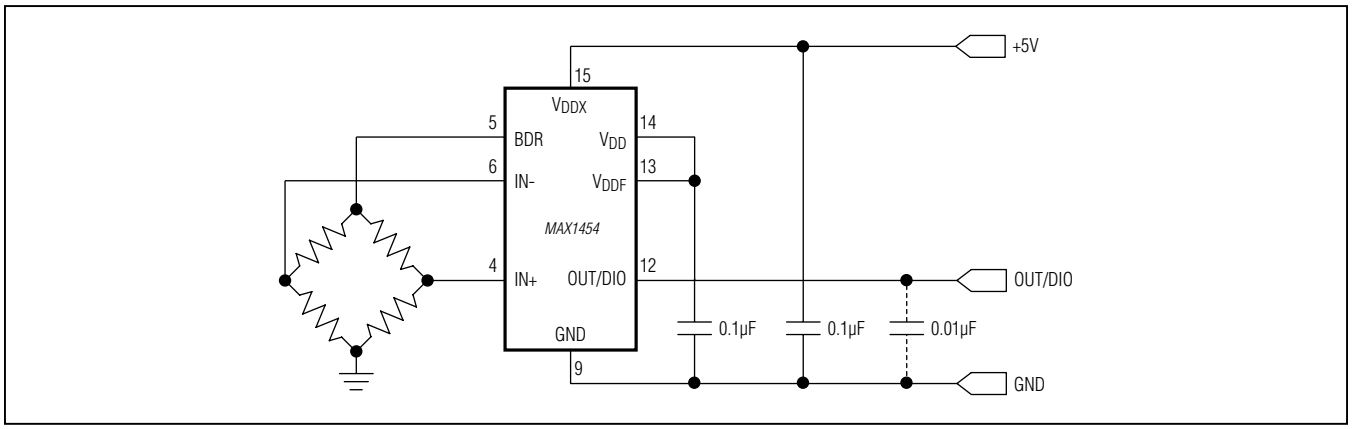


Figure 5. Basic Ratiometric Output Configuration

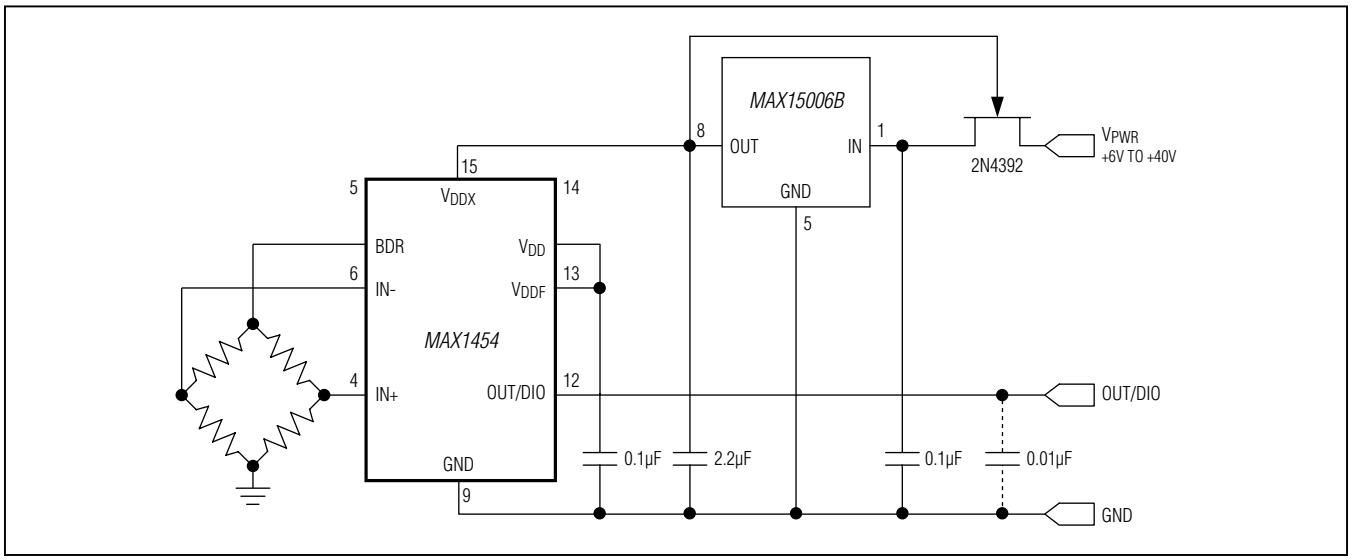
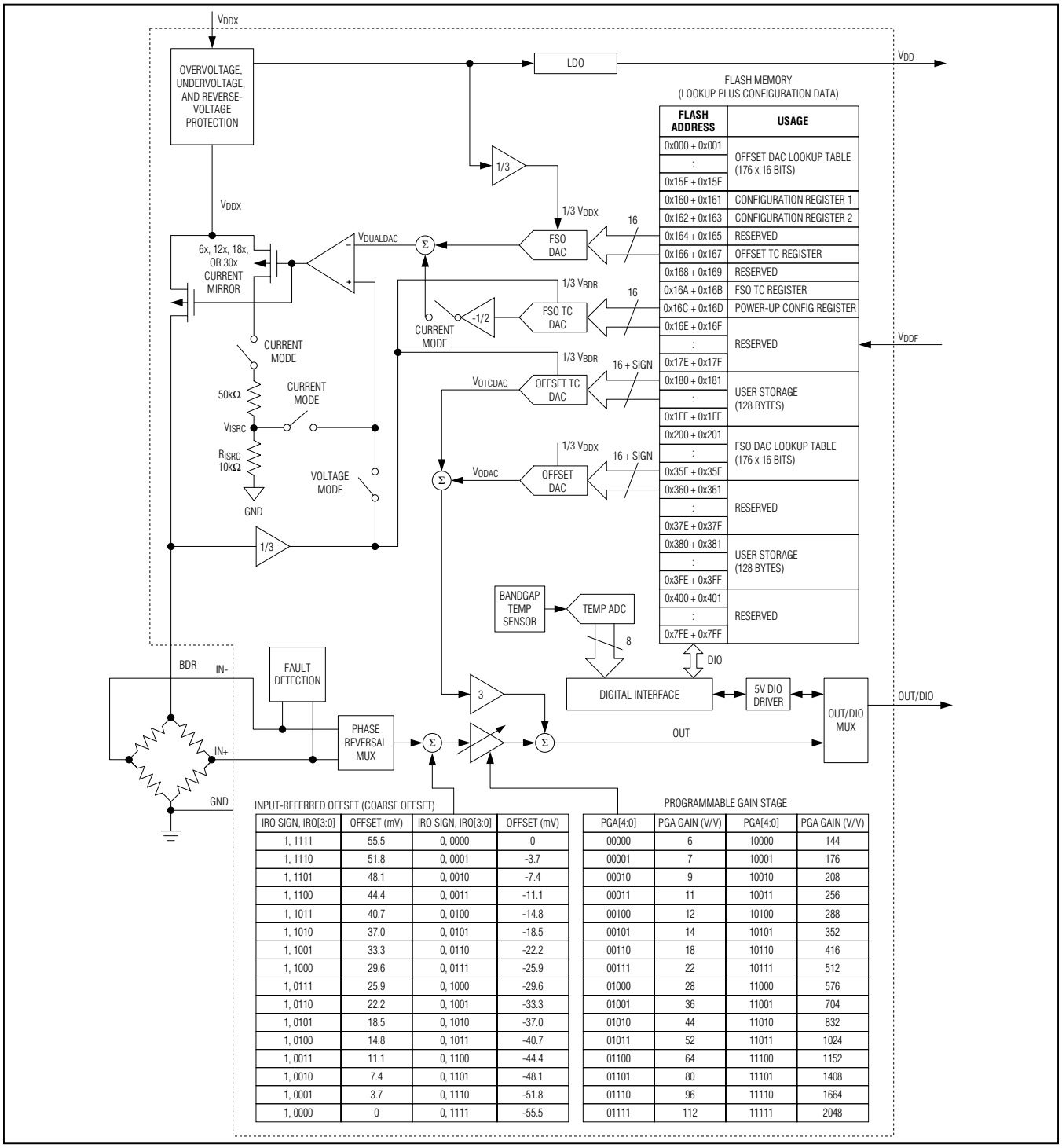


Figure 6. Basic Nonratiometric Output Configuration

Detailed Block Diagram



FLASH ADDRESS	USAGE
0x000 + 0x001 : 0x15E + 0x15F	OFFSET DAC LOOKUP TABLE (176 x 16 BITS)
0x160 + 0x161	CONFIGURATION REGISTER 1
0x162 + 0x163	CONFIGURATION REGISTER 2
0x164 + 0x165	RESERVED
0x166 + 0x167	OFFSET TC REGISTER
0x168 + 0x169	RESERVED
0x16A + 0x16B	FSO TC REGISTER
0x16C + 0x16D	POWER-UP CONFIG REGISTER
0x16E + 0x16F : 0x17E + 0x17F	RESERVED
0x180 + 0x181 : 0x1FE + 0x1FF	USER STORAGE (128 BYTES)
0x200 + 0x201 : 0x35E + 0x35F	FSO DAC LOOKUP TABLE (176 x 16 BITS)
0x360 + 0x361 : 0x37E + 0x37F	RESERVED
0x380 + 0x381 : 0x3FE + 0x3FF	USER STORAGE (128 BYTES)
0x400 + 0x401 : 0x7FE + 0x7FF	RESERVED

INPUT-REFERRED OFFSET (COARSE OFFSET)

IRO SIGN, IRO[3:0]	OFFSET (mV)	IRO SIGN, IRO[3:0]	OFFSET (mV)
1, 1111	55.5	0, 0000	0
1, 1110	51.8	0, 0001	-3.7
1, 1101	48.1	0, 0010	-7.4
1, 1100	44.4	0, 0011	-11.1
1, 1011	40.7	0, 0100	-14.8
1, 1010	37.0	0, 0101	-18.5
1, 1001	33.3	0, 0110	-22.2
1, 1000	29.6	0, 0111	-25.9
1, 0111	25.9	0, 1000	-29.6
1, 0110	22.2	0, 1001	-33.3
1, 0101	18.5	0, 1010	-37.0
1, 0100	14.8	0, 1011	-40.7
1, 0011	11.1	0, 1100	-44.4
1, 0010	7.4	0, 1101	-48.1
1, 0001	3.7	0, 1110	-51.8
1, 0000	0	0, 1111	-55.5

PROGRAMMABLE GAIN STAGE

PGA[4:0]	PGA GAIN (V/V)	PGA[4:0]	PGA GAIN (V/V)
00000	6	10000	144
00001	7	10001	176
00010	9	10010	208
00011	11	10011	256
00100	12	10100	288
00101	14	10101	352
00110	18	10110	416
00111	22	10111	512
01000	28	11000	576
01001	36	11001	704
01010	44	11010	832
01011	52	11011	1024
01100	64	11100	1152
01101	80	11101	1408
01110	96	11110	1664
01111	112	11111	2048

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1454AUE/V+	-40°C to +125°C	16 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP	U16M+1	21-0066	90-0117

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—