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82C86H

CMOS Octal Bus Transceiver

FN2977
Rev 2.00
June 2004

Features

- **Full Eight Bit Bi-Directional Bus Interface**
- **Industry Standard 8286 Compatible Pinout**
- **High Drive Capability**
  - **B Side I_{OL} 20mA**
  - **A Side I_{OL} 12mA**
- **Three-State Outputs**
- **Propagation Delay . . . . 35ns Max.**
- **Gated Inputs**
  - **Reduce Operating Power**
  - **Eliminate the Need for Pull-Up Resistors**
- **Single 5V Power Supply**
- **Low Power Operation. . . . . ICCSB = 10μA**
- **Operating Temperature Range**
  - **ID82C86H . . . . -40°C to +85°C**

Description

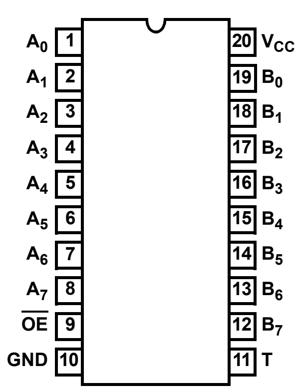
The Intersil 82C86H is a high performance CMOS Octal Transceiver manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C86H provides a full eight-bit bi-directional bus interface in a 20 lead package. The Transmit (T) control determines the data direction. The active low output enable ($\overline{OE}$) permits simple interface to the 80C86, 80C88 and other microprocessors. The 82C86H has gated inputs, eliminating the need for pull-up/pull-down resistors and reducing overall system operating power dissipation.

Ordering Information

PART NUMBER 8MHz	PACKAGE	TEMP. RANGE	PKG DWG. #
ID82C86H	20 Ld CERDIP	-40°C to +85°C	F20.3

Pinout

82C86H (CERDIP)
TOP VIEW



TRUTH TABLE

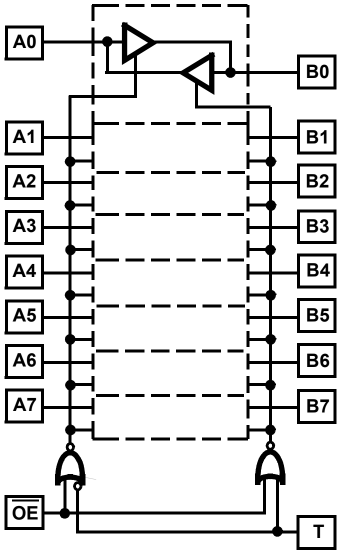
T	OE	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = Logic One
L = Logic Zero
I = Input Mode
O = Output Mode
X = Don't Care
Hi-Z = High Impedance

PIN NAMES

PIN	DESCRIPTION
A_0-A_7	Local Bus Data I/O Pins
B_0-B_7	System Bus Data I/O Pins
T	Transmit Control Input
$\overline{OE}$	Active Low Output Enable

Functional Diagram



Gated Inputs

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Intersil 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (See Figures 1 and 2). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in ICC if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). ICC remains below the maximum ICC standby specification of 10μA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C86H/87H data sheet is determined by:

$$I = C_L(dv/dt) \quad \text{(EQ. 1)}$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L\frac{(VCC \times 80\%)}{tR/tF} \quad \text{(EQ. 2)}$$

where tR = 20ns, V_{CC} = 5.0V, C_L = 300pF on each eight outputs.

$$I = (80 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9}) = 480mA \quad \text{(EQ. 3)}$$

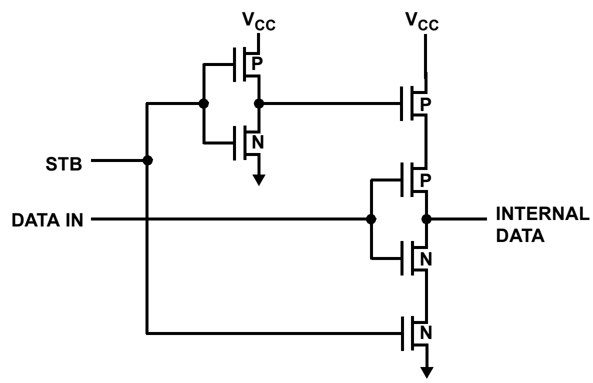


FIGURE 1. 82C82/83H

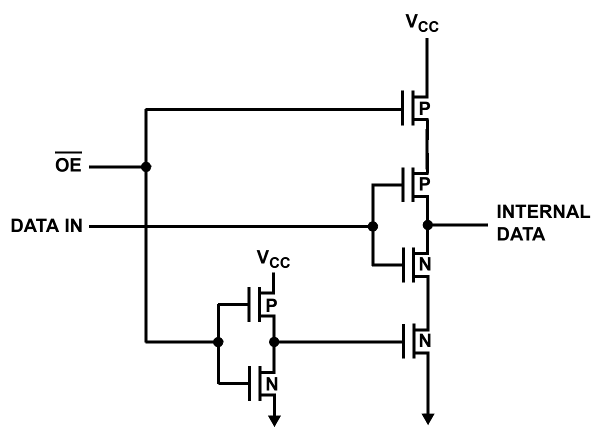


FIGURE 2. 82C86H/87H GATED INPUTS

This current spike may cause a large negative voltage spike on V_{CC} which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1μF ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

Absolute Maximum Ratings

Supply Voltage . . . . +8.0V
Input, Output or I/O Voltage . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . +4.5V to +5.5V
Operating Temperature Range . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	70	16

Maximum Storage Temperature Range . . . . -65°C to +150°C
Maximum Junction Temperature . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . +300°C

Die Characteristics

Gate Count . . . . 265 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One	2.0	-	V	C82C86H, I82C86H
	Input Voltage	2.2		V	M82C86H (Note 1)
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
V_{OH}	Logical One Output Voltage				
	B Outputs	3.0		V	I_{OH} = -8mA
	A Outputs	3.0		V	I_{OH} = -4mA
	A or B Outputs	V_{CC} -0.4		V	I_{OH} = -100µA
V_{OL}	Logical Zero Output Voltage				
	B Outputs		0.45	V	I_{OL} = 20mA
	A Outputs		0.45	V	I_{OL} = 12mA
I_I	Input Leakage Current	-10.0	10.0	µA	V_{IN} = GND or V_{CC} DIP Pins 9, 11
IO	Output Leakage Current	-10.0	10.0	µA	VO = GND or V_{CC}, $\overline{OE}$ Š Š≥ V_{CC} -0.5V DIP Pins 1 - 8, 12 - 19
ICCSB	Standby Power Supply Current	-	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
ICCOP	Operating Power Supply Current	-	1	mA/MHz	T_A = +25°C, Typical (See Note 2)

NOTES:

1. V_{IH} is measured by applying a pulse of magnitude = $V_{IH(MIN)}$ to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (T, $\overline{OE}$) are tested separately with all device data input pins at V_{CC} -0.4
2. Typical ICCOP = 1mA/MHz of read/ cycle time. (Example: 1.0µs read/write cycle time = 1mA).

Capacitance T_A = +25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance			
	B Inputs	18	pF	Freq = 1MHz, all measurements are referenced to device GND
	A Inputs	14	pF	

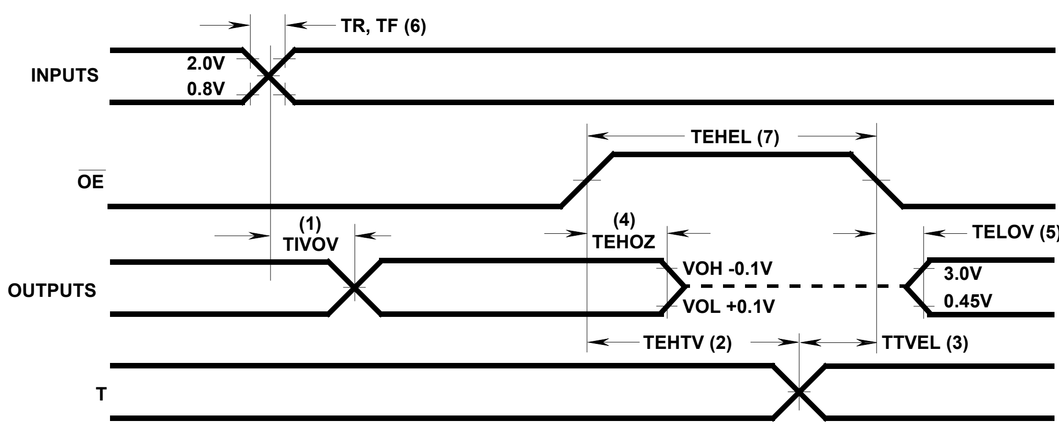
AC Electrical Specifications V_{CC} = 5.0V ± 10%; Freq = 1MHz: T_A = -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TIVOV	Input to Output Delay				Notes 1, 2
	Inverting	5	30	ns	
	Non-Inverting	5	32	ns	
(2) TEHTV	Transmit/Receive Hold Time	5	-	ns	Notes 1, 2
(3) TTVEL	Transmit/Receive Setup Time	10	-	ns	Notes 1, 2
(4) TEHOZ	Output Disable Time	5	30	ns	Notes 1, 2
(5) TELOV	Output Enable Time	10	50	ns	Notes 1, 2
(6) TR, TF	Input Rise/Fall Times	-	20	ns	Notes 1, 2
(7) TEHEL	Minimum Output Enable High Time				Note 3
	82C86H	30	-	ns	
	82C86H-5	35	-	ns	

NOTES:

1. All AC parameters tested as per test circuits and definitions in timing waveforms and test load circuits. Input rise and fall times are driven at 1ns/V.
2. Input test signals must switch between V_{IL} - 0.4V and V_{IH} +0.4V.
3. A system limitation only when changing direction. Not a measured parameter.

Timing Waveform

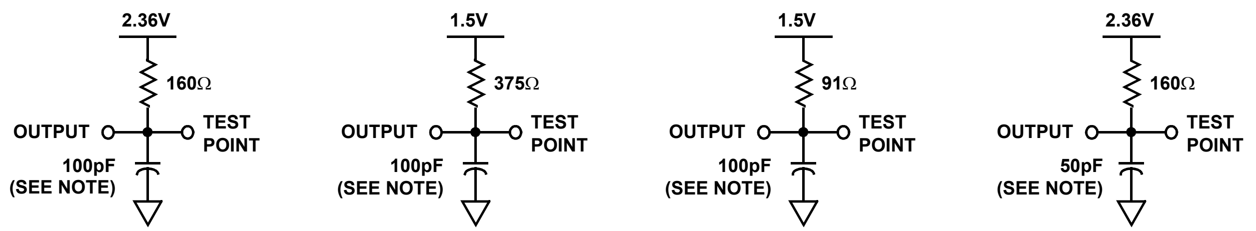


NOTE: All timing measurements are made at 1.5V unless otherwise noted.

Test Load Circuits

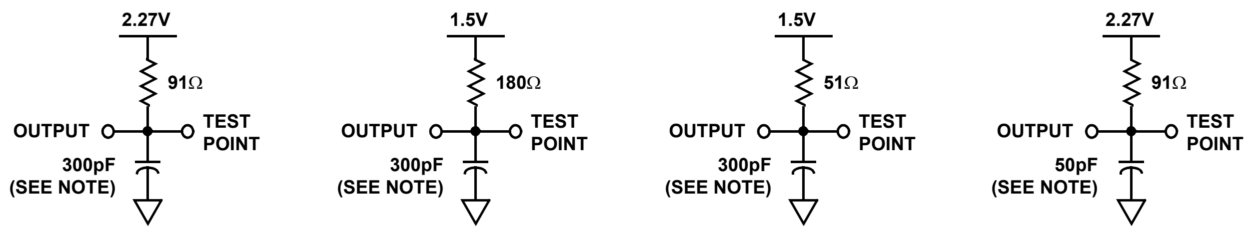
A SIDE OUTPUTS

TIVOV LOAD CIRCUIT | **TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT** | **TELOV OUTPUT LOW ENABLE LOAD CIRCUIT** | **TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT**



B SIDE OUTPUTS

TIVOV LOAD CIRCUIT | **TELOV OUTPUT HIGH ENABLE LOAD CIRCUIT** | **TELOV OUTPUT LOW ENABLE LOAD CIRCUIT** | **TEHOZ OUTPUT LOW/HIGH DISABLE LOAD CIRCUIT**



NOTE: Includes jig and stray capacitance.

Die Characteristics

DIE DIMENSIONS:
138.6 x 155.5 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

Metallization Mask Layout

82C86H