



64K x 8 Static RAM

Features

- High speed
— $t_{AA} = 15 \text{ ns}$
- CMOS for optimum speed/power
- Low active power
— 770 mW
- Low standby power
— 28 mW
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} options

Functional Description

The CY7C1512 is a high-performance CMOS static RAM organized as 65,536 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}_1), an active HIGH chip enable (CE_2), an active LOW output enable (\overline{OE}),

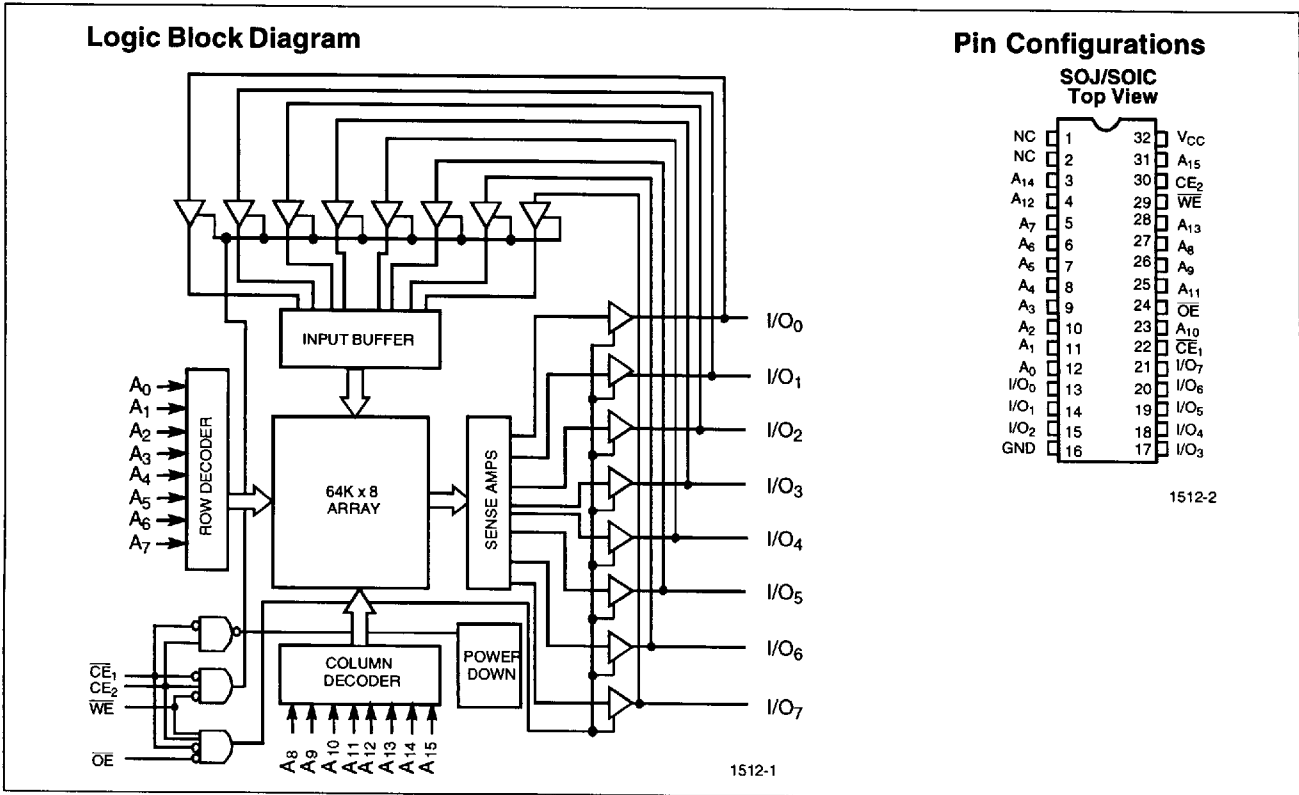
and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking chip enable one (\overline{CE}_1) and write enable (\overline{WE}) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking chip enable one (\overline{CE}_1) and output enable (\overline{OE}) LOW while forcing write enable (\overline{WE}) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

The CY7C1512 is available in standard 450-mil-wide plastic SOIC and 400-mil plastic SOJ packages.



Selection Guide

		7C1512-15	7C1512-20	7C1512-25	7C1512-35	7C1512-70
Maximum Access Time (ns)		15	20	25	35	70
Maximum Operating Current (mA)	Commercial	140	130	120	110	110
Maximum CMOS Standby Current (mA)	Commercial	5	5	5	5	5



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} +0.5V

DC Input Voltage^[1] -0.5V to V_{CC} +0.5V
 Current into Outputs (LOW) 20 mA
 Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C1512-15		7C1512-20		7C1512-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.3	2.2	V _{CC} +0.3	2.2	V _{CC} +0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/τ _{RC}		140		130		120	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		40		30		30	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f=0		5		5		5	mA

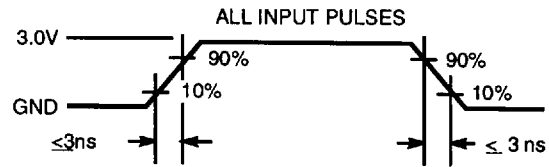
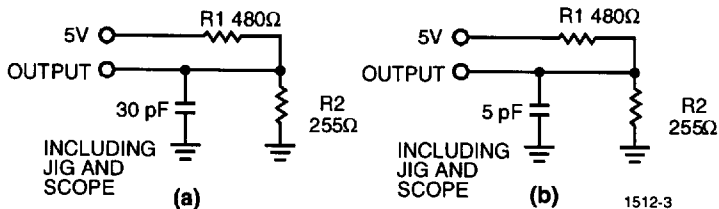
Parameter	Description	Test Conditions	7C1512-35		7C1512-70		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.3	2.2	V _{CC} +0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/τ _{RC}		110		110	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		25		25	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f=0		5		5	mA

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	9	pF
C_{OUT}	Output Capacitance		9	pF

AC Test Loads and Waveforms


Equivalent to: THVENIN EQUIVALENT
 OUTPUT $\text{---} 167\Omega \text{---} 1.73\text{V}$

1512-4

Switching Characteristics^[3, 6] Over the Operating Range

Parameter	Description	7C1512-15		7C1512-20		7C1512-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address to Data Valid		15		20		25	ns
t_{OHA}	Data Hold from Address Change	3		3		5		ns
t_{ACE}	\overline{CE}_1 LOW to Data Valid, CE_2 HIGH to Data Valid		15		20		25	ns
t_{DOE}	\overline{OE} LOW to Data Valid		7		8		10	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]		7		8		10	ns
t_{LZCE}	\overline{CE}_1 LOW to Low Z, CE_2 HIGH to Low Z ^[8]	3		3		5		ns
t_{HZCE}	\overline{CE}_1 HIGH to High Z, CE_2 LOW to High Z ^[7, 8]		7		8		10	ns
t_{PU}	\overline{CE}_1 LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		0		ns
t_{PD}	\overline{CE}_1 HIGH to Power-Down, CE_2 LOW to Power-Down		15		20		25	ns
WRITE CYCLE^[9]								
t_{WC}	Write Cycle Time	15		20		25		ns
t_{SCE}	CE_1 LOW to Write End, CE_2 HIGH to Write End	12		15		20		ns
t_{AW}	Address Set-Up to Write End	12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	12		15		20		ns
t_{SD}	Data Set-Up to Write End	8		10		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[8]	3		3		5		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		7		8		10	ns

5. Tested initially and after any design or process changes that may affect these parameters.

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured $\pm 500\text{ mV}$ from steady-state voltage.

8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{LZOE} is less than t_{LZCE} , and t_{LZWE} is less than t_{LZCE} for any given device.

9. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

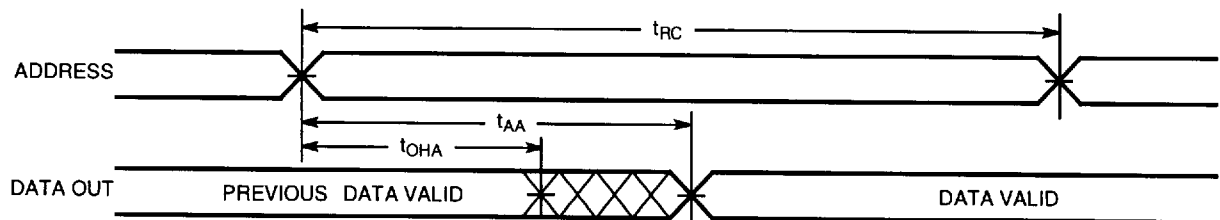


Switching Characteristics^[3, 6] Over the Operating Range (continued)

Parameter	Description	7C1512-35		7C1512-70		Unit
		Min.	Min.	Min.	Min.	
READ CYCLE						
t_{RC}	Read Cycle Time	35		70		ns
t_{AA}	Address to Data Valid		35		70	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	\overline{CE}_1 LOW to Data Valid, CE_2 HIGH to Data Valid		35		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		15		15	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]		15		15	ns
t_{LZCE}	\overline{CE}_1 LOW to Low Z, CE_2 HIGH to Low Z ^[8]	5		5		ns
t_{HZCE}	\overline{CE}_1 HIGH to High Z, CE_2 LOW to High Z ^[7, 8]		15		15	ns
t_{PU}	\overline{CE}_1 LOW to Power-Up, CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	\overline{CE}_1 HIGH to Power-Down, CE_2 LOW to Power-Down		35		70	ns
WRITE CYCLE^[9]						
t_{WC}	Write Cycle Time	35		70		ns
t_{SCE}	\overline{CE}_1 LOW to Write End, CE_2 HIGH to Write End	25		60		ns
t_{AW}	Address Set-Up to Write End	25		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	25		60		ns
t_{SD}	Data Set-Up to Write End	20		55		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[8]	5		5		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7, 8]		15		15	ns

Switching Waveforms

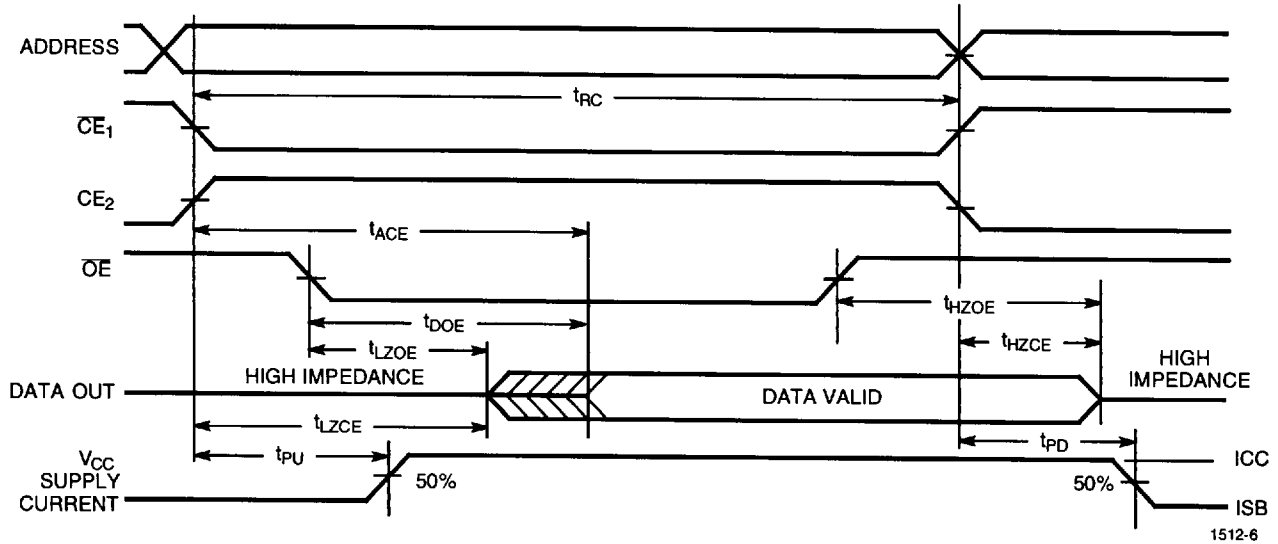
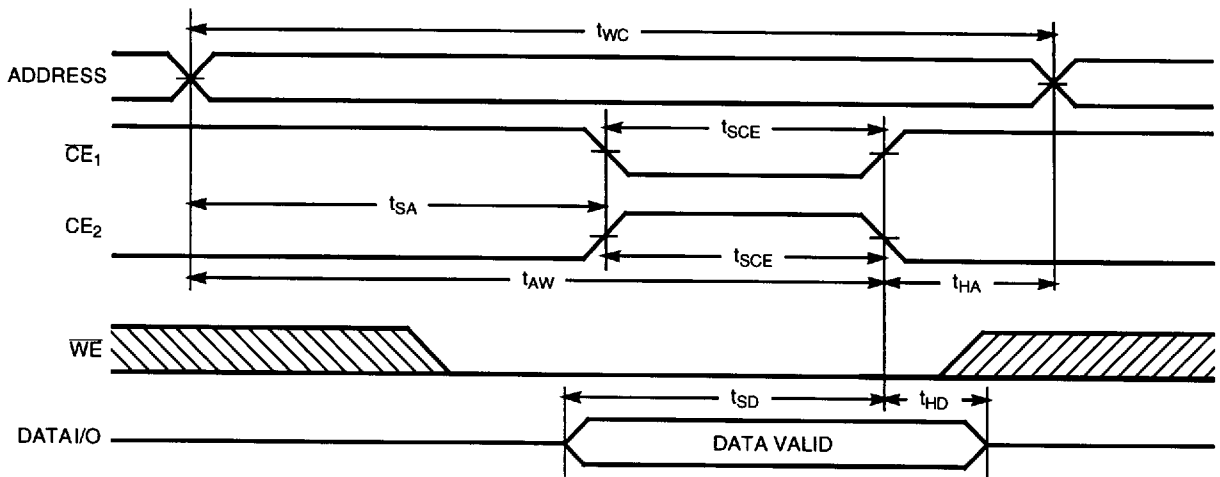
Read Cycle No. 1^[10, 11]



1512-5

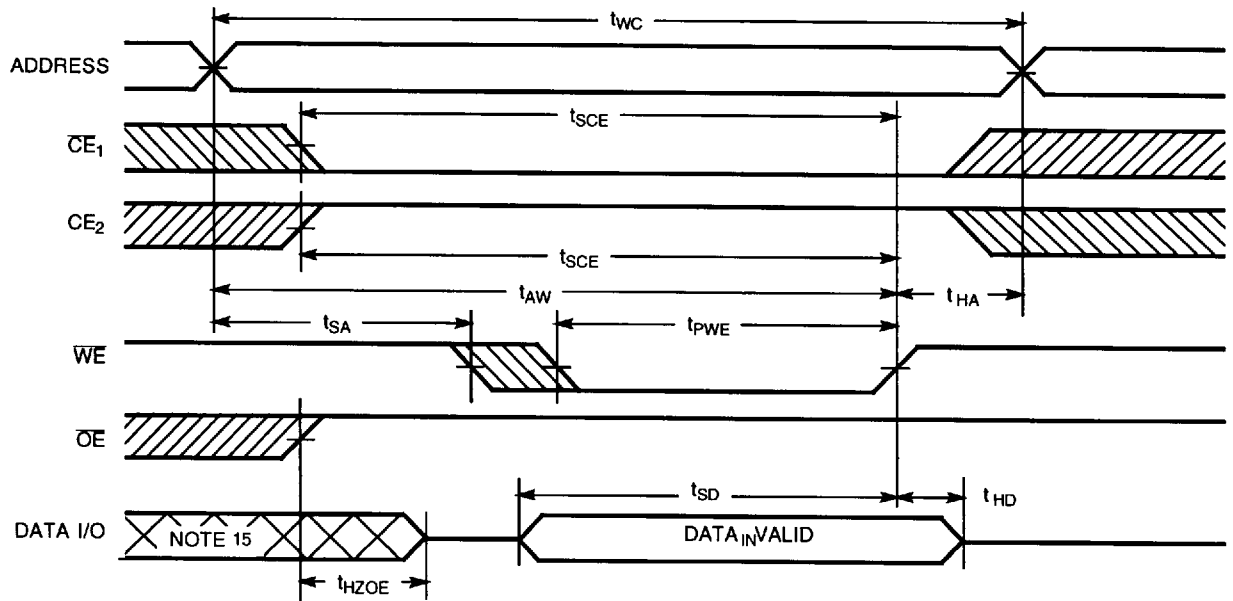
Notes:

- 10. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- 11. \overline{WE} is HIGH for read cycle.

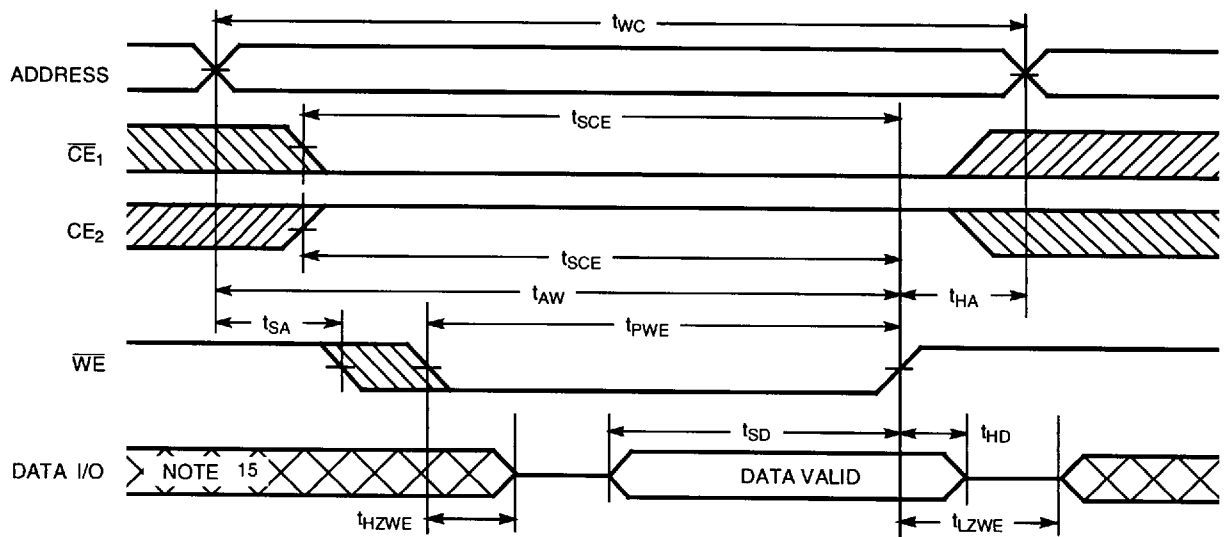
Switching Waveforms (continued)
Read Cycle No. 2 (\overline{OE} Controlled) [11, 12]

Write Cycle No. 1 (\overline{CE}_1 or \overline{CE}_2 Controlled) [13, 14]

Notes:

12. Address valid prior to or coincident with \overline{CE}_1 transition LOW and \overline{CE}_2 transition HIGH.
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If \overline{CE}_1 goes HIGH or \overline{CE}_2 goes LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

1512-7

Switching Waveforms (continued)
Read Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[13, 14]


1512-8

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[14]


1512-9

Note:

15. During this period the I/Os are in the output state and input signals should not be applied.



Truth Table

CE ₁	CE ₂	OE	WE	I/O ₀ - I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I _{SB})
X	L	X	X	High Z	Power-Down	Standby (I _{SB})
L	H	L	H	Data Out	Read	Active (I _{CC})
L	H	X	L	Data In	Write	Active (I _{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

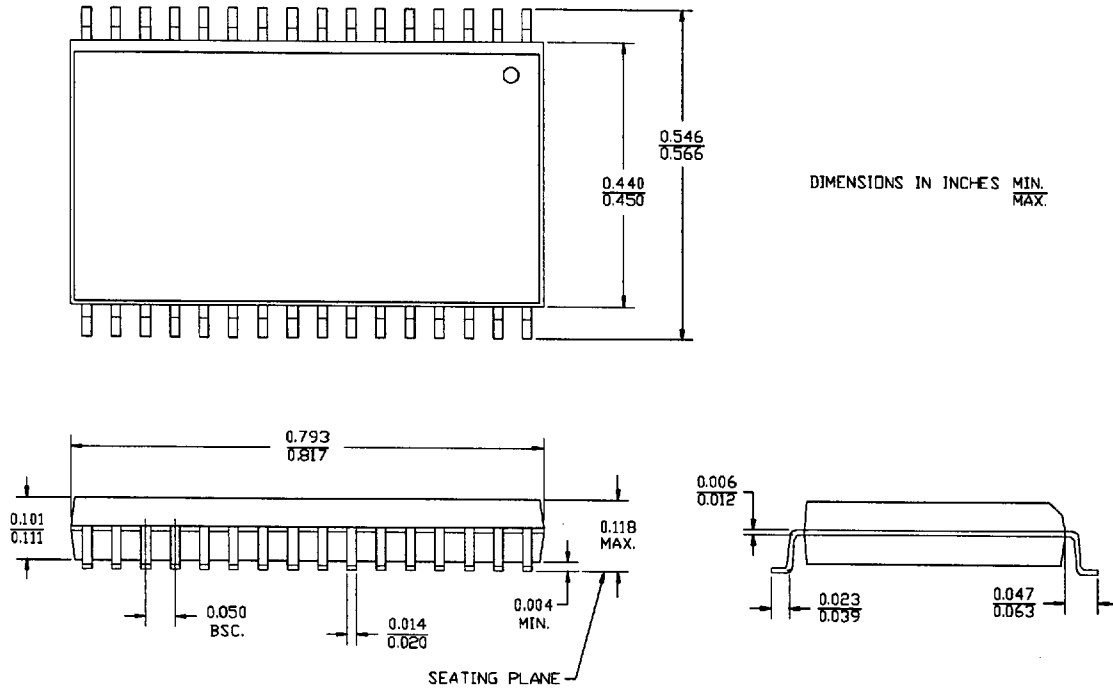
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1512-15SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY7C1512-15VC	V33	32-Lead (400-Mil) Molded SOJ	
20	CY7C1512-20SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY7C1512-20VC	V33	32-Lead (400-Mil) Molded SOJ	
25	CY7C1512-25SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY7C1512-25VC	V33	32-Lead (400-Mil) Molded SOJ	
35	CY7C1512-35SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY7C1512-35VC	V33	32-Lead (400-Mil) Molded SOJ	
70	CY7C1512-70SC	S34	32-Lead (450-Mil) Molded SOIC	Commercial
	CY7C1512-70VC	V33	32-Lead (400-Mil) Molded SOJ	

Shaded areas contain advanced information.

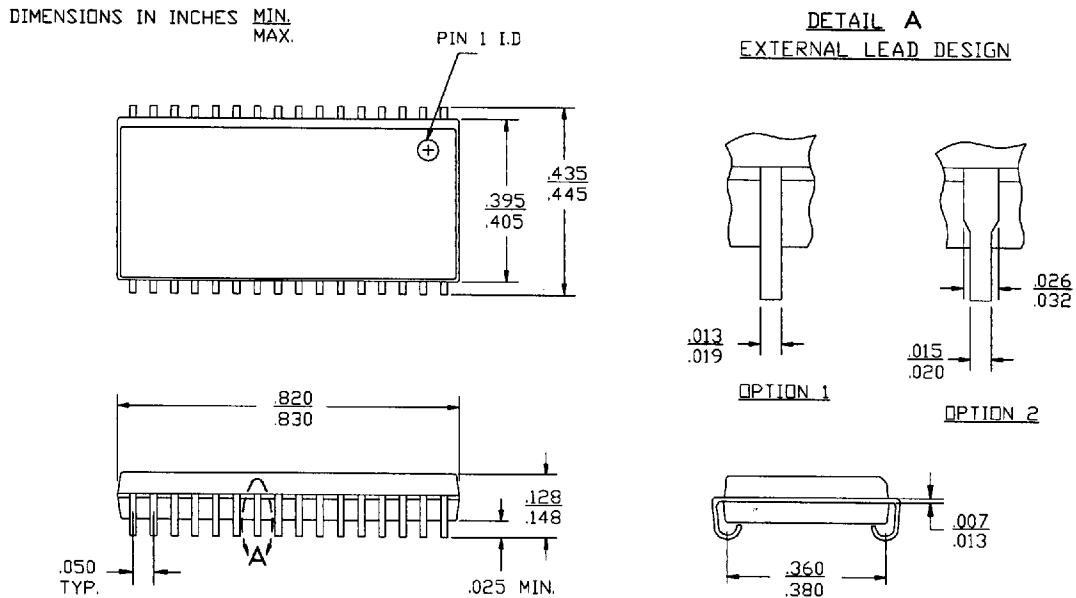
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Package Diagrams

32-Lead (450-Mil) Molded SOIC S34



32-Lead (400-Mil) Molded SOJ V33



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