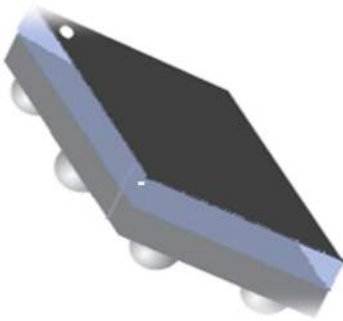
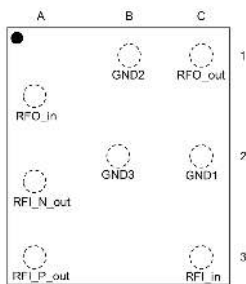


50 Ω nominal input / conjugate matched balun to BGA-4L STM32WL in low power mode, 862-928 MHz with integrated harmonic filter



Chip scale package on glass
8 bumps - 1.83 x 2.13 mm²



Features

- BGA STM32WL sub-GHz wireless microcontrollers impedance matched balun and Tx harmonics filter
- Optimized for BGA STM32WL sub-GHz wireless microcontrollers in low power mode and dedicated to 4-layers PCB
- 50 Ω nominal input / conjugate matched balun to BGA STM32WL
- 50 Ω nominal impedance on antenna side Tx and Rx
- Deep Tx rejection harmonic filter
- Low insertion loss
- Small footprint
- Low profile ≤ 630 μm after reflow
- High RF performance
- RF BOM and area reduction
- **ECOPACK2** compliant component

Applications

- STM32WL sub-GHz wireless microcontrollers
- LPWAN-compliant radio solution, enabling the following modulations: LoRa®, (G)FSK, (G)MSK, and BPSK

Description

STMicroelectronics **BALFHB-WL-04D3** is an ultra-miniature balun. This device integrates a matching network, balun, and harmonics filter. Matching impedance has been customized for the STM32WL sub-GHz wireless microcontrollers.

It is using STMicroelectronics IPD technology on a nonconductive glass substrate, which optimizes RF performances.

Product status

BALFHB-WL-04D3

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
P_{IN}	Input power RF_{IN}	27	dBm
V_{ESD}	ESD ratings human body model (JESD22-A114), all I/O one at a time while others connected to GND	2000	V
	ESD ratings machine model, all I/O	200	
T_{OP}	Operating temperature	-40 to +105	°C

Table 2. Impedances ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z_{RX}	Nominal differential Rx balun impedance	-	Matched to STM32WL	-	Ω
Z_{TX}	Nominal Tx filter impedance	-	Matched to STM32WL	-	
Z_{RX-ANT}	Nominal Rx balun antenna impedance	-	50	-	
Z_{TX-ANT}	Nominal Tx filter antenna impedance	-	50	-	

Table 3. Electrical characteristics and RF performances ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
f	Frequency range		862	868	928	MHz
IL_{RX}	Rx balun insertion loss differential mode $ S_{DS} $ without mismatch loss	Typical value given at 868 MHz		1.30	1.50	dB
IL_{TX}	LP Tx filter insertion loss $ S_{21} $ without mismatch loss	Typical value given at 868 MHz		0.75	1.00	dB
RL_{RX-ANT}	Rx balun input return loss differential mode $ S_{DD} $ on antenna	Typical value given at 868 MHz	15	18		dB
RL_{TX-ANT}	Tx filter output return loss $ S_{11} $ on antenna	Typical value given at 868 MHz	14	20		dB
ϕ_{imb}	RX balun phase imbalance		-1.8		1.8	°
A_{imb}	RX balun amplitude imbalance		-1.0		1.0	dB
Att_{TX}	Tx filter harmonic rejection levels $ S_{21} $	Attenuation at 2fo	31	34		dB
		Attenuation at 3fo	49	63		
		Attenuation at 4fo	43	56		
		Attenuation at 5fo	31	51		
		Attenuation at 6fo	32	54		
		Attenuation at 7fo	20	43		
		Attenuation at 8fo	27	37		
		Attenuation at 9fo	17	32		
		Attenuation at 10fo	20	27		

1.1 RF measurements (Rx balun)

Figure 1. Insertion loss (dB)

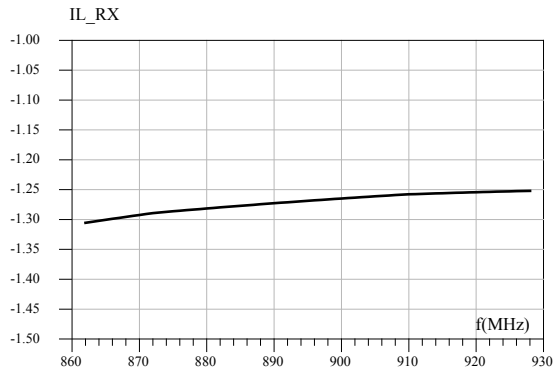


Figure 2. Return loss on antenna (dB)

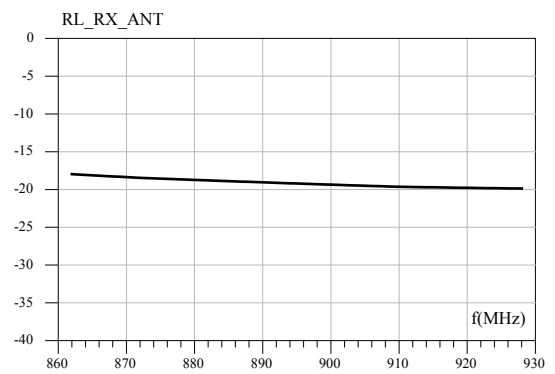


Figure 3. Amplitude imbalance (dB)

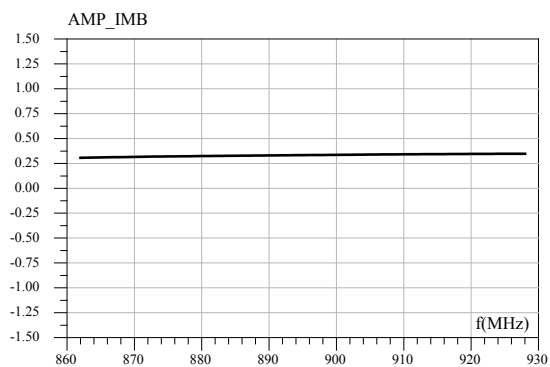
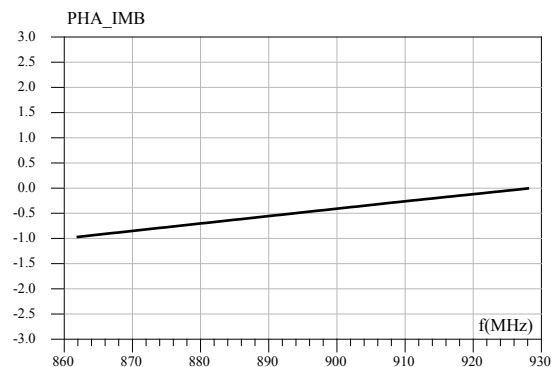


Figure 4. Phase imbalance (°)



1.2 RF measurements (Tx filter)

Figure 5. Transmission wide band with harmonics attenuation (dB)

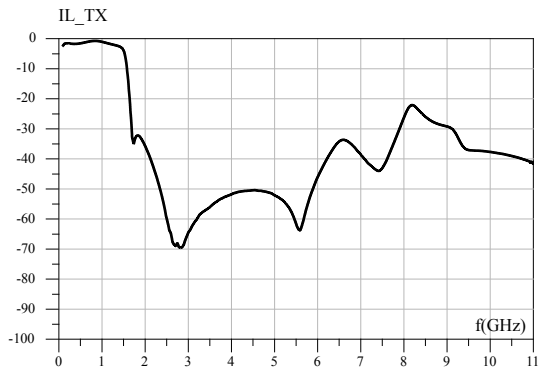


Figure 6. Insertion loss (dB)

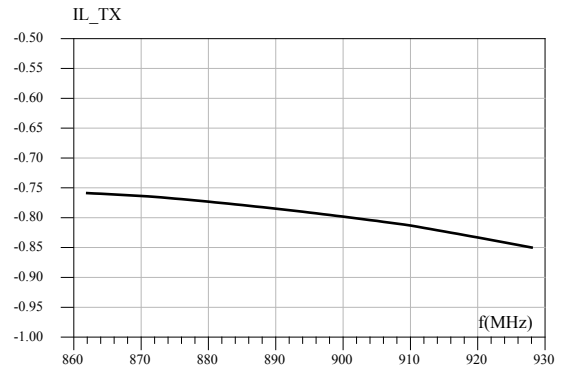
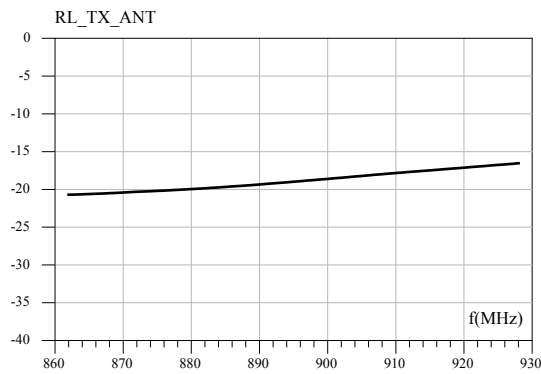


Figure 7. Return loss on antenna (dB)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 CSPG 8 bumps package information

Figure 8. CSPG 8 bumps package outline (bottom view - bumps up) (in μm)

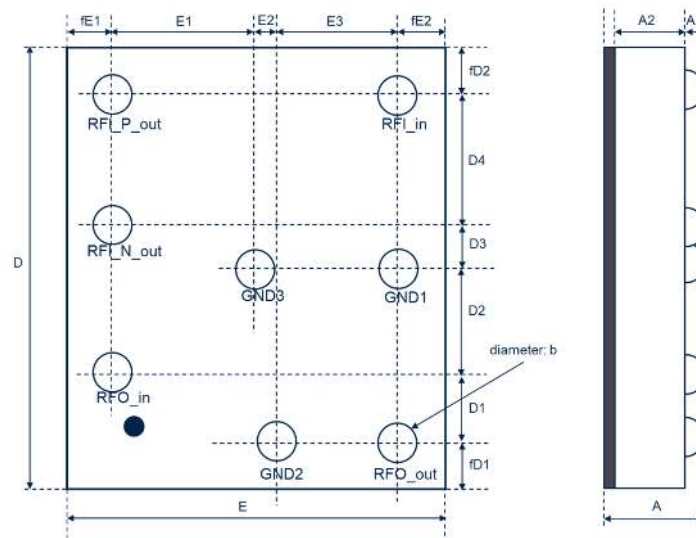


Table 4. CSPG 8 bumps dimensions (in μm)

Parameter	Min.	Typ.	Max.
A	580	630	680
A1	180	205	230
A2	380	400	420
b	230	255	280
D	2080	2130	2150
D1		340	
D2		500	
D3		210	
D4		630	
E	1780	1830	1880
E1		690	
E2		85	
E3		605	
fd1		225	
fd2		225	
fE1		225	
fE2		225	

2.2 CSPG 8 bumps packing information

Figure 9. Marking

Dot, ST logo
 ■ ECOPACK® Grade
 xx = marking
 z = manufacturing location
 yww = datecode
 (y = year
 ww = week)

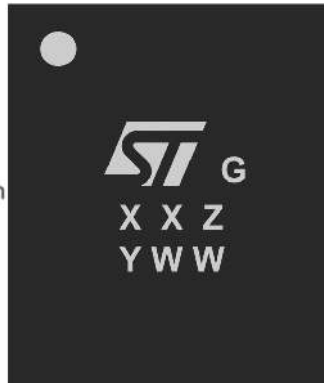


Figure 10. Top view

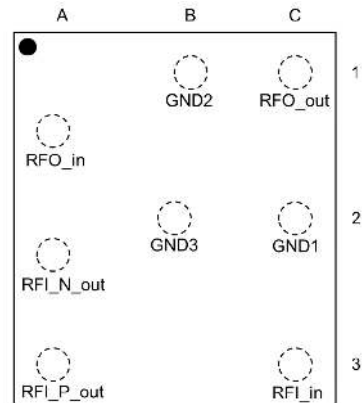
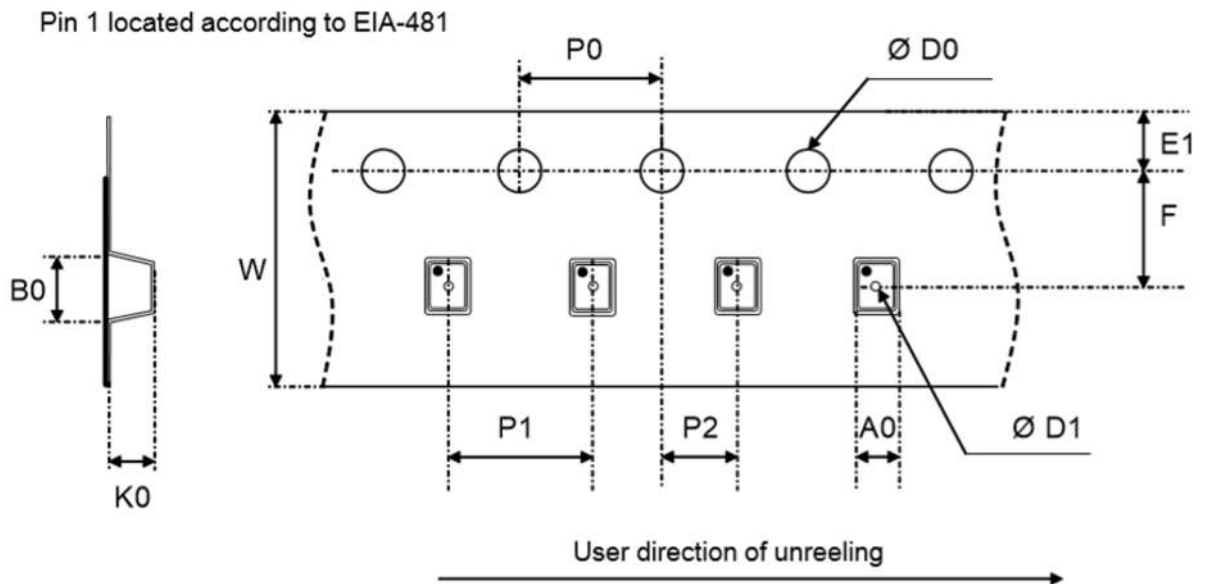


Table 5. Pads description top view (pads down)

Pad ref.	Pad name	Description
A1	RFO_in	Tx filter input
A2	RFI_N_out	Differential-N Rx balun output
A3	RFI_P_out	Differential-P Rx balun output
B1	GND2	Ground #2
B2	GND3	Ground #3
C1	RFO_out	Tx filter output
C2	GND1	Ground #1
C3	RFI_in	Single ended Rx balun input

Figure 11. Tape and reel outline



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 6. Tape and reel mechanical data

Ref	Dimensions		
	Millimeters		
	Min	Typ	Max
A0	1.89	1.94	1.99
B0	2.19	2.24	2.29
Ø D0	1.40	1.50	1.60
Ø D1	0.95	1.00	1.05
E1	1.65	1.75	1.85
F	3.45	3.50	3.55
K0	0.70	0.75	0.80
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

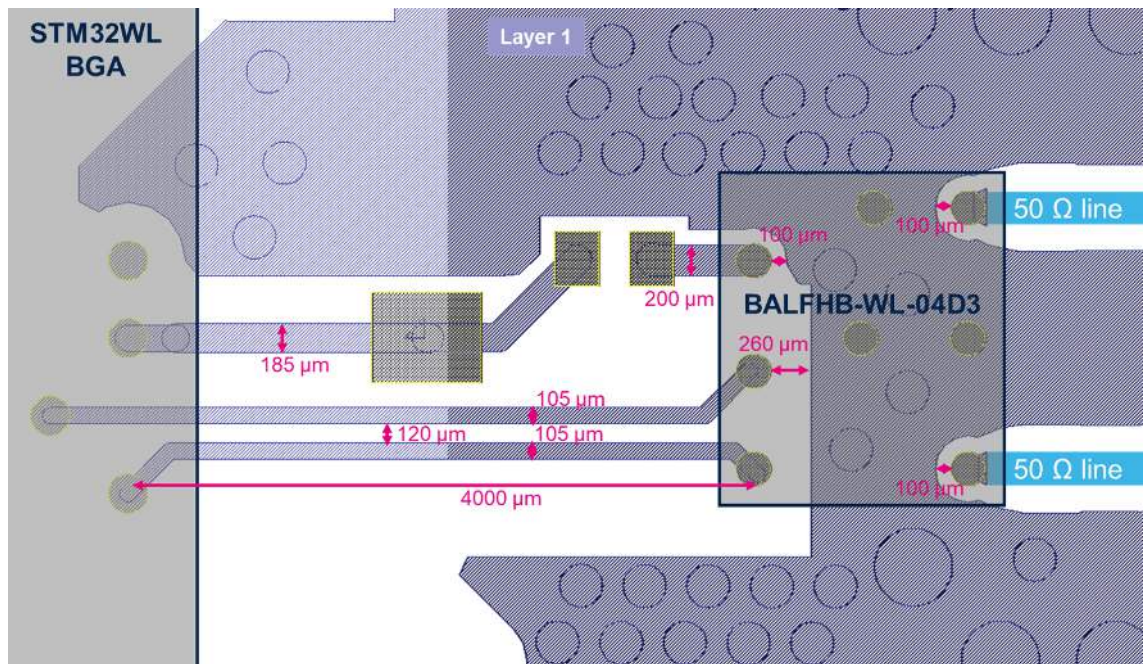
Note: More packing information is available in the application note:

- [AN2348 Flip-Chip: "Package description and recommendations for use"](#)

3 PCB assembly recommendations

3.1 Land pattern

Figure 12. BGA-4L PCB recommended land pattern



Layout example using STM32WL in BGA package / 4 layers PCB for low power mode.

Figure 13. BGA-4L PCB stack-up recommendations

Layer Stack Manager

Save Load Presets 3D Layer Pairs

Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.002	Solder Resist	3.7		
Top Layer	Signal	Copper	0.035				Top
Dielectric 1	Dielectric	Prepreg	0.108	1 x 2116	3.8		
MidLayer 1	Signal	Copper	0.035				Not Allowed
Dielectric 2	Dielectric	Core	0.71	FR4	5		
MidLayer 2	Signal	Copper	0.035				Not Allowed
Dielectric 3	Dielectric	Prepreg	0.108	1 x 2116	3.8		
Bottom Layer	Signal	Copper	0.035				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.002	Solder Resist	3.7		
Bottom Overlay	Overlay						

Total Thickness: 1.07001mm

Add Layer Delete Layer Move Up Move Down Drill Pairs... Impedance Calculation...

Advanced >> OK Cancel

3.2 Stencil opening design

Figure 14. Footprint - 3 mils stencil -non solder mask defined

Copper pad diameter:
220 μm recommended
180 μm minimum
260 μm maximum

Solder mask opening:
320 μm recommended
300 μm minimum
340 μm maximum

Solder stencil opening:
220 μm recommended

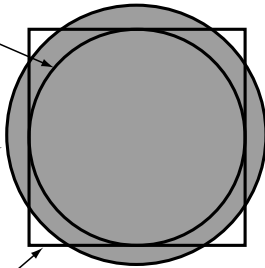
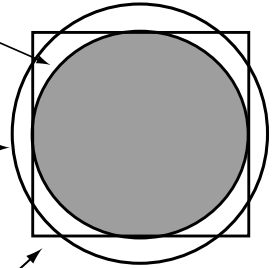


Figure 15. Footprint - 3 mils stencil - solder mask defined

Solder mask opening:
220 μm recommended
180 μm minimum
260 μm maximum

Copper pad diameter:
320 μm recommended
300 μm minimum

Solder stencil opening:
220 μm recommended



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 μm .

3.4 Placement

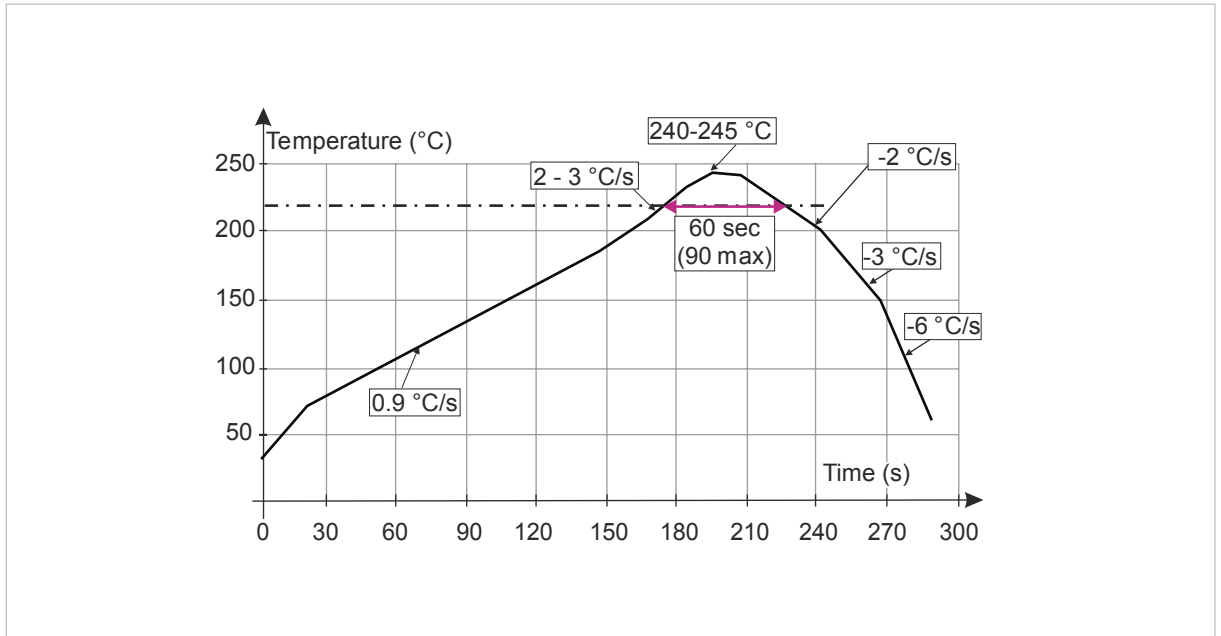
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 16. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: More information is available in the application note:

- AN2348 Flip-Chip: "Package description and recommendations for use"

4 Ordering information

Table 7. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
BALFHB-WL-04D3	W4	CSPG	3.9 mg	5000	Tape and reel

Revision history

Table 8. Document revision history

Date	Revision	Changes
14-Oct-2022	1	Initial release.
21-Dec-2022	2	Updated Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ °C}$).

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved