

PSMN3R0-60ES

N-channel 60 V 3.0 mΩ standard level MOSFET in I2PAK.

3 June 2014 Product data sheet

1. General description

Standard level N-channel MOSFET in a I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; <u>Fig. 2</u>	[1]	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	306	W
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 11; Fig. 12		-	2.4	3	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 80 A; V_{DS} = 12 V; Fig. 13; Fig. 14		-	28	-	nC

[1] Continuous current is limited by package.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D I
2	D	drain		
3	S	source		G
mb	D	mounting base; connected to drain	1 2 3	mbb076 S
			I2PAK (SOT226)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN3R0-60ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226		

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R0-60ES	PSMN3R0-60ES

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	60	V
V_{DGR}	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	306	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>		-	83.4	Α
		V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	[1]	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; Fig. 3		-	824	Α
T _{stg}	storage temperature			-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
Source-drain diode						
Is	source current	T _{mb} = 25 °C	[1]	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	824	Α
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 60 V; R_{GS} = 50 Ω; unclamped		-	800	mJ

[1] Continuous current is limited by package.

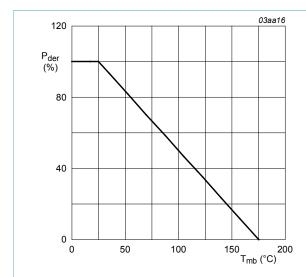


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{\textit{der}} = \frac{P_{\textit{tot}}}{P_{\textit{tot}(25^{\circ}\textit{C})}} \times \textbf{100 \%}$$

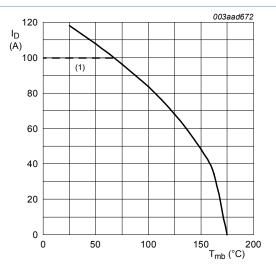


Fig. 2. Continuous drain current as a function of mounting base temperature.

 $V_{\textit{GS}}\!\geq$ 10 V; (1) Capped at 100 A due to package

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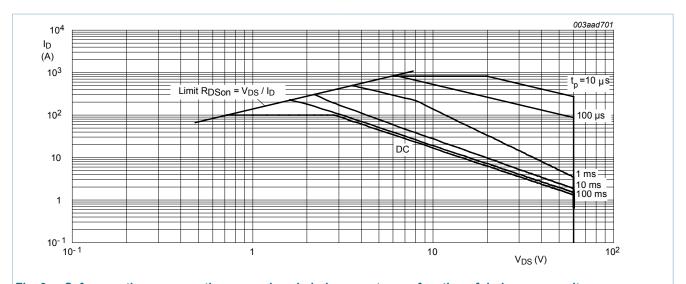


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 T_{mb} = 25 °C; I_{DM} is a single pulse; Capped at 100 A due to package

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 4	-	0.3	0.49	K/W

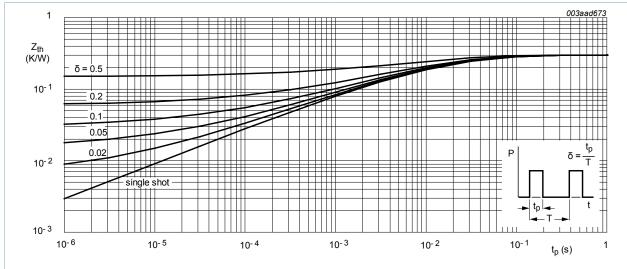


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	54	-	-	V
	breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 8; Fig. 9	2	3	4	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; Fig. 9	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; Fig. 9	-	-	4.6	V
I _{DSS} drain	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μΑ
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ
I _{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon} drain-source on-state resistance	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 10	-	-	7.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11; Fig. 12	-	2.4	3	mΩ
R _G	gate resistance	f = 1 MHz	0.55	1.1	2.2	Ω
Dynamic ch	naracteristics					
Q _{G(tot)}	total gate charge	I _D = 80 A; V _{DS} = 12 V; V _{GS} = 10 V; Fig. 13; Fig. 14	-	130	-	nC
Q_{GS}	gate-source charge	I _D = 80 A; V _{DS} = 12 V; V _{GS} = 10 V; Fig. 14; Fig. 13	-	43	-	nC
Q_{GD}	gate-drain charge	I _D = 80 A; V _{DS} = 12 V; V _{GS} = 10 V; Fig. 13; Fig. 14	-	28	-	nC
C _{iss}	input capacitance	V _{DS} = 30 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; <u>Fig. 15</u> ; <u>Fig. 16</u>	-	8079	-	pF
C _{oss}	output capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; Fig. 15$	-	971	-	pF
C _{rss}	reverse transfer capacitance	V _{DS} = 30 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; <u>Fig. 15</u> ; <u>Fig. 16</u>	-	492	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 10 \text{ V};$	-	31	-	ns
t _r	rise time	$R_{G(ext)} = 1.5 \Omega$	-	26	-	ns
t _{d(off)}	turn-off delay time		-	77	-	ns
t _f	fall time		-	22	_	ns

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}; Fig. 17$		-	0.88	1.2	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	54	-	ns
Q _r	recovered charge	V _{DS} = 30 V		-	97	-	nC

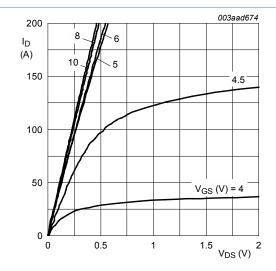


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

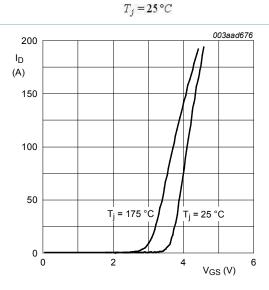


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DSon}$$

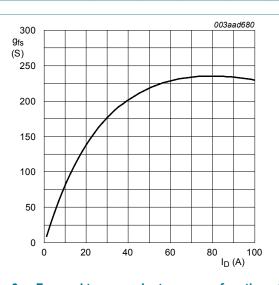


Fig. 6. Forward transconductance as a function of drain current; typical values

$$T_j = 25$$
 °C; $V_{DS} = 30$ V

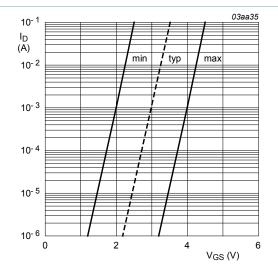


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25 \,{}^{\circ}C; V_{DS} = 5V$$

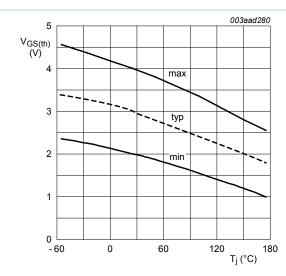


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$

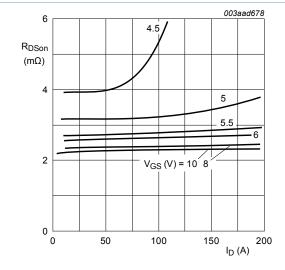


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25 \,^{\circ}C$$

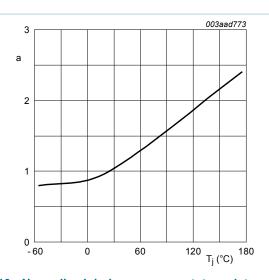


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\mathbf{a} = \frac{R_{DSon}}{R_{DSon(25\,^{\circ}\text{C})}}$$

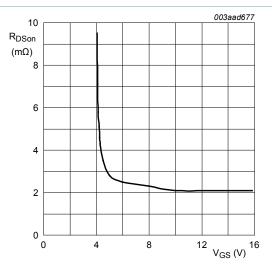


Fig. 12. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25$$
 °C; $I_D = 25$ A

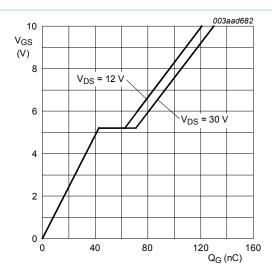


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
 °C; $I_D = 25$ A

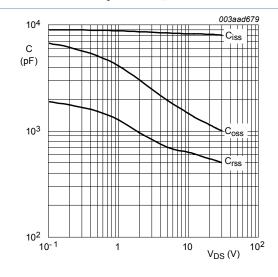


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0 \text{ V; } f = 1 \text{ MHz}$$

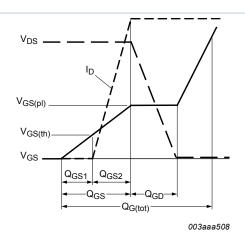


Fig. 14. Gate charge waveform definitions

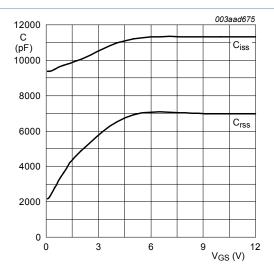


Fig. 16. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$$V_{DS} = 0 \text{ V}; \mathbf{f} = 1 \text{ MHz}$$

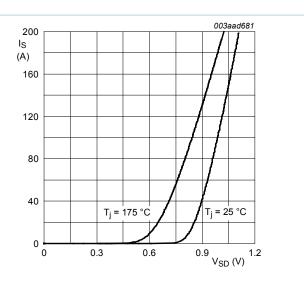


Fig. 17. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0 \text{ V}$$

11. Package outline

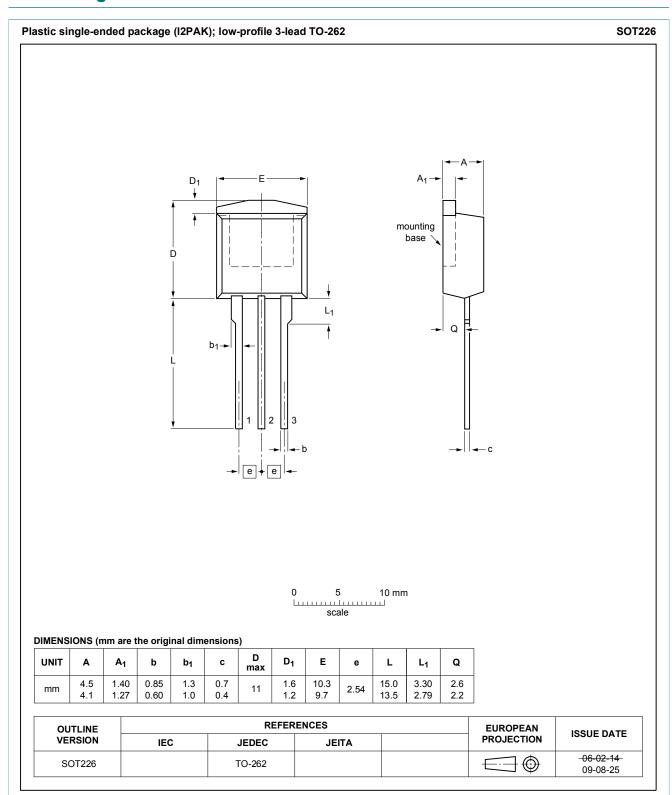


Fig. 18. Package outline I2PAK (SOT226)

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Date of release: 03 June 2014

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