Dual Low Noise Amplifier

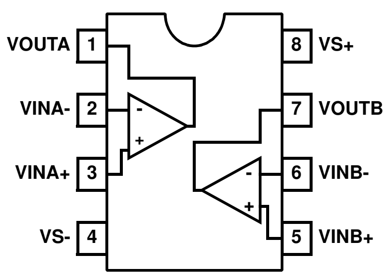
The EL2228 is a dual, low-noise amplifier, ideally suited to filtering applications in ADSL and HDSLII designs. It features low noise specification of just 4.9nV/√Hz and 1.2pA/√Hz, making it ideal for processing low voltage waveforms.

The EL2228 has a -3dB bandwidth of 80MHz and is gain-of-1 stable. It also affords minimal power dissipation with a supply current of just 4.5mA per amplifier. The amplifier can be powered from supplies ranging from ±2.5V to ±12V.

The EL2228 is available in a space saving 8 Ld MSOP package as well as the industry-standard 8 Ld SOIC. It is specified for operation over the -40°C to +85°C temperature range.

Pinout

EL2228
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



Features

- Voltage noise of only 4.9nV/√Hz
- Current noise of only 1.2pA/√Hz
- Bandwidth (-3dB) of 80MHz -@ A_V = +1
- Gain-of-1 stable
- Just 4.5mA per amplifier
- 8 Ld MSOP package
- ±2.5V to ±12V operation
- Pb-free plus anneal available (RoHS compliant)

Applications

- ADSL filters
- HDSLII filters
- Ultrasound input amplifiers
- Wideband instrumentation
- Communications equipment
- Wideband sensors

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	TAPE & REEL	PACKAGE	PKG. DWG. #
EL2228CY	N	-40 to +85	-	8 Ld MSOP (3.0mm)	MDP0043
EL2228CY-T13	N	-40 to +85	13”	8 Ld MSOP (3.0mm)	MDP0043
EL2228CY-T7	N	-40 to +85	7”	8 Ld MSOP (3.0mm)	MDP0043
EL2228CYZ (Note)	BAAAV	-40 to +85	-	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL2228CYZ-T13 (Note)	BAAAV	-40 to +85	13”	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL2228CYZ-T7 (Note)	BAAAV	-40 to +85	7”	8 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL2228CS	2228CS	-40 to +85	-	8 Ld SOIC (150 mil)	MDP0027
EL2228CS-T13	2228CS	-40 to +85	13”	8 Ld SOIC (150 mil)	MDP0027
EL2228CS-T7	2228CS	-40 to +85	7”	8 Ld SOIC (150 mil)	MDP0027
EL2228CSZ (Note)	2228CSZ	-40 to +85	-	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL2228CSZ-T13 (Note)	2228CSZ	-40 to +85	13”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL2228CSZ-T7 (Note)	2228CSZ	-40 to +85	7”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . .+28V
Input Voltage . . . . V_S - 0.3V, V_S +0.3V
Maximum Continuous Output Current 40mA
ESD Voltage. 2kV

Thermal Information

Maximum Die Temperature . . . .+150°C
Storage Temperature . . . .-65°C to +150°C
Power Dissipation . . . . See Curves
Operating Temperature . . . .-40°C to +85°C
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +12V, V_S- = -12V, R_L = 500Ω and C_L = 3pF to 0V, R_F = 420Ω and T_A = +25°C Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		0.2	3	mV
TCV_{OS}	Average Offset Voltage Drift	Measured over operating temperature range		-4		µV/°C
I_B	Input Bias Current	V_{CM} = 0V	-9	-4.5	-1	µA
R_{IN}	Input Impedance			8		MΩ
C_{IN}	Input Capacitance			1		pF
CMIR	Common-Mode Input Range		-11.8		+10.4	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -11.8V to +10.4V	60	90		dB
		for V_{IN} from -10V to +10V	60	75		dB
A_{VOL}	Open-Loop Gain	-5V ≤ V_{OUT} ≤ 5V	60	75		dB
e_N	Voltage Noise	f = 100kHz		4.9		nV/√Hz
i_N	Current Noise	f = 100kHz		1.2		pA/√Hz
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	R_L = 500Ω		-10.3	-10	V
		R_L = 250Ω		-9.5	-9	V
V_{OH}	Output Swing High	R_L = 500Ω	10	10.3		V
		R_L = 250Ω	9.5	10		V
I_{SC}	Short Circuit Current	R_L = 10Ω	140	180		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±10.8V to ±13.2V	65	83		dB
I_S	Supply Current (per Amplifier)	No load	4	5	6	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 1)	±2.5V square wave, measured 25% to 75%	44	65		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		50		ns
BW	-3dB Bandwidth			80		MHz
HD2	2nd Harmonic Distortion	f = 1MHz, V_O = 2V_{P-P}, R_L = 500Ω, A_V = 2		-86		dBc
		f = 1MHz, V_O = 2V_{P-P}, R_L = 150Ω, A_V = 2		-79		dBc
HD3	3rd Harmonic Distortion	f = 1MHz, V_O = 2V_{P-P}, R_L = 500Ω, A_V = 2		-93		dBc
		f = 1MHz, V_O = 2V_{P-P}, R_L = 150Ω, A_V = 2		-70		dBc

NOTE:

1. Slew rate is measured on rising and falling edges

Electrical Specifications

$V_S+ = +5V$, $V_S- = -5V$, $R_L = 500\Omega$ and $C_L = 3pF$ to 0V, $R_F = 420\Omega$ and $T_A = +25°C$ unless otherwise specified.

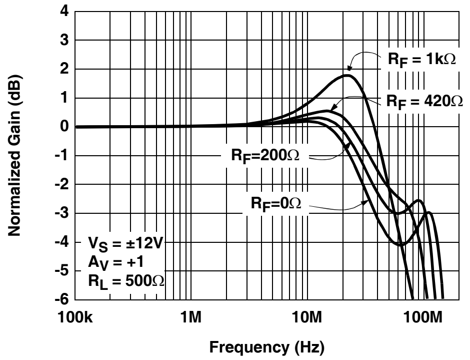
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$		0.6	3	mV
TCV_{OS}	Average Offset Voltage Drift	Measured over operating temperature range		4.9		µV/°C
I_B	Input Bias Current	$V_{CM} = 0V$	-9	-4.5	-1	µA
R_{IN}	Input Impedance			6		MΩ
C_{IN}	Input Capacitance			1.2		pF
CMIR	Common-Mode Input Range		-4.7		+3.4	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -4.7V to +3.4V	60	90		dB
		for V_{IN} from -2V to +2V				dB
A_{VOL}	Open-Loop Gain	$-2.5V \leq V_{OUT} \leq 2.5V$	60	72		dB
e_N	Voltage Noise	f = 100kHz		4.7		nV/√Hz
i_N	Current Noise	f = 100kHz		1.2		pA/√Hz
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$R_L = 500\Omega$		-3.8	-3.5	V
		$R_L = 250\Omega$		-3.7	-3.5	V
V_{OH}	Output Swing High	$R_L = 500\Omega$	3.5	3.7		V
		$R_L = 250\Omega$	3.5	3.6		V
I_{SC}	Short Circuit Current	$R_L = 10\Omega$	60	100		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4.5V to ±5.5V	65	83		dB
I_S	Supply Current (Per Amplifier)	No load	3.5	4.5	5.5	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 1)	±2.5V square wave, measured 25%-75%	35	50		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		50		ns
BW	-3dB Bandwidth			75		MHz
HD2	2nd Harmonic Distortion	f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 500\Omega$, $A_V = 2$		-90		dBc
		f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 150\Omega$, $A_V = 2$		-71		dBc
HD3	3rd Harmonic Distortion	f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 500\Omega$, $A_V = 2$		-99		dBc
		f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 150\Omega$, $A_V = 2$		-69		dBc

NOTE:

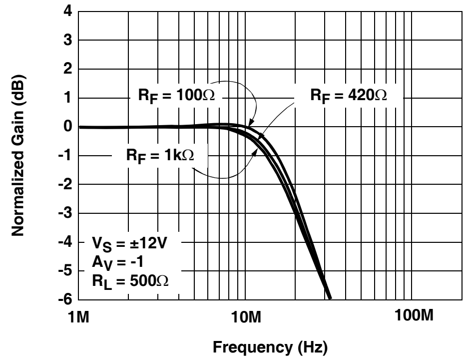
1. Slew rate is measured on rising and falling edges

Typical Performance Curves

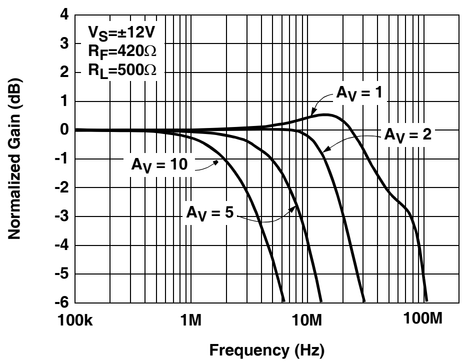
Non-Inverting Frequency Response for Various R_F



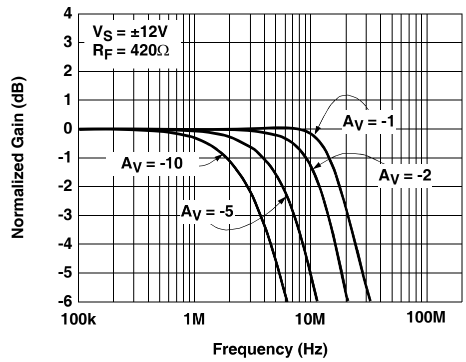
Inverting Frequency Response for Various R_F



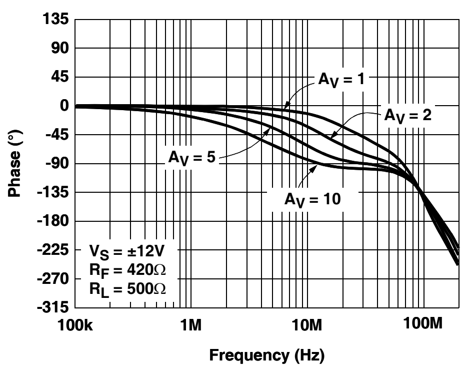
Non-Inverting Frequency Response (Gain)



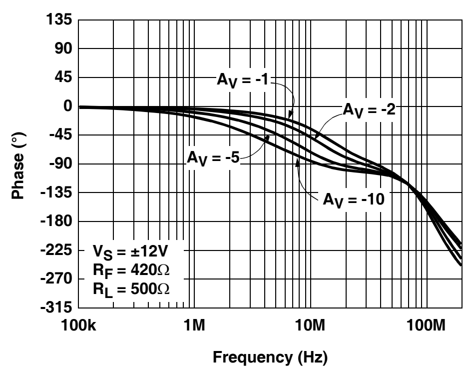
Inverting Frequency Response (Gain)



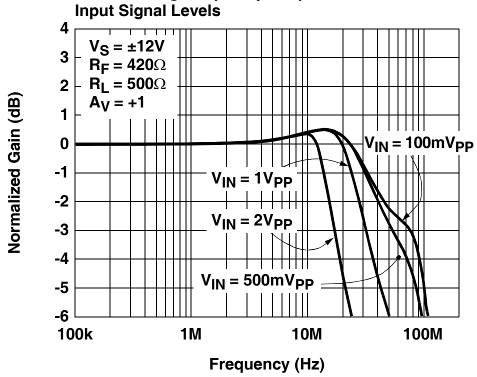
Non-Inverting Frequency Response (Phase)



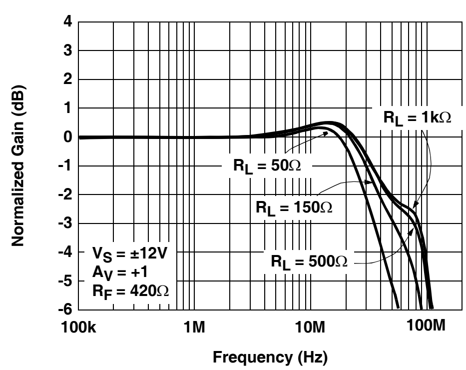
Inverting Frequency Response (Phase)



Non-Inverting Frequency Response for Various Input Signal Levels

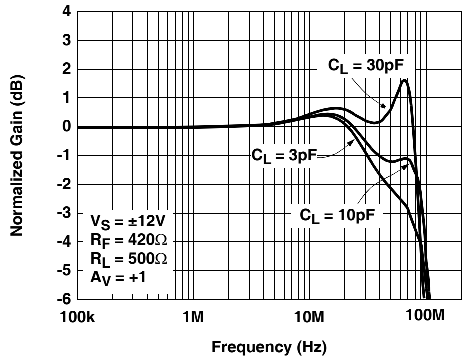


Non-Inverting Frequency Response for Various R_L

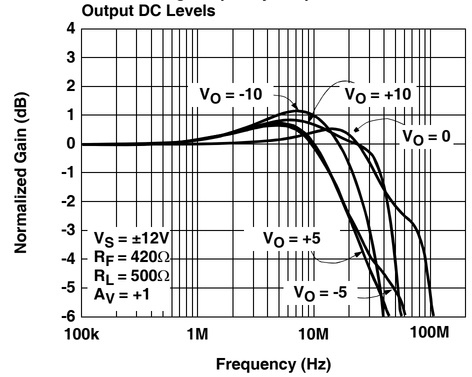


Typical Performance Curves (Continued)

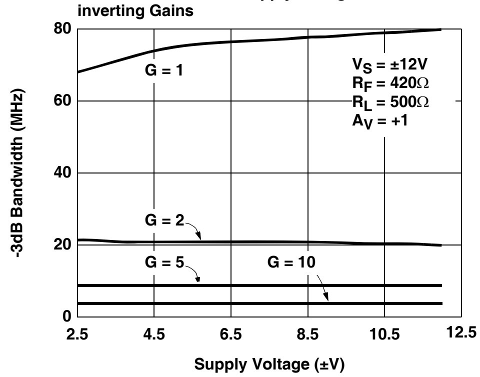
Non-Inverting Frequency Response for Various C_L



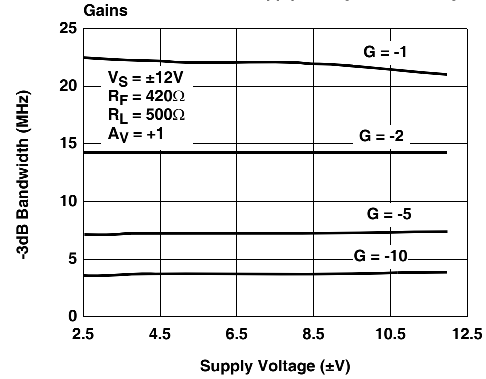
Non-Inverting Frequency Response for Various Output DC Levels



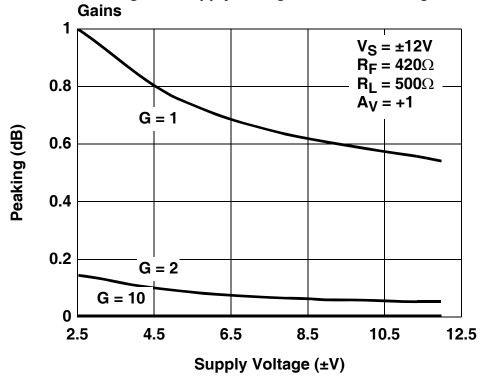
-3dB Bandwidth vs ± Supply Voltage for Non-inverting Gains



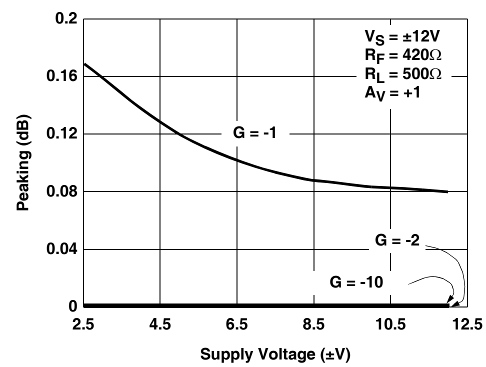
-3dB Bandwidth vs ± Supply Voltage for Inverting Gains



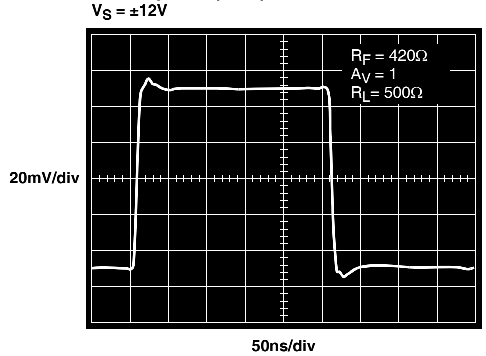
Peaking vs ± Supply Voltage for Non-inverting Gains



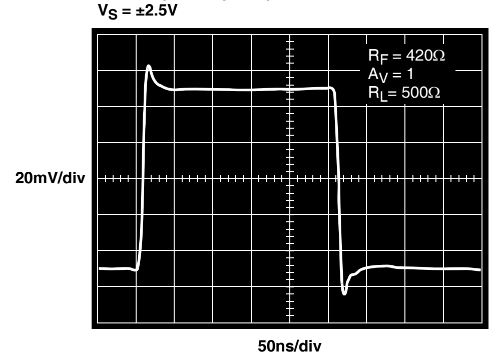
Peaking vs ± Supply Voltage for Inverting Gains



Small Signal Step Response
V_S = ±12V

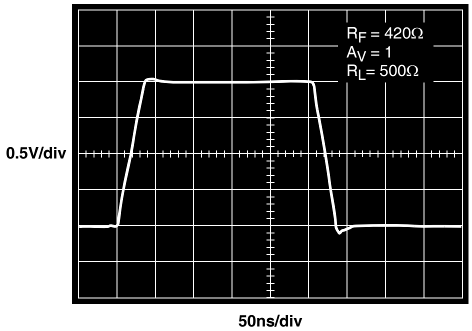


Small Signal Step Response
V_S = ±2.5V

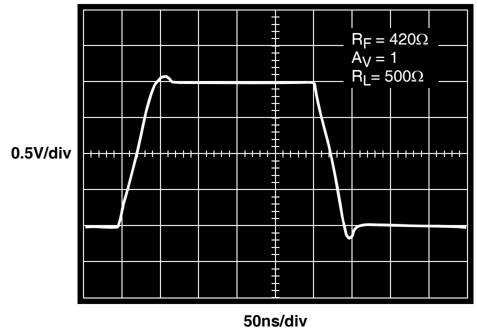


Typical Performance Curves (Continued)

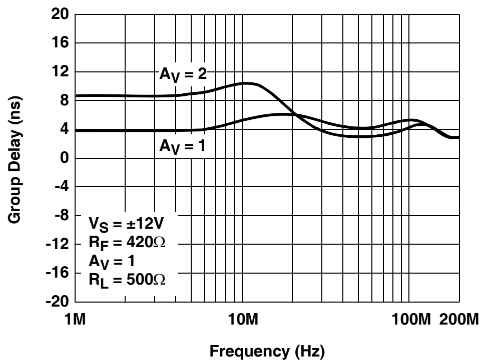
Large Signal Step Response
V_S = ±12V



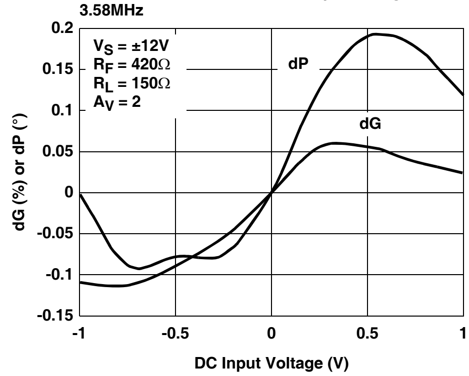
Large Signal Step Response
V_S = ±2.5V



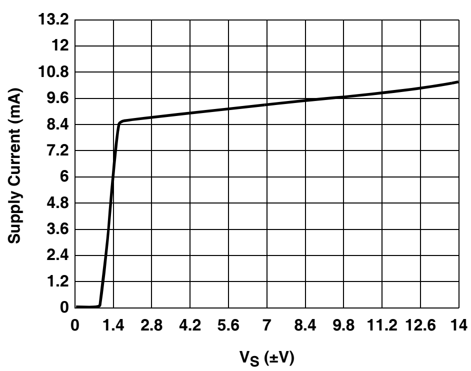
Group Delay vs Frequency



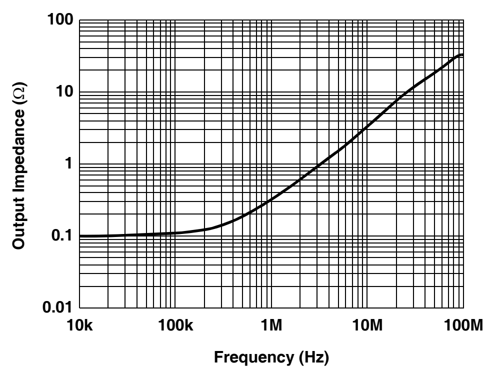
Differential Gain/Phase vs DC Input Voltage at 3.58MHz



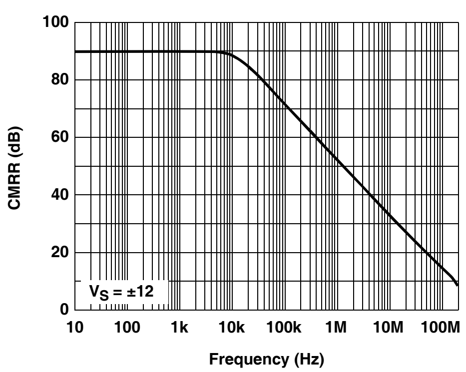
Supply Current vs Supply Voltage



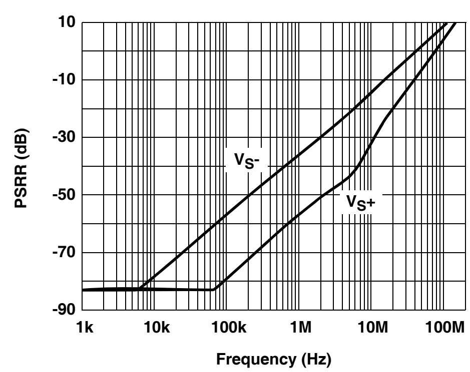
Closed Loop Output Impedance vs Frequency



CMRR vs Frequency

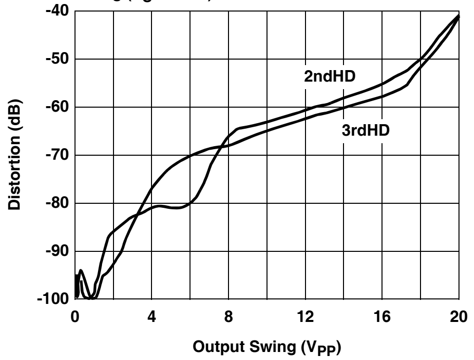


PSRR vs Frequency

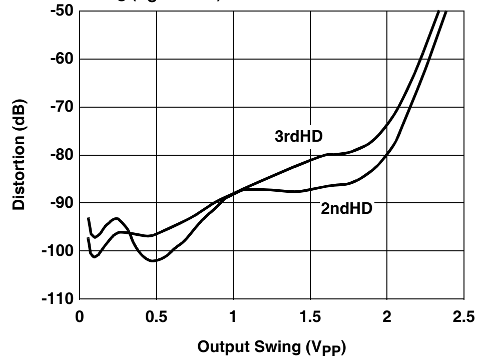


Typical Performance Curves (Continued)

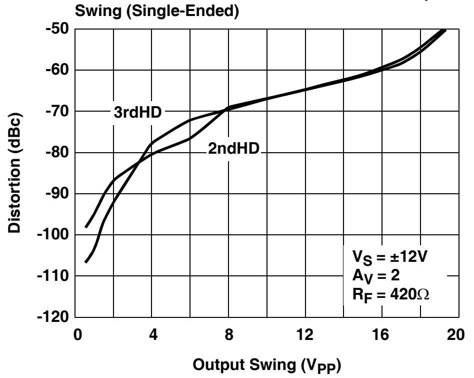
1MHz 2nd and 3rd Harmonic Distortion vs Output Swing (V_S = ±12V)



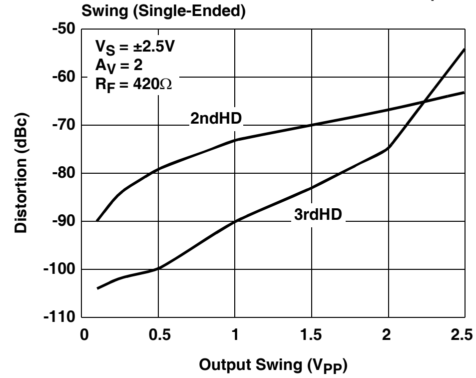
1MHz 2nd and 3rd Harmonic Distortion vs Output Swing (V_S = ±2.5V)



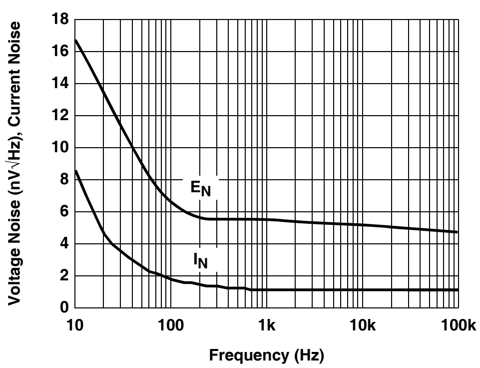
1MHz 2nd and 3rd Harmonic Distortion vs Output Swing (Single-Ended)



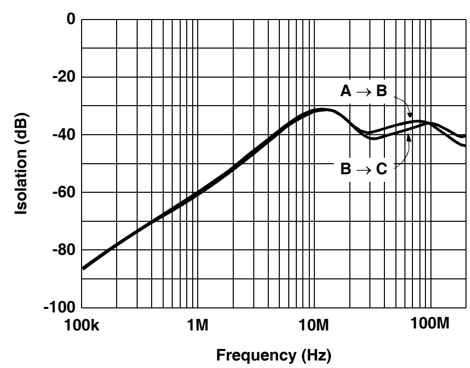
1MHz 2nd and 3rd Harmonic Distortion vs Output Swing (Single-Ended)



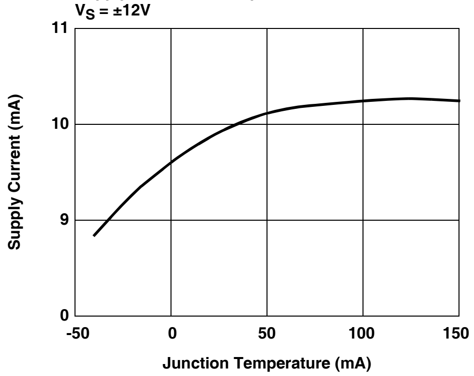
Voltage and Current Noise vs Frequency



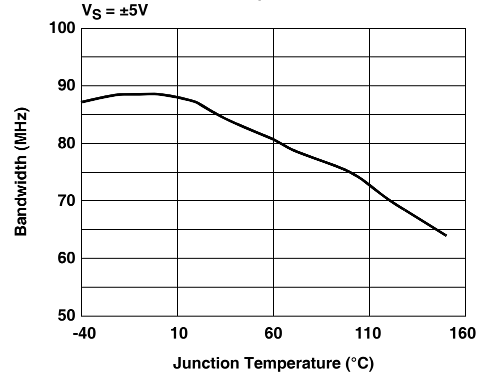
Channel to Channel Isolation vs Frequency



Supply Current vs Temperature
V_S = ±12V

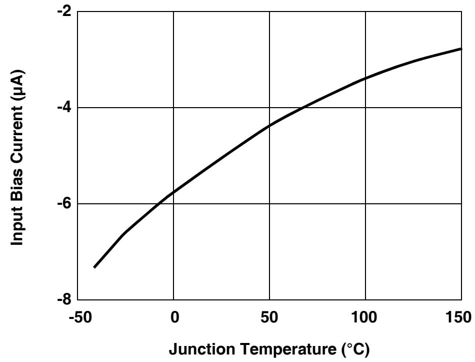


3dB Bandwidth vs Temperature
V_S = ±5V

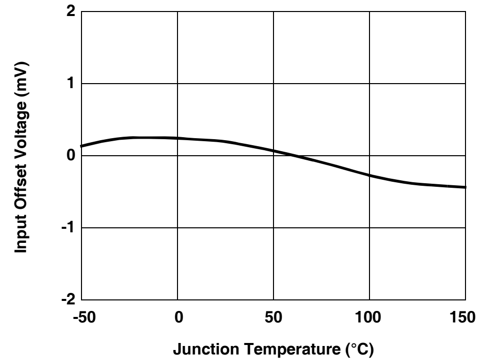


Typical Performance Curves (Continued)

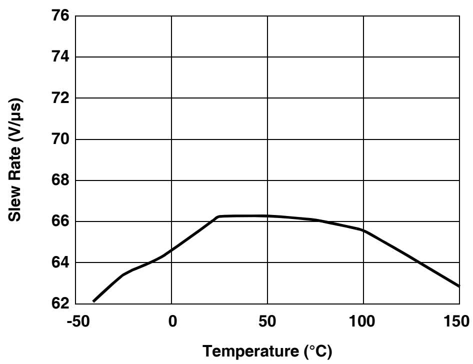
Input Bias Current vs Temperature



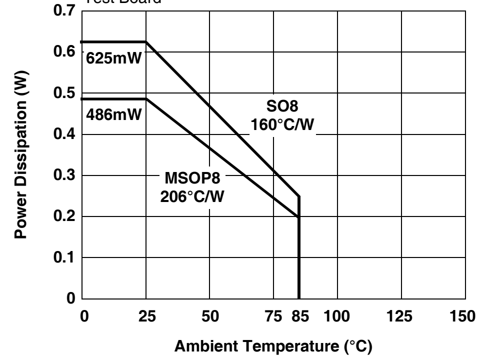
Input Offset Voltage vs Temperature



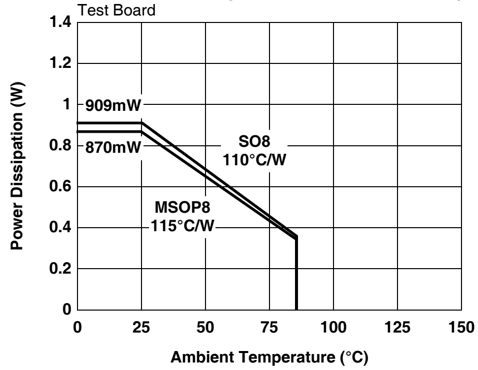
Slew Rate vs Temperature



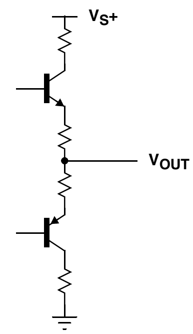
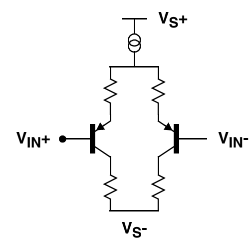
Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-3 Low Effective Thermal Conductivity Test Board



Package Power Dissipation vs Ambient Temperature
JEDEC JESD51-7 High Effective Thermal Conductivity Test Board



Pin Descriptions

8 Ld MSOP	8 Ld SOIC	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	1	$V_{OUT}A$	Output	 Circuit 1
2	2	$V_{IN}A-$	Input	 Circuit 2
3	3	$V_{IN}A+$	Input	Reference Circuit 2
4	4	VS-	Supply	
5	5	$V_{IN}B+$	Input	
6	6	$V_{IN}B-$	Input	Reference Circuit 2
7	7	$V_{OUT}B$	Output	Reference Circuit 1
8	8	V_S+	Supply	

Applications Information

Product Description

The EL2228 is a dual voltage feedback operational amplifier designed especially for DMT ADSL and other applications requiring very low voltage and current noise. It also features low distortion while drawing moderately low supply current and is built on Elantec's proprietary high-speed complementary bipolar process. The EL2228 uses a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2228 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators.

Single-Supply Operation

The EL2228 was designed to have a wide input and output voltage range. This design also makes the EL2228 an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 300mV of ground (R_L = 500Ω), and the lower output voltage range is within 875mV of ground. Upper input voltage range reaches 3.6V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 2.625V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 28V.

Gain-Bandwidth Product and the -3dB Bandwidth

The EL2228 has a gain-bandwidth product of 40MHz while using only 5mA of supply current per amplifier. For gains greater than 1, their closed-loop -3dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains of 1, higher-order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL2228 have a -3dB bandwidth of 80MHz at a gain of 1, dropping to 9MHz at a gain of 5. It is important to note that the EL2228 is designed so that this "extra" bandwidth in low-gain application does not come at the expense of stability. As seen in the typical performance curves, the EL2228 in a gain of only 1 exhibited 0.5dB of peaking with a 500Ω load.

Output Drive Capability

The EL2228 is designed to drive a low impedance load. It can easily drive $6V_{P-P}$ signal into a 500Ω load. This high output drive capability makes the EL2228 an ideal choice for RF, IF, and video applications. Furthermore, the EL2228 is current-limited at the output, allowing it to withstand momentary short to ground. However, the power dissipation with output-shorted cannot exceed the power dissipation capability of the package.

Driving Cables and Capacitive Loads

Although the EL2228 is designed to drive low impedance load, capacitive loads will decreases the amplifier's phase margin. As shown in the performance curves, capacitive load can result in peaking, overshoot and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated with a series resistor between 5Ω to 20Ω. When driving coaxial cables, double termination is always recommended for reflection-free performance. When properly terminated, the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier.

Power Dissipation

With the wide power supply range and large output drive capability of the EL2228, it is possible to exceed the 150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2228 to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL})$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = 2{*}V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L}$$

where:

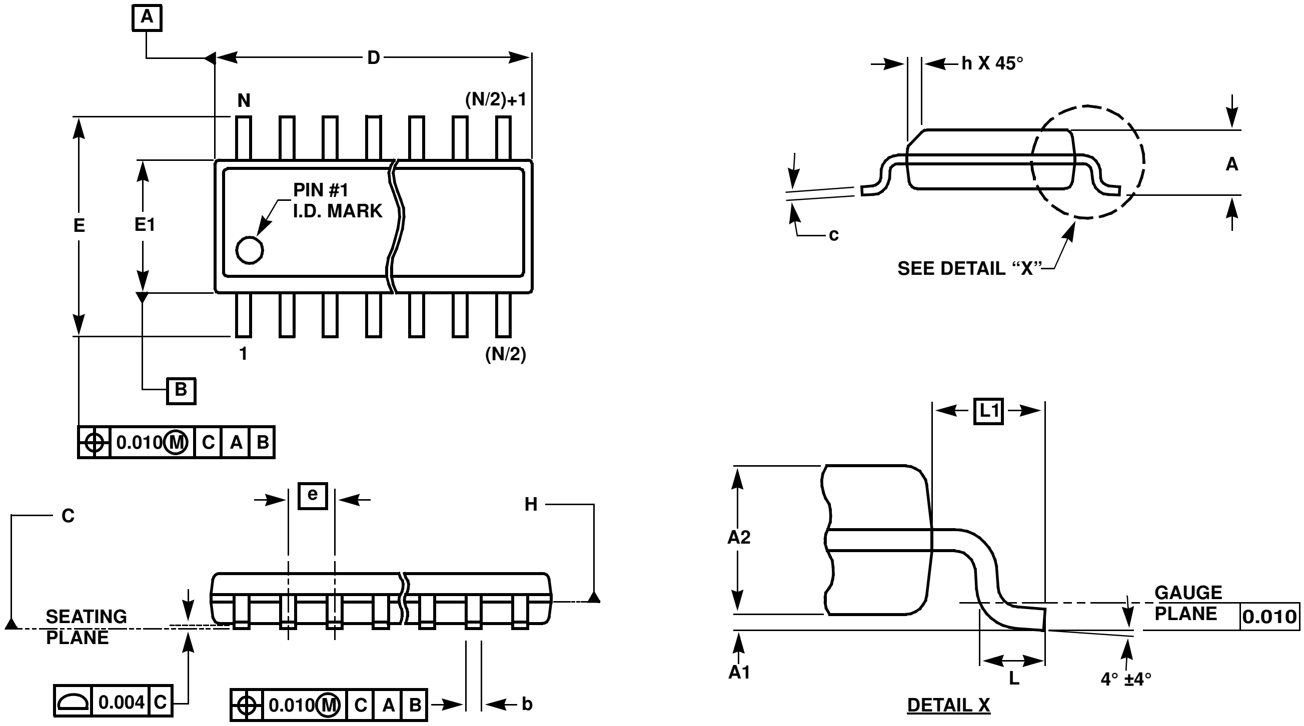
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Power Supply Bypassing And Printed Circuit Board Layout

As with any high frequency devices, good printed circuit board layout is essential for optimum performance. Ground plane construction is highly recommended. Pin lengths should be kept as short as possible. The power supply pins must be closely bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with 0.1µF ceramic capacitor has been proven to work well when placed at each supply pin. For single supply operation, where pin 4 (V_S-) is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor across pin 8 (V_S+).

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction again should be used. Small chip resistors are recommended to minimize series inductance. Use of sockets should be avoided since they add parasitic inductance and capacitance which will result in additional peaking and overshoot.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

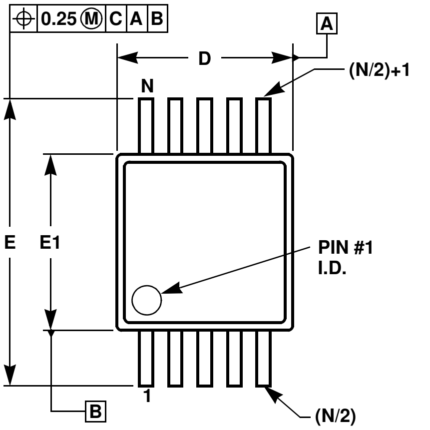
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

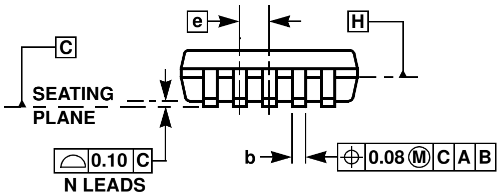
Rev. M 2/07

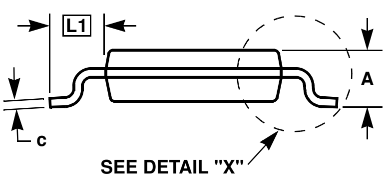
NOTES:

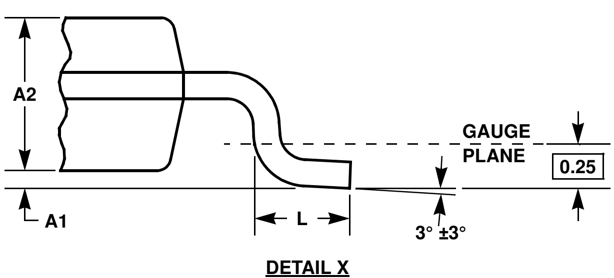
1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)









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MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.