



IDT™ 89EBPES12T3G2 Evaluation Board Manual

(Eval Board: 18-635-001)

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Table of Contents

Notes

Description of the EB12T3G2 Eval Board

Introduction	1-1
Board Features	1-2
Hardware	1-2
Software.....	1-2
Other.....	1-2
Revision History	1-2

Installation of the EB12T3G2 Eval Board

EB12T3G2 Installation	2-1
Hardware Description	2-1
Reference Clocks.....	2-1
Power Sources.....	2-2
External Power Source	2-2
PCI Express Analog High Power Voltage Converter	2-3
PCI Express Analog Power Voltage Converter	2-3
PCI Express Transmitter Analog Power Voltage Converter	2-3
Core Logic Voltage Converter	2-3
3.3V I/O Voltage Regulator	2-3
Power-up Sequence	2-3
Required Jumpers	2-3
Reset.....	2-3
Fundamental Reset	2-4
Downstream Reset	2-4
Boot Configuration Vector.....	2-4
SMBus Interfaces.....	2-6
SMBus Slave Interface	2-6
SMBus Master Interface	2-7
JTAG Header	2-7
Attention Buttons.....	2-7
Miscellaneous Jumpers, Headers	2-8
LEDs	2-8
PCI Express Connectors.....	2-9
EB12T3G2 Board Figure	2-12

Software for the EB12T3G2 Eval Board

Introduction	3-1
Device Management Software.....	3-1

Schematics

Schematics	4-1
------------------	-----

Notes



List of Tables

Notes

Table 2.1	Clock Source Selection	2-1
Table 2.2	Clock Frequency Selection	2-2
Table 2.3	Clock Spread Spectrum Selection	2-2
Table 2.4	SMA Connectors - Onboard Reference Clock	2-2
Table 2.5	External Power Connector - J1	2-3
Table 2.6	Downstream Reset Selection	2-4
Table 2.7	Boot Configuration Vector Signals	2-4
Table 2.8	Boot Configuration Vector Switches S7 & S8 (ON=0, OFF=1)	2-5
Table 2.9	Slave SMBus Interface Connector	2-6
Table 2.10	SMBus Slave Interface Address Configuration	2-6
Table 2.11	EEPROM SMBus Address Setting	2-7
Table 2.12	JTAG Connector Pin Out	2-7
Table 2.13	Attention Buttons	2-7
Table 2.14	Miscellaneous Jumpers, Headers	2-8
Table 2.15	LED Indicators	2-8
Table 2.16	PCI Express x16 Connector Pinout	2-9

Notes



List of Figures

Notes

Figure 1.1 Function Block Diagram of the EB12T3G2 Eval Board1-1

Notes



Description of the EB12T3G2 Eval Board

Notes

Introduction

The 89HPES12T3G2 switch (also referred to as PES12T3G2 in this manual) is a member of IDT's PCI Express® standard (PCIe®) based line of products. It is a Gen2 3-port switch, with 4 serial lanes per port. One upstream port is provided for connecting to the root complex (RC), and up to two downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES12T3G2 User Manual.

The 89EBPES12T3G2 Evaluation Board (also referred to as EB12T3G2 in this manual) provides an evaluation platform for the PES12T3G2 switch. It is also a cost effective way to add a PCIe downstream port (x4) to an existing system with a limited number of PCIe downstream ports. The EB12T3G2 eval board is designed to function as an add-on card to be plugged into a x4 PCIe slot available on a motherboard hosting an appropriate root complex, microprocessor(s), and two downstream ports. The EB12T3G2 is a vehicle to test and evaluate the functionality of the PES12T3G2 chip. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB12T3G2 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB12T3G2 board.

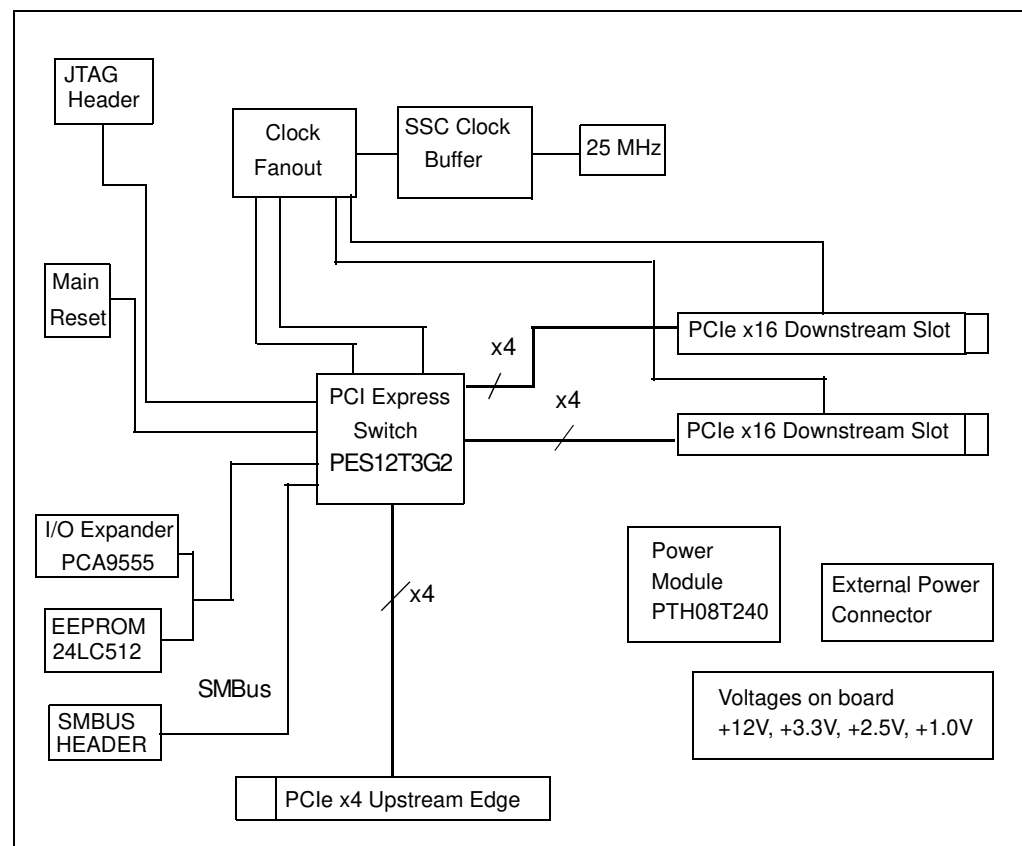


Figure 1.1 Function Block Diagram of the EB12T3G2 Eval Board

Notes

Board Features

Hardware

- ◆ PES12T3G2 PCIe 3 port switch
 - Three x4 ports, 12 PCIe lanes
 - PCIe Base Specification Revision 2.0 compliant
 - 12 GBps (96 Gbps) aggregate switching capacity
 - Up to 2048 byte maximum Payload Size
 - Automatic lane reversal and polarity inversion supported on all lanes
 - Automatic per port link width negotiation to x4, x2, x1
 - Load configuration from an optional serial EEPROM via SMBUS
- ◆ Upstream, Downstream Port
 - One edge connector on the upstream port, to be plugged into a slot with at least x4 capable on a host motherboard
 - Two slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in. These slot connectors are x16 mechanically but electronically connected as x4 only.
- ◆ Numerous user selectable configurations set using onboard jumpers and DIP-switches
 - Source of clock - host clock or onboard clock generator
 - Two clock rates and spread spectrum settings
 - Boot mode selection
- ◆ SMBUS Slave Interface (4 pin header)
- ◆ SMBUS Master Interface connected to the Serial EEPROMs through I/O expander
- ◆ “Attention” button for each downstream port to initiate a hot swap event on each port
- ◆ Four pin connector for optional external power supply
- ◆ Push button for Warm Reset
- ◆ Several LEDs to display status, reset, power, “Attention”, etc.
- ◆ One 10-pin JTAG connector (pitch 2.54 mm x 2.54 mm)

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES12T3G2 within host systems running popular operating systems.

- ◆ Installation programs
 - Operating Systems Supported: Windows2000, WindowsXP, Vista, Linux
- ◆ GUI based application for Windows and Linux
 - Allows users to view and modify registers in the PES12T3G2
 - Binary file generator for programming the serial EEPROMs attached to the SMBUS.

Other

- ◆ A metal bracket is required to firmly hold in place two endpoints plugged into the EB12T3G2 board.
- ◆ An external power supply may be required under some conditions.
- ◆ SMBUS cable may be required for certain evaluation exercises.
- ◆ SMA connectors are provided on the EB12T3G2 board for specific test points.

Revision History

September 19, 2007: Initial publication of version 18-635-001 board manual.

October 3, 2007: Updated Schematics: replace 0.1uF at C25/C26 with 0 ohm.



Installation of the EB12T3G2 Eval Board

Notes

EB12T3G2 Installation

This chapter discusses the steps required to configure and install the EB12T3G2 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Insert the evaluation board into the host system (motherboard with root complex chipset).
4. Apply power to the host system.

The EB12T3G2 board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

Hardware Description

The PES12T3G2 is a 12-lane, 3-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 2 downstream ports or peer-to-peer switching between downstream ports.

The EB12T3G2 has two PCI Express downstream ports, accessible through two x16 connectors. All two ports are capable of negotiating a x1, x2, or x4 link width. All endpoint cards connected to the PES12T3G2 must support at least one of these link widths.

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x4 configuration through a PCI Express x4 slot.
- x1, x2, or x4 PCI Express Endpoint Cards.

Reference Clocks

The PES12T3G2 requires a differential reference clock. The EB12T3G2 derives this clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by stuffing resistors described in Table 2.1.

Clock Configuration Stuffing Option	
W6 and W7	Clock Source
Pins 2 and 3	Onboard Reference Clock – Use onboard clock generator
Pins 1 and 2	Upstream Reference Clock – Host system provides clock (Default)

Table 2.1 Clock Source Selection

The source for the onboard clock is the ICS557-03 clock generator device (U8) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB12T3G2 allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Notes

Clock Frequency Switch - S2[2:1]		
S2[2]	S2[1]	Clock Frequency
OFF	OFF	Reserved
OFF	ON	125 MHz
ON	OFF	100 MHz (Default)
ON	ON	<Reserved>

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S2[4:3]		
S2[4]	S2[3]	Spread%
OFF	OFF	No Spread (Default)
OFF	ON	Down -0.75
ON	OFF	Down -0.50
ON	ON	Center ±0.25

Table 2.3 Clock Spread Spectrum Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock should be used instead.

The output of the onboard clock generator is accessible through two SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J7, J6	
J6	Positive Reference Clock
J7	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Power Sources

The EB12T3G2 and all downstream ports are powered from the upstream port slot power. If add-in cards require more power than the upstream slot can support, an external source is required to supply this extra power via an auxiliary 4-pin power connector on the board. Header W1, W2, and W3 (see Table 2.14) are used to select proper power source for the switch and all downstream ports.

External Power Source

If necessary, external power is supplied to the EB12T3G2 board through a 4-pin auxiliary power connector attached to J1. The external power supply provides +12V to the EB12T3G2 as described in Table 2.5. The +5V is unused.

Notes

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.5 External Power Connector - J1

PCI Express Analog High Power Voltage Converter

A DC-DC converter (U18) provides a 2.5V PCI Express analog high power voltage (shown as VDDHA) to the PES12T3G2.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U16) provides a 1.0V PCI Express analog power voltage (VDDA) to the PES12T3G2.

PCI Express Transmitter Analog Power Voltage Converter

A separate DC-DC converter (U17) provides a 1.0V PCI Express transmitter analog power voltage (shown as VDDPETA) to the PES12T3G2.

Core Logic Voltage Converter

A separate DC-DC converter (U15) provides the 1.0V core voltage (VDDCORE) to the PES12T3G2.

3.3V I/O Voltage Regulator

A 12V to 3.3V voltage regulator (VR1) provides the 3.3V I/O voltage (VDDIO) to the PES12T3G2.

Power-up Sequence

During power supply ramp-up, VDDCORE must remain at least 1.0V below VDDIO at all times. There are no other power-up sequence requirements for the various operating supply voltages.

Required Jumpers

To deliver power to the PES12T3G2 switch, the following jumpers must be shunted: W25, W21, W22, W23, and W24. These jumpers were implemented so that the power consumption of the PES12T3G2 can be measured.

Reset

The PES12T3G2 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES12T3G2, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES12T3G2 User Manual. The EB12T3G2 evaluation board provides seamless support for Hot Reset.

Notes

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB12T3G2 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES12T3G2.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
 - Pressing a push-button switch (S1) located on EB12T3G2 board
 - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB12T3G2. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W4.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES12T3G2 while power is on.

Downstream Reset

The PES12T3G2 provides a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.6.

Port #	Jumper	Selection
2	W19	[1-2] Software controlled reset through GPIO0 [2-3] Fundamental reset PERST# (default)
4	W17	[1-2] Software controlled reset through GPIO1 [2-3] Fundamental reset PERST# (default)

Table 2.6 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.7 is sampled by the PES12T3G2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S7 and S8 as defined in Table 2.8.

Signal	Description
CCLKDS	Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This pin is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in the downstream port's PCIELSTS register. Default: 0x1
CCLKUS	Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This pin is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register. Default: 0x1
MSMBSMODE	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. Default: 0x0

Table 2.7 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
RSTHALT	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, the PES12T3G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. Default: 0x0
SWMODE[2:0]	Switch Mode. These configuration pins determine the PES12T3G2 switch operating mode. Default: 0x0 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x7 - Reserved
REFCLKM	PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. Default: 0x0 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[2:0]	Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. Default: 0x0

Table 2.7 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S8[1]	CCLKDS	OFF
S8[2]	CCLKUS	OFF
S8[3]	MSMBSMODE	ON
S8[4]	Not Used	ON
S8[5]	Not Used	ON
S8[6]	Not Used	ON
S8[7]	Not Used	ON
S8[8]	RSTHALT	ON
S7[1]	SWMODE[0]	ON
S7[2]	SWMODE[1]	ON
S7[3]	SWMODE[2]	ON
S7[4]	Not Used	ON
S7[5]	REFCLKM	ON
S7[6]	MSMBADDR[0]	ON
S7[7]	MSMBADDR[1]	ON
S7[8]	MSMBADDR[2]	ON

Table 2.8 Boot Configuration Vector Switches S7 & S8 (ON=0, OFF=1)

Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I²C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES12T3G2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROM used for initialization and the I/O expanders used for hot-plug signals.

SMBus Slave Interface

On the PES12T3G2 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.9.

Note: The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R160 and R161.

Slave SMBus Interface Connector J8	
Pin	Signal
1	N/C
2	SCL
3	GND
4	SDA

Table 2.9 Slave SMBus Interface Connector

A fixed slave SMBus address (0b1100_000) specified by the SSMBADDR[5,3:1] pins is used.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.10 SMBus Slave Interface Address Configuration

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

Notes

SMBus Master Interface

Connected to the master SMBus interface are three 16-bit I/O Expanders (PCA9555) and a serial EEPROM (24LC512). Three I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander0/2/4 are fixed as 0x0, 0x2 and 0x4, respectively.

The seven bits address for the selected EEPROM device is **0b1010_000** by default and the lower three bit is configurable using switch S7 as described in Table 2.11.

S7[8]	S7[7]	S7[6]	Bus Address
OFF	OFF	OFF	0b111
OFF	OFF	ON	0b110
OFF	ON	OFF	0101
OFF	ON	ON	0b100
ON	OFF	OFF	0b011
ON	OFF	ON	0b010
ON	ON	OFF	0b001
ON	ON	ON	0b000 (Default)

Table 2.11 EEPROM SMBus Address Setting

JTAG Header

The PES12T3G2 provides a JTAG connector J5 for access to the PES12T3G2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.15 for the JTAG Connector J5 pin out.

JTAG Connector J5					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.12 JTAG Connector Pin Out

Attention Buttons

The PES12T3G2 features two attention buttons, shown in Table 2.13. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S5	Port 2 Attention Button
S3	Port 4 Attention Button

Table 2.13 Attention Buttons

Notes

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	Type	Default	Description
W1-W3	Header	1-2 Shunted	1-2: 12.0V source from Upstream Port (Default) 2-3: 12.0V source from external power connector
W20	Header	Shunted	Disable EEPROM Write protect feature (Default)
S6[1]	Switch	ON	ON: Port2, Force hot-plug controller on OFF: Port2, Power Enable bit controls hot-plug controller
S6[2]	Switch	On	ON: Port4, Force hot-plug controller on OFF: Port4, Power Enable bit controls hot-plug controller
W15	Header	2-3 Shunted	2-3: Port 2, +12V source from Upstream port (Default) 1-2: Port 2, +12V source from hot-plug controller
W9	Header	2-3 Shunted	2-3: Port 4, +12V source from Upstream port (Default) 1-2: Port 4, +12V source from hot-plug controller
W16	Header	2-3 Shunted	2-3: Port 2, +3.3V source from Upstream port (Default) 1-2: Port 2, +3.3V source from hot-plug controller
W10	Header	2-3 Shunted	2-3: Port 4, +3.3V source from Upstream port (Default) 1-2: Port 4, +3.3V source from hot-plug controller
W14	Header	2-3 Shunted	2-3: Port 2, +3.3AUX source from upstream port (Default) 1-2: Port 2, +3.3V source from hot-plug controller
W8	Header	2-3 Shunted	2-3: Port 4, +3.3AUX source from upstream port (Default) 1-2: Port 4, +3.3V source from hot-plug controller

Table 2.14 Miscellaneous Jumpers, Headers

LEDs

There are several LED indicators on the EB12T3G2 which convey status feedback. A description of each is provided in Table 2.15.

Location	Color	Definition
DS21	Green	Port 2: Power-is-good indicator
DS9	Green	Port 4: Power-is-good indicator
DS20	Green	Port 2: Power Indicator
DS8	Green	Port 4: Power Indicator
DS19	Yellow	Port 2: Attention Indicator
DS7	Yellow	Port 4: Attention Indicator
DS18	Green	Port2: Activity Indicator
DS6	Green	Port4: Activity Indicator

Table 2.15 LED Indicators (Part 1 of 2)

Notes

Location	Color	Definition
DS17	Green	Port2: Linkup Indicator
DS5	Green	Port4: Linkup Indicator
DS23	Green	Port0: Linkup Indicator
DS24	Green	Port0: Activity Indicator
DS3	Red	Port2/4: Power Fault Indicator
DS25	Green	GPIO3
DS26	Green	GPIO5
DS27	Green	GPIO6
DS28	Green	GPIO11

Table 2.15 LED Indicators (Part 2 of 2)

PCI Express Connectors

Pin	Side A		Side B	
	1	+12V	12V power	PRSNT1#
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential

Table 2.16 PCI Express x16 Connector Pinout (Part 1 of 3)

Notes

Pin	Side A		Side B	
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground
50	PETp8	Transmitter differential	RSVD	Reserved
51	PETn8	pair, Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential
53	GND	Ground	PERn8	pair, Lane 8
54	PETp9	Transmitter differential	GND	Ground
55	PETn9	pair, Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential
57	GND	Ground	PERn9	pair, Lane 9
58	PETp10	Transmitter differential	GND	Ground

Table 2.16 PCI Express x16 Connector Pinout (Part 2 of 3)

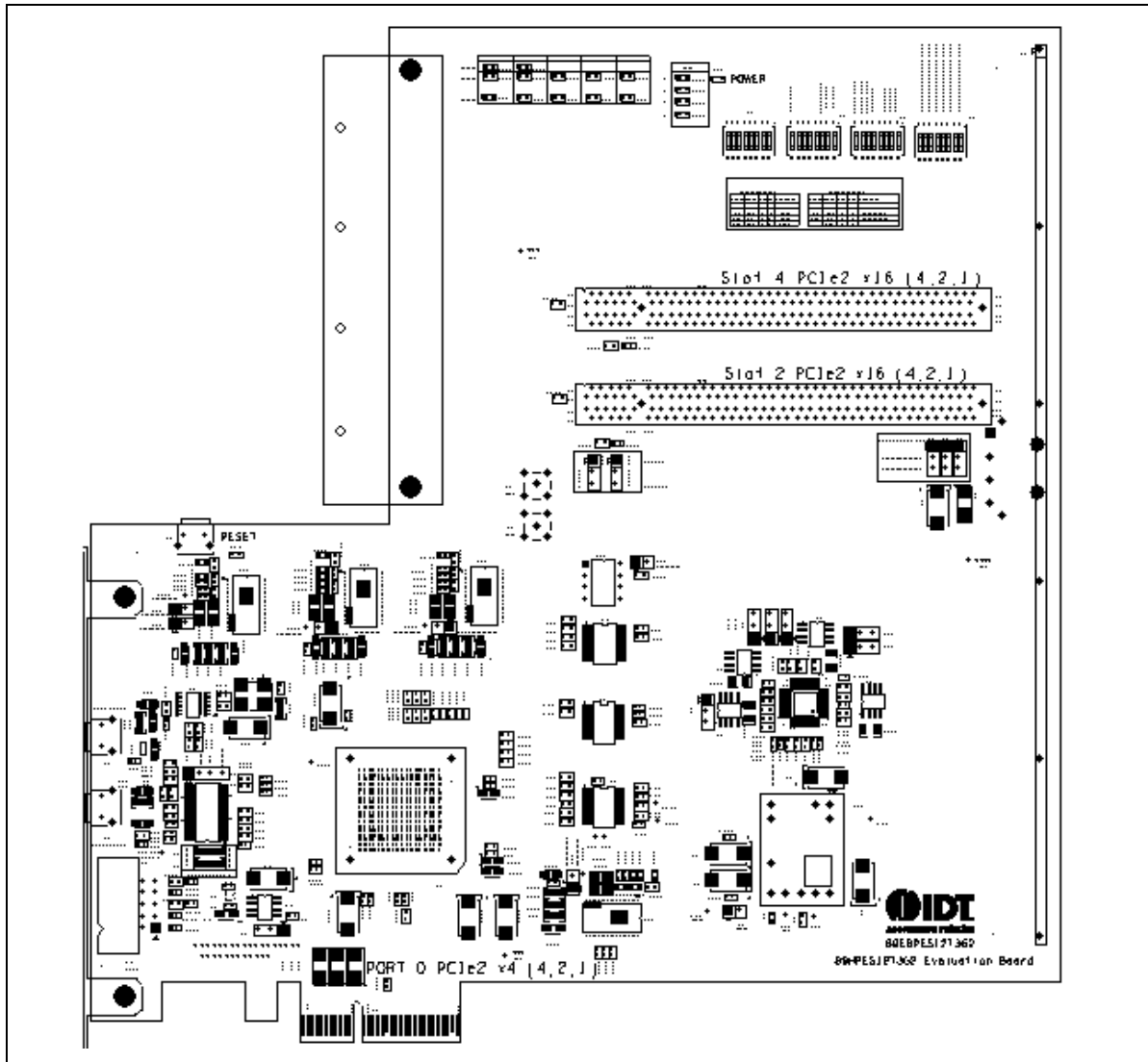
Notes

Pin	Side A		Side B	
59	PETn10	pair, Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential
61	GND	Ground	PERn10	pair, Lane 10
62	PETp11	Transmitter differential	GND	Ground
63	PETn11	pair, Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential
65	GND	Ground	PERn11	pair, Lane 11
66	PETp12	Transmitter differential	GND	Ground
67	PETn12	pair, Lane 12	GND	Ground
68	GND	Ground	PERp12	Receiver differential
69	GND	Ground	PERn12	pair, Lane 12
70	PETp13	Transmitter differential	GND	Ground
71	PETn13	pair, Lane 13	GND	Ground
72	GND	Ground	PERp13	Receiver differential
73	GND	Ground	PERn13	pair, Lane 13
74	PETp14	Transmitter differential	GND	Ground
75	PETn14	pair, Lane 14	GND	Ground
76	GND	Ground	PERp14	Receiver differential
77	GND	Ground	PERn14	pair, Lane 14
78	PETp15	Transmitter differential	GND	Ground
79	PETn15	pair, Lane 15	GND	Ground
80	GND	Ground	PERp15	Receiver differential
81	PRSNT2#	Hot-Plug presence detect	PERn15	pair, Lane 15
82	RSVD	Reserved	GND	Ground

Table 2.16 PCI Express x16 Connector Pinout (Part 3 of 3)

Note: These x16 PCI Express connectors comply with the PCIe specification. However, the downstream ports on the EB12T3G2 are electronically connected in x4 configuration. According to the PCI Express specification, the PRSNT1# pin should be wired to the farthest available PRSNT2# pin on the connector. In the EB12T3G2, all PRSNT2# pins are tied together. This allows the board to be installed in a x1 or a x4 slot via a slot reducer.

EB12T3G2 Board Figure



Notes



Software for the EB12T3G2 Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB12T3G2 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES12T3G2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES12T3G2.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES12T3G2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES12T3G2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

Notes



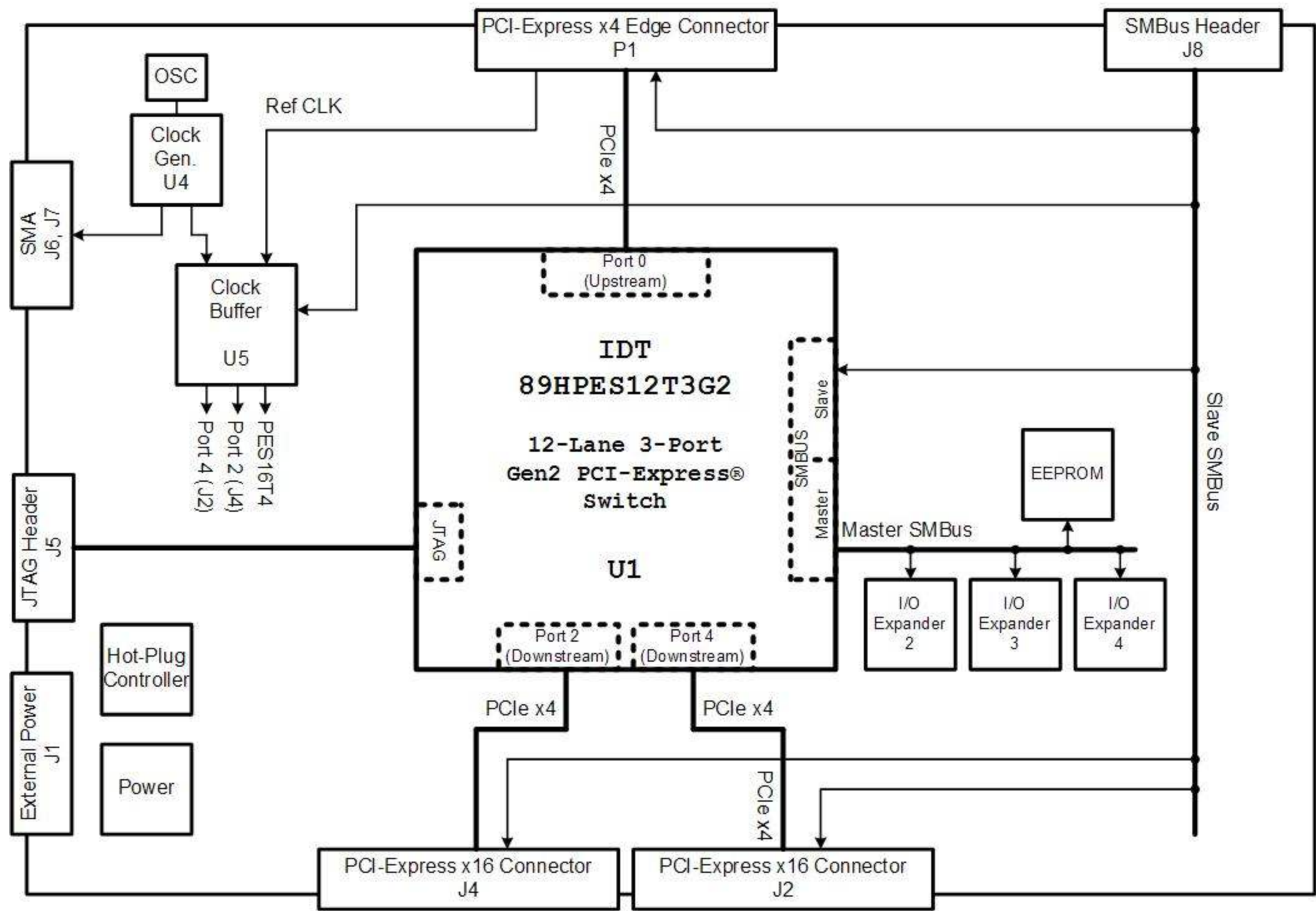
Schematics

Notes

Schematics

89EBPES12T3G2 – 89HPES12T3G2 Evaluation Board

REVISIONS				
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STGC-0139R01	1.0	INITIAL RELEASE	2007-10-02	K. LEUNG



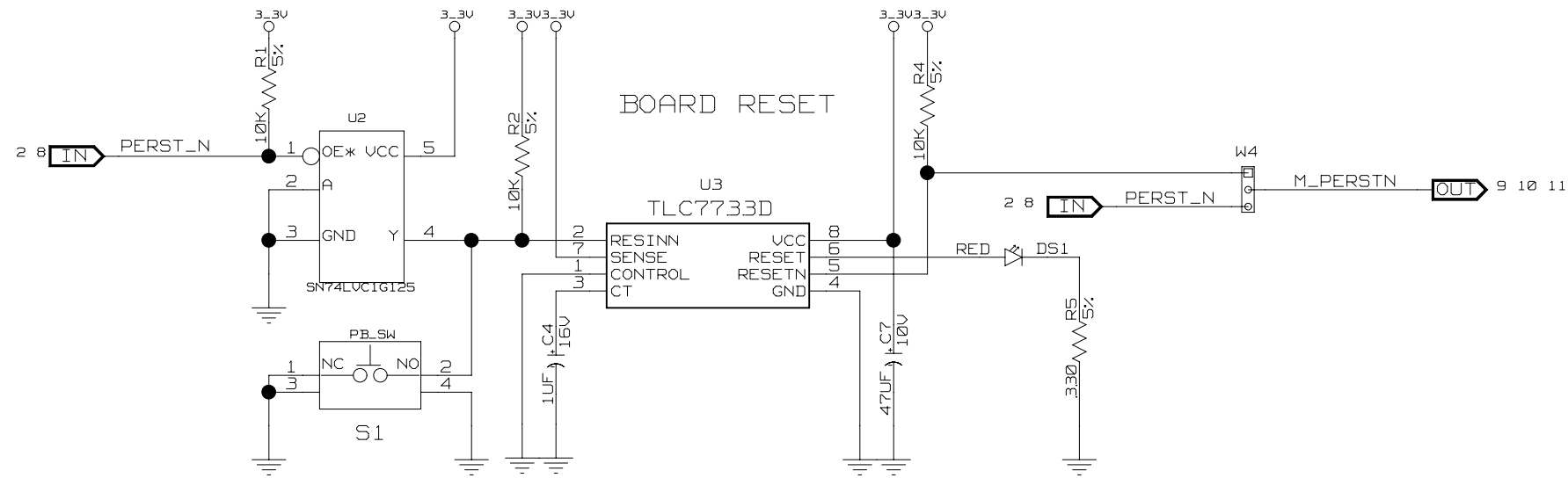
SHEET DESCRIPTION

- 1 TITLE PAGE
- 2 RESET, POWER CONNECTOR
- 3 POWER REGULATORS
- 4 CLOCKS
- 5 I/O EXP, WAKE, ATTN
- 6 HOT PLUG CONTROLLERS
- 7 HOT PLUG – MOSFETS
- 8 PORT 0 EDGE CONN (U/S)
- 9 PORT 2 CONNECTOR (D/S)
- 10 PORT 4 CONNECTOR (D/S)
- 11 PES12T3G2 – EEPROM, JTAG
- 12 PES12T3G2 – POWER

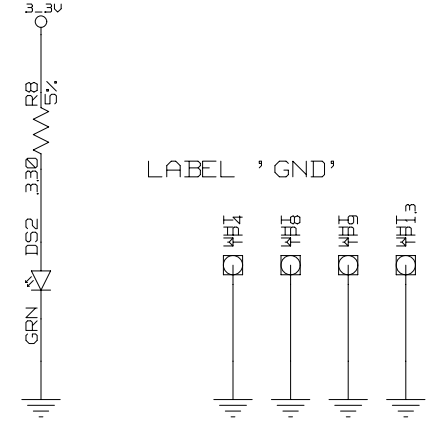


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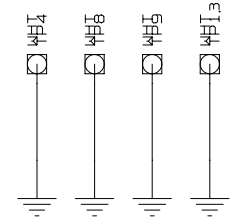
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SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Tue Oct 02 17:11:08 2007			SHEET 1 OF 12



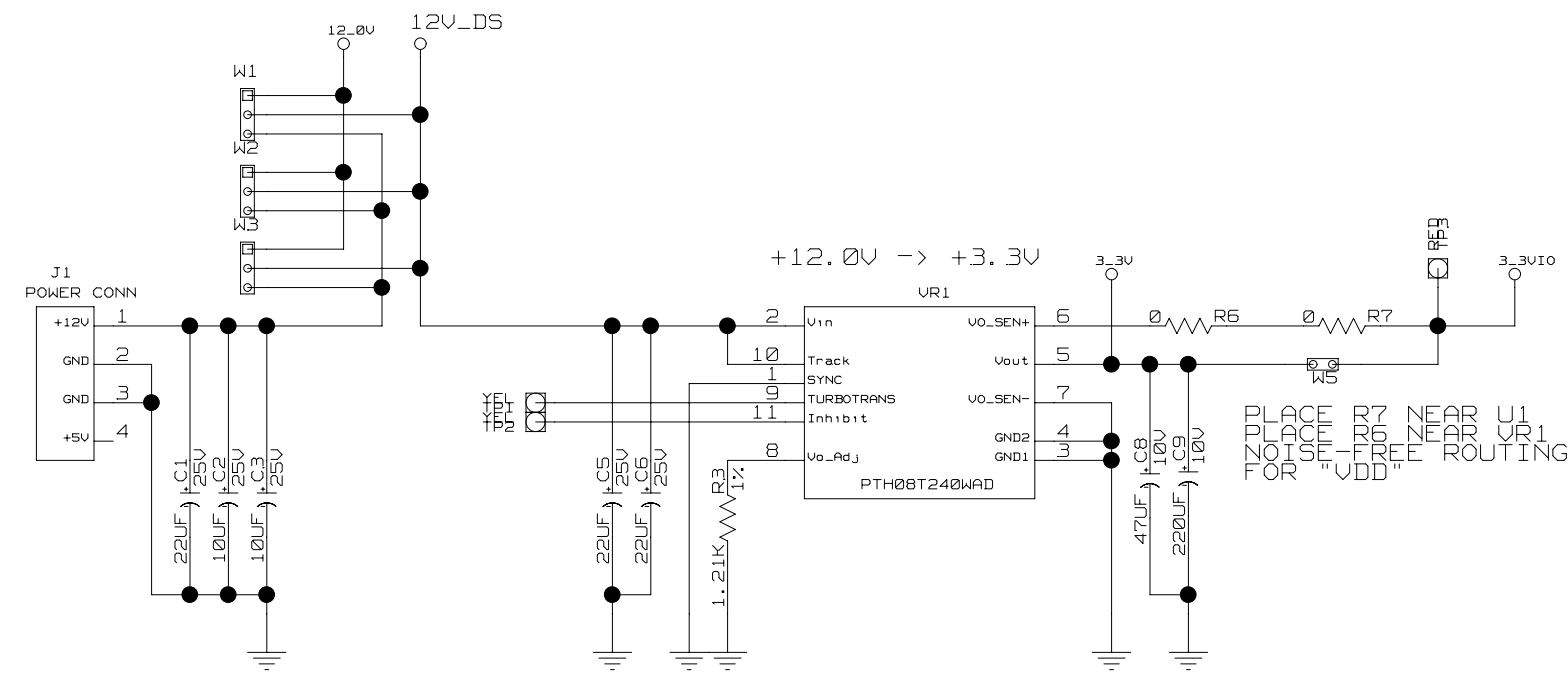
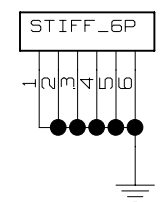
POWER INDICATOR
PLACE NEAR TOP EDGE
LABEL 'POWER'



LABEL 'GND'

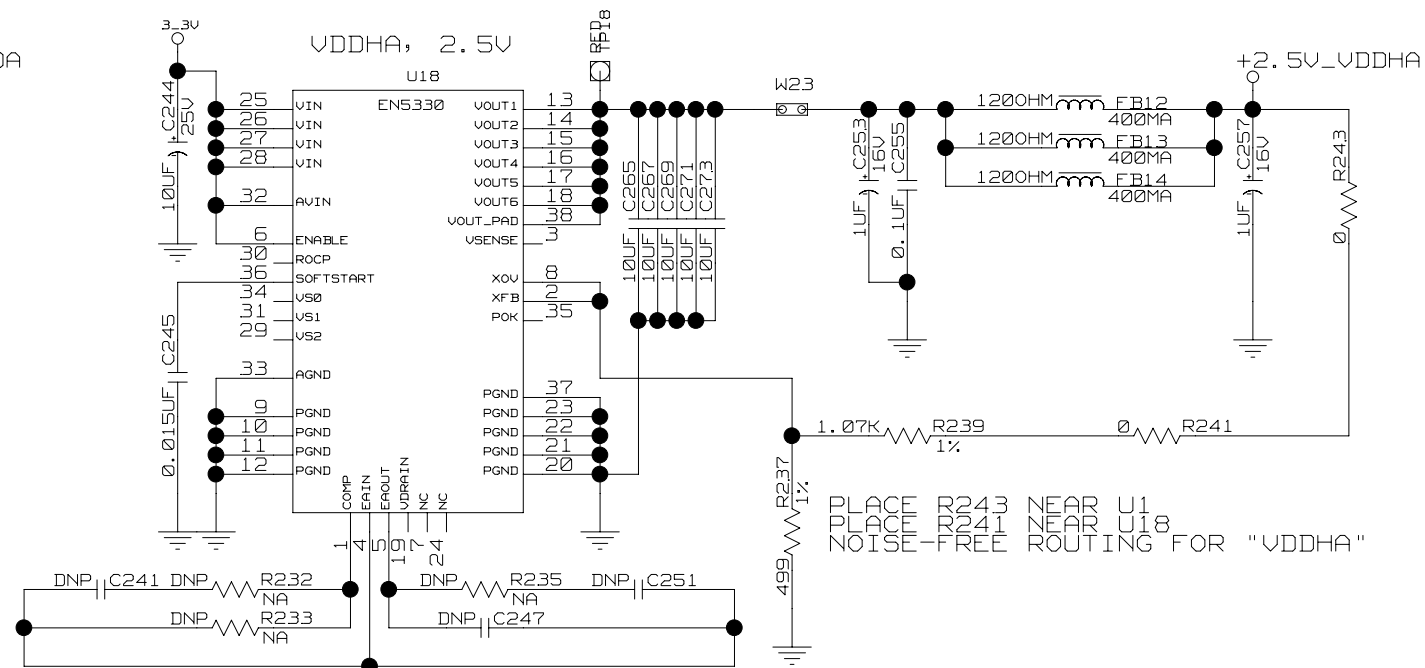
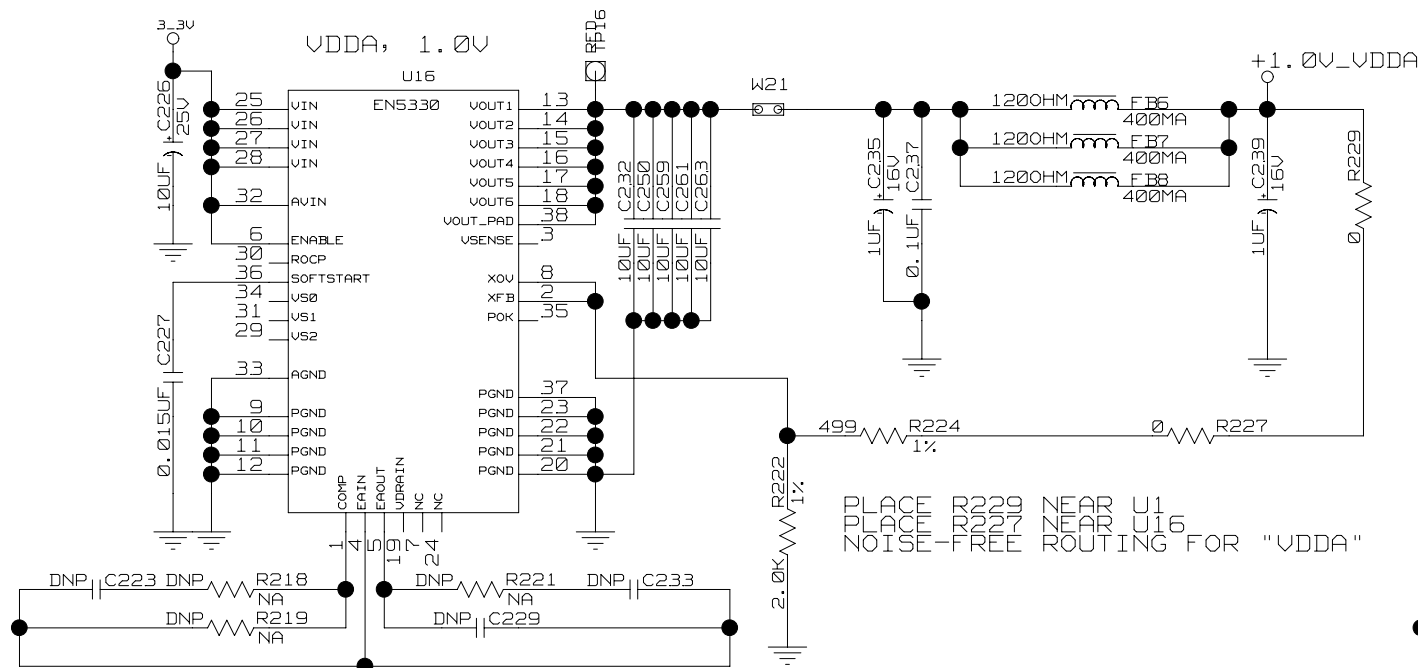
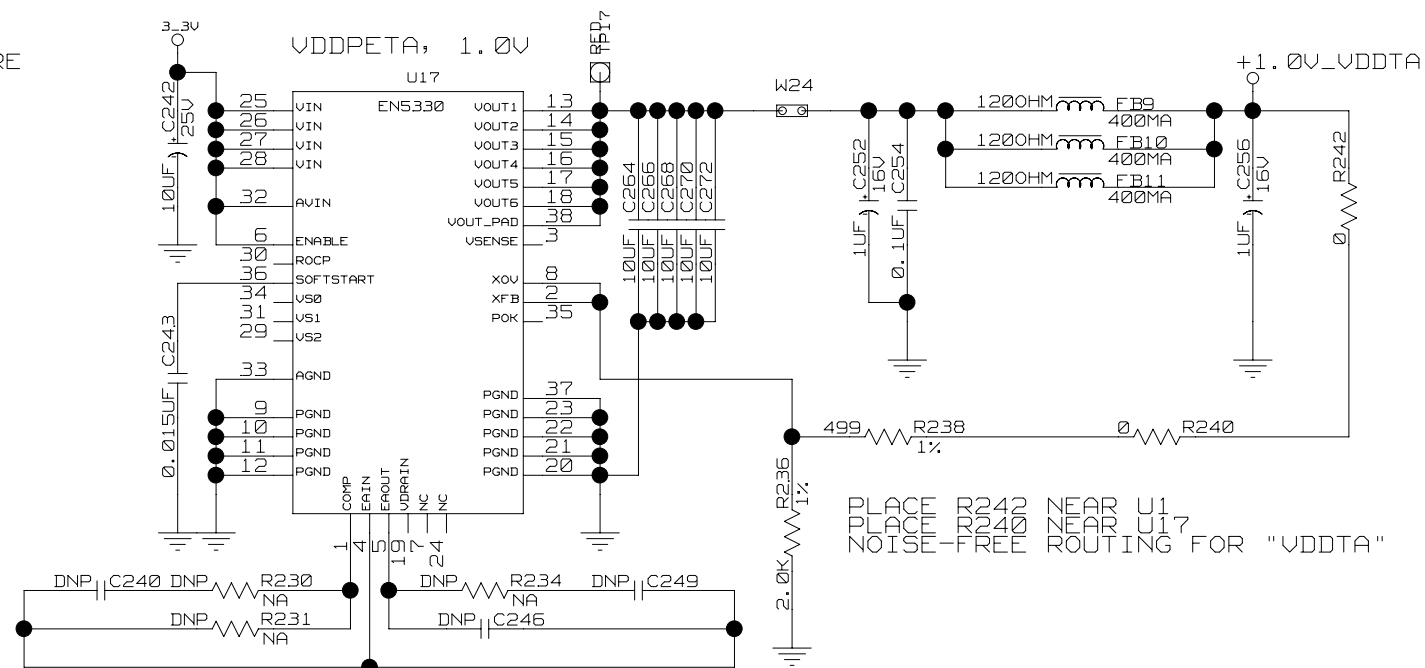
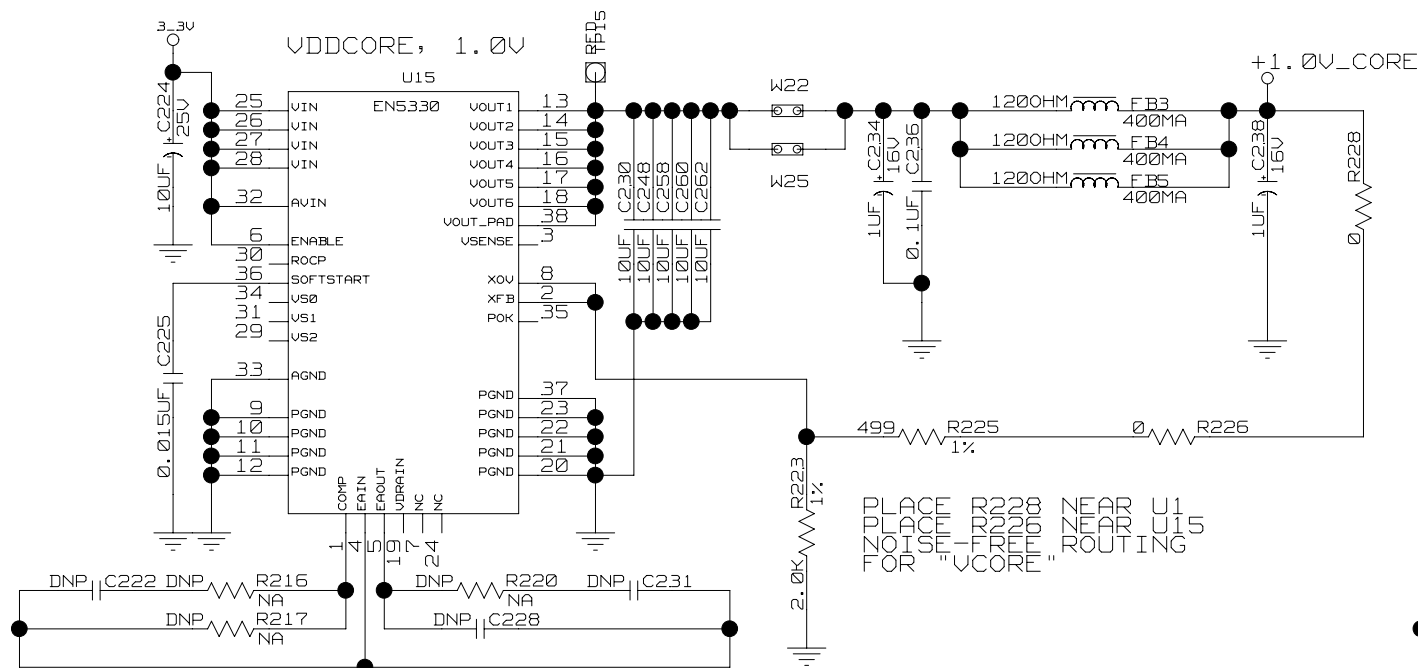


M1



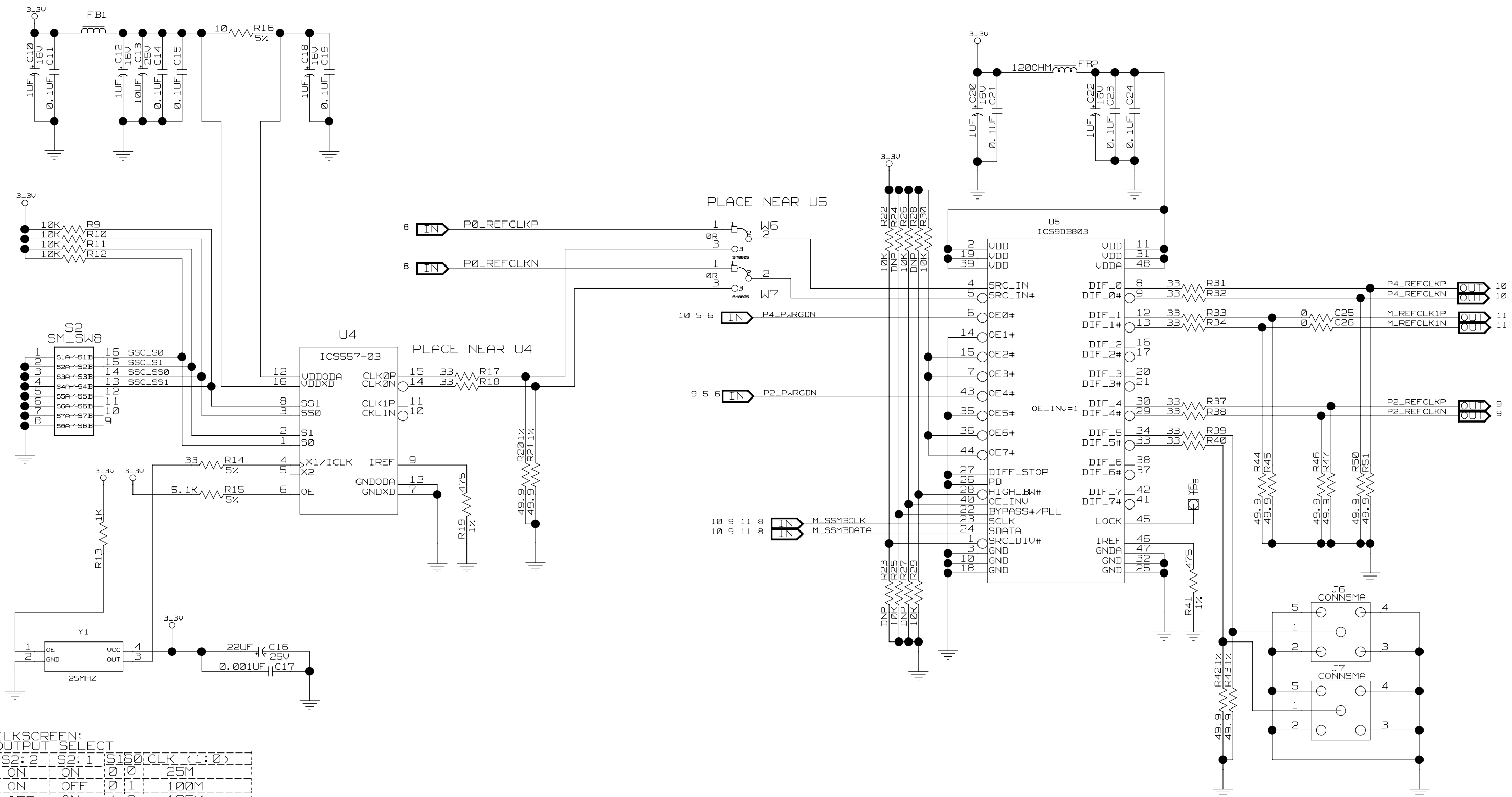
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TITLE 89EBPES12T3G2			
RESET, POWER CONNECTOR			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Mon Sep 10 17:39:41 2007			SHEET 2 OF 12



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TITLE 89EBPES12T3G2			
POWER REGULATORS			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Mon Sep 10 17:39:41 2007			SHEET 3 OF 12



SILKSCREEN:
OUTPUT SELECT

S2: 2	S2: 1	S1S0	CLK (1:0)
ON	ON	0 0	25M
ON	OFF	0 1	100M
OFF	ON	1 0	125M
OFF	OFF	1 1	200M

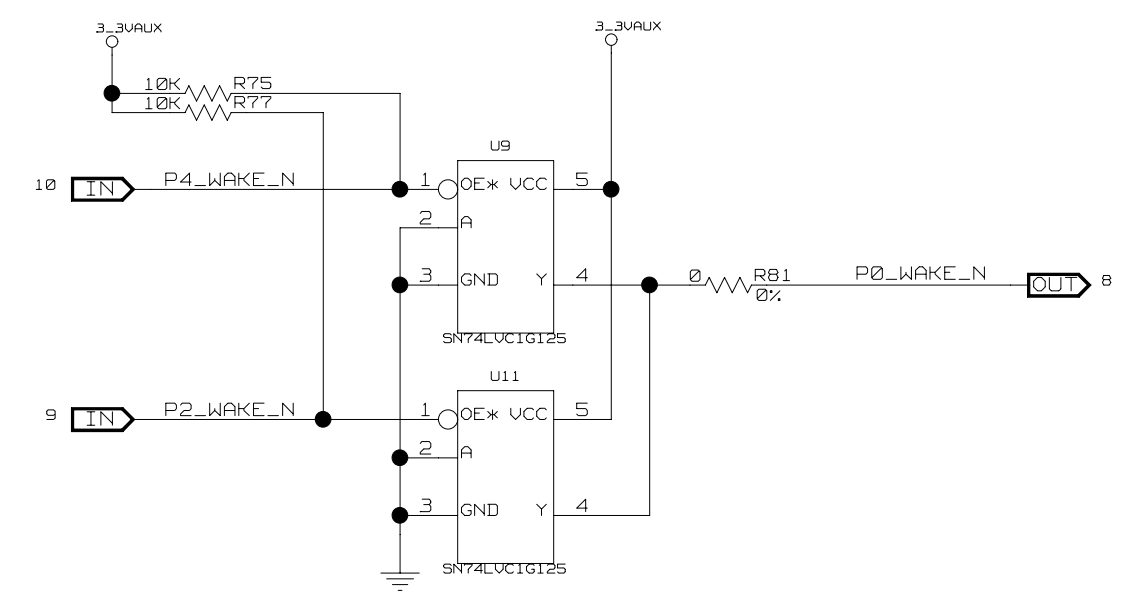
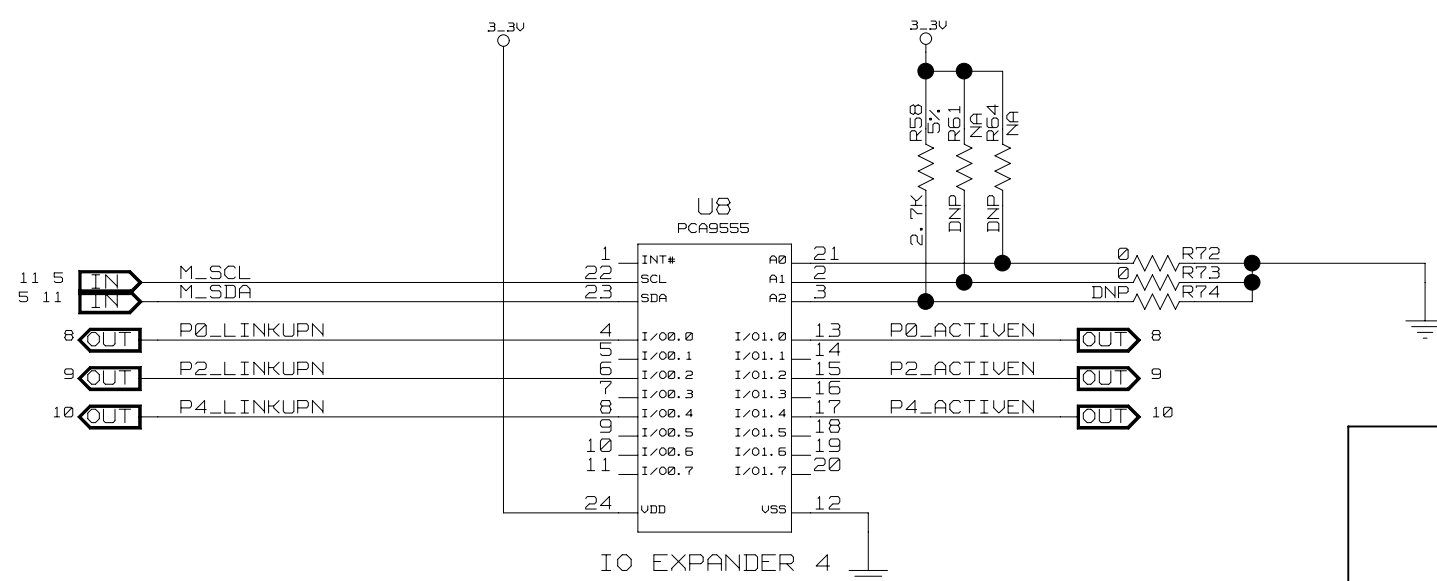
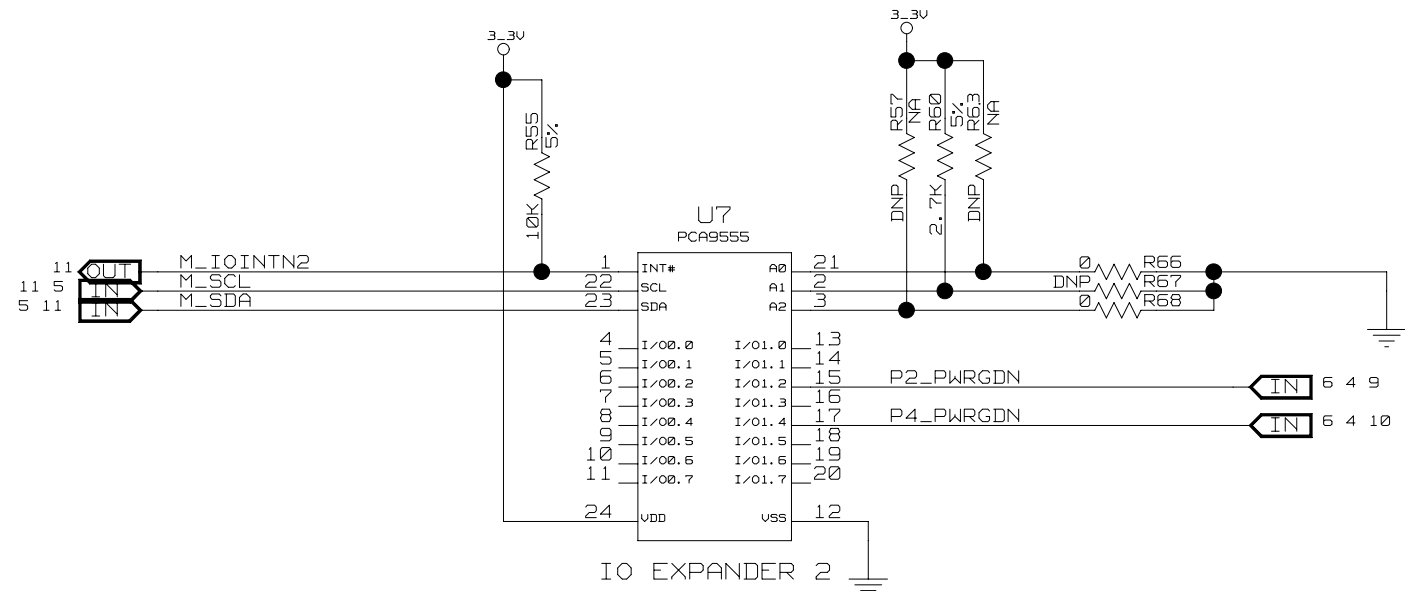
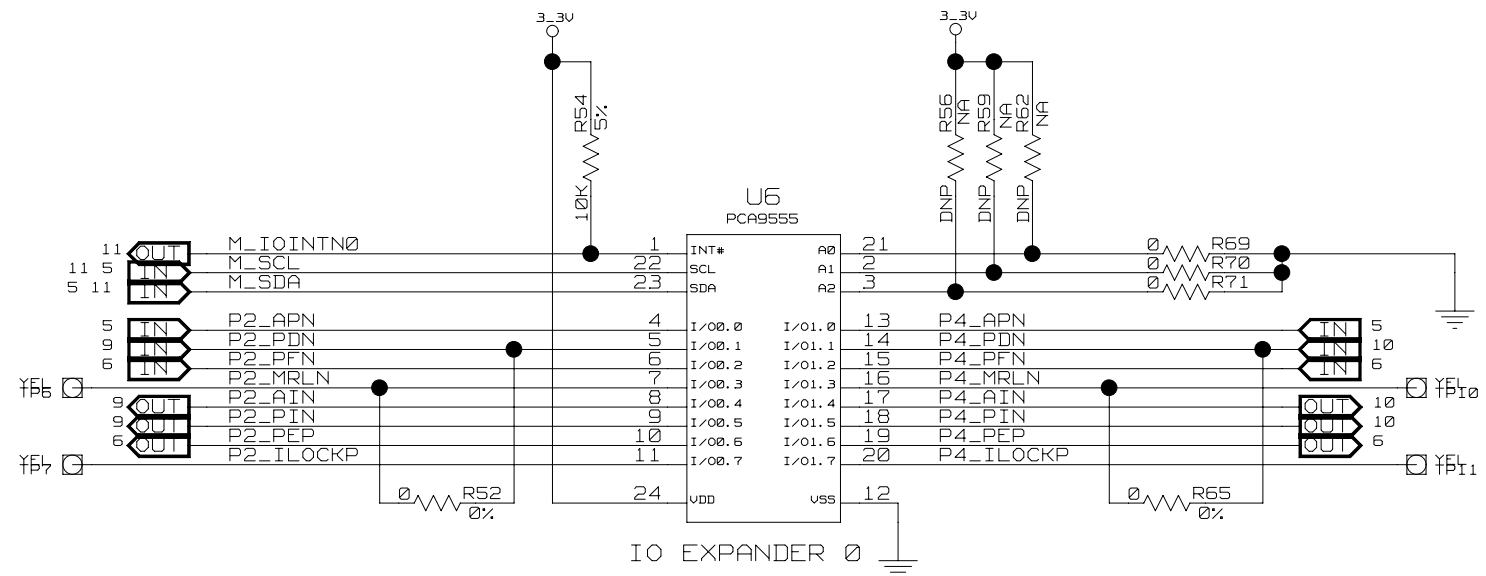
SPREAD SELECTION

S2: 4	S2: 3	SS1:SS0	SPREAD %
ON	ON	0 0	CENTER +0.25
ON	OFF	0 1	DOWN -0.5
OFF	ON	1 0	DOWN -0.75
OFF	OFF	1 1	NO SPREAD

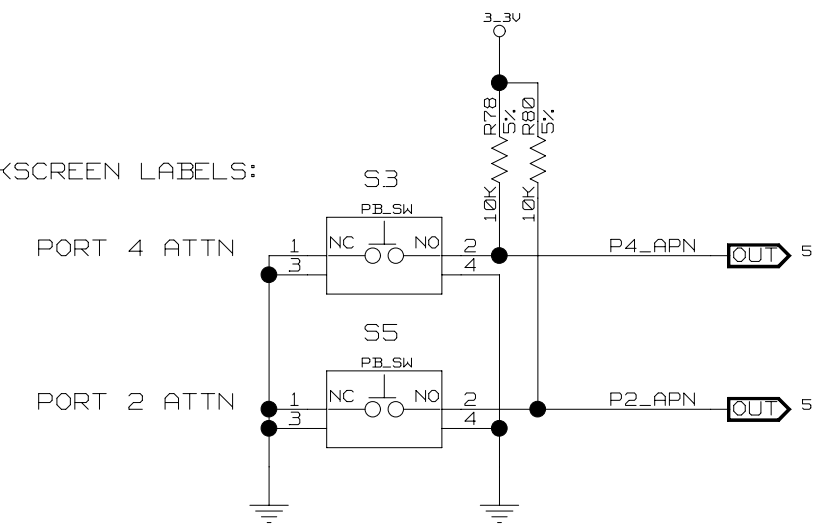


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TITLE 89EBPES12T3G2			
CLOCKS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00138	18-635-001	1.0
AUTHOR		CHECKED BY	
K. LEUNG		B. OH	
Tue Oct 02 17:11:52 2007			SHEET 4 OF 12

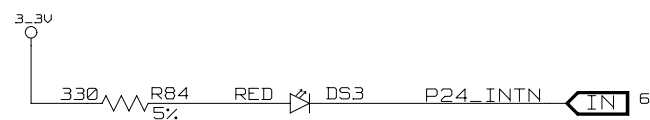
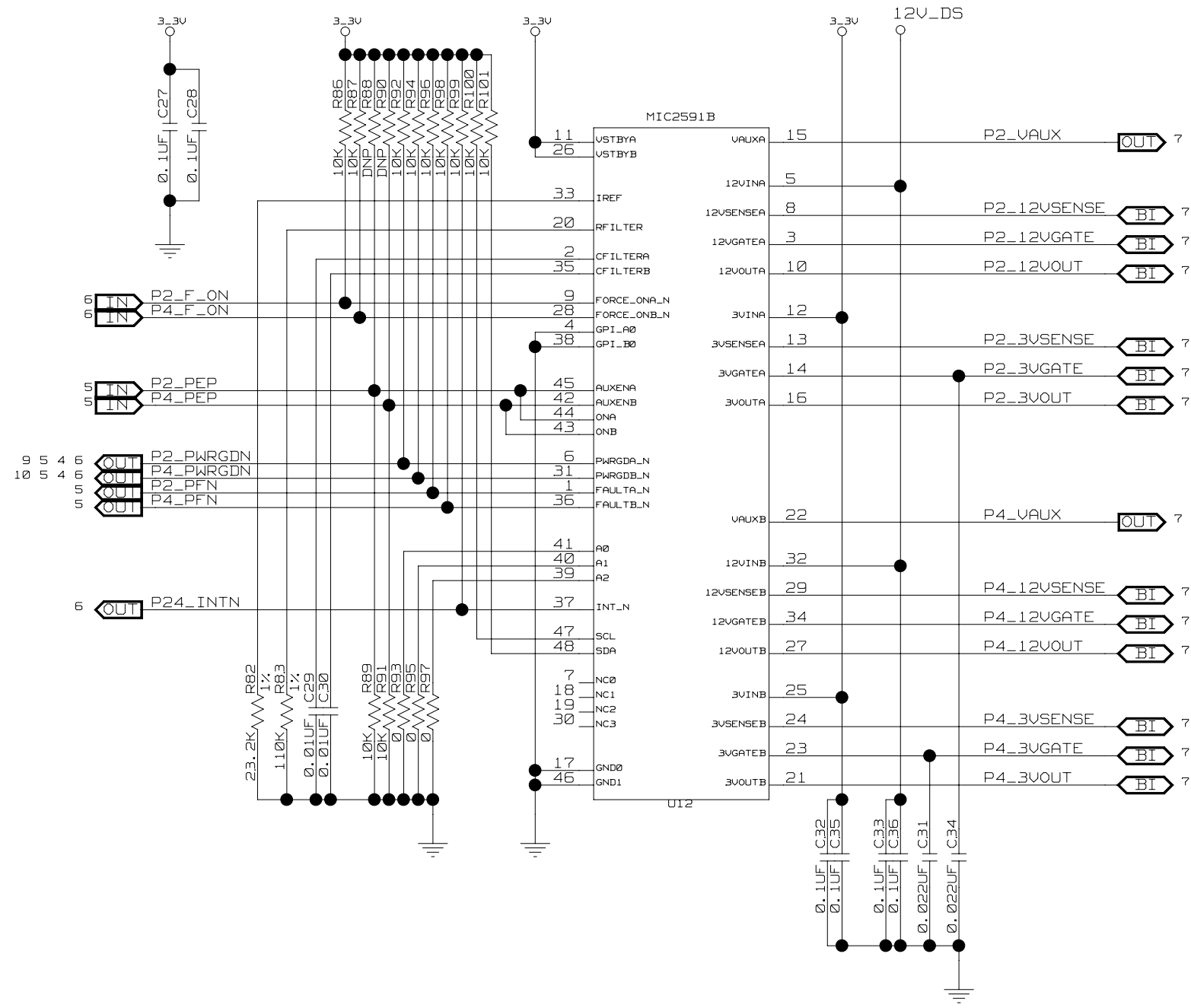


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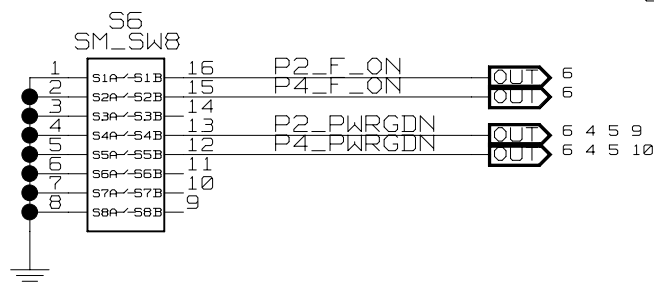


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TITLE 89EBPES12T3G2			
IO EXP, WAKE, ATTN BUTTONS			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Mon Sep 10 17:39:42 2007			SHEET 5 OF 12



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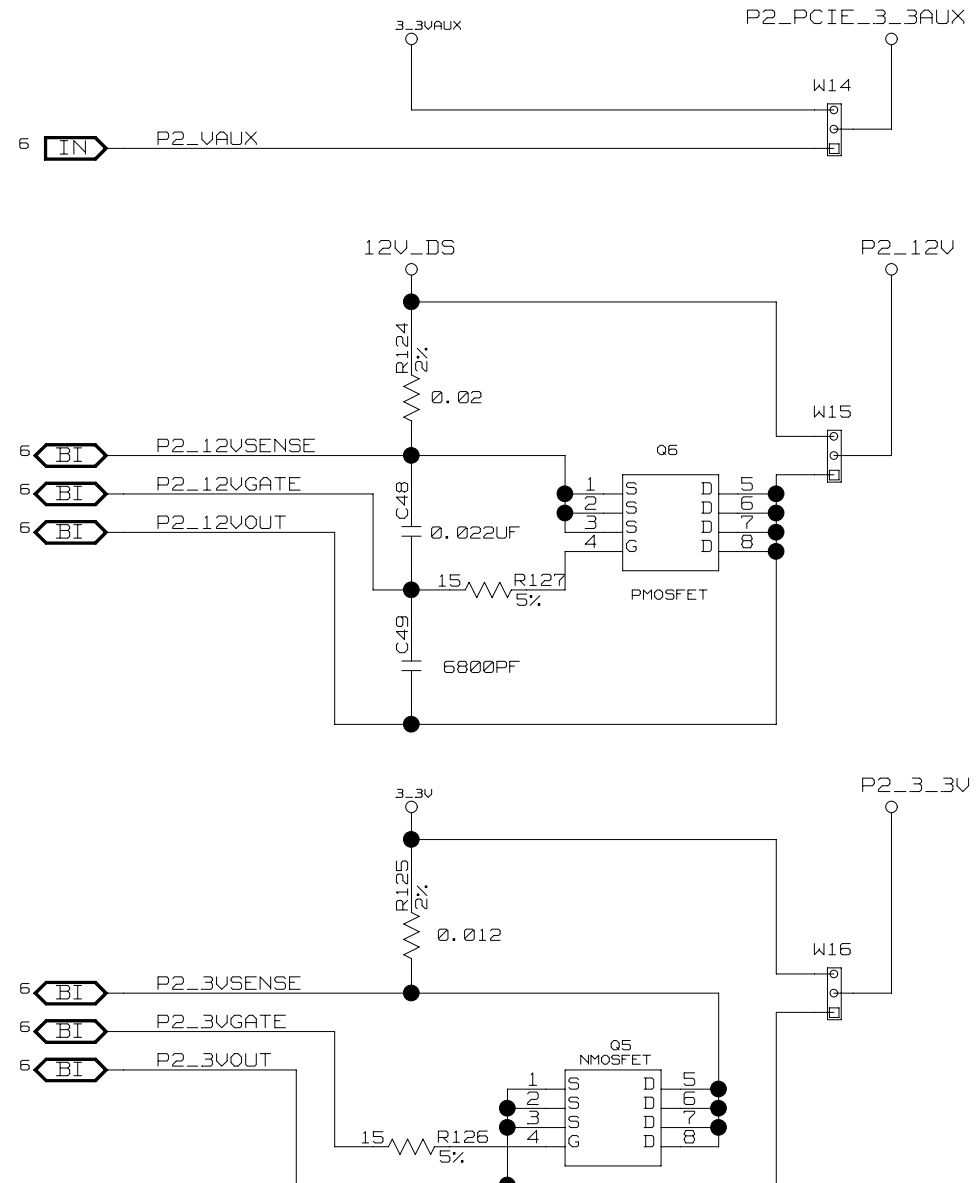
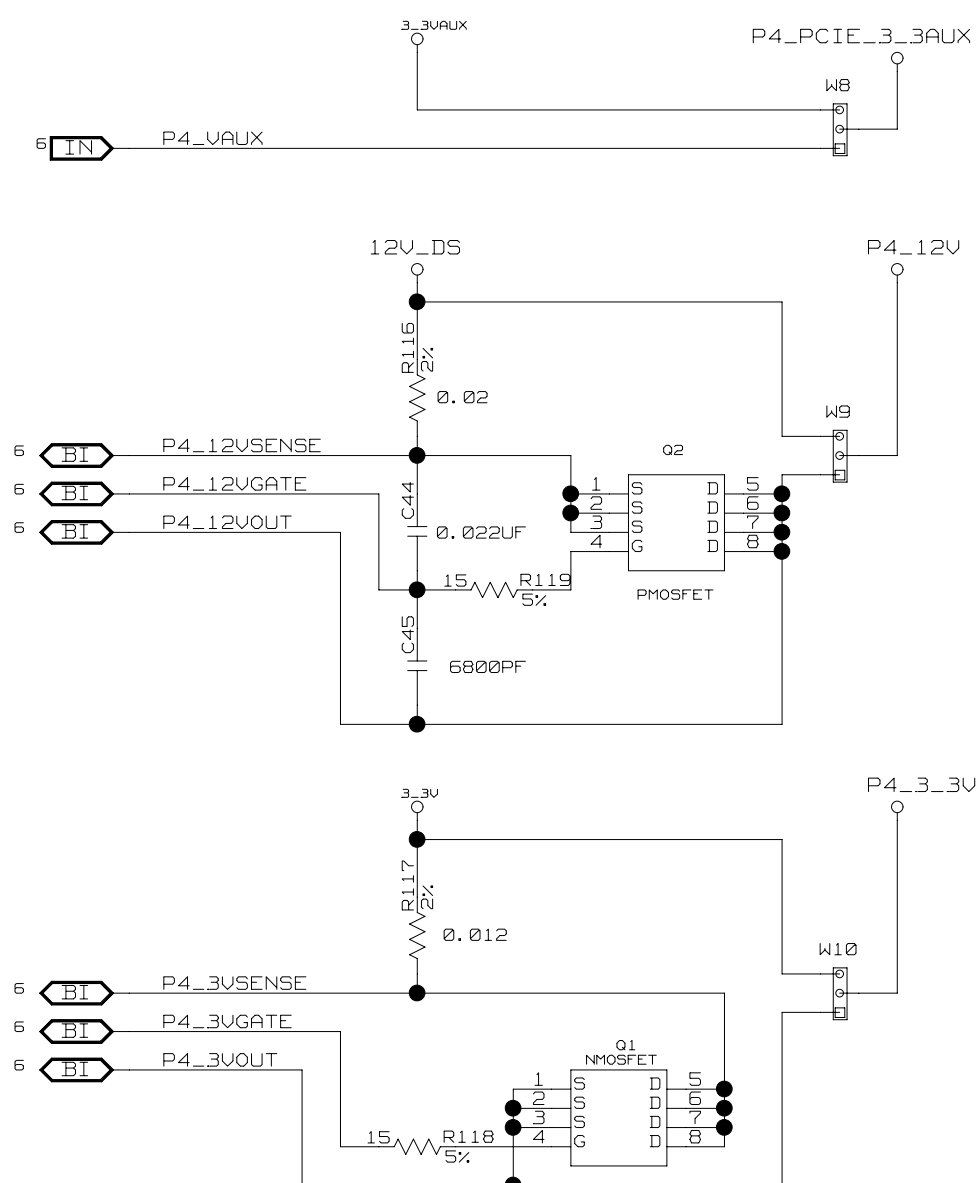


POS	DESCRIPTION
1	PORT 2 - FORCE ON
2	PORT 4 - FORCE ON
4	PORT 2 - PWR GOOD
5	PORT 4 - PWR GOOD



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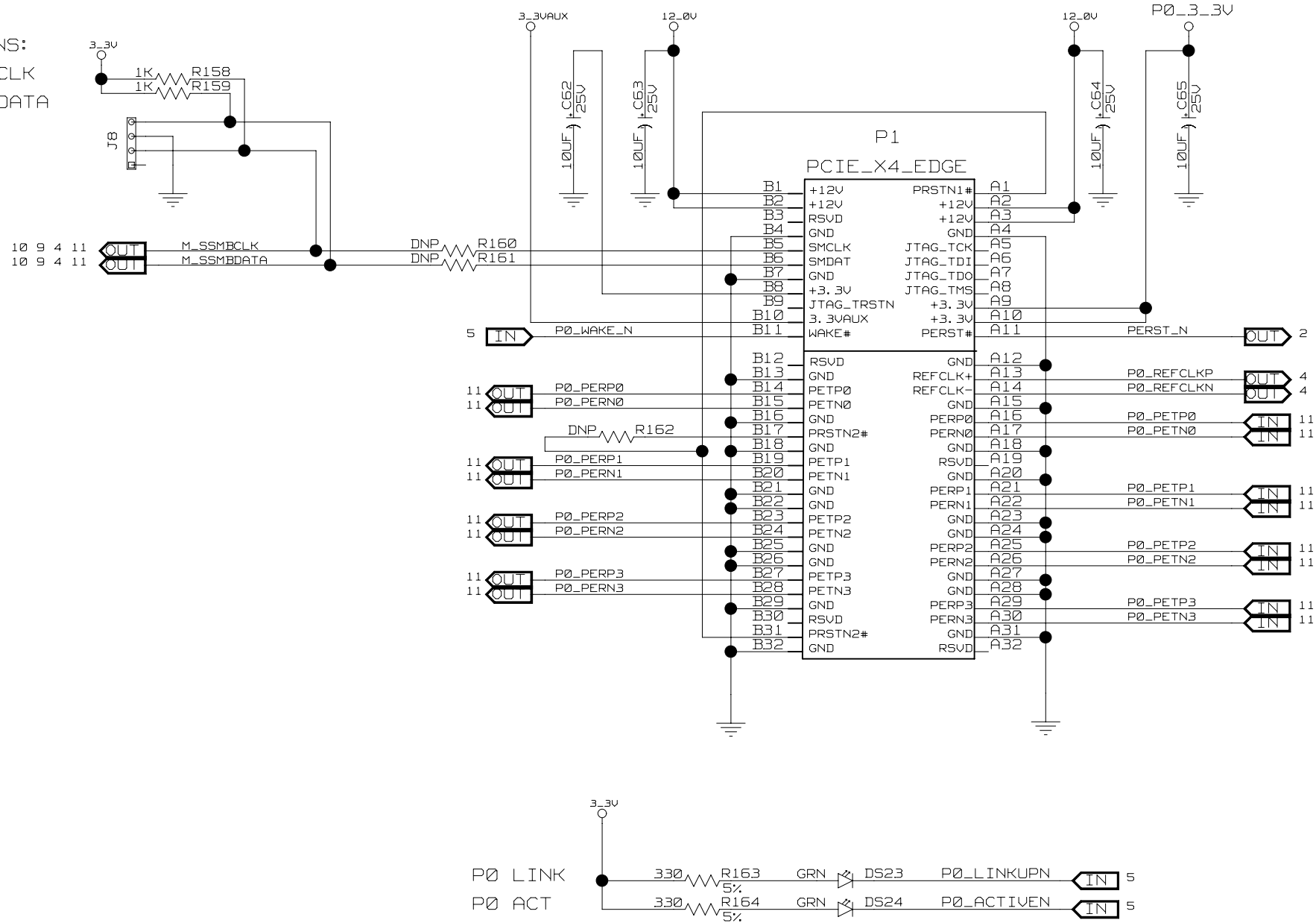
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HOT PLUG CONTROLLERS			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
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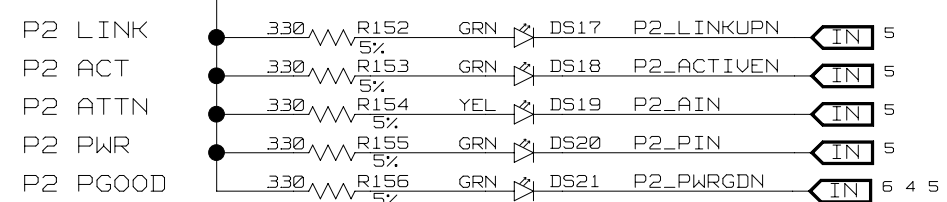
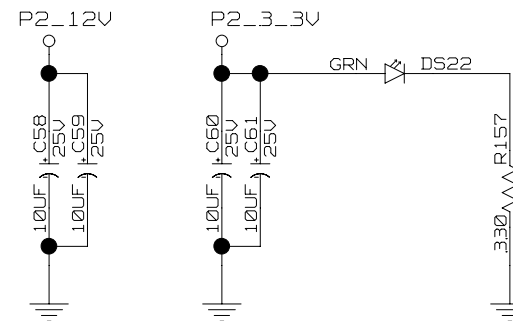
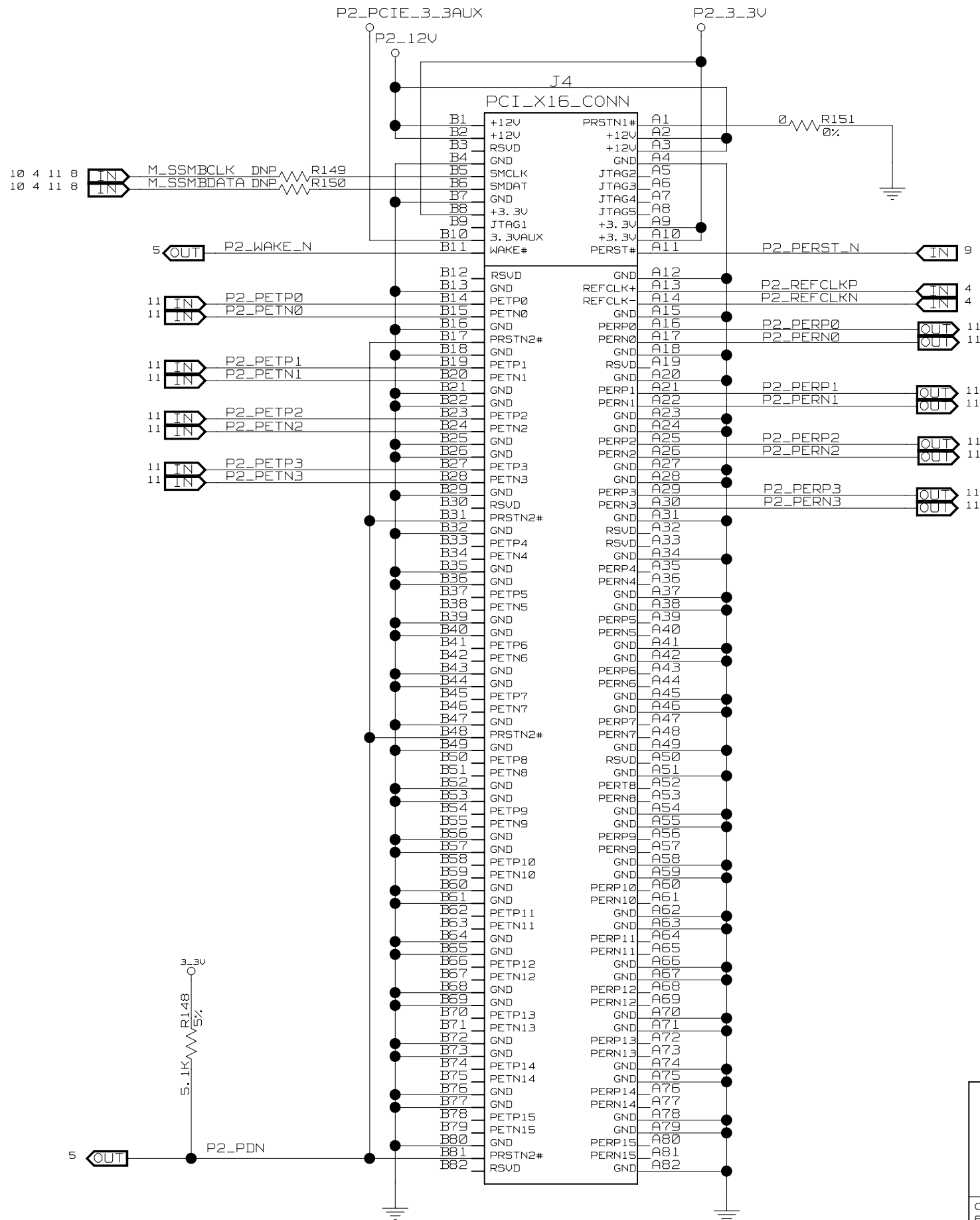
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HOT PLUG - MOSFETS			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Mon Sep 10 17:39:42 2007			SHEET 7 OF 12

LABEL PINS:
 1 3V3
 2 GND
 3 SMBCLK
 4 SMBDATA



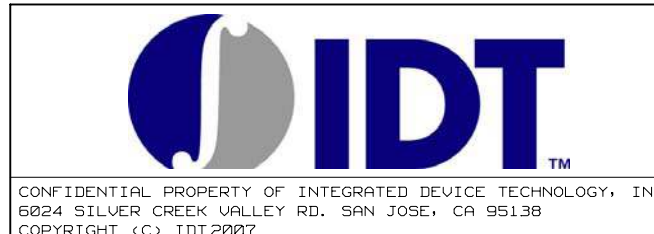
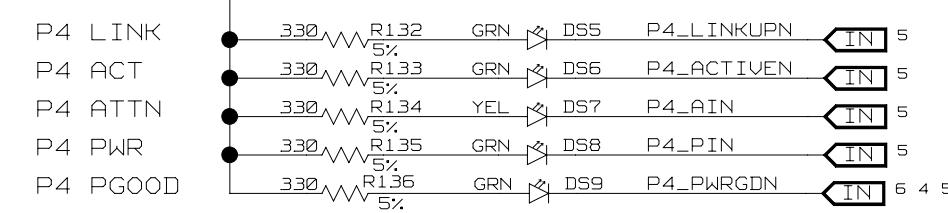
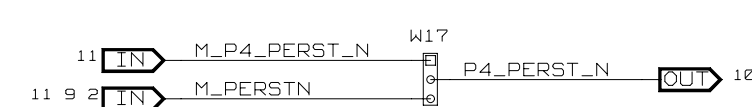
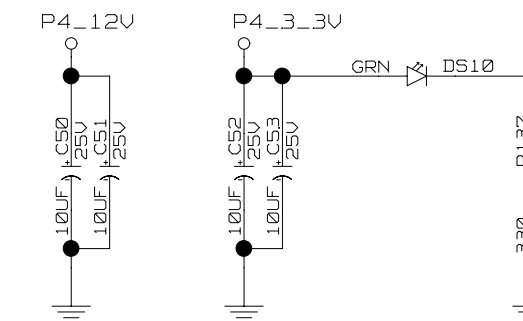
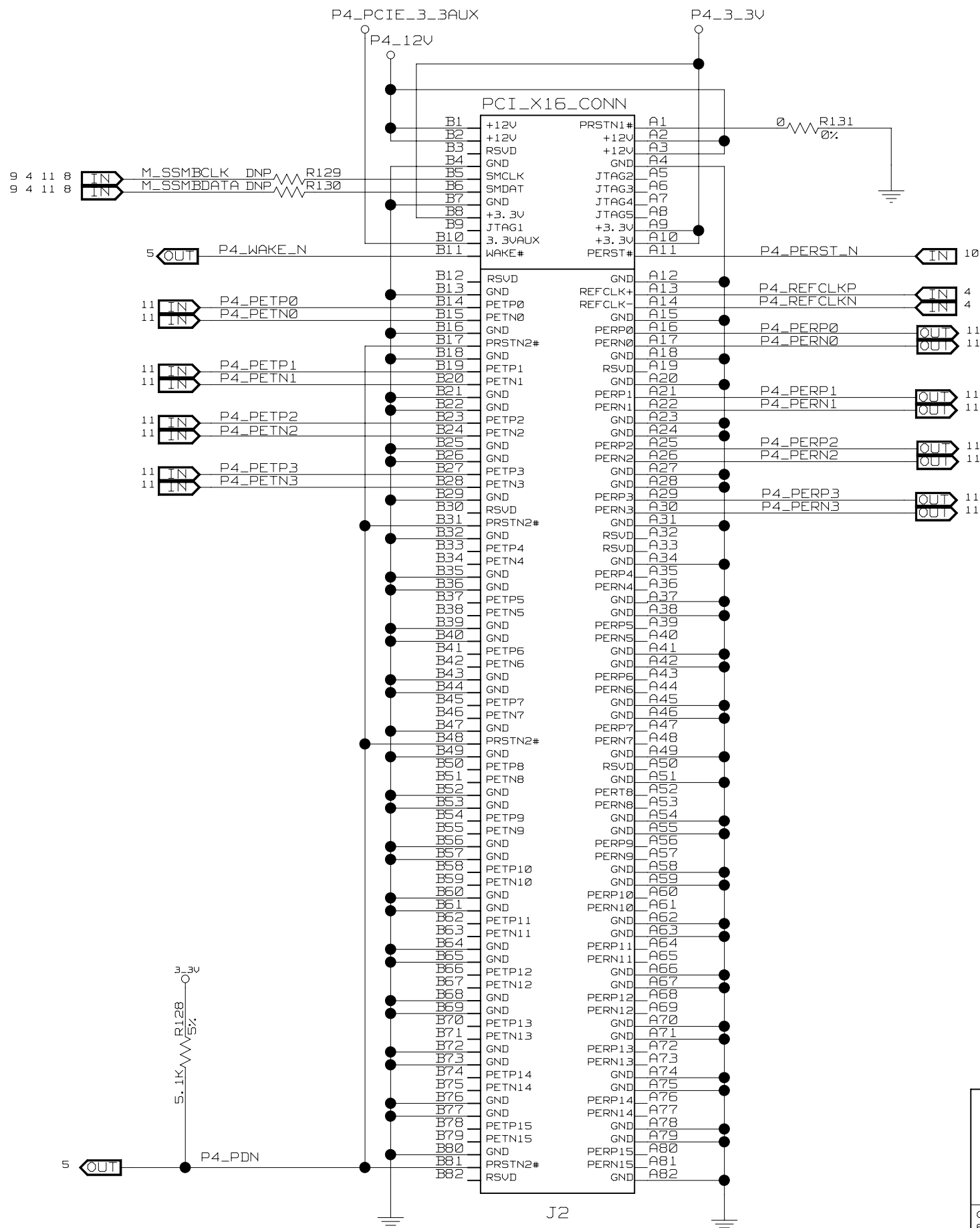
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TITLE B9EBPES12T3G2			
PORT 0 UPSTREAM EDGE CONN.			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Mon Sep 10 17:39:40 2007			SHEET 8 OF 12

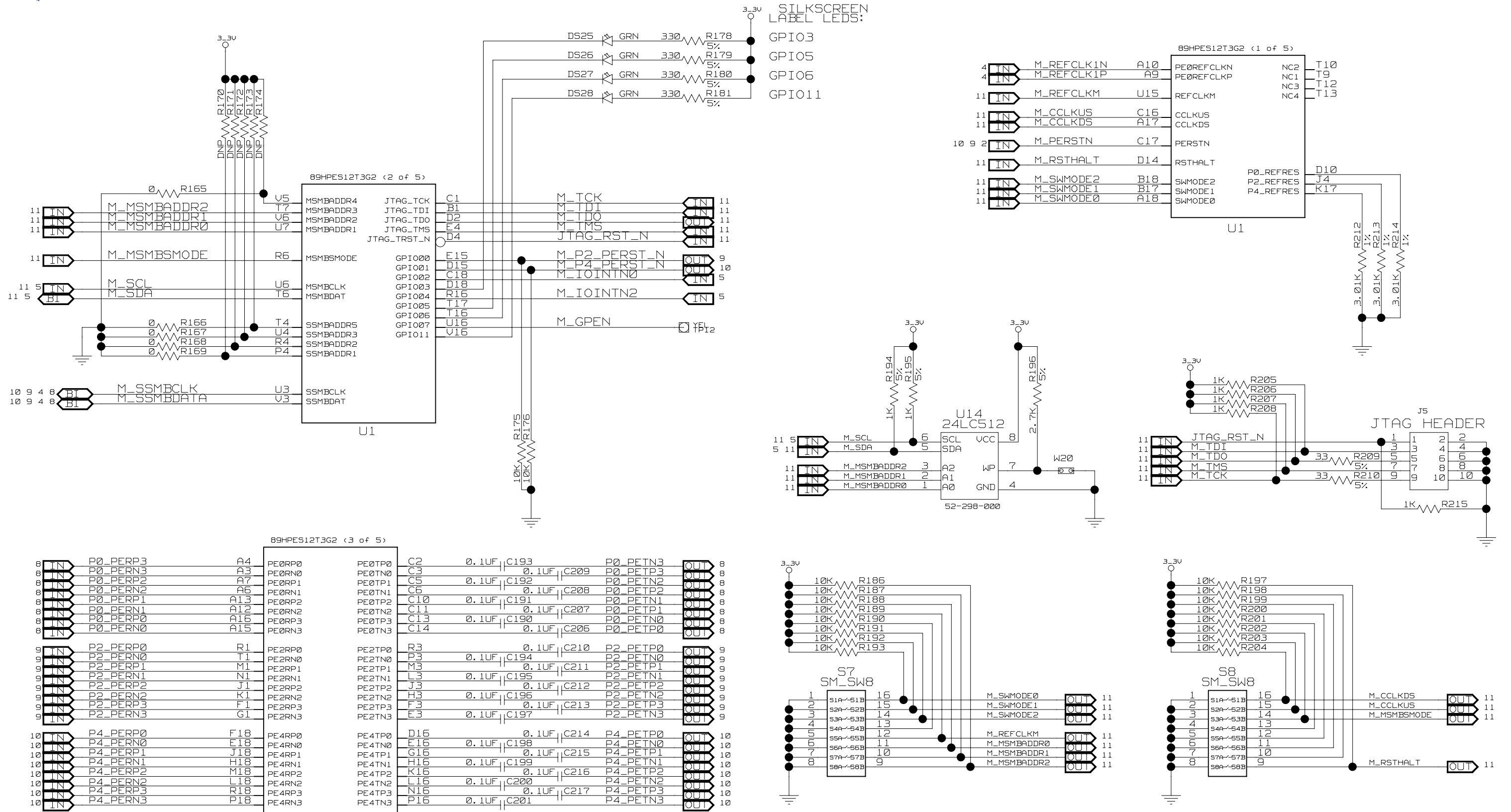



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TITLE 89EBPES12T3G2			
PORT 2 CONNECTOR			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Mon Sep 10 17:39:40 2007			SHEET 9 OF 12



TITLE 89EBPES12T3G2			
PORT 4 CONNECTOR			
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
Mon Sep 10 17:39:43 2007			SHEET 10 OF 12





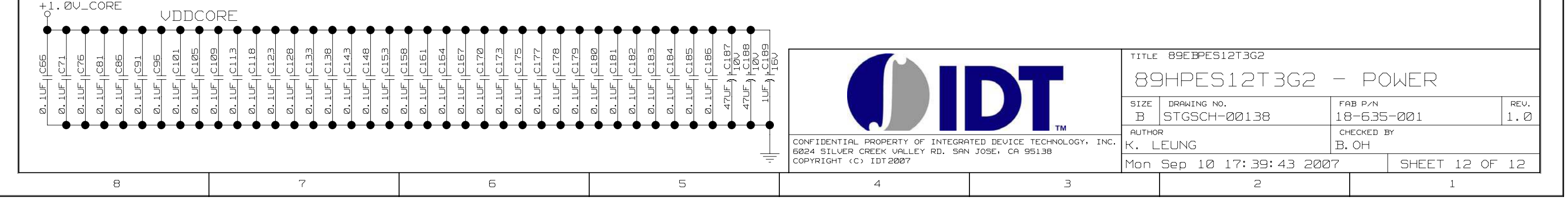
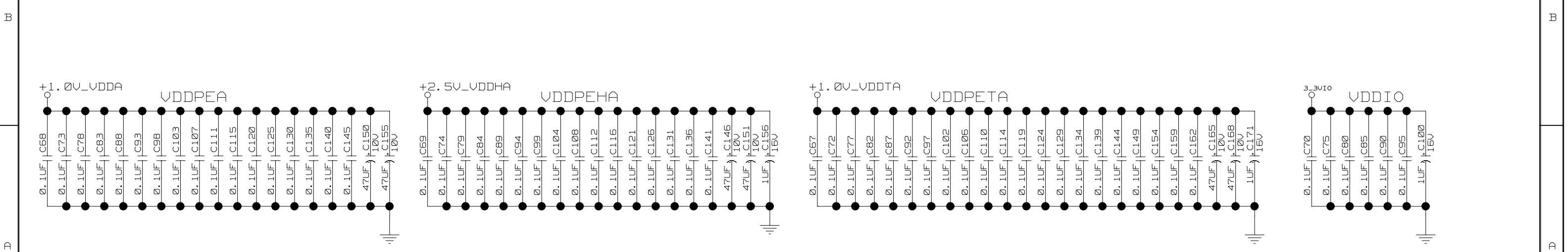
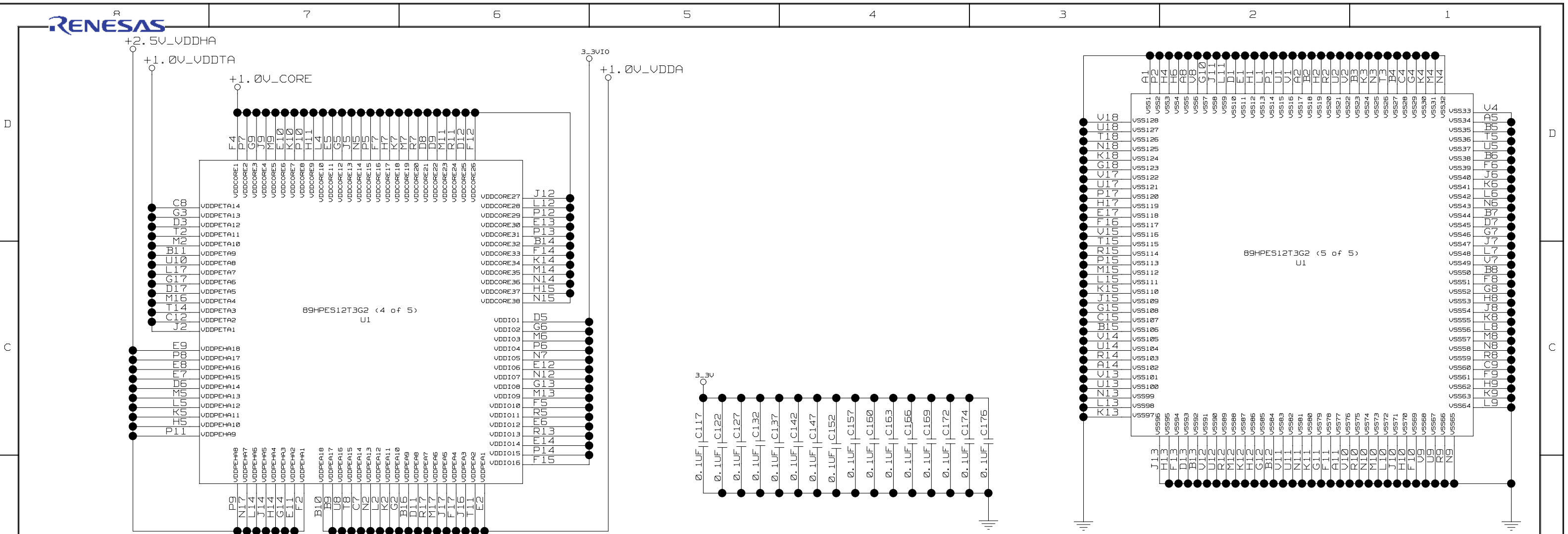
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TITLE 89HPES12T3G2

89HPES12T3G2 - EEPROM, JTAG

SIZE	DRAWING NO.	FAB P/N	REV.
B	STGSCH-00138	18-635-001	1.0
AUTHOR		CHECKED BY	
K. LEUNG		B. OH	

Mon Sep 10 17:39:41 2007



		TITLE 89HPES12T3G2	
		89HPES12T3G2 - POWER	
SIZE B	DRAWING NO. STGSCH-00138	FAB P/N 18-635-001	REV. 1.0
AUTHOR K. LEUNG		CHECKED BY B. OH	
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