Technical Specification

BMR481 series Direct Conversion Input 40-60 V, Output 0.5 V to 1.35 V up to 70 A	28701-BMR481 revF May 2022 © Flex

Key Features

- Direct Conversion 48V to 1V single stage
- High efficiency – 92% @ 1V multi-phase
- Multi-phase design – up to 6 phases @ 70A each
- Small footprint
  - Main – 27.7mm x 12mm x 14mm (1.1” x 0.47” x 0.55”)
  - Satellite – 27.7mm x 12mm x 12.6mm (1.1” x 0.47” x 0.5”)
- Fast transient response
- Meets safety requirements per IEC/EN/UL 62368-1
- PMBus 1.3 Compliant
- MTBF
  - Main – 8.7 million hours
  - Satellite – 9.7 million hours

Main

Satellite

General Characteristics

- Configurable with PMBus
- Full configuration support with Flex Power Designer
- Full featured input/output telemetry
- Configurable protections
  - OV/UV
  - Overcurrent
  - Over temperature
- Differential remote sense
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality

Safety Approvals

Design for Environment

Meets requirements in high-temperature lead-free soldering processes.

Contents

Ordering Information

Product program	Function	Output
BMR4810021/002C	Main	1 V / 70 A
BMR4810022C	Satellite	1 V / 70 A

Product number and Packaging

BMR481 $n_1n_2n_3n_4/n_5n_6n_7n_8$						
Options	n_1	n_2 n_3	n_4	/	$n_5n_6n_7$	n_8
Mounting	x			/		
Output Config		xx		/		
Functional			x	/		
Config File (Main only)				/	xxx	
Package information				/		x

Options	Description	
n_1	0 0	Main – Open Frame, LGA Satellite – Open Frame, Box Pin
n_2n_3	00	Vout = 1.0V, Iout = 70 A Vadjust range = 0.5 V to 1.35 V
n_4	1 2	Main Satellite
$n_5n_6n_7$	002	Single Main, AVSBus Vout Control
n_8	C	Antistatic tape and reel packaging

Example: An open frame Main with LGA and Vout setpoint at 1.0V configured for single module operation would be BMR481 0021/002C

1) The "Main" configuration sets all PMBus registers for proper module operation. Application specific registers can be modified to customize the configuration to meet a wide variety of performance objectives. The configuration can be changed using the PMBus communication and stored in non-volatile memory. Customized configurations can be created as orderable parts and would be defined with an individual value for $n_5n_6n_7$. The "002" part is configured for single phase operation with PMBus output voltage control. Please refer to additional details in this document for further definition of the "002" configuration.

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF= 1/λ) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Flex Power uses Telcordia SR-332 Issue 4 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 4 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ(nFailures/h)	Std. deviation, σ (nFailures/h)
Main - 104 Satellite - 93	Main – 7.8 Satellite – 7.4

Main
MTBF (mean value) for BMR481 series = 9.6 Mh
MTBF at 90% confidence level = 8.7 Mh

Satellite
MTBF (mean value) for BMR481 series = 10.7 Mh
MTBF at 90% confidence level = 9.7 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2011/65/EU and 2015/863 and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, DIBP and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex Power products are found in the Statement of Compliance document.

Flex Power fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Flex Power General Terms and Conditions of Sale.

Limitation of Liability

Flex Power does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

Safety Specification

General information

Flex Power DC/DC converters and DC/DC regulators are designed in accordance with the safety standards IEC 62368-1, EN 62368-1 and UL 62368-1 *Audio/video, information and communication technology equipment - Part 1: Safety requirements*

IEC/EN/UL 62368-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Electrically-caused fire
- Injury caused by hazardous substances
- Mechanically-caused injury
- Skin burn
- Radiation-caused injury

On-board DC/DC converters, Power interface modules and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without “conditions of acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use shall comply with the requirements in IEC/EN/UL 62368-1. Product related standards, e.g. IEEE 802.3af *Power over Ethernet*, and ETS-300132-2 *Power interface at the input to telecom equipment, operated by direct current (dc)* are based on IEC/EN/UL 60950-1 with regards to safety.

Flex Power DC/DC converters, Power interface modules and DC/DC regulators are UL 62368-1 recognized and certified in accordance with EN 62368-1. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

Isolated DC/DC converters & Power interface modules

The product may provide basic or functional insulation between input and output according to IEC/EN/UL 62368-1 (see Safety Certificate), different conditions shall be met if the output of a basic or a functional insulated product shall be considered as ES1 energy source.

For basic insulated products (see Safety Certificate) the output is considered as ES1 energy source if one of the following conditions is met:

- The input source provides supplementary or double or reinforced insulation from the AC mains according to IEC/EN/UL 62368-1.
- The input source provides functional or basic insulation from the AC mains and the product’s output is reliably connected to protective earth according to IEC/EN/UL 62368-1.

For functional insulated products (see Safety Certificate) the output is considered as ES1 energy source if one of the following conditions is met:

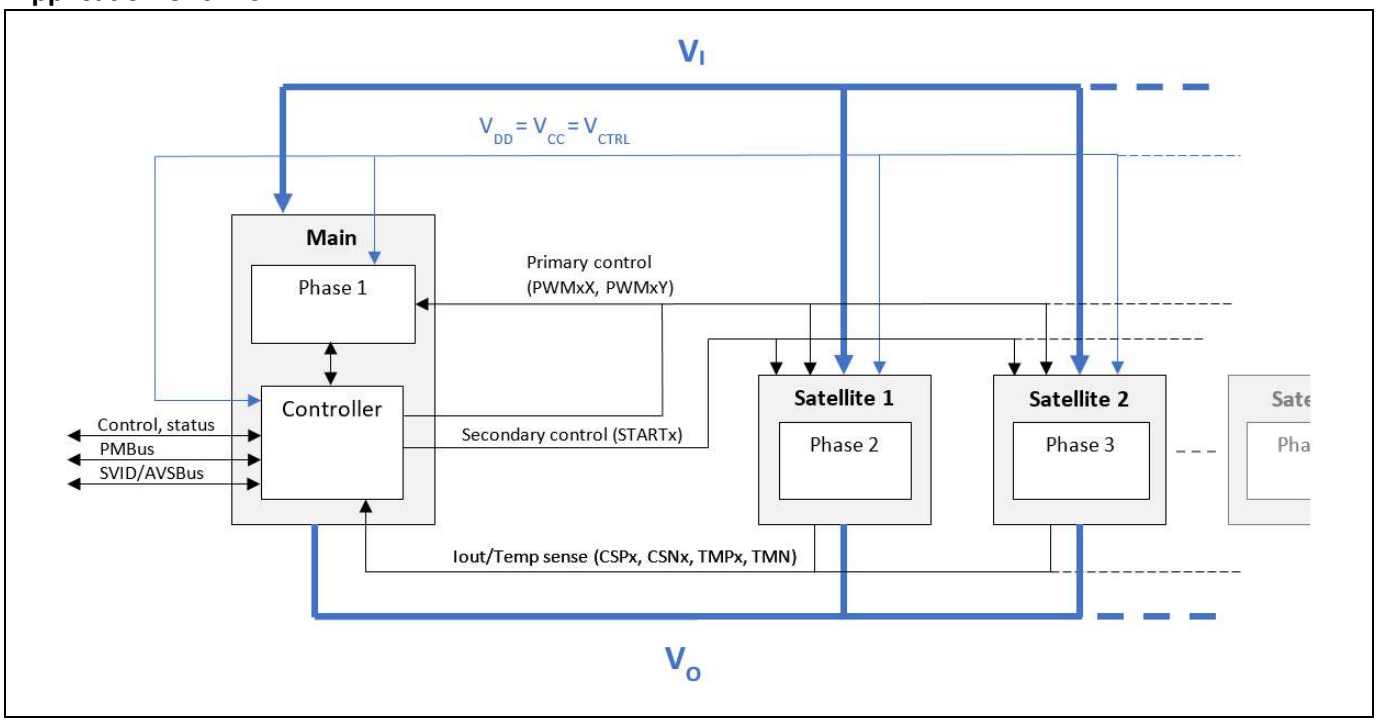
- The input source provides double or reinforced insulation from the AC mains according to IEC/EN/UL 62368-1.
- The input source provides basic or supplementary insulation from the AC mains and the product’s output is reliably connected to protective earth according to IEC/EN/UL 62368-1.
- The input source is reliably connected to protective earth and provides basic or supplementary insulation according to IEC/EN/UL 62368-1 and the maximum input source voltage is 60 Vdc.

Galvanic isolation between input and output is verified in an electric strength test and the isolation voltage (V_{iso}) meets the voltage strength requirement for basic insulation according to IEC/EN/UL 62368-1.

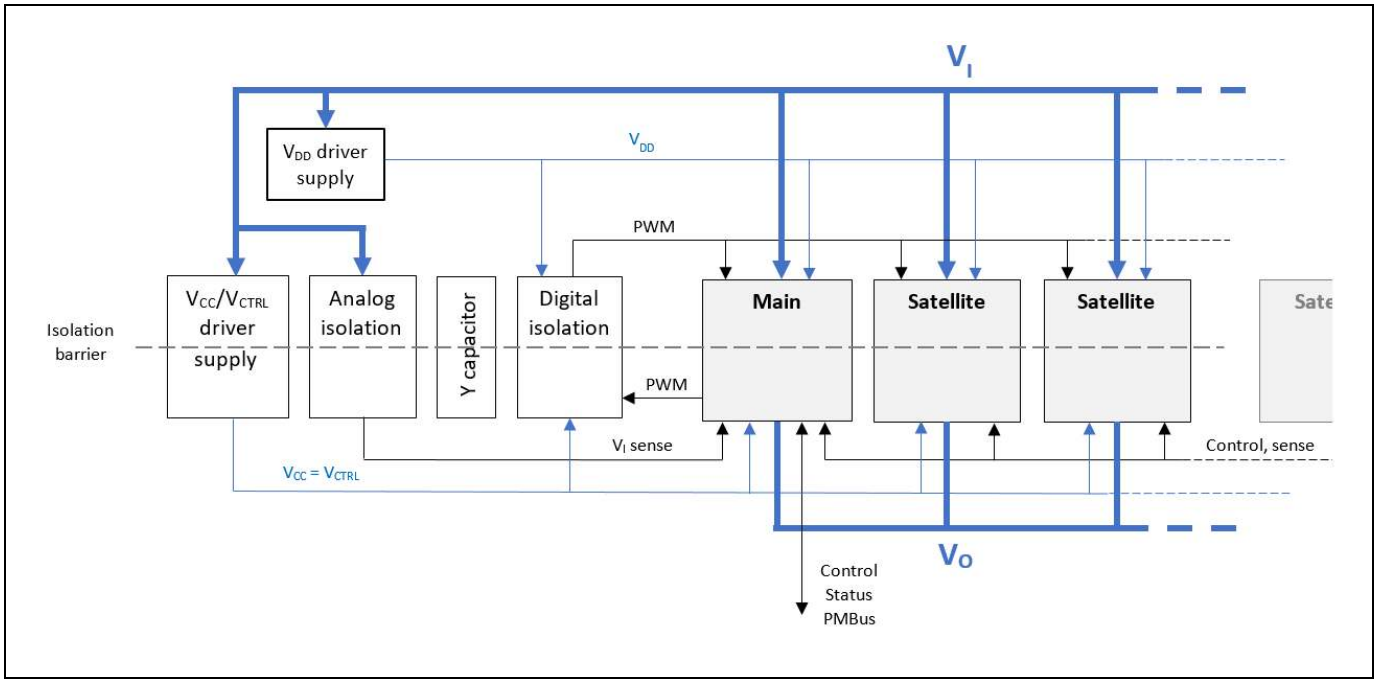
It is recommended to use a slow blow fuse at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter. In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

Application Overview

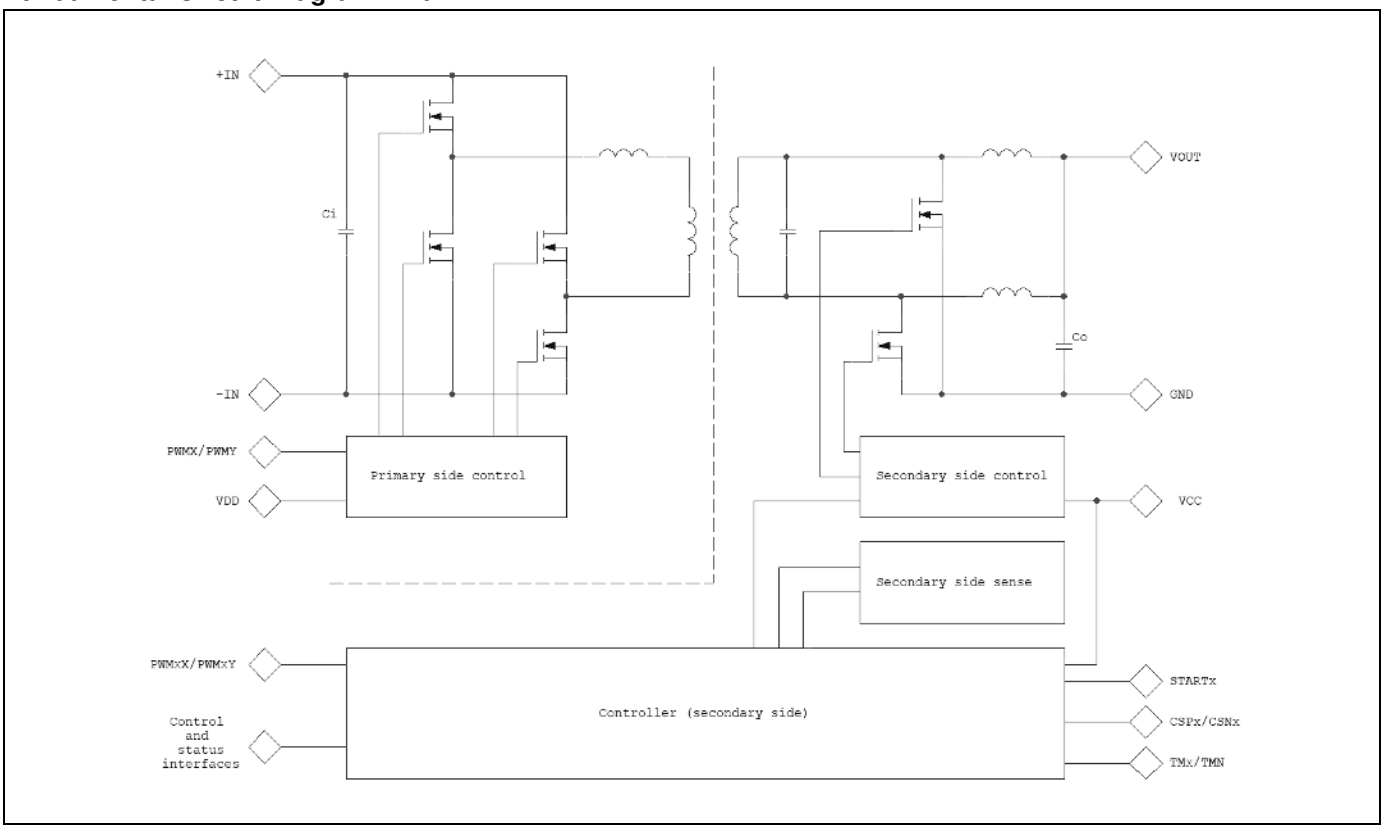


Power supply system including one Main product and 0-5 Satellite products (in total 1-6 phases). Non-isolated solution.

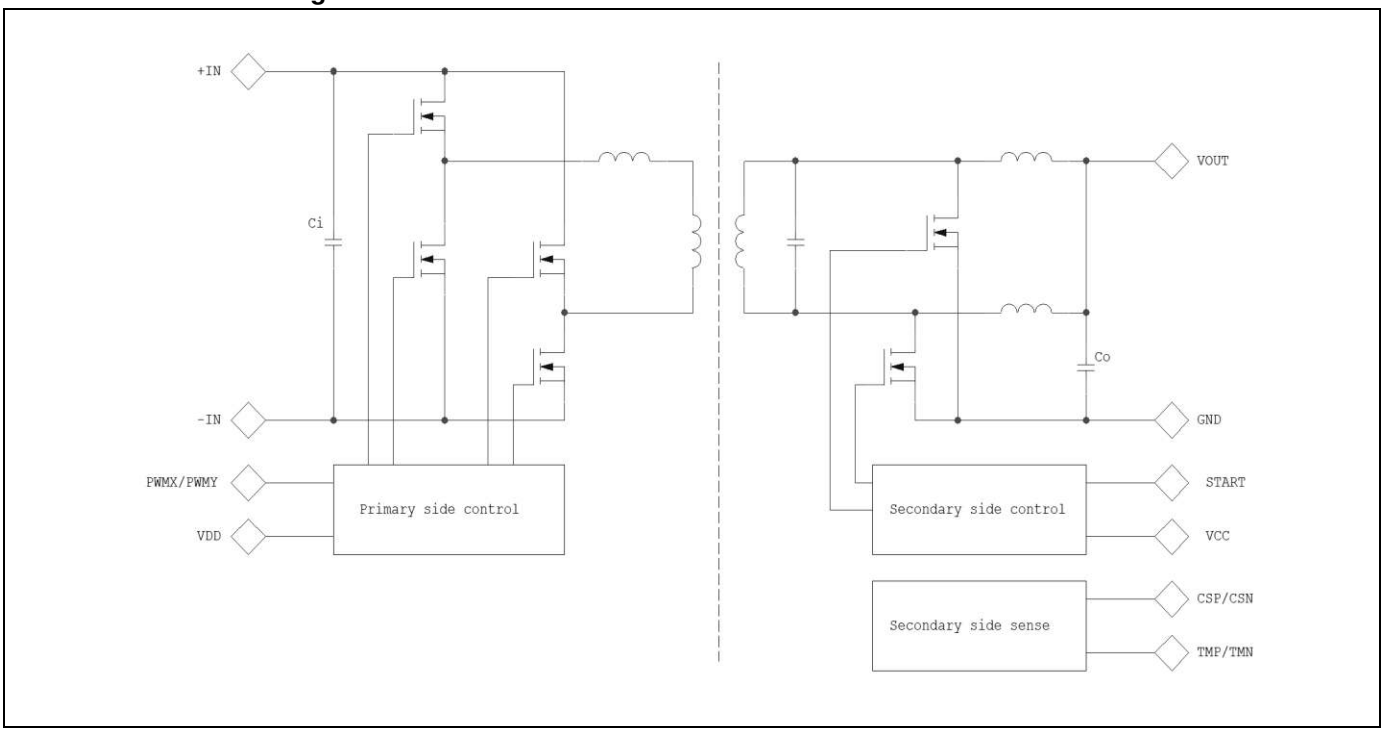


Complete isolated solution with included supplies for driver and controller voltages.

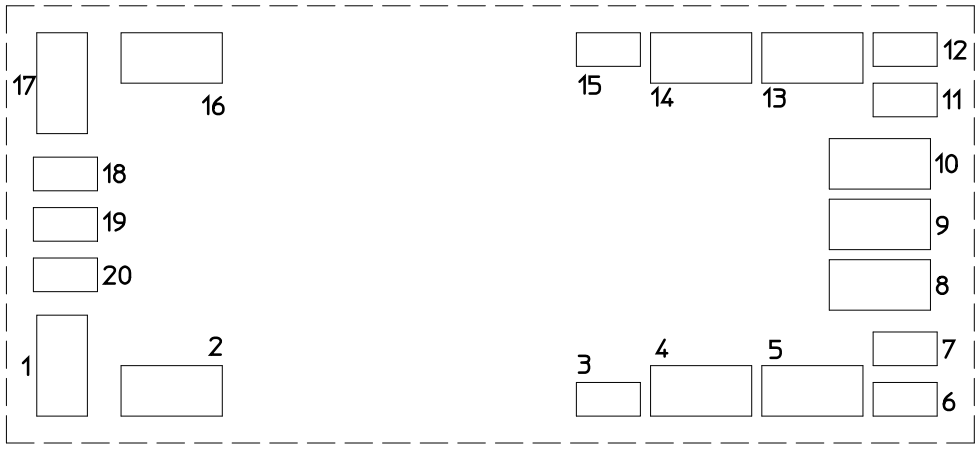
Fundamental Circuit Diagram - Main



Fundamental Circuit Diagram – Satellite



Pin-Out Description Satellite

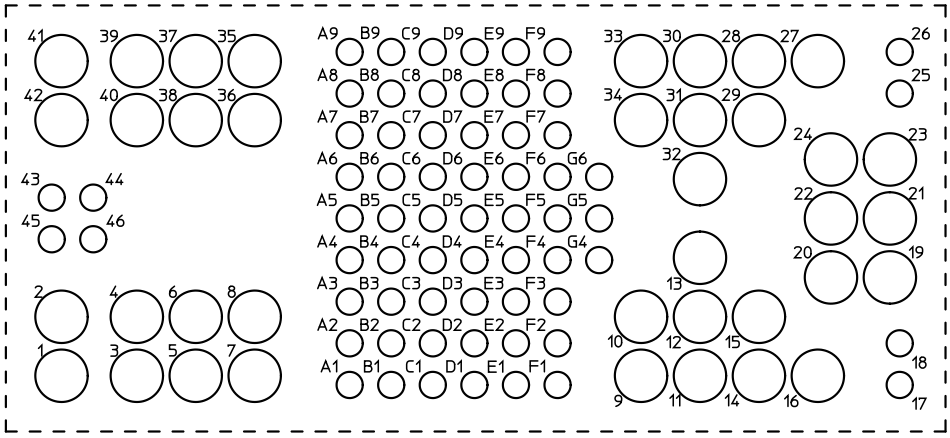


Pin layout, top view.

Pin	Designation	Type	Function
1, 17	+IN	Power	Input voltage positive.
2, 16	-IN	Power	Input voltage negative.
3	START	Input	Secondary side synchronization input. Connect to STARTx* output of Main.
4, 5, 13, 14	GND	Power	Power ground and digital ground.
6	TMN	Output	Temperature sense ground. Connect to common temperature sense ground TMN of Main.
7	TMP	Output	Temperature sense output. Connect to TMPx* input of Main.
8, 9, 10	VOUT	Power	Output voltage.
11	CSN	Output	Output current sense negative. Connect to CSNx* input of Main.
12	CSP	Output	Output current sense positive. Connect to CSPx* input of Main.
15	VCC	Power	Secondary side driver voltage supply.
18	PWMX	Input	Primary side PWM signal. Connect to PWMXx* output of Main (through digital isolator if isolation needed).
19	VDD	Power	Primary side driver voltage supply. References to -IN.
20	PWMY	Input	Primary side PWM signal. Connect to PWMYx* output of Main (through digital isolator if isolation needed).

Note 1. x = 2, 3, 4, 5 or 6 depending on satellite number in application.

Pin-Out Description Main



Pin layout, top view.

Pin	Designation	Type	Function
1, 2, 41, 42	+IN	Power	Input voltage positive.
3-8, 35-40	-IN	Power	Input voltage negative.
9-16, 27-34	GND	Power	Output voltage ground and digital ground.
17	Reserved	-	Do not connect.
18	TMP1	Input	Temperature sense input for Phase 1. Internally routed to Phase 1 power train in Main. For test purpose only. Do not connect.
19-24	VOUT	Power	Output voltage.
25	CSN1	Input	Output current sense negative for Phase 1. Internally routed to Phase 1 power train in Main. For test purpose only. Do not connect.
26	CSP1	Input	Output current sense positive for Phase 1. Internally routed to Phase 1 power train in Main. For test purpose only. Do not connect.
43	PWMX	Input	Primary side PWM signal to Phase 1 power train in Main. Connect to PWMX1 pin (through digital isolator if isolated application).
44	VDD	Power	Primary side driver voltage supply to Phase 1 power train in Main. References to -IN.
45	PWMY	Input	Primary side PWM signal to Phase 1 power train in Main. Connect to PWMY1 pin (through digital isolator if isolated application).
46	Reserved	-	Do not connect.
A1	PFAULT_IN	Output	Analog signal output for internal testing. Connect to test point or leave floating.
A2	CSP6	Input	Output current sense input positive for Phase 6. Connect to CSP output of Satellite 5. If no Satellite 5, terminate CSP6 and CSN6 to a VOUT pin.

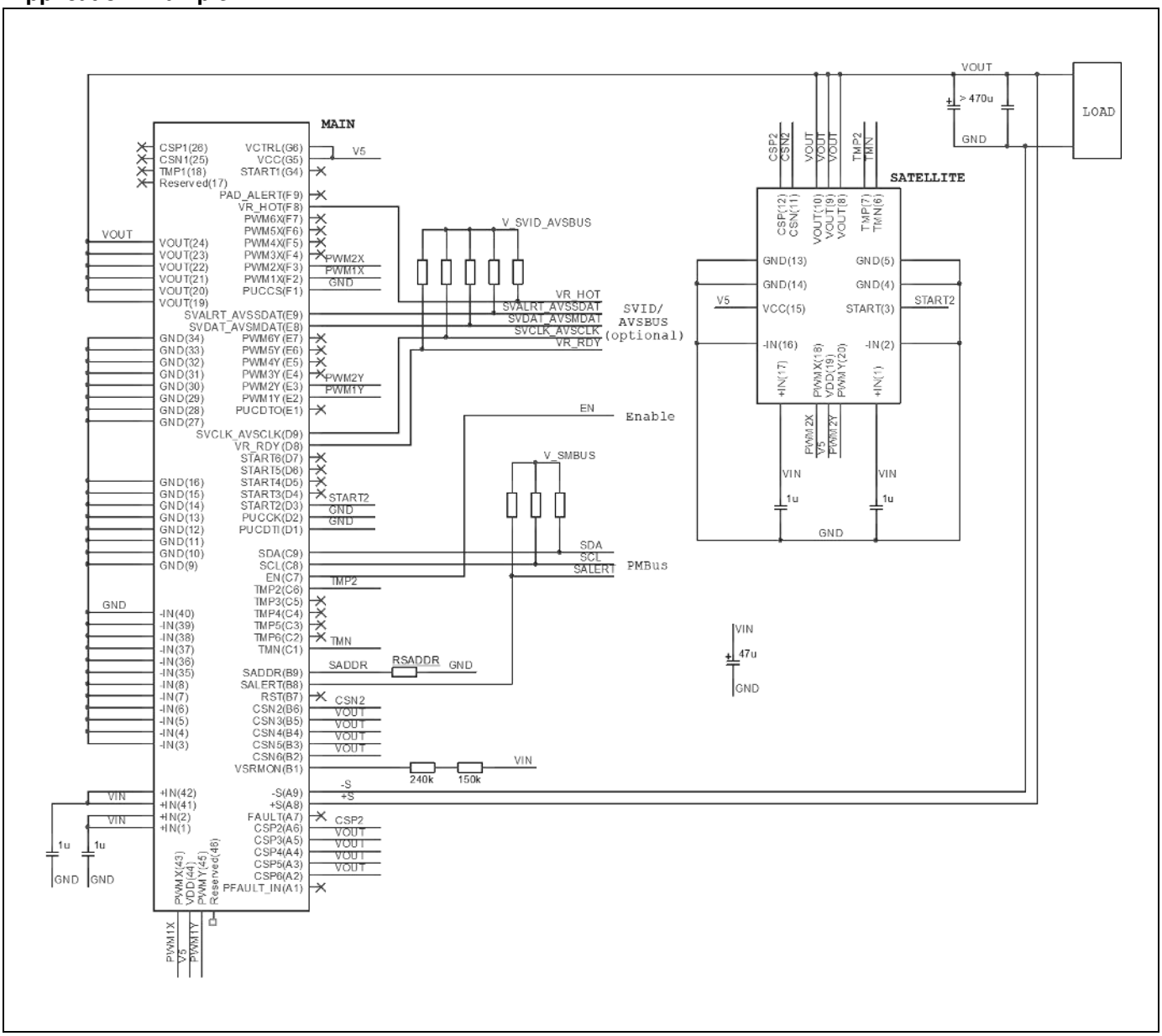
Pin	Designation	Type	Function
A3	CSP5	Input	Output current sense input positive for Phase 5. Connect to CSP output of Satellite 4. If no Satellite 4, terminate CSP5 and CSP5 to a VOUT pin.
A4	CSP4	Input	Output current sense input positive for Phase 4. Connect to CSP output of Satellite 3. If no Satellite 3, terminate CSP4 and CSN4 to a VOUT pin.
A5	CSP3	Input	Output current sense input positive for Phase 3. Connect to CSP output of Satellite 2. If no Satellite 2, terminate CSP3 and CSN3 to a VOUT pin.
A6	CSP2	Input	Output current sense input positive for Phase 2. Connect to CSP output of Satellite 1. If no Satellite 1, terminate CSP2 and CSN2 to a VOUT pin.
A7	FAULT	Output Open drain	Programmable fault indicator, active low. It is pulled low when any of the selected fault conditions are triggered. Pull-up to any external voltage equal or lower than VS. If not used leave floating.
A8	+S	Input	Output voltage positive sense. Connect to the positive side of the load to perform remote sense compensating for copper losses on the PCB. Route differentially with -S.
A9	-S	Input	Output voltage negative sense. Connect to the negative side of the load to perform remote sense compensating for copper losses on the PCB. Route differentially with +S.
B1	VSRMON	Input	Input voltage monitoring and feed forward input. See section Input Voltage Sense.
B2	CSN6	Input	Output current sense input negative for Phase 5. Connect to CSN output of Satellite 4. If no Satellite 4, terminate CSPx and CSNx together to VOUT pins. Note 1, 2
B3	CSN5	Input	Output current sense input negative for Phase 3. Connect to CSN output of Satellite 2. If no Satellite 2, terminate CSPx and CSNx together to VOUT pins. Note 1, 2
B4	CSN4	Input	Output current sense input negative for Phase 2. Connect to CSN output of Satellite 1. If no Satellite 1, terminate CSPx and CSNx together to VOUT pins. Note 1, 2
B5	CSN3	Input	Output current sense input negative for Phase 4. Connect to CSN output of Satellite 3. If no Satellite 3, terminate CSPx and CSNx together to VOUT pins. Note 1, 2
B6	CSN2	Input	Output current sense input negative for Phase 6. Connect to CSN output of Satellite 5. If no Satellite 5, terminate CSPx and CSNx together to VOUT pins. Note 1, 2
B7	RST	Input	Reset, active low. Puts the controller in the lowest power consumption state. Internally pulled high. Leave unconnected if unused.
B8	SALERT	Output Open drain	PMBus Alert. Asserted low when any of the configured protection mechanisms indicate a fault. If not used leave floating.
B9	SADDR	Input	Address setting. Connect a resistor divider to VCC5/GND in order to define PMBus and VR12.5 / VR13 addresses (if applicable). See section PMBus Interface.
C1	TMN	Input	Temperature sense input ground common for Main and Satellites. Connect to TMN of Satellites. If no Satellites, leave unconnected.
C2	TMP6	Input	Temperature sense input for Phase 6. Connect to TMP output of Satellite 5. If no Satellite 5, leave unconnected.
C3	TMP5	Input	Temperature sense input for Phase 5. Connect to TMP output of Satellite 4. If no Satellite 4, leave unconnected.
C4	TMP4	Input	Temperature sense input for Phase 4. Connect to TMP output of Satellite 3. If no Satellite 3, leave unconnected.

Pin	Designation	Type	Function
C5	TMP3	Input	Temperature sense input for Phase 3. Connect to TMP output of Satellite 2. If no Satellite 2, leave unconnected.
C6	TMP2	Input	Temperature sense input for Phase 2. Connect to TMP output of Satellite 1. If no Satellite 1, leave unconnected.
C7	EN	Input	Output voltage enable/CTRL pin. Can be left open if unused due to internal pull-up. See section Remote Control.
C8	SCL	Input	PMBus Clock. Clock for PMBus communication. Requires a pull-up resistor, also when unused. See section PMBus Interface.
C9	SDA	Input/ Output Open drain	PMBus Data. Data signal for PMBus communication. Requires a pull-up resistor, also when unused. See section PMBus Interface.
D1	PUCDTI	Input	Optional microcontroller interface chip select. 5 V compatible. Connect to GND if unused. See section PuC Interface.
D2	PUCCK	Input	Optional microcontroller interface clock. 5 V compatible. Connect to GND if unused. See section PuC Interface.
D3	START2	Output	Secondary side synchronization output for Phase 2/Satellite 1. If no Satellite 1 leave floating.
D4	START3	Output	Secondary side synchronization output for Phase 3/Satellite 2. If no Satellite 2 leave floating.
D5	START4	Output	Secondary side synchronization output for Phase 4/Satellite 3. If no Satellite 3 leave floating.
D6	START5	Output	Secondary side synchronization output for Phase 5/Satellite 4. If no Satellite 4 leave floating.
D7	START6	Output	Secondary side synchronization output for Phase 6/Satellite 5. If no Satellite 5 leave floating.
D8	VR_RDY	Output Open drain	Power good or VR ready output. Pull-up to any external voltage equal or lower than VCTRL. If not used leave floating.
D9	SVCLK_AVSCLK	Input	Optional Intel domain VR1x serial bus clock or AVSBus clock. Connect to GND if unused. See sections SVID Interface and AVSBus Interface.
E1	PUCDTO	Output	Optional microcontroller interface data output. 5 V compatible. If not used leave floating. See section PuC Interface.
E2	PWM1Y	Output	Primary side PWMY output to Phase 1. Connect to PWMY pin (through digital isolator if isolated application).
E3	PWM2Y	Output	Primary side PWMY output to Phase 2. Connect to PWMY pin of Satellite 1 (through digital isolator if isolated application). If no Satellite 1 leave floating.
E4	PWM3Y	Output	Primary side PWMY output to Phase 3. Connect to PWMY pin of Satellite 2 (through digital isolator if isolated application). If no Satellite 2 leave floating.
E5	PWM4Y	Output	Primary side PWMY output to Phase 4. Connect to PWMY pin of Satellite 3 (through digital isolator if isolated application). If no Satellite 3 leave floating.
E6	PWM5Y	Output	Primary side PWMY output to Phase 5. Connect to PWMY pin of Satellite 4 (through digital isolator if isolated application). If no Satellite 4 leave floating.
E7	PWM6Y	Output	Primary side PWMY output to Phase 6. Connect to PWMY pin of Satellite 5 (through digital isolator if isolated application). If no Satellite 5 leave floating.

Pin	Designation	Type	Function
E8	SVDAT_AVSMDAT	Input/ Output Open drain	Optional Intel domain VR1x serial bus data or AVSBus master data. Connect to GND if unused. See sections SVID Interface and AVSBus Interface.
E9	SVALRT_AVSSDAT	Output Open drain	Optional Intel domain VR1x serial bus alert or AVSBus slave data. If not used leave floating. See sections SVID Interface and AVSBus Interface.
F1	PUCCS	Input	Optional microcontroller interface chip select. 5 V compatible. Connect to GND if unused. See section PuC Interface.
F2	PWM1X	Output	Primary side PWMX output to Phase 1. Connect to PWMX pin (through digital isolator if isolated application).
F3	PWM2X	Output	Primary side PWMX output to Phase 2. Connect to PWMX pin of Satellite 1 (through digital isolator if isolated application). If no Satellite 1 leave floating.
F4	PWM3X	Output	Primary side PWMX output to Phase 3. Connect to PWMX pin of Satellite 2 (through digital isolator if isolated application). If no Satellite 2 leave floating.
F5	PWM4X	Output	Primary side PWMX output to Phase 4. Connect to PWMX pin of Satellite 3 (through digital isolator if isolated application). If no Satellite 3 leave floating.
F6	PWM5X	Output	Primary side PWMX output to Phase 5. Connect to PWMX pin of Satellite 4 (through digital isolator if isolated application). If no Satellite 4 leave floating.
F7	PWM6X	Output	Primary side PWMX output to Phase 6. Connect to PWMX pin of Satellite 5 (through digital isolator if isolated application). If no Satellite 5 leave floating.
F8	VR_HOT	Input/ Output Open drain	Intel Domain Voltage Regulator Hot, active low. Alarm signal being asserted when the temperature of one of the sensed Phases exceed the maximum programmed (TMAX). If not used leave floating.
F9	PAD_ALERT	Output Open drain	Input power sensor alert pin (pin_alert), active low. Can only be used if input power information is provided through the PuC interface. The threshold is set by command MFR_SVID_PIN_ALERT_THR. If not used leave floating.
G4	START1	Output	Secondary side synchronization output to Phase 1. Internally routed to Phase 1 in Main. For test purpose only. Do not connect.
G5	VCC	Power	Secondary side driver voltage supply to Phase 1 in Main.
G6	VCTRL	Power	Controller supply.

Note 1. x = 2, 3, 4, 5 or 6 depending on satellite number in application.
Note 2. In the layout for the termination of CSP and CSN, pay special attention and terminate at the exact same point in order to eliminate any potential voltage drop. Keep termination lines as short as possible.

Application Example



Non-isolated application with one Main and one Satellite (2 phase system).

Note 1. The optional use of SVID or AVSBus is dependent on the variant of product used and the specifications of the load. See section Additional Interfaces for more information.
Note 2. Value of output capacitance will depend on the applicaion and load transient requirements. See section External Output Capacitors.
Note 3. For PMBus pull-up resistor values, see section SMBus Interface.

Absolute Maximum Ratings

Characteristics			min	typ	max	Unit
T_{P1}	Operating temperature (see Thermal Consideration section)		-20		125	°C
T_S	Storage temperature		-40		125	°C
V_I	Input voltage (See Operating Information Section for input and output voltage relations)		-0.3		75	V
V_{DD}	Primary side driver voltage		-0.3		14	V
V_{CC}	Secondary side driver voltage		-0.3		7	V
V_{CTRL}	Secondary side controller voltage		-0.3		7	V
C_{out}	Output capacitance		470			µF
V_{iso}	Isolation voltage (input to output qualification test voltage)				1500	Vdc
V_{tr}	Input voltage transient				TBD	V
Signal I/O voltage		PWMX, PWMY (Satellite inputs, referenced to -IN)	-0.3		6	V
		CSN, CSP	-0.3		4	V
		All other	-0.3		7	V
Ground voltage differential		-S, GND	-0.3		0.3	V
Analog pin voltage		V_O, +S	-0.3		4	V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Electrical Specification section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Configuration File (Main)

The Main product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the Standard configuration, unless otherwise specified. The Standard configuration is designed for standalone Main product operation only. Changes in Standard configuration is required if adding additional external Satellites connected to the Main. Changes in Standard configuration might also be required to optimize performance in specific application.

Electrical Specification – Control and Monitoring (Main)

This section includes parameter specifications related to controller incorporated in the Main product. In the table below, PMBus commands for configurable parameters are written in capital letters.

T_{P1} = -20 °C to +95 °C, V_{CTRL} = 4.5 to 5.5 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_{CTRL} = 5.0 V, unless otherwise specified under Conditions.
Standard configuration. Single phase.

Characteristics		Conditions	min	typ Standard config.	max	Unit
T_{INIT}	Initialization Time	From V_{CTRL} > 4.2 V to ready to be enabled		12		ms
T_{ONdel}	Output voltage On Delay Time	Turn on delay duration		0		ms
		Delay duration range PMBus configurable, TON_DELAY	0		127	ms
T_{ONrise}/ $T_{OFFfall}$	Output voltage On/Off Ramp Time (0-100%-0 of V_O)	Ramp duration		1.3		ms
		Ramp duration range, PMBus configurable, DVID_SR_SLOW_STEP MFR_SVID_SLOW_SR_SELECTOR	0.02		5.1	ms
Power Good	Threshold VR_RDY pin	Rising		100		% V_O
		Falling		When output voltage disabled		
V_{Ion}	Turn-on input voltage	V_I rising threshold		0		V
	Turn-on input voltage range	PMBus configurable VIN_ON	0		60	

Characteristics		Conditions	min	typ Standard config.	max	Unit
$UVLO_{VDD}$	Under Voltage Lock-Out	V_{DD} rising threshold		4.4		V
		Hysteresis		200		mV
$UVLO_{VCC}$	Under Voltage Lock-Out	V_{CC} rising threshold		3.6	4.1	V
		Hysteresis		300		mV
$UVLO_{VCTRL}$	Under Voltage Lock-Out	V_{CTRL} rising threshold		4.2	4.3	V
		Hysteresis		500		mV
Remote Sense Protection	Threshold	+S vs VOUT pin		700		mV
		-S vs GND pin		500		mV
Input Under Voltage Protection, IUVP	Threshold			35		V
	Threshold range	PMBus configurable VIN_UV_FAULT_LIMIT	0		60	V
	Set point accuracy			125		mV
	Fault response	VIN_UV_FAULT_RESPONSE		Ignore (0x00)		
Input Over Voltage Protection, IOVP	Threshold			65		V
	Threshold range	PMBus configurable VIN_OV_FAULT_LIMIT	0		70	V
	Set point accuracy			125		mV
	Response time				400	us
	Fault response	VIN_OV_FAULT_RESPONSE		Latch (0x80)		
Input Peak Protection	Threshold	VSRMON pin		3.045		V
Output voltage Under Voltage Protection, UVP	Offset threshold			150		mV
	Offset threshold range	PMBus configurable VOUT_UV_FAULT_LIMIT	50		400	mV
	Fault response	VOUT_UV_FAULT_RESPONSE		Latch (0x80)		
Output voltage Over Voltage Protection, OVP	Offset threshold			150		mV
	Offset threshold range	PMBus configurable VOUT_OV_FAULT_LIMIT	50		400	mV
	Response time			90		ns
	Fault response	VOUT_OV_FAULT_RESPONSE		Latch (0x80)		
Over Current Protection, OCP	Peak OCP threshold	Set value		86		A
	Peak OCP threshold range	PMBus configurable MFR_IMON, TEL_IOUT_FSR	0		600	A
	Peak OCP response time			150		ns
	Average OCP threshold	Set value		80		A
	Average OCP threshold range	PMBus configurable IOUT_OC_FAULT_LIMIT	0		500	A
	Average OCP warning threshold	Set value		75		A
	Average OCP warning threshold range	PMBus configurable IOUT_OC_WARN_LIMIT	0		500	A
	Response time				400	us
	Fault response	IOUT_OC_FAULT_RESPONSE		Latch (0x80)		
Over Temperature Protection, OTP	Threshold			130		°C
	Threshold range	PMBus configurable OT_FAULT_LIMIT	25		130	°C
	Warning threshold	PMBus configurable		115		°C
	Response time				400	us
	Fault response	OT_FAULT_RESPONSE		Latch (0x80)		
Monitoring accuracy	Input voltage	READ_VIN, V_I = 53 V		0.25		V
	Output voltage	READ_VOUT, V_O = 1.0 V		2.5		mV
	Output current	READ_IOUT, V_O = 1.0 V, V_I = 40-60 V, I_O > (0.25 x max I_O)		3		% of value
	Temperature	READ_TEMPERATURE, T_{READ} = 8 to +100 °C		3		°C

Characteristics		Conditions	min	typ Standard config.	max	Unit
V_{SENSE}	Input resistance	+S/-S		64		kΩ
	Internal resistance to VOUT/GND			1		kΩ
V_{IL}	Logic input low threshold	SCL, SDA			1.4	V
		SVDAT_AVSMDAT, SVCLK_AVSCLK			0.45	V
		PUCCS, PUCDTI, RST			1.5	V
		EN			0.4	V
V_{IH}	Logic input high threshold	SCL, SDA	1.8			V
		SVDAT_AVSMDAT, SVCLK_AVSCLK	0.65			V
		PUCCS, PUCDTI, RST	1.7			V
		EN	0.7			V
R_{LO}	Logic output low resistance @ 5 mA	SDA, SALERT			25	Ω
		SVDAT_AVSMDAT, SVALRT_AVSSDAT, PIN_ALERT, VR_HOT, VR_RDY			13	Ω
		FAULT			45	Ω
V_{OL}	Logic output low signal level	PUCDO @ 5 mA		125	250	mV
V_{OH}	Logic output high signal level	PUCDO @ 1 mA	4.5			V
I_{OL}	Logic output low sink current	Open drain outputs			20	mA
I_{I_LEAK}	Logic input leakage current				1	uA
C_{I_PIN}	Logic input capacitance			10		pF
R_{I_PU}	Internal pull-up resistance to V_{CTRL}	SCL, SDA, SALERT, SVCLK_ASCLK, SVDAT_AVSMDAT, SVALRT_AVSSDAT		No internal pull-up		
		EN, RST		10		kΩ
R_{I_PD}	Internal pull-down resistance	VSRMON		10		kΩ
f_{SMB}	SMBus Operating frequency		10		400	kHz
T_{BUF}	SMBus Bus free time	STOP bit to START bit See section SMBus – Timing	1.3			µs
t_{set}	SMBus SDA setup time from SCL	See section SMBus – Timing	100			ns
t_{hold}	SMBus SDA hold time from SCL	See section SMBus – Timing	300			ns

Electrical Specification – Main / Satellite

BMR 481 002x (1.0V)

T_{P1} = -20 °C to +95 °C, V_I = 40 to 60 V, V_{DD} = V_{CC} = V_{CTRL} = 5.0 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 53 V, V_O = 1.0 V, max I_O, unless otherwise specified under Conditions.
Measurements made on Reference board ROA 170 014 P5A. Standard configurations used.
External C_{IN} = 1 x 47 µF OSCON (2 x 47 µF for multiphase) + 2 x 1 µF ceramic for each Main or Satellite.
External C_{OUT} = 1 x 470 µF/3 mΩ POSCAP (5 x 470 µF for multiphase) + 20 x 10 µF ceramic.

Characteristics		Conditions	min	typ Standard config.	max	Unit
V_I	Input supply		40		60	V
V_{DD}	Primary side driver supply		4.75	5	13	V
V_{CC}	Secondary side driver supply		4.5	5	5.5	V
V_{CTRL}	Controller supply		4.5	5	5.5	V
V_O	Default output voltage			1.0		V
	Output voltage adjustment range		0.5		1.35	V
	Output voltage set-point resolution			5		mV
	Output voltage accuracy (including line, load, temp.)	V_O ≤ 1.0 V		10		mV
		V_O > 1.0 V		1		% V_O
	Line regulation			1		mV
	Load regulation	I_O = 0 - 100%		1		mV
V_{Oac}	Output ripple & noise	V_O = 1.0 V, 20 MHz BW		2		mVp-p
f_{SW}	Switching frequency	T_{P1} = +25 °C, Note 1	520	730	1120	kHz
C_I	Main / Satellite internal input cap.	V_I = 0 V		600		nF
C_O	Main / Satellite internal output cap.	V_O = 0 V		300		µF

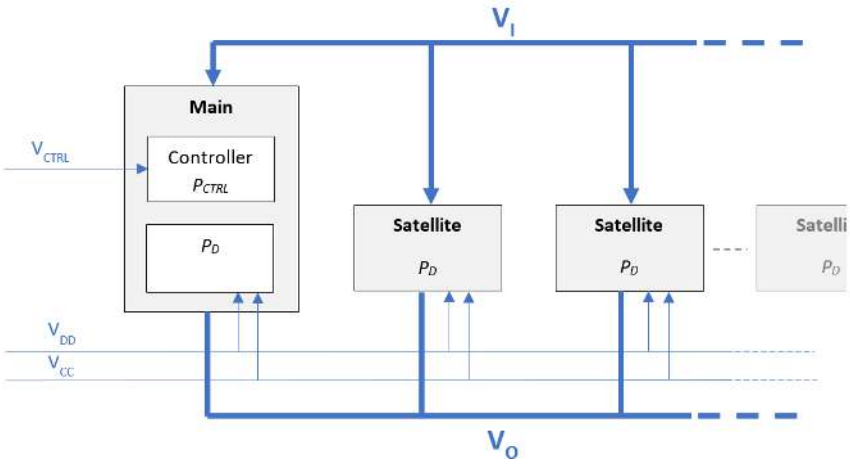
I_O	Output current (Main / Satellite)		V_O ≤ 1.0 V	0	70	A
			V_O > 1.0 V	See Output Current Capability graph		

η	Efficiency Main only Note 2	Peak value	V_O = 1.0 V	91.6		%
		I_O = max I_O	V_O = 1.0 V	88.8		%
P_D	Power dissipation Main only Note 2	I_O = max I_O	V_O = 1.0 V	8.8		W
		No load	V_O = 1.0 V	1.7		W

η	Efficiency Main + 5 Satellites Note 2	Peak value	V_O = 1.0 V	92.0		%
		I_O = max I_O	V_O = 1.0 V	89.2		%
P_D	Power dissipation Main + 5 Satellites Note 2	I_O = max I_O	V_O = 1.0 V	50		W
		No load	V_O = 1.0 V	1.9		W

P_{CTRL}	Controller power dissipation (Main)		Phase 1 active only	450		mW
			For each added phase	12		mW
I_{VDD}	VDD input current (Main / Satellite)		For each active phase V_O = 1.0 V	20 For V_O ≠ 1.0 V, see graphs	22	mA
			For each inactive phase	6		mA
I_{VCC}	VCC input current (Main / Satellite)		For each active phase V_O = 1.0 V	60 For V_O ≠ 1.0 V, see graphs	63	mA
			For each inactive phase	1		mA
I_{VCTRL}	VCTRL input current (Main)		Phase 1 active only	90	100	mA
			For each added phase	2.4		mA
			Turned off with EN pin	70		mA
			RST de-asserted	10		mA

Note 1. Measurement from single unit.
Note 2. Including V_{CC}/V_{DD} driver losses. Excluding controller power dissipation P_{CTRL}. See figure below.



Driver losses included, controller losses excluded:

$$P_D = V_I I_{VI} + V_{DD} I_{VDD} + V_{CC} I_{VCC} - V_O I_O$$

$$\eta = \frac{V_O I_O}{P_D + V_O I_O}$$

Driver and controller losses included:

$$P_{TOT} = P_D + P_{CTRL}$$

$$\eta_{TOT} = \eta \frac{P_D + V_O I_O}{P_D + P_{CTRL} + V_O I_O}$$

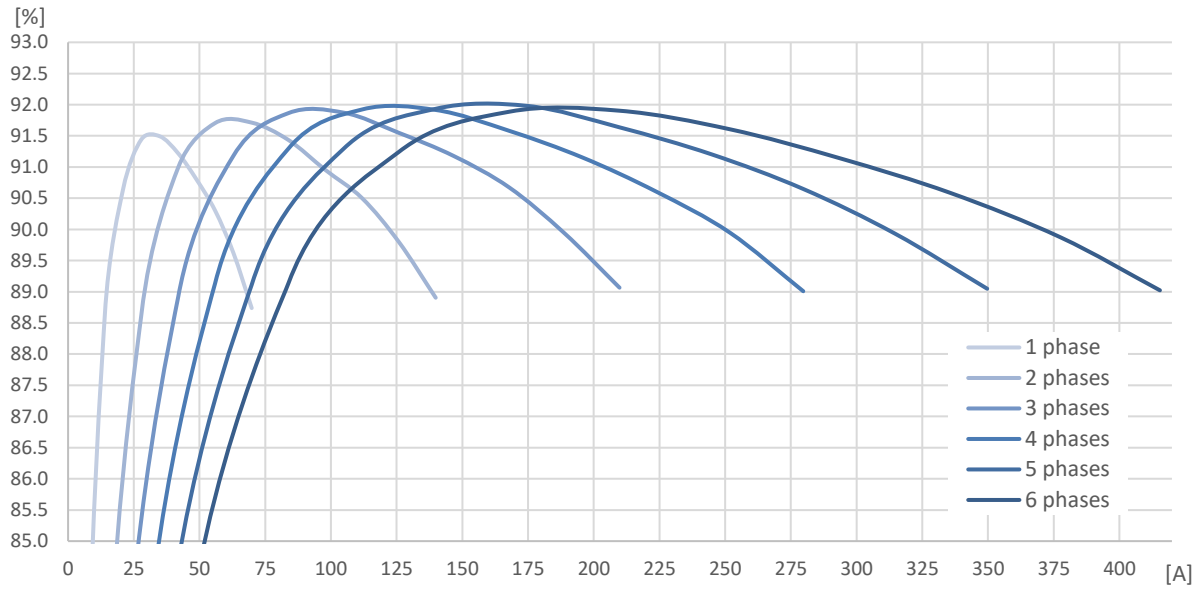
Calculation of efficiency and power dissipation.

Typical Output Characteristics, V_O = 1.0 V

Multiphase, T_{P1}=+25 °C, Standard configuration

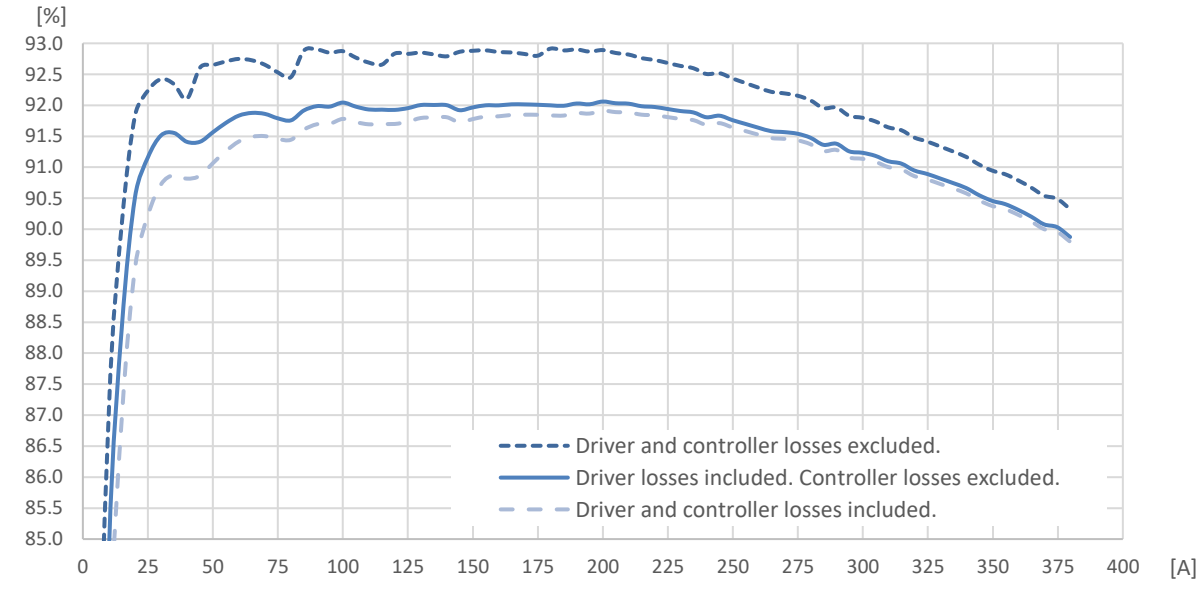
BMR 481 002x (1.0V)

Efficiency



Efficiency vs. load current and fixed number of phases. V_I= 53 V. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Efficiency



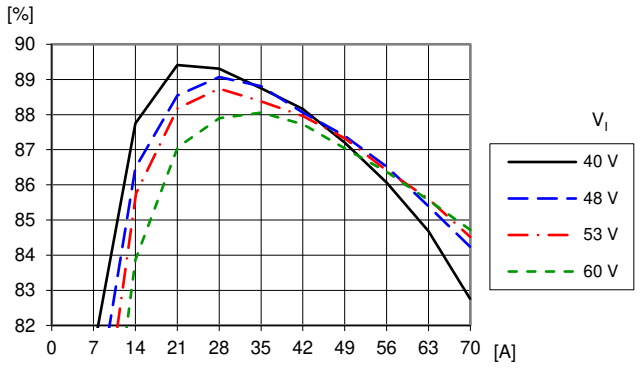
Efficiency vs. load current. 6-phase with phase shedding . V_I= 53 V.

Typical Output Characteristics, V_O = 0.5 V

BMR 481 002x (1.0V)

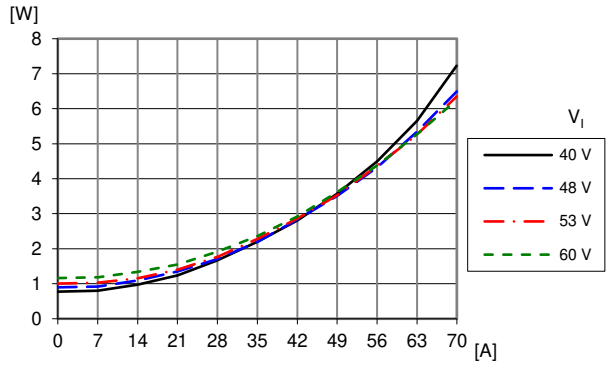
Main only, T_{P1}=+25 °C, Standard configuration

Efficiency (ŋ)



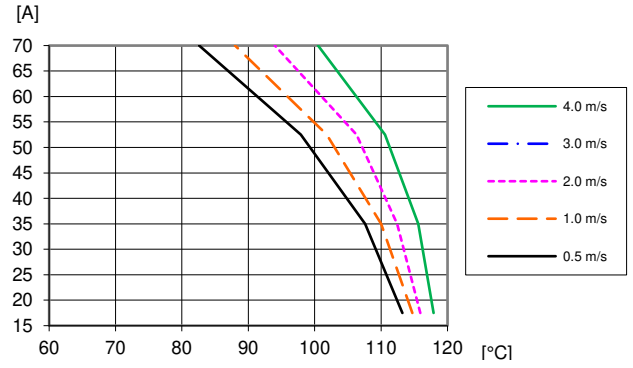
Efficiency vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Power Dissipation (P_D)



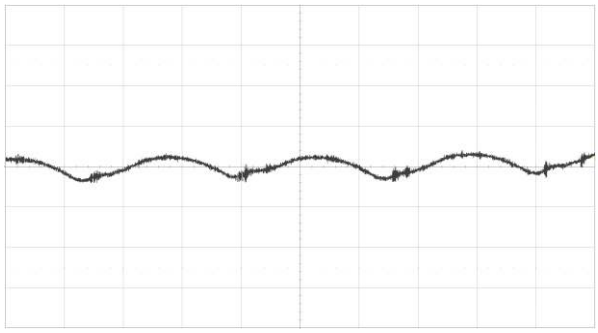
Dissipated power vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Output Current Derating



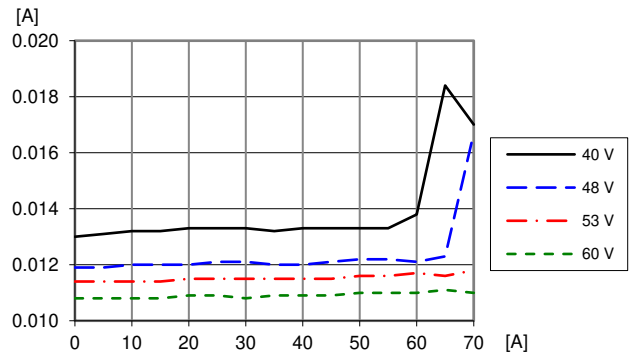
Available load current vs. ambient air temperature and airflow at V_I= 53 V. See section Thermal Consideration.

Output Ripple and Noise



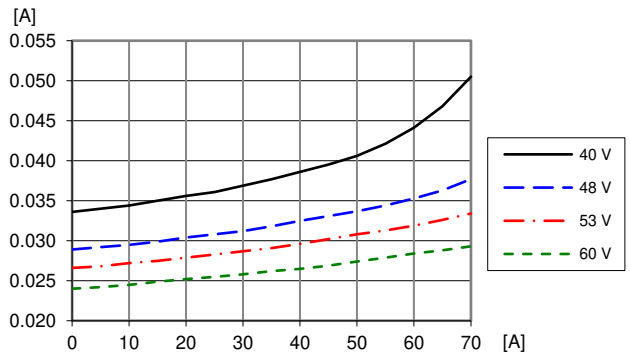
Full bandwidth, V_I = 53 V, I_O = max I_O.
COUT = 1 x 470 µF/3 mΩ POSCAP + 20 x 10 µF ceramic.
Scale: 5 mV/div, 0.5 µs/div
See section Output Ripple and Noise.

VDD Input Current



VDD input current vs. load and input voltage.
For each active phase.

VCC Input Current



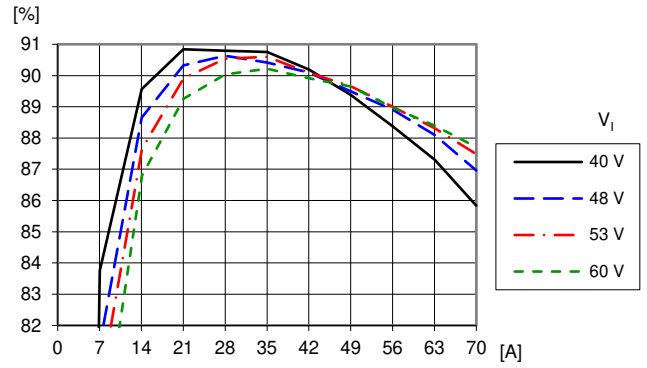
VCC input current vs. load and input voltage.
For each active phase.

Typical Output Characteristics, V_O = 0.75 V

BMR 481 002x (1.0V)

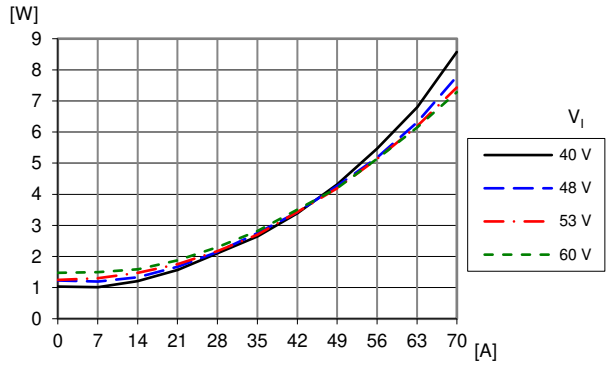
Main only, T_{P1}=+25 °C, Standard configuration

Efficiency (ŋ)



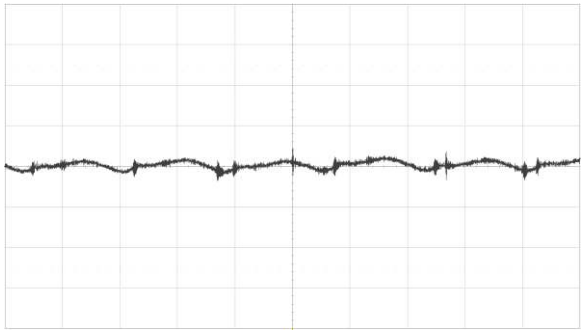
Efficiency vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Power Dissipation (P_D)



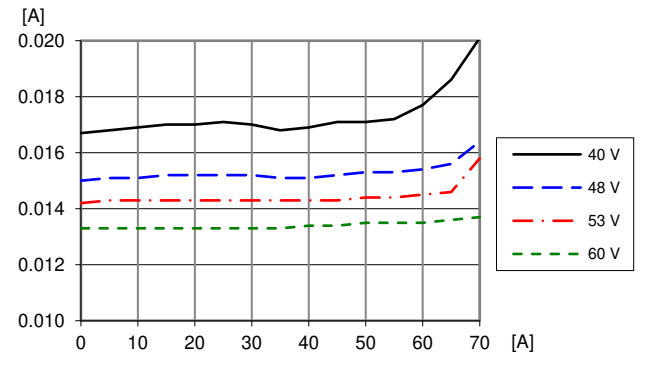
Dissipated power vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Output Ripple and Noise



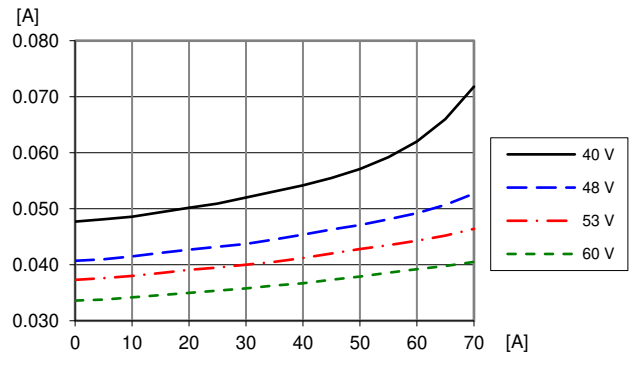
Full bandwidth, V_I = 53 V, I_O = max I_O.
COUT = 1 x 470 µF/3 mΩ POSCAP + 20 x 10 µF ceramic.
Scale: 5 mV/div, 0.5 µs/div
See section Output Ripple and Noise.

VDD Input Current



VDD input current vs. load and input voltage.
For each active phase.

VCC Input Current



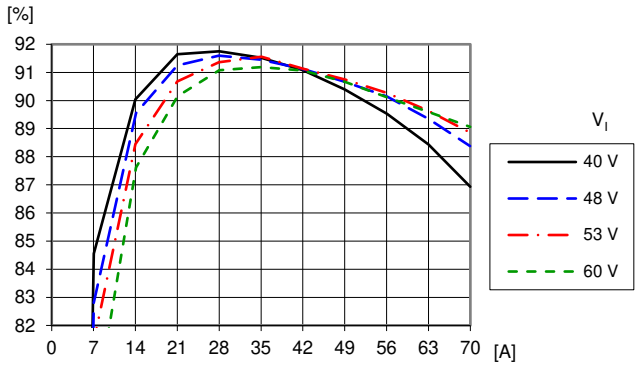
VCC input current vs. load and input voltage.
For each active phase.

Typical Output Characteristics, V_O = 1.0 V

BMR 481 002x (1.0V)

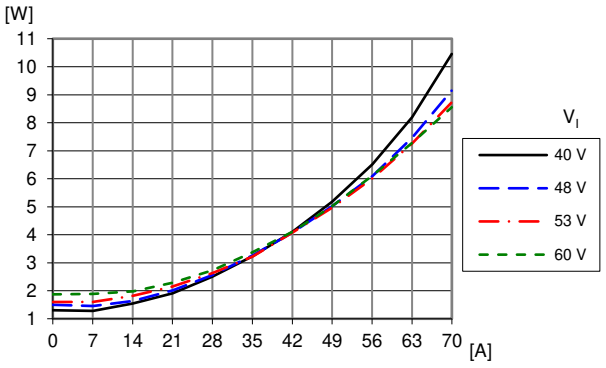
Main only, T_{P1}=+25 °C, Standard configuration

Efficiency (ŋ)



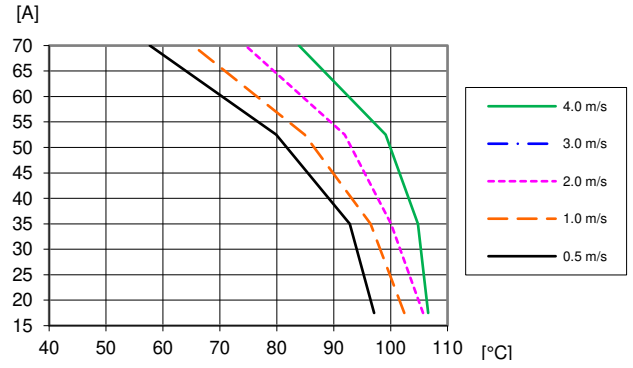
Efficiency vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Power Dissipation (P_D)



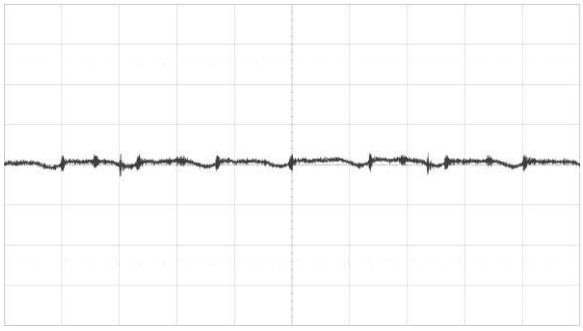
Dissipated power vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Output Current Derating



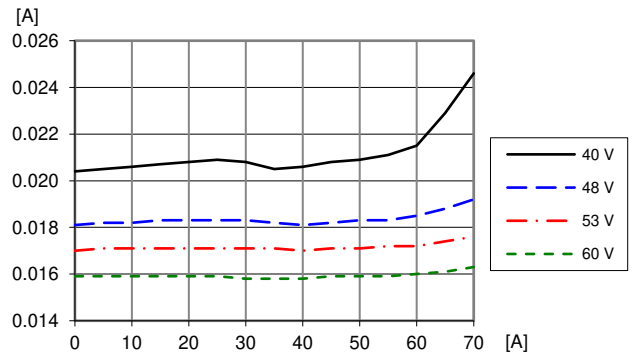
Available load current vs. ambient air temperature and airflow at V_I= 53 V. See section Thermal Consideration.

Output Ripple and Noise



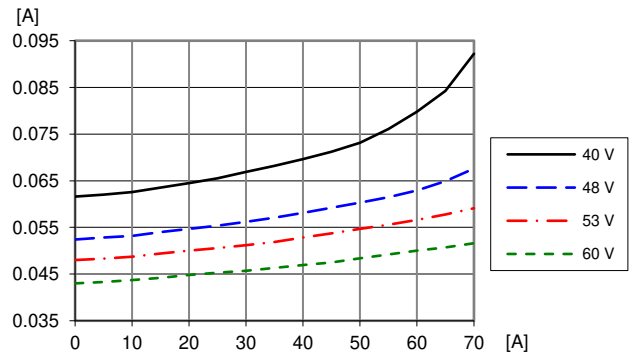
Full bandwidth, V_I = 53 V, I_O = max I_O.
COUT = 1 x 470 µF/3 mΩ POSCAP + 20 x 10 µF ceramic.
Scale: 5 mV/div, 0.5 µs/div
See section Output Ripple and Noise.

VDD Input Current



VDD input current vs. load and input voltage.
For each active phase.

VCC Input Current



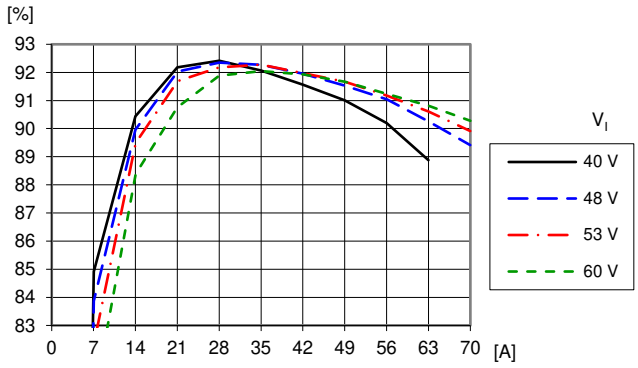
VCC input current vs. load and input voltage.
For each active phase.

Typical Output Characteristics, V_O = 1.35 V

BMR 481 002x (1.0V)

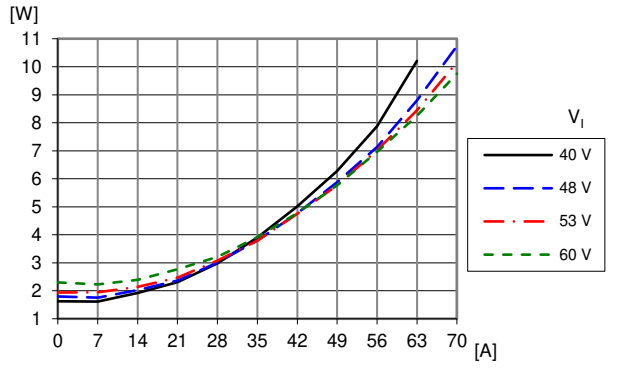
Main only, T_{P1}=+25 °C, Standard configuration

Efficiency (ŋ)



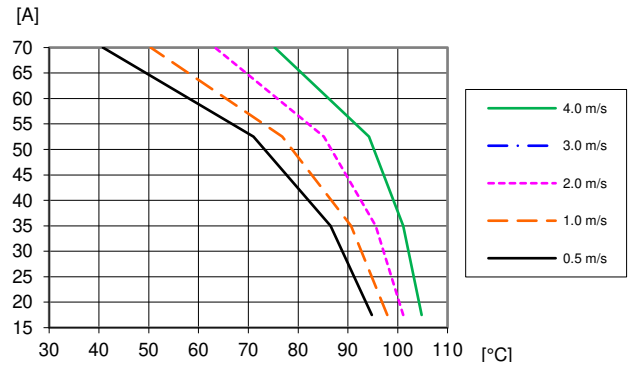
Efficiency vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Power Dissipation (P_D)



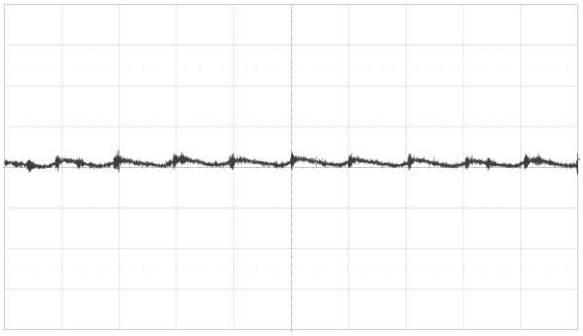
Dissipated power vs. load current and input voltage. Driver losses included (V_{CC}, V_{DD}). Controller losses excluded (V_{CTRL}).

Output Current Derating



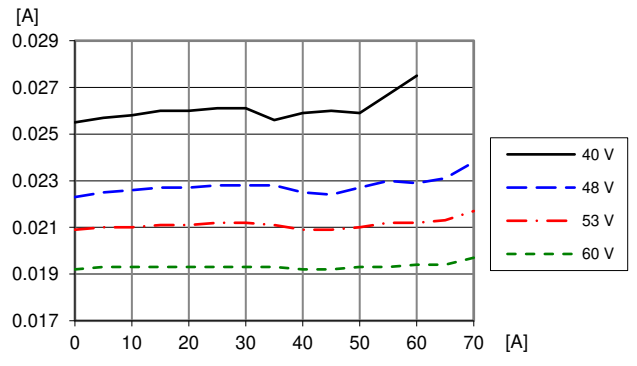
Available load current vs. ambient air temperature and airflow at V_I= 53 V. See section Thermal Consideration.

Output Ripple and Noise



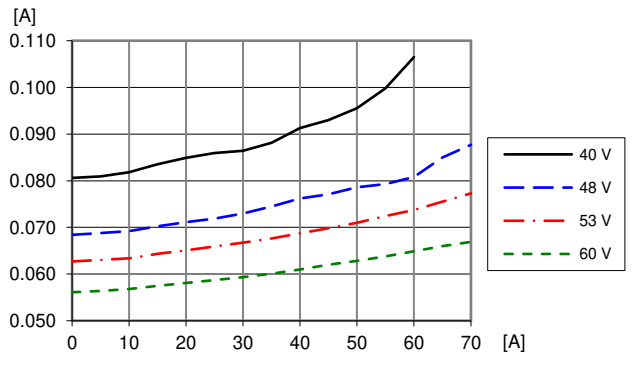
Full bandwidth, V_I = 53 V, I_O = max I_O.
COUT = 1 x 470 µF/3 mΩ POSCAP + 20 x 10 µF ceramic.
Scale: 5 mV/div, 0.5 µs/div
See section Output Ripple and Noise.

VDD Input Current



VDD input current vs. load and input voltage.
For each active phase.

VCC Input Current



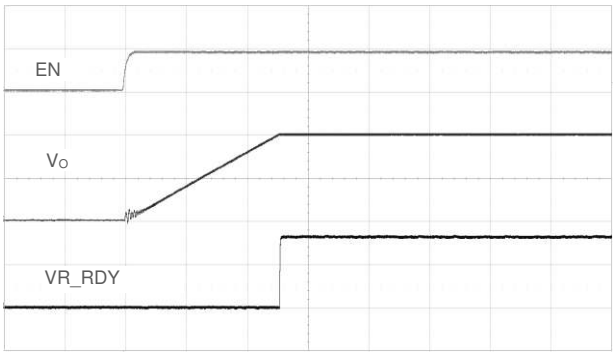
VCC input current vs. load and input voltage.
For each active phase.

Typical Characteristics

BMR 481 002x (1.0V)

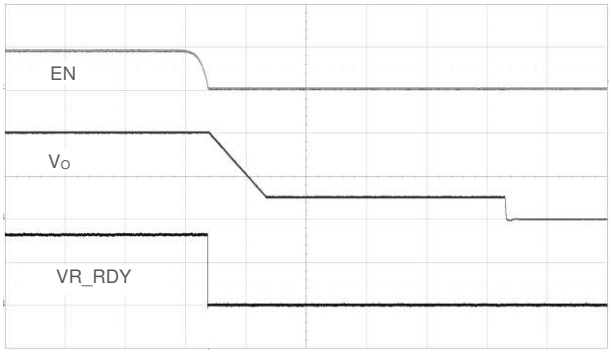
Main only, Standard configuration, T_{P1} = +25 °C

Enable by EN pin



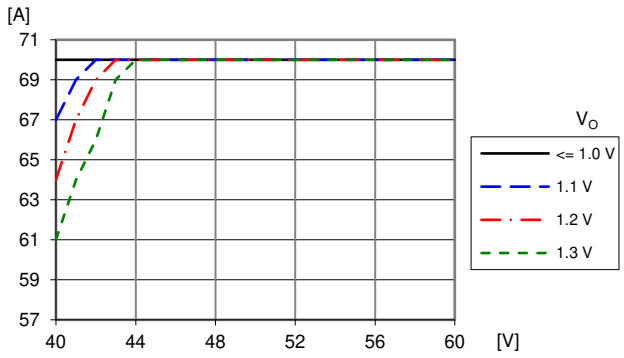
Output enabled by EN pin. V_I = 53 V, V_O = 1.0 V, I_O = max I_O.
VR_RDY pulled up to external voltage.
Scale from top: 5, 0.5, 2 V/div, 0.5 ms/div.

Disable by EN pin



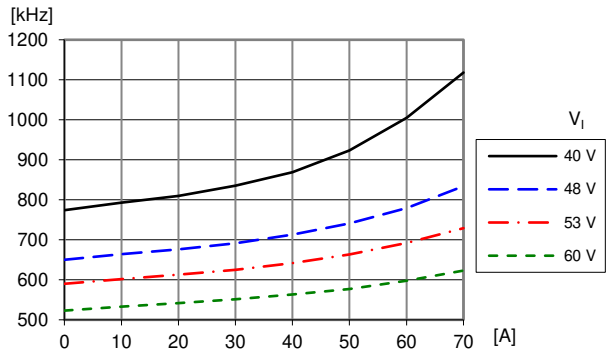
Output disabled by EN pin. V_I = 53 V, V_O = 1.0 V, I_O = max I_O.
VR_RDY pulled up to external voltage.
Scale from top: 5, 0.5, 2 V/div, 1 ms/div.

Output Current Capability



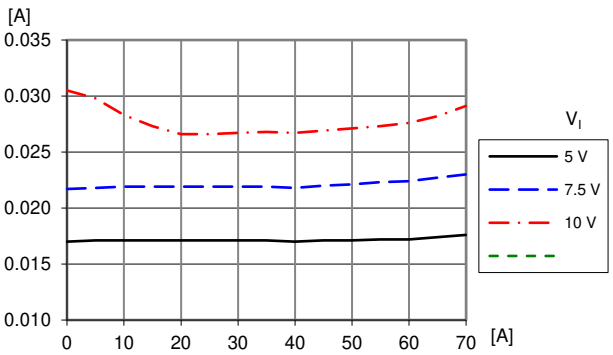
Typical output current capability per Main or Satellite vs. input voltage and output voltage.

Switching Frequency



Switching frequency vs. load current and input voltage. V_O = 1.0 V.

VDD Input Current vs VDD

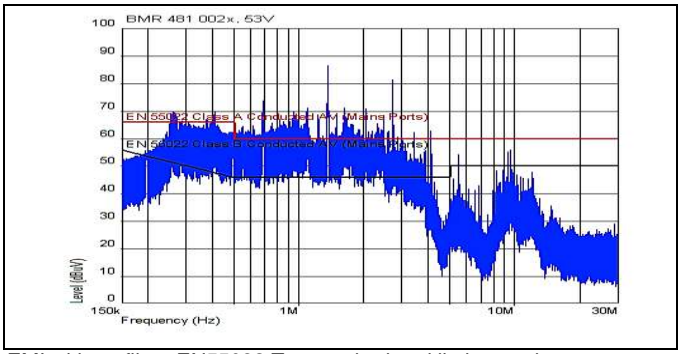


VDD input current vs load and VDD voltage. V_I = 53 V, V_O = 1.0 V.

EMC Specification

Conducted EMI measured according to EN 55022/EN 55032, CISPR 22/CISPR 23 and FCC part 15J (see test set-up). See Design Note 029 for further information. Due to the constant on-time topology used, the switching frequency varies with input voltage, output voltage and output current. See Typical Characteristics for details. The EMI characteristics below are measured at V_I = 53 V, V_O = 1.0 V and I_O= 63 A.

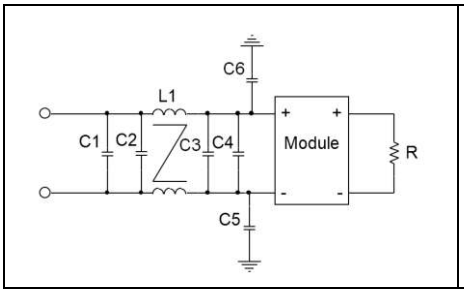
Conducted EMI Input terminal value (typ)



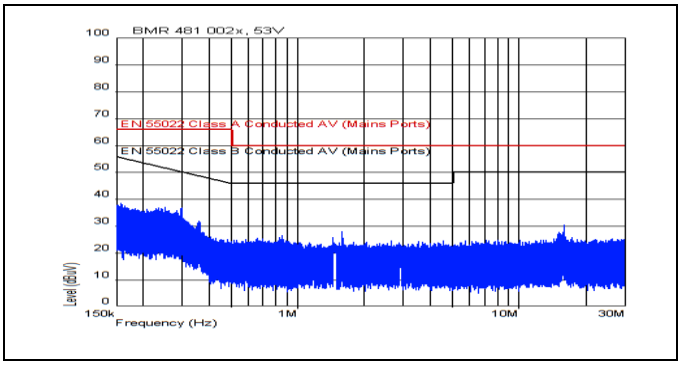
EMI without filter, EN55032 Test method and limits are the same as EN55022.

Optional external filter for class B

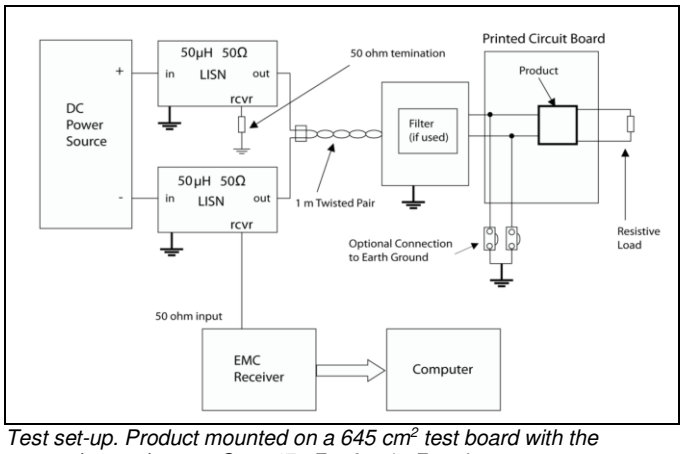
Suggested external input filter in order to meet class B in EN 55022, CISPR 22 and FCC part 15J.



Filter components:
C1, C2, C3, C4 = 2.2 µF
C5, C6 = 2.2 nF
L1 = 0.22 mH
(Pulse P0421)



EMI with filter, EN55022 Test method and limits are the same as EN55023.

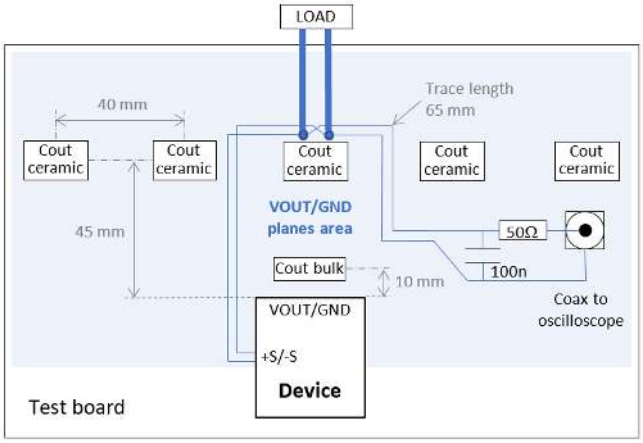


Test set-up. Product mounted on a 645 cm² test board with the external capacitances C_{IN} = 47 µF + 2 x 1 µF and C_{OUT} = 1 x 470 µF/3 mΩ + 20 x 10 µF.

Output Ripple and Noise

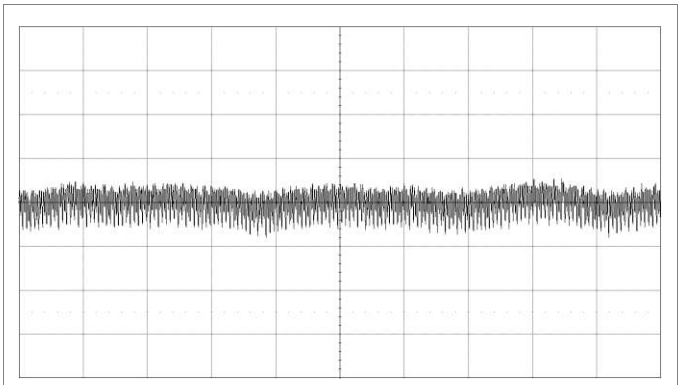
The quasi-resonant topology of the product utilizes both zero voltage switching (ZVS) and zero current switching (ZCS), giving a highly reduced high frequency noise level on the output compared to traditional topologies.

Output ripple and noise is measured according to figure below using the ROA 170 014 test board. Sense jumpers (J13/J14) are set in position LOAD and coax connector for output voltage in position LOAD (K14) is used.
Measurements are made with no bandwidth limitation of oscilloscope input.



Output ripple and noise test set-up.

The digital compensation of the product is designed to automatically provide stability, accurate line and load regulation and good transient performance for a wide range of operating conditions (switching frequency, input voltage, output voltage, output capacitance). Inherent from the implementation and normal to the product there will be some low frequency ripple at the output in addition to the fundamental switching frequency output ripple. The total output ripple and noise is maintained at a low level.



V_I = 53 V, V_O = 1.0 V, I_O = 70 A, C_{OUT} = 470 µF/3 mΩ + 20 x 10 µF
Full bandwidth, Main module only
5 mV/div, 50 µs/div

Example of low frequency ripple at the output.

PMBus Interface

Power Management Overview

The Main product incorporates a wide range of configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults.

The product's standard configuration is suitable for a wide range of operation in terms of input voltage, output voltage and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. A detailed description of each command is provided in the appendix PMBus Commands at the end of this specification.

The Flex Power Designer software suite can be used to configure and monitor this product via the PMBus interface. For more information see https://flexdigitalpowerdesigner.com/.

SMBus Interface

The product can be used with any standard two-wire I²C or SMBus host device. See Electrical Specification for allowed clock frequency range. In addition, the product is compatible with PMBus version 1.3 and includes an SALERT line to help mitigate limitations related to continuous fault monitoring. The PMBus signals SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors values should be selected to guarantee the rise time according to equation below:

$$\tau = R_P C_p \leq 1\ \mu s$$

where R_p is the pull-up resistor value and C_p is the bus loading. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.5 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.
See application note AN304, section SMBus Basics, for details on interfacing the product with a microcontroller.

Extended Command Protocol

The product utilizes the extended command format specified in the PMBus specification, Part I. Thus, some of the supported PMBus commands requires a two-byte command code.

PMBus Addressing

The PMBus address is configured with a resistor, R_{SADDR}, connected between the SADDR pin and GND, as shown in the Typical Application Circuit. Recommended resistor values are shown in the table below. 1% tolerance resistors are required.

R_{SADDR} [kΩ]	Address
10.5	0x60
12	0x61
14	0x62
15.4	0x64
18	0x68
20.5	0x69
24	0x6A
27	0x6C
33	0x70
39	0x71
47	0x72
62	0x74
82	0x58
120	0x59
220	0x5A
Infinite (open)	0x5C

Reserved Addresses

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address	Comment
0x00	General Call Address / START byte
0x01	CBUS address
0x02	Address reserved for different bus format
0x03 - 0x07	Reserved for future use
0x08	SMBus Host
0x09 - 0x0B	Assigned for Smart Battery
0x0C	SMBus Alert Response Address
0x28	Reserved for ACCESS.bus host
0x2C - 0x2D	Reserved by previous versions of the SMBus specification
0x37	Reserved for ACCESS.bus default address
0x40 - 0x44	Reserved by previous versions of the SMBus specification
0x48 - 0x4B	Unrestricted addresses
0x61	SMBus Device Default Address
0x78 - 0x7B	10-bit slave addressing
0x7C - 0x7F	Reserved for future use

Output Voltage Format

Depending on product variant different format of output voltage is used:

Output voltage control *	Upper Limit of Output Voltage Adjustment Range *	Output Voltage Format		
		AVSBus	SVID 5 mV	SVID 10 mV
PMBus	<= 1.5 V		X	
	> 1.5 V			X
SVID	<= 1.5 V		X	
	> 1.5 V			X
AVSBus	All	X		

* See Ordering Information. All options and voltage ranges may not be applicable.

The SVID formats are compatible with the Intel® VR13 PWM rev1.1, document #544905.

The output voltage format affects the specification of output voltage related PMBus commands:

PMBus Command	Output Voltage Format		
	AVSBus	SVID 5 mV	SVID 10 mV
VOUT_MODE	0x20	0x23	0x23
VOUT_COMMAND VOUT_MAX VOUT_MARGIN_HIGH VOUT_MARGIN_LOW MFR_VBOOT_SET READ_VOUT	0 V + 5 mV per LSB	0.245 V + 5 mV per LSB	0.490 V + 10 mV per LSB
MFR_VOUT_TRIM	5 mV per LSB		10 mV per LSB
MFR_READ_VOUT	Linear		

As a consequence of the output voltage formats the output voltage is not always monitored as 0 V when the output is turned off:

Response when output voltage disabled	Output Voltage Format		
	AVS	SVID 5 mV	SVID 10 mV
READ_VOUT *	0x0000 = 0 V	0x0000 = 0.245 V	0x0000 = 0.490 V
MFR_READ_VOUT	0.5 V		

* 0x0000 will also be reported if the output voltage is enabled and the actual output voltage is below 0.5 V.

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below. The averaging time for monitored values is configurable by the command MFR_AVERAGE_TIME_SCALE.

Parameter	PMBus Command
Input voltage	READ_VIN
Output voltage	READ_VOUT
	MFR_READ_VOUT
Output current	READ_IOUT
Output power **	READ_POUT
Energy **	MFR_POUT_THREAD
Highest temperature of all Main/Satellites	READ_TEMPERATURE_1
Temperature of Main/Satellite representing phase x	*MFR_RD_TEMPERATURE_CELLx

* Temperature is reported only when phase is active.
** Computed values.

The sensor of the monitored temperatures is close to position P3, see section Thermal Considerations. The monitored temperature will be in the approximate range 0-5°C lower than T_{P3}, depending on operating and thermal conditions.

The lowest temperature that can be monitored, and be used for temperature compensation of monitored output current (READ_IOUT), is +8°C. For temperatures below this level the temperature +8°C is reported and used for temperature compensation.

Monitoring Faults

Fault conditions can be monitored using the SALERT pin, or the FAULT pin, which will be asserted low when any number of pre-configured fault conditions (not warning) occurs. The SALERT and FAULT pins will be held low until faults are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled.
It is possible to mask which fault conditions should not assert the SALERT pin by the command SMBALERT_MASK. Selection of fault conditions for the FAULT pin are set by the command MFR_FAULT_CONFIG.

In response to the SALERT and FAULT signals, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault & Warning Status	PMBus Command
Overview	STATUS_WORD STATUS_BYTE
Output voltage level	STATUS_VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

Black Box Recorder (BBR)

The Black Box feature captures precise status of the device at the fault occurrence. Status flags before and after a fault event occurred are recorded and stored into dedicated NVM sectors.

By sending command MFR_READ_BLACKBOX the stored data is copied from NVM to RAM. Then, by reading command MFR_BLACKBOX, the user can review the data according to the following cases:

1. If Before Status = 1 and After Status = 1 then the fault has not triggered the BBR because the fault was triggered before.

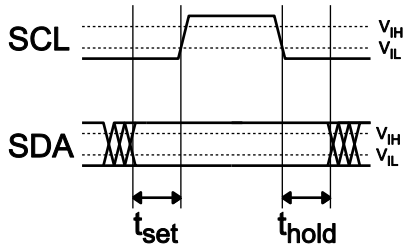
2. If Before Status = 0 and After Status = 1 then the fault has triggered the BBR.

3. If Before Status = 0 and After Status = 0 then the fault has not triggered the BBR.

The BBR data stored into the NVM is preserved also in case of power cycling and/or re-trigger of the same protection.

Command MFR_CONFIG_BBR selects which faults shall trigger writing of BBR data to the NVM. After a valid condition has occurred the Black Box Full status bit in STATUS_MFR_SPECIFIC is set. To clear this status bit and the BBR content the command MFR_CLEAR_BB has to be sent. Note that sending CLEAR_FAULTS will not clear the bit.

PMBus/I²C Timing



Setup and hold times timing diagram.

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the falling edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus 2.0 specification, for SMBus electrical and timing requirements.

This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A bus-free time delay according to this specification must occur between every SMBus transmission (between every stop & start condition).
The product supports PEC (Packet Error Checking) according to the SMBus specification.

After sending commands that involve writing to the NVM a delay according to the table below is required before V_{CTRL} is powered off. If sending a subsequent command the user may insert these delays or the BUSY flag in STATUS_BYTE can be polled to detect when the device is ready to receive a new command.

After sending PMBus command	Required delay before additional command or V_{CTRL} power off
STORE_DEFAULT_ALL	100 ms
MFR_STORE_MAP	
MFR_SECT_WR	20 ms

Memory Structure

The product incorporates a Non-Volatile Memory area for storage of PMBus command and System register values. The NVM is pre-loaded with Flex factory default values. The values in NVM are loaded during initialization according to section Initialization Procedure, where after commands can be changed through the PMBus Interface.

The STORE_DEFAULT _ALL command will store the changed PMBus command values to the NVM, while the MFR_STORE_MAP command will store both PMBus command values and System register values to the NVM. When sending any of these two store commands, the CRC code in NVM is automatically recalculated and updated. Commands RESTORE_DEFAULT_ALL and MFR_RESTORE_MAP transfer data in the opposite direction, from NVM to RAM.

NVM memory cells are qualified for 1000 read/erase/write cycles and 10 years data retention at 125 °C.

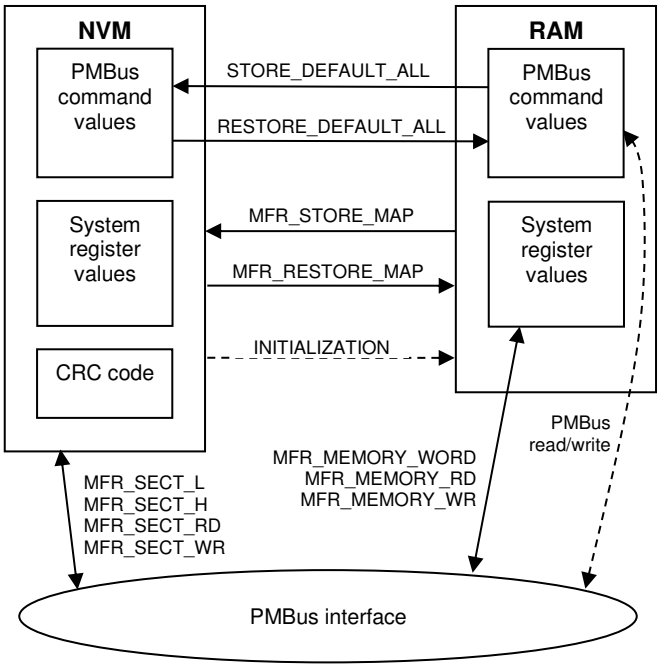


Illustration of memory areas of the product and associated PMBus commands.

In general V_{CTRL} must be cycled before a change in a System Register have an effect (thus, storing to NVM is required), while changes to PMBus commands will have immediate effect once written to RAM.

Parameter Protection
Several possibilities are provided to protect configuration parameters in the NVM and RAM:

PMBus Command	Function
WRITE_PROTECT	Control of PMBus command writes in general.
MFR_WRITE_LOCK	
MFR_UNLOCK	Control of System register reads/writes, as well as reads/writes of critical PMBus commands.
MFR_LOCK	
MFR_SVID_REGLOCK	Control of PMBus command and System register writes related to SVID/AVS CPU-link registers.
MFR_PROTECT_DEFAULT	Control of NVM writes.

Initialization Procedure
The product follows an internal initialization procedure after the supply voltage on the VCTRL pin becomes larger than the UVLO threshold:

1. Startup and initialization.
2. The address pin-strap resistor is measured and the associated PMBus address is defined. If a non-valid pin-strap resistor value is used, power conversion will be prohibited and the device is set to respond to PMBus address 0x7C.
3. Flex factory default values stored in the NVM memory are loaded to operational RAM.
4. A CRC check is performed over memory content and compared with CRC code in NVM. If an error is detected, power conversion is prohibited and STATUS_CML[4] (Memory fault detected) is set and the device is set to respond to PMBus address 0x7C. Thus, the address setting by SADDR pin is ignored.
5. Self-calibration is performed to cancel out offsets in output voltage and output current readings.

Once this procedure is completed and the Initialization Time, T_{INIT}, has passed (see Electrical Specification), the output voltage is ready to be enabled using the EN pin. The product is also ready to accept commands via the PMBus interface, which in case of writes will overwrite any values loaded during the initialization procedure.

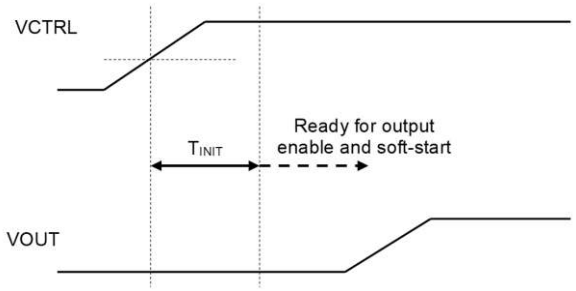


Illustration Initialization time

Additional Interfaces

PuC (Primary uC) Interface
The Main product is prepared for using a primary side microcontroller interface of SPI type. This interface is optional and may be used to provide input voltage and input current information to the product. For more information please contact your local Flex sales representative.

SVID Interface
An SVID bus interface for dynamic change of output voltage level, according to Intel VR13 Specification, is available for SVID product variants, see Ordering Information. The SVID interface is fully compliant to the Intel® DVID protocol Rev1.7, document #456098.

AVSBus Interface
An AVSBus bus interface for dynamic change of output voltage level, according to the PMBus Specification 1.3 Part III, is available for AVSBus product variants, see Ordering Information.

Operating Information

Product Overview

The products provides a compact and scalable direct conversion solution for loads with demanding current levels and low noise requirements.

Auxiliary Supplies

In addition to the main input voltage the product requires additional auxiliary supplies:

Supply	Function
VDD	Primary driver supply
VCC	Secondary driver supply
VCTRL	Controller supply (secondary side, Main product only)

In non-isolated applications a single 5V±5% supply can be used to support all three voltages.

In isolated applications where PWM signals are connected through digital isolators, it must be made sure that the PWMX/PWMY inputs are defined before VDD is applied. This can be achieved by supplying VCTRL before VDD. It can also be achieved by selecting a digital isolator that has a low signal as default level before supply of both sides are applied.

Input Voltage

The product is designed for a 40-60 V input voltage range. Operation with input voltage below 40 V may be supported depending on application requirements such as output voltage and current level and load transient response. See also section Output Current Capability. For more information please contact your local Flex sales representative.

Input Turn-On Voltage

The PMBus command VIN_ON controls the minimum input voltage at which output voltage can be enabled. If the output voltage is enabled while the input voltage is below the VIN_ON threshold, conversion will not start and an input under voltage fault is reported. If the input voltage rises above the VIN_ON threshold while the output voltage is enabled, conversion will start automatically (no re-enable required).

Note that the VIN_ON threshold applies only to the first enable after VCTRL has been applied. After the first successful enable, the VIN_ON threshold is no longer checked.

Input Voltage Sense

An input voltage sense, needed for feed forward function and monitoring, is connected externally to the Main device, in order to support both isolated and non-isolated solutions.

For a non-isolated solution, a 390 kohm external resistance is simply connected between the VSRMON pin and the input voltage. It is recommended to use two resistors in series, e.g. 120 + 270 kohm, to provide protection for shorted resistor. Together with an internal 10 kohm pull-down resistor the external resistance forms a voltage divider with 1/40 ratio. The ratio is chosen to make sure the voltage at the VSRMON pin is kept within optimal range; below 2 V.

For an isolated solution an analog isolator, such as an isolated amplifier circuit or linear opto coupler, must be used to maintain a 1/40 ratio between input voltage and VSRMON pin voltage across an isolation barrier.

Input Voltage Protections (IUVP, IOVP)

The product monitors the input voltage continuously and will respond as configured when the input voltage falls below or rises above the configured threshold levels (see Electrical Specification). The product can be configured to respond in different ways when a limit is passed:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup). See section Automatic Restart.

The default response is option 1 for Input Over Voltage Protection and option 2 for Input Under Voltage protection. The protections are configured using the PMBus commands:
VIN_UV_FAULT_LIMIT
VIN_UV_FAULT_RESPONSE
VIN_OV_FAULT_LIMIT
VIN_OV_FAULT_RESPONSE.

Peak Input Voltage Protection

A peak input voltage fault is triggered if the voltage at the VSRMON pin is greater than 3.045 V.
The product can be configured to respond in different ways when the limit is passed:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.

The default response is option 2. The peak input under voltage voltage protection is configured using the PMBus commands MFR_PEAK_FAULT_RESPONSE.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

It is recommended to use at least 2 x 1 uF ceramic external input capacitors for each module, placed closed to input pins and with low impedance connections to the VIN and GND pins

in order to be effective. See application note AN323 for further guidelines on how to choose and apply input capacitors.

External Output Capacitors

The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to minimize output voltage deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product. Adding output capacitance decreases loop band-width.

It is recommended to place low ESR ceramic and low ESR electrolytic/polymer capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts in order for capacitance to be effective.

Optimization of output filter together with load step simulations can be made using the Flex Power Designer software. See application note AN321 for further guidelines on how to choose and apply output capacitors.

Output Current Capability

Inherent to the resonant topology used the product has a limited output current capability, which depends on the input voltage and output voltage, see Typical Output Characteristics. In a multiphase setup where Satellites are used, it is recommended to de-rate the capability by typically 5% in order to account for current sharing unbalance between devices, which occur due to layout asymmetry and/or variations between individual units. In applications where Satellites are placed at a long distance from the Main, or from each other, a stronger de-rating may be considered.

Control Loop

The controller of the Main device features a high performance resonant digital control loop. During operation, the output voltage is sensed differentially and the error in the regulation is digitized by a fast analog-to-digital converter (ADC). The resultant digital error signal is fed into an oversampled (40 MHz) digital PID compensator and then processed by digital control and converted into PWM pulses using a digital pulse width modulator (DPWM). The pulse scheme is Constant On-time (COT) with variable frequency. Thus, the PWM pulses has a fixed on time while switching frequency (and consequently duty cycle) will depend on operating conditions such as input voltage, output voltage and load levels.

By default the product is configured with robust PID coefficients to provide stability for a wide range of operating conditions and output filters. Where specific load transient response requirements exists Flex Power Designer should be used to simulate and find optimized control loop settings.

In addition to the PID coefficients, set by PMBus command MFR_PID, additional control parameters are available to further improve the load transient response:

Pre and post filters. By PMBus command MFR_FILT_PRE_POST it is possible to adjust the time constant of the lowpass filters preceding and succeeding the PID regulator.

Transient Gain Boost (TGB). When the negative error in output voltage exceeds the threshold set by system register TGB_CONFIG the control loop gain is doubled. Limits the undershoot during load application.

Error clamp. Stops the integrator of the PID during load removal. Limits the overshoot during load release. The error threshold for activation of the clamp is set by system register CTRL_VERR_CLAMP.

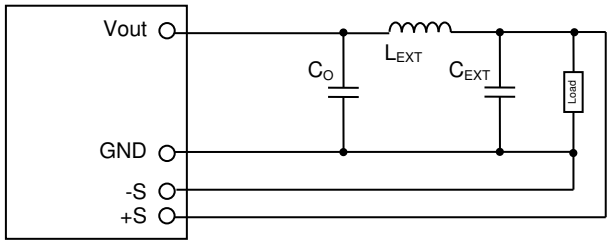
Feed forward control. Configured by PMBus command MFR_KK_FEEDFRWD_GAIN_CTRL.

Remote Sense

The product has remote sense to compensate the voltage drops between the regulator output and the load.

Generally, the module is designed for an external capacitive decoupling near the device, see Section External Output Capacitors for further information. The Flex Power Designer software can be used to simulate the condition and help to place the correct decoupling and configure the module for optimal performance.

In case of parasitic or deliberate inductance in the output power train, it can influence the stability of the regulator. The placement of the sense point is then critical.



External output filter with inductor (PI filter).

Remote Sense Protection

A Feedback Disconnected fault is triggered if the voltage at the +S/-S sense pins differ too much from the voltage at the VOUT/GND pins, see thresholds in Electrical Characteristics. If such condition occurs the output voltage is shutdown immediately until fault is cleared and the output voltage is re-enabled.

Enabling Output Voltage

The following options are available to enable and disable the output voltage:

1. Through the EN pin. Only active high logic is supported.
2. By using the PMBus command OPERATION.

The EN pin has an internal 10 kΩ pull-up resistor to 5 V. The external device must have a sufficient sink current ability to be able pull EN pin voltage down below logic low threshold level (see Electrical Characteristics).

Output Voltage Adjust

For product variants with PMBus interface only the output voltage level is controlled by PMBus command VOUT_COMMAND.

For AVS product variants the output voltage can be controlled by PMBus command VOUT_COMMAND or the AVSBus bus, as selected by the OPERATION command according to the PMBus Specification 1.3 Part III. In AVSBus mode the default output voltage level is set by command MFR_VBOOT_SET.

For SVID product variants the output voltage can be controlled by PMBus command VOUT_COMMAND or the SVID bus, as selected by the MFR_SVI_PMBUS_SELECT command. In SVID bus mode the default output voltage level is set by command MFR_VBOOT_SET.

See Electrical Specification for output voltage adjustment range.

Output Voltage Positioning

A droop function, set by command VOUT_DROOP, introduces a dependence of the output voltage on the load current, recovering part of the ESR in a load transient.
The Main device monitors the total delivered current from all phases and adjusts the output voltage in proportion, to achieve the desired load-line slope.
The current information from each phase is individually thermally compensated.

Voltage Margining Up/Down

Using the PMBus interface it is possible to adjust the output voltage to one of two predefined levels above or below the nominal voltage setting in order to determine whether the load device is capable of operating outside its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit outside its typical operating range. This functionality can also be used to test of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus commands VOUT_MARGIN_LOW and VOUT_MARGIN_HIGH. Margining is activated by the command OPERATION and can be used regardless of the output voltage being enabled by the EN pin or by the PMBus.

Output Voltage Range Limitation

The output voltage range that is possible to set by the PMBus or AVS/SVID interface is limited by the PMBus command VOUT_MAX. The limitation applies to the actual regulated output voltage rather than to the configured value. Thus, it is possible to write and read back a VOUT_COMMAND value higher than the limit, but the actual output voltage will be limited.

Power Good/VR Ready

The VR_RDY pin indicates when the product is ready to provide regulated output voltage to the load. During ramp-up and during a fault condition when the output voltage has shutdown, VR_RDY is held low. VR_RDY is asserted high after the output has completed ramping to the set voltage level and de-asserted low when the output voltage is controlled to off. Thus, de-assertion is not controlled by the voltage level.

The VR_RDY output is held low during the initialization procedure.

Output Under Voltage Protection (UVP)

The product includes under voltage limiting circuitry. The threshold is set as a negative offset, 50-400 mV in 50 mV steps, to the commanded output voltage level (see Electrical Specification). The product can be configured to respond in different ways when the UVP limit is passed:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup).See section Automatic Restart.

The default response is option 1. The UVP limit and fault response are configured using the PMBus commands MFR_UV_LIMIT_OFFSET and VOUT_UV_FAULT_RESPONSE.

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The threshold is set as a positive offset, 50-400 mV in 50 mV steps, to the commanded output voltage level (see Electrical Specification). The product can be configured to respond in different ways when the OVP limit is exceeded, see below options.

1. HIZ_HALFB_SYMMETRIC[0] = 0. Ramp down the output voltage to a regulated level of 0.25V for indefinite time. This in order to safeguard the power train from over voltage stress due to reversed current. In order to re-enable the output voltage, the controller supply (VCTRL) must be re-cycled.
2. HIZ_HALFB_SYMMETRIC[0] = 1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).

The default response is option 1. In addition, it is possible to configure automatic restart (hiccup). See section Automatic Restart.

Setting the OVP response setting to ignore is not supported. The OVP limit is configured using the PMBus command MFR_OV_LIMIT_OFFSET.

Over Current Protection (OCP)

The product includes robust current limiting circuitry for protection at overload. The OCP function has two parts; a fast peak detection and a detection that works on average current. In both cases the protection applies to the total output current of all Main/Satellites in the rail.
The peak protection is always enabled with a latched response, while for the average current protection different response options are available:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup). See section Automatic Restart.

The default response from an over current fault is option 1. Delayed shutdown is not supported. The load distribution should be designed for the current set by the current limit threshold.

The average OCP warning and fault limits are configured using the commands IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT. The response options are set by IOUT_OC_FAULT_RESPONSE.

The peak OCP limit, OC_{PEAK} is configured using the command MFR_IMON.

$$OC_{PEAK}[A] = 2.1 \cdot \frac{1}{IMONX2_{RAW} + 1} \cdot \frac{DCR\_INV\_COEFF_{RAW}}{0.291 \cdot 64} \cdot \frac{1000}{2.678571 \cdot (MFR\_IMON_{RAW} + 1)}$$

where OC_{PEAK} [A] is the peak limit and IMONX2 and DCR_INV_COEFF are fixed System Register values. Note that since MFR_IMON can only be set to discrete values in the interval 0-63, only certain values is possible to set for the peak OCP limit.

When adjusting MFR_IMON, also the output current monitoring range, set by System Register TEL_IOUT_FSR, must be configured as:

$$TEL\_IOUT\_FSR\ [A] = OC_{PEAK}[A]$$

The Flex Power Designer tool lists the possible peak OCP values and will automatically set MFR_IMON and TEL_IOUT_FSR based on selected value.

Over Power Protection

The product includes a protection mechanism that works on the output power, computed as sensed Vout times the monitored output current. Different response options are available:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup). See section Automatic Restart.

The default response is option 2.

The over power limit is configured using the command POUT_OP_FAULT_LIMIT. The response option is set by POUT_OP_FAULT_RESPONSE.

Automatic restart (hiccup)

By setting bit 7 in System register SVI_ADDITIONAL_OFFSET hiccup fault response mode is enabled. When hiccup is enabled, after a fault occurred and the output voltage has shut down the controller will continuously attempt to restart the output voltage in 1 ms intervals. The interval time is not reconfigurable. The automatic restart applies to the fault types enabled for the FAULT pin, set by PMBus command MFR_FAULT_CONFIG. Thus, it is possible to mask which protection mechanisms will use the hiccup functionality.

Soft-on

The soft-on functionality allows the output voltage to ramp-up with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple loads.
The rise time is the time taken for the output to ramp to its target voltage. The on delay time sets a delay from when the output is enabled until the output voltage starts to ramp up.

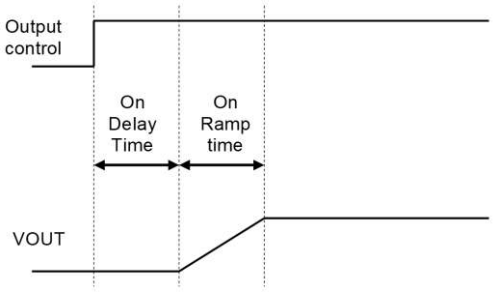


Illustration of soft-on.

The on delay time is reconfigured using the PMBus command TON_DELAY, while the on ramp time is reconfigured by setting a slew rate by PMBus command MFR_SVID_SLOW_SR_SELECTOR together with System Register DVID_SR_SLOW_STEP.

Detailed optimization of soft-on is possible by settings in PMBus command MFR_KK_FEEDFRWD_GAIN_CTRL (error clamp) and System registers HIGH_CURR_PROT_EN (gain reduction) and EN_DROOP_START (droop effect).

Soft-off

When enabled, the soft-off functionality makes the output voltage to ramp down with a defined slew rate, after output voltage being turned off. In order to prevent a reverse current through the power train, which may cause excessive voltage across switching elements, the regulator will ramp down to a voltage of ~0.25 V and keep this level for a few ms, before finally turn switching completely off.
The time after output control is turned off until voltage starts to ramp down is not reconfigurable.

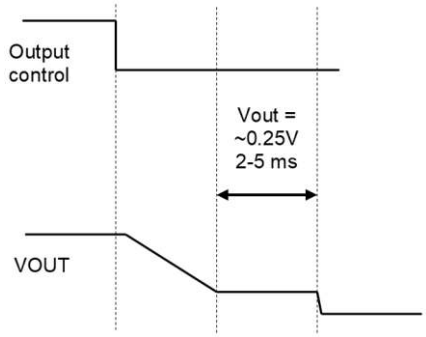


Illustration of soft-off.

By default soft-off is enabled. It can be disabled by setting bit 0 in System Register HIZ_HALFB_SYMMETRIC. The slew rate of the ramp is set by PMBus command MFR_SVID_SLOW_SR_SELECTOR together with System Register DVID_SR_SLOW_STEP.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. There could also be still charged output capacitors when starting up shortly after turn-off.
The product incorporates synchronous rectifiers, but will not sink current during startup. If soft-off is disabled (see above), the same applies for turn-off or whenever a fault shuts down the product in a pre-bias condition.

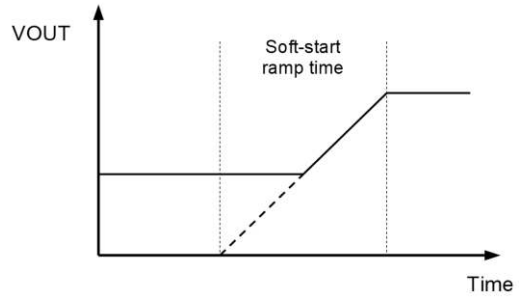


Illustration of pre-bias startup.

Switching Frequency

Due to the constant on-time (COT) topology used the switching frequency is not configurable, but will vary with input voltage, output voltage and output current. Refer to Electrical Specification for switching frequency vs operating conditions.

Synchronization

Due to the constant on-time (COT) topology used the product cannot be synchronized with an external clock source.

Multiphase Operation (Current Sharing)

Up to five Satellite devices can be connected to a Main device, to increase the output current capability of a single power rail. All Satellites are managed by the Main device, that provides a common interface for control and telemetry as a single rail.

Active current sharing balancing can be activated by the PMBus command MFR_CS_PROP_INTEGR. The Main will actively control the output current of each Satellite, based on the monitored output current from each Satellite, to achieve balance between all phases. This function can correct for unit and layout differences and increase the thermal performance of a multiphase rail.
It is not recommended to enable the active current sharing function in cold applications, since the monitored output current is not temperature compensated when the monitored temperature is +8°C or lower.

Phase Interleaving

When operating the product in a multiphase setup, the Main device will automatically spread the phases evenly in time, based on the number of active phases at the moment, in order to minimize the input and voltage ripple.

Phase Shedding (Dynamic Phase Management, DPM)

When operating the product in a multiphase setup, the Main will automatically add and drop phases based on load level, in order to provide flat efficiency across the load range.

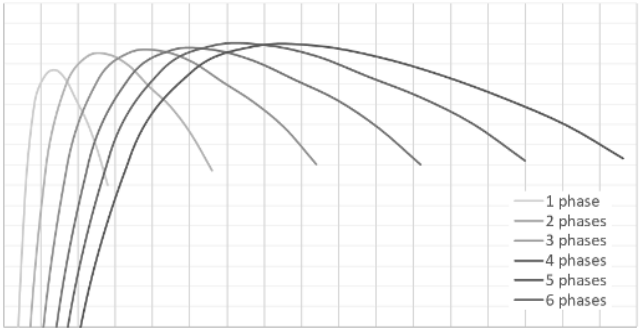


Illustration of efficiency vs load and number of active phases.

The shedding function is configured by the following PMBus commands:

PMBus Command	Function
MFR_CELL_CONFIG	Sets the maximum number of phases to operate (typically the number of Main + Satellite modules in the design).
MFR_MANUAL_CELL_SHED	Sets the minimum number of phases to operate.
MFR_DPMx_THR	x=1-5. Sets the output current thresholds at which each phase is added.
DPM_HYSTERESIS	Sets the output current hysteresis used for dropping phases.

A phase add is triggered when the maximum between ($IOUT_{PEAK}$ – DPM_OFFSET) and $IOUT_{AVG}$ increases above the MFR_DPMx_THR threshold.

A phase drop is triggered when the maximum between ($IOUT_{PEAK}$ – DPM_OFFSET) and $IOUT_{AVG}$ decreases below (MFR_DPMx_THR – DPM_HYSTERESIS) where $IOUT_{PEAK}$ is the positive high of output current ripple and $IOUT_{AVG}$ is the average output current. Thus, DPM_OFFSET is used to compensate for the output current ripple so that the MFR_DPMx_THR thresholds corresponds to the average current. In general, the default value of DPM_OFFSET shall not be changed.

To disable the shedding function and operate with a fixed number of phases, set MFR_MANUAL_CELL_SHED = MFR_CELL_CONFIG.

Note that during ramp-up (Soft-on) and ramp-down (Soft-off) of output voltage the number of phases set by MFR_CELL_CONFIG is always operated, regardless of load level.

Efficiency simulation and optimization of shedding thresholds, based on operating conditions such as input and output voltage levels and temperature, can be made using the Flex Power Designer software.

Phase Shedding Protection

The DPM (Dynamic Phase Management) protection algorithm will increase the number of phases if the internal switching frequency increases over a certain threshold (internally fixed). It could be due to fast application of load or in static condition where the input to output voltage ratio is low. The purpose of the DPM protection function is to make sure the regulator always has enough headroom to increase frequency in response to a load transient.

DPM protection is enabled by default and the recommendation is to keep it turned on. The function can however be disabled or adjusted by system register DISABLE_DPM_PROT and PMBus command MFR_FSWITCH_PROTECT_COEFF.

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Electrical Specification Output section for each model provides the available output current versus ambient air temperature and air velocity at specified V_I.

The product is tested on a 254 x 254 mm test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 8 layers with average 70 µm (2 oz) copper thickness.

Note that the cooling via power pins does not only have to handle the power loss from the module. A low resistance between module and target device is of major importance to reduce additional power loss.

See Design Note 019 for further information.

Definition of Product Operating Temperature

The temperature at position P1 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperature above specified maximum measured at the specified position is not allowed and may cause permanent damage.

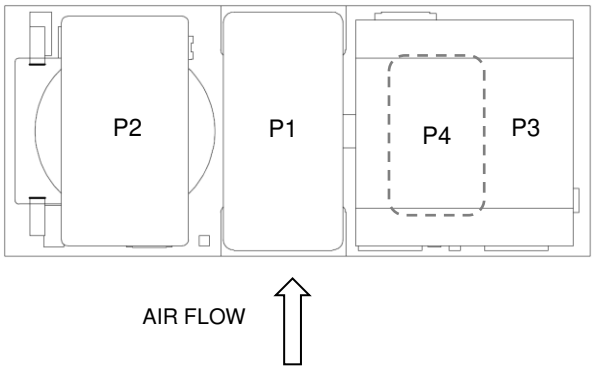
Note that the maximum value is the maximum operating temperature and that the provided Electrical Specification data is guaranteed up to T_{P1} = +95°C.

Position	Description	Max Temperature
P1	M2, Transformer core Reference point Hot spot	T_{P1} = 125°C
P2	M1, Inductor core Hot spot	T_{P2} = 125°C
P3	M3, Inductor core	T_{P3} = 125°C
P4	Power switches Hot spot	T_{P4} = 130°C

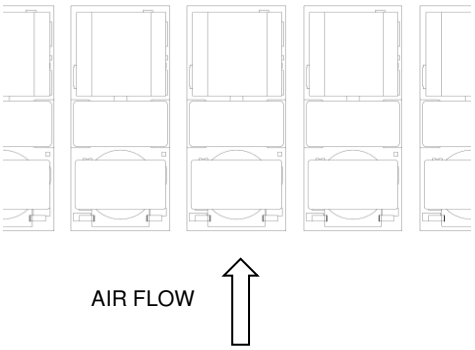
Depending on operating and thermal conditions, P1, P2 or P4 is the position with a limiting temperature (hot spot). Since it is difficult to access position P4, using an adjusted max limit for P1/P2 is a method to verify proper thermal conditions. Using a max temperature limit of 120°C for T_{P1}/T_{P2} will make sure that also T_{P4} stays below its maximum temperature.

Air Flow Direction

For a single Main device an air flow direction towards one of the long sides of the module should be chosen for best thermal performance. When several devices are grouped together side by side in multiphase operation an air flow direction towards the short sides of the modules should be chosen for best thermal performance. The recommended air flow directions are shown in the pictures below.



Temperature positions and air flow direction – Main only operation (top view).



Air flow direction – multiphase operation (top view).

Definition of Reference Temperature T_{P1}

The temperature at position P1 has been used as a reference temperature for the Electrical Specification data provided.

Over Temperature Protection (OTP)

The product is protected from thermal overload by an internal over temperature shutdown function monitoring the temperature in a point close to position P3.

The temperature is continuously monitored and when the temperature rises above the configured fault threshold level the product will respond as configured. The product can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup). See section Automatic Restart.

Default response is option 1. The default OTP limit is specified in Electrical Characteristics.

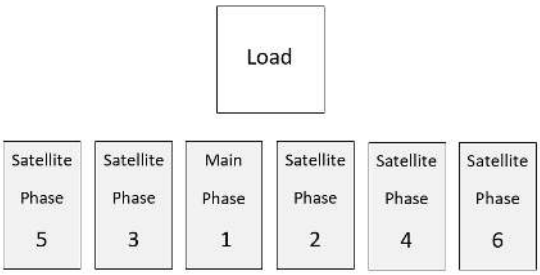
The OTP fault and warning limits and response are configured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE.

PCB Layout Consideration

The radiated EMI performance of the product will depend on the PCB layout and ground layer design. A ground plane shall be used, to increase the stray capacitance in the PCB and improve the high frequency EMC performance. The ground plane shall connect to the GND pins of the devices and the equipment ground or chassis.

Further layout recommendations are listed below.

1. For a multiphase rail layout should be as symmetrical as possible in order to give a good current balance between devices. Assuming that automatic phase shedding is not turned off, Main and Satellites should be placed in an interleaved manner, see illustration below. In this way power trains with the highest degree of operation (= the lower numbered phases) will have the lowest impedance to load.



Interleaving of Main/Satellite positions.

2. If possible use planes on several layers to carry V_I, V_O and ground. There should be a large number of vias close to the -IN, +IN, VOUT and GND pins in order to lower input and output impedances and improve heat spreading between the product and the host board.
3. The address pin strap resistor R_{SADDR} should be placed as close to the product as possible to minimize loops that may pick up noise. Avoid capacitive load on these signals as it may result in false pin strap reading. Also avoid current carrying planes under the pin strap resistor.
4. The external input capacitors, C_{I_EXT}, shall be placed as close to the input pins as possible and with low impedance connections, e.g. using via stitching around capacitors' terminals. See AN323 for more details.
5. The external output capacitors, C_{O_EXT}, should in general be placed close to the load. However typically you would like to place larger ceramic output capacitors close to the regulator module output in order to handle the output ripple current. See AN321 for more details. Low impedance connections must be used, e.g. via stitching around capacitors' terminals.
6. Care should be taken in the routing the following connections:

   Sense lines from the point of load to the S+ and S- terminals.

   Current sense lines CSPx/CSNx from Satellites to the Main.

   Temperature sense lines TMPx/TMN from Satellites to the Main.

   These sensing connections must be routed as a differential pair, preferably between ground planes which are not carrying high currents, to reduce noise susceptibility. The routing should avoid areas of switching signals or high electric or magnetic fields, e.g. keep away from PWMxX, PWMxY and STARTx signals.

BMR481 series Direct Conversion Input 40-60 V, Output 0.5 V to 1.35 V up to 70 A	28701-BMR481 revF	May 2022
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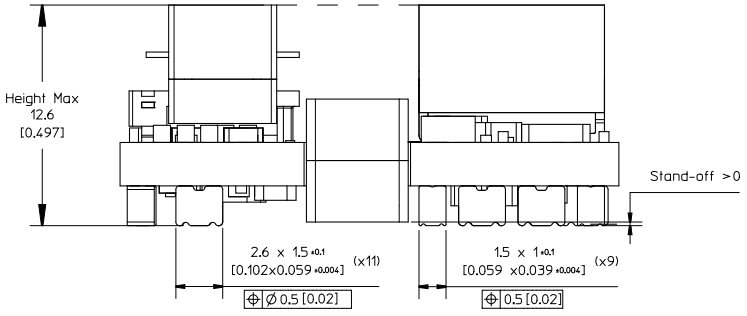
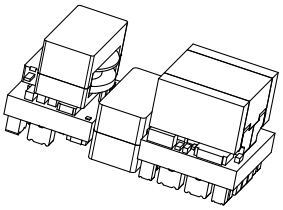
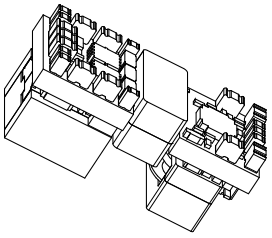
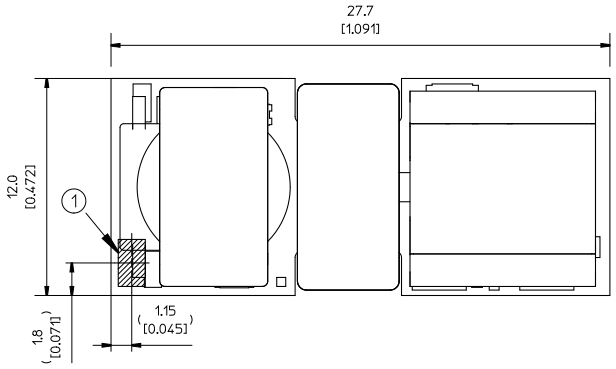
Mechanical Information – Satellite Unit





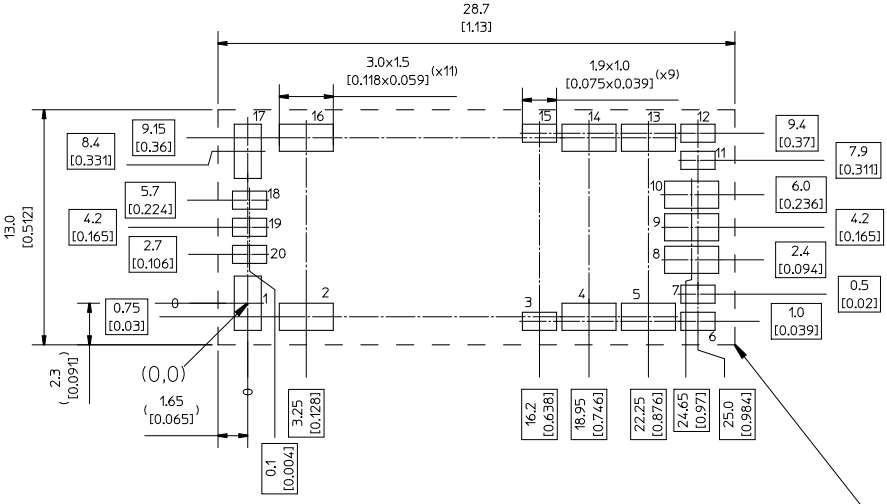


Pin positions according to recommended footprint



PIN SPECIFICATIONS
Material: C11000
Plating Min Au 0.1 µm over 2 µm Ni

Recommended footprint - Top view



Recommended keep away area for user components
The stand-off in combination with insulating material ensures that requirements as per IEC/EN/UL 62368-1 are met and 1500 V isolation maintained even if open vias and traces are present under the DC/DC converter

Weight: Typical 10 g
All dimensions in mm [inch]
Tolerances unless specified:
x.x ±0.50 [0.02]
x.xx±0.25 [0.01]
(not applied on footprint or typical values

BMR481 series Direct Conversion Input 40-60 V, Output 0.5 V to 1.35 V up to 70 A	28701-BMR481 revF	May 2022
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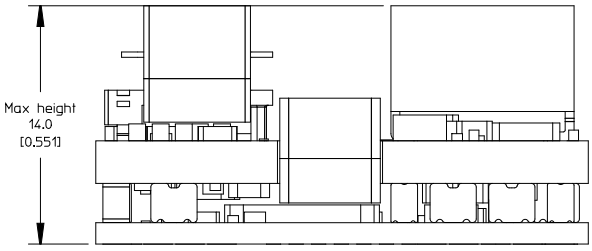
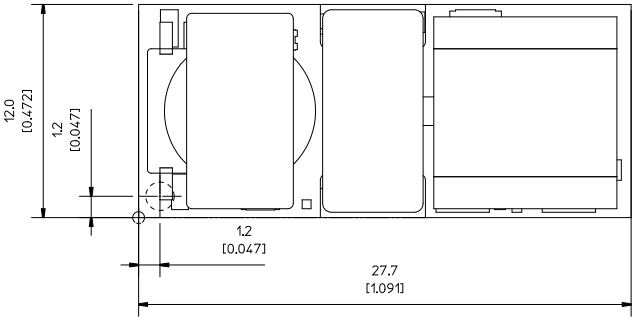
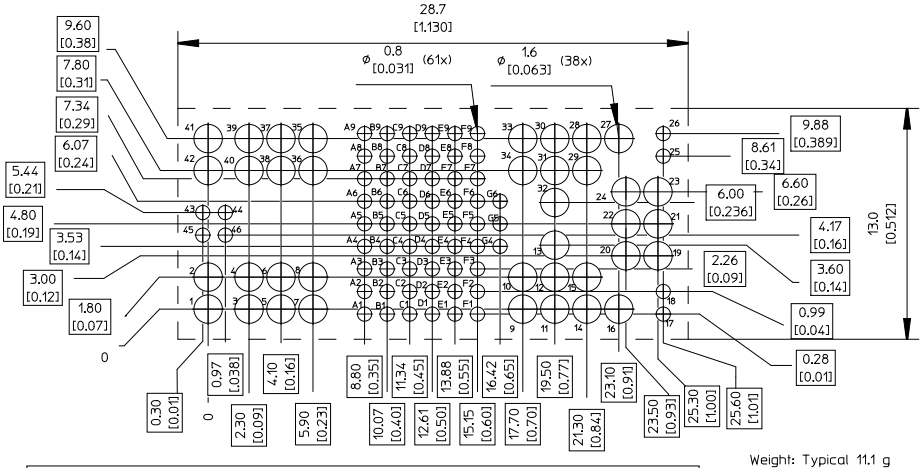
Mechanical Information – Main Unit



Pad position according to recommended footprint



Recommended footprint - Top view



Recommended keep away area for user components
The stand-off in combination with insulating material ensures that requirements as per IEC/EN/UL 62368-1 are met and 1500 V isolation maintained even if open vias and traces are present under the DC/DC converter

Weight: Typical 11.1 g
All dimensions in mm [inch]
Tolerances unless specified:
x.x ±0.50 [0.02]
x.xx±0.25 [0.01]
(not applied on footprint or typical values)

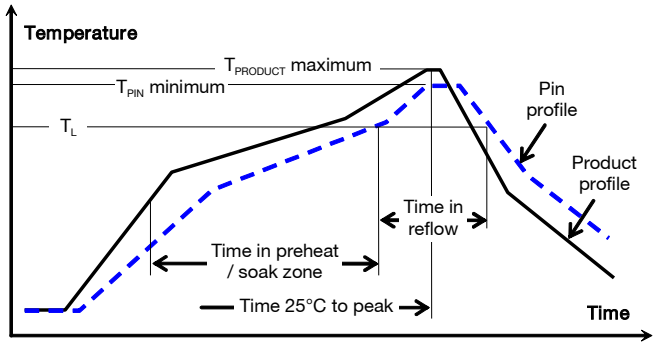
Main Product Soldering Information - Surface Mounting

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PCB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up ($T_{PRODUCT}$)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		60 s	60 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	245°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Near pad number 7 or 35 is chosen as reference location for the minimum pin temperature recommendation since these will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L, 183°C for Sn63Pb37) for more than 60 seconds and a peak temperature of 210°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, 217 to 221°C for SnAgCu solder alloys) for more than 30 seconds and a peak temperature of 235°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PCB near pad 44 is chosen as reference locations for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since these will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020E.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020E.

During reflow $T_{PRODUCT}$ must not exceed 245 °C at any time.

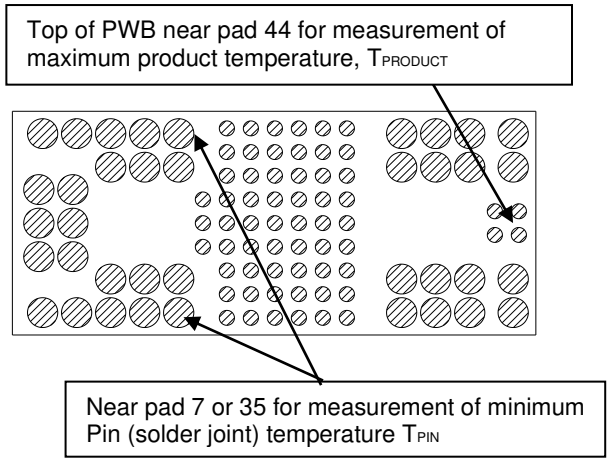
Dry Pack Information

Surface mounted versions of the products are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

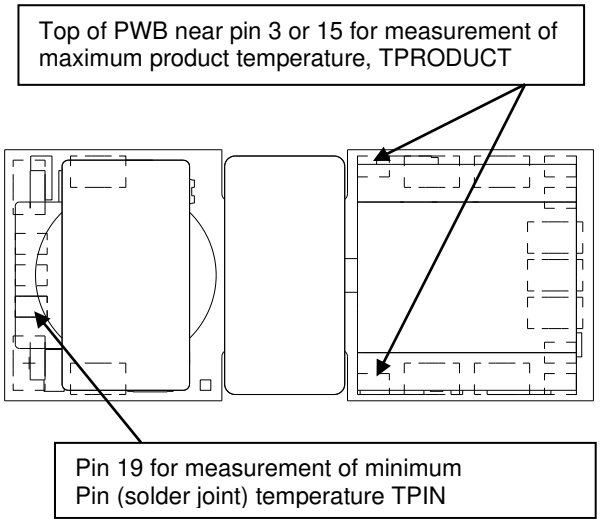
Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Thermocouple Attachment

Main



Satellite



Surface Mount Assembly and Repair

The LGA of the product require particular care during assembly since the LGA´s are hidden between the host board and the product's PCB. Special procedures are required for successful rework of these products.

Assembly

Automatic pick and place equipment should be used to mount the product on the host board. The use of a vision system, utilizing the fiducials on the bottom side of the product, will ensure adequate accuracy. Manual mounting of solder bump products is not recommended.

This module is **not** recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Repair

For a successful repair (removal and replacement) of a LGA product, a dedicated rework system should be used. The rework system should preferably utilize a reflow station and a bottom side heater might also be needed for the operation.

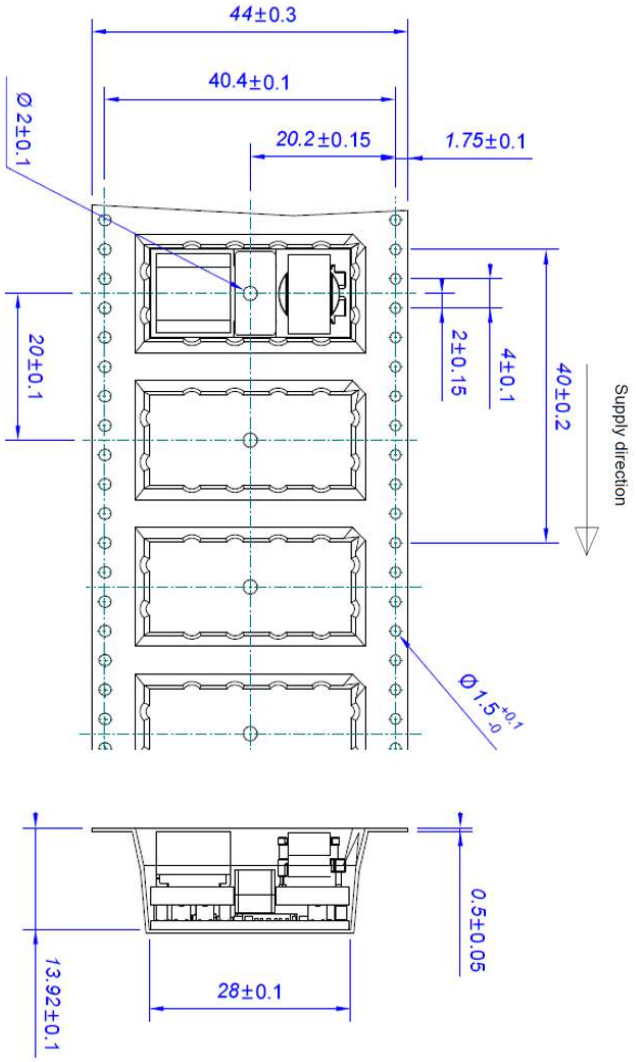
The product is an open frame design with a pick-up surface on a large central component (in this case the choke). This pick-up surface can be used for removal of the module provided that it is glued against module PCB before removal to prevent it from separating from the module PCB.

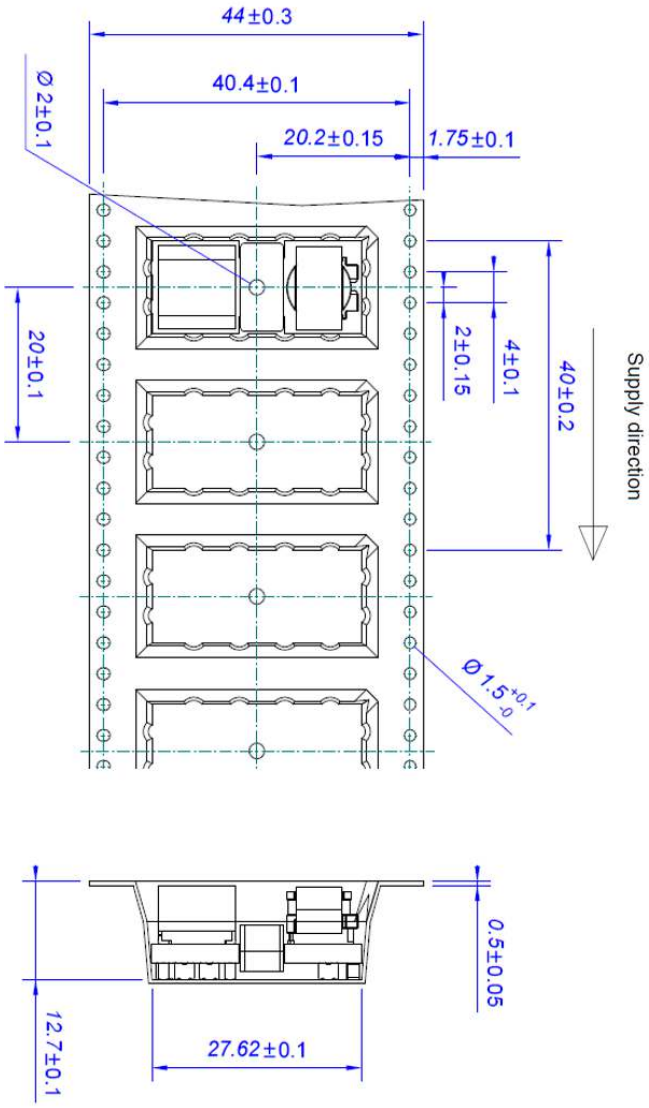
Delivery Package Information

Both Main and Satellite products are delivered in antistatic carrier tape (EIA 481 standard).

Carrier Tape Specifications - **Main**	
Material	PS, antistatic
Surface resistance	< 10^{11} Ohm/square
Bakeability	The tape is not bakeable
Tape width, W	44 mm [1.73 inch]
Pocket pitch, P_1	20 mm [0.79 inch]
Pocket depth, K_0	13.92 mm [0.55 inch]
Reel diameter	330 mm [13 inch]
Reel capacity	200 products /reel
Reel weight - main	2500 g/full reel

Carrier Tape Specifications - **Satellite**	
Material	PS, antistatic
Surface resistance	< 10^{11} Ohm/square
Bakeability	The tape is not bakeable
Tape width, W	44 mm [1.73 inch]
Pocket pitch, P_1	20 mm [0.79 inch]
Pocket depth, K_0	12.7mm [0. 5 inch]
Reel diameter	330 mm [13 inch]
Reel capacity	250 products /reel
Reel weight - satellite	2900 g/full reel





Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Temperature shock	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 200 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity [1]	J-STD-020E	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 245°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat [2]	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td [1] IEC 60068-2-20 test Ta [2]	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each direction

Notes
[1] Only for products intended for reflow soldering (surface mount products & pin-in paste[3] products)
[2] Only for products intended for wave soldering (plated through hole products)
[3] Pin-in paste refers to hole mounted products that utilizes reflow soldering

Template for PMBus Command Appendix

This appendix contains a detailed reference of the PMBus commands supported by the product.

Data Formats
The products make use of a few standardized numerical formats, along with custom data formats. A detailed walkthrough of the above formats is provided in AN304, as well as in sections 7 and 8 of the PMBus Specification Part II. The custom data formats vary depending on the command, and are detailed in the command description.

Standard Commands
The functionality of commands with code 0x00 to 0xCF is usually based on the corresponding command specification provided in the PMBus Standard Specification Part II (see Power System Management Bus Protocol Documents below). However there might be different interpretations of the PMBus Standard Specification or only parts of the Standard Specification applied, thus the detailed command description below should always be consulted.

Forum Websites
The System Management Interface Forum (SMIF)
http://www.powersig.org/
The System Management Interface Forum (SMIF) supports the rapid advancement of an efficient and compatible technology base that promotes power management and systems technology implementations. The SMIF provides a membership path for any company or individual to be active participants in any or all of the various working groups established by the implementer forums.

Power Management Bus Implementers Forum
(PMBUS-IF)
http://pmbus.org/
The PMBus-IF supports the advancement and early adoption of the PMBus protocol for power management. This website offers recent PMBus specification documents, PMBus articles, as well as upcoming PMBus presentations and seminars, PMBus Document Review Board (DRB) meeting notes, and other PMBus related news.

PMBus – Power System Management Bus Protocol Documents
These specification documents may be obtained from the PMBus-IF website described above. These are required reading for complete understanding of the PMBus implementation. This appendix will not re-address all of the details contained within the two PMBus Specification documents.

Specification Part I – General Requirements Transport And Electrical Interface
Includes the general requirements, defines the transport and electrical interface and timing requirements of hard wired signals.

Specification Part II – Command Language
Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

SMBus – System Management Bus Documents
System Management Bus Specification, Version 2.0, August 3, 2000
This specification specifies the version of the SMBus on which Revision 1.2 of the PMBus Specification is based. This specification is freely available from the System Management Interface Forum Web site at:
http://www.smbus.org/specs/

PMBus Command Summary and Factory Default Values of Standard Configuration

The factory default values provided in the table below are valid for the Standard configuration. Factory default values for other configurations can be found using the Flex Power Designer tool.

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 481 X021/002 R1	
0x01	OPERATION	R/W Byte	0x48	
0x02	ON_OFF_CONFIG	R/W Byte	0x16	
0x03	CLEAR_FAULTS	Send Byte		
0x10	WRITE_PROTECT	R/W Byte	0x00	
0x11	STORE_DEFAULT_ALL	Send Byte		
0x12	RESTORE_DEFAULT_ALL	Send Byte		
0x19	CAPABILITY	Read Byte		
0x1B	SMBALERT_MASK (STATUS_BYTE)	SMBAlert Mask	0x80	
0x1B	SMBALERT_MASK (STATUS_VOUT)	SMBAlert Mask	0x08	
0x1B	SMBALERT_MASK (STATUS_IOUT)	SMBAlert Mask	0x2A	
0x1B	SMBALERT_MASK (STATUS_INPUT)	SMBAlert Mask	0x00	
0x1B	SMBALERT_MASK (STATUS_TEMPERATURE)	SMBAlert Mask	0x40	
0x1B	SMBALERT_MASK (STATUS_CML)	SMBAlert Mask	0xF1	
0x1B	SMBALERT_MASK (STATUS_MFR_SPECIFIC)	SMBAlert Mask	0xFD	
0x20	VOUT_MODE	Read Byte		
0x21	VOUT_COMMAND	R/W Word	0x0097	
0x24	VOUT_MAX	R/W Word	0x00E7	
0x25	VOUT_MARGIN_HIGH	R/W Word	0x00A1	
0x26	VOUT_MARGIN_LOW	R/W Word	0x008D	
0x28	VOUT_DROOP	R/W Word	0xD000	
0x35	VIN_ON	R/W Word	0xE92C	
0x40	VOUT_OV_FAULT_LIMIT	Read Word		
0x41	VOUT_OV_FAULT_RESPONSE	Read Byte	0x80	
0x44	VOUT_UV_FAULT_LIMIT	Read Word		
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	0x80	
0x46	IOUT_OC_FAULT_LIMIT	R/W Word	0xF8A0	
0x47	IOUT_OC_FAULT_RESPONSE	R/W Byte	0x80	
0x4A	IOUT_OC_WARN_LIMIT	R/W Word	0xF896	
0x4F	OT_FAULT_LIMIT	R/W Word	0xF208	
0x50	OT_FAULT_RESPONSE	R/W Byte	0x80	
0x51	OT_WARN_LIMIT	R/W Word	0xF1CC	
0x55	VIN_OV_FAULT_LIMIT	R/W Word	0xEA08	
0x56	VIN_OV_FAULT_RESPONSE	R/W Byte	0x80	
0x59	VIN_UV_FAULT_LIMIT	R/W Word	0xE918	
0x5A	VIN_UV_FAULT_RESPONSE	R/W Byte	0x00	
0x60	TON_DELAY	R/W Byte	0x00	
0x68	POUT_OP_FAULT_LIMIT	R/W Word	0x0837	
0x69	POUT_OP_FAULT_RESPONSE	R/W Byte	0x00	
0x78	STATUS_BYTE	Read Byte		
0x79	STATUS_WORD	Read Word		
0x7A	STATUS_VOUT	Read Byte		
0x7B	STATUS_IOUT	Read Byte		
0x7C	STATUS_INPUT	Read Byte		
0x7D	STATUS_TEMPERATURE	Read Byte		
0x7E	STATUS_CML	Read Byte		
0x80	STATUS_MFR_SPECIFIC	Read Byte		
0x88	READ_VIN	Read Word		
0x8B	READ_VOUT	Read Word		
0x8C	READ_IOUT	Read Word		
0x8D	READ_TEMPERATURE_1	Read Word		
0x96	READ_POUT	Read Word		

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 481 X021/002 R1	
0x98	PMBUS_REVISION	Read Byte		
0x99	MFR_ID	Read Block3	Unit Specific	
0x9A	MFR_MODEL	Read Block8	Unit Specific	
0x9B	MFR_REVISION	Read Block3	Unit Specific	
0x9D	MFR_DATE	Read Block4	Unit Specific	
0xB0	USER_DATA_00	Read Word	Unit Specific	
0xB1	USER_DATA_01	Read Word	Unit Specific	
0xD1	MFR_AVERAGE_TIME_SCALE	R/W Byte	0x06	
0xD2	MFR_READ_VOUT	Read Word		
0xD3	MFR_IOUT_CAL_OFFSET	R/W Word	0x0000	0 ADC steps
0xD4	MFR_VOUT_CAL_OFFSET	R/W Word	0x0066	
0xD6	MFR_PID	R/W Block7	0x00032400100064	
0xD7	MFR_FILT_PRE_POST	R/W Word	0x2A2B	
0xD9	MFR_DUTY_PARAMETER	R/W Block3	0x000000	
0xDA	MFR_UNLOCK	Write Block5		
0xDB	MFR_LOCK	Send Byte		
0xDC	MFR_FAULT_CONFIG	R/W Word	0x02C7	
0xDE	MFR_IMON	R/W Byte	0x21	
0xDF	MFR_STORE_MAP	Write Byte		
0xE0	MFR_RESTORE_MAP	Send Byte		
0xE4	MFR_CELL_CONFIG	R/W Byte	0x00	
0xE5	MFR_OV_LIMIT_OFFSET	R/W Byte	0x02	
0xE6	MFR_UV_LIMIT_OFFSET	R/W Byte	0x02	
0xE7	MFR_VBOOT_SET	R/W Word	0x0097	
0xE8	MFR_SVI_PMBUS_SELECT	R/W Byte	0x01	
0xE9	MFR_ICC_MAX_ADD	R/W Byte	0x00	
0xEA	MFR_PWR_IN_MAX_ADD	R/W Byte	0x00	
0xEB	MFR_PWR_IN_ALERT_ADD	R/W Byte	0x00	
0xEF	MFR_READ_PIN_PUC	Read Word		
0xF0	MFR_READ_VIN_PUC	Read Word		
0xF1	MFR_DPM1_THR	R/W Word	0xF858	
0xF2	MFR_DPM2_THR	R/W Word	0xF89A	
0xF3	MFR_DPM3_THR	R/W Word	0xF8D8	
0xF4	MFR_DPM4_THR	R/W Word	0xF91C	
0xF5	MFR_DPM5_THR	R/W Word	0xF954	
0xF6	MFR_FSWITCH_PROTECT_COEFF	R/W Byte	0x0F	
0xF7	MFR_CS_PROP_INTEGR	R/W Word	0x0000	
0xF9	MFR_KK_FEEDFRWD_GAIN_CTRL	R/W Block6	0x000022DBB301	
0xFA	MFR_VOUT_TRIM	R/W Byte	Unit Specific	
0xFB	MFR_MANUAL_CELL_SHED	R/W Word	0x0409	
0xFE02	MFR_SVID_TEMPZONE	R/W Byte		
0xFE03	MFR_SVID_IOUT	R/W Byte		
0xFE04	MFR_SVID_VIDSETTING	R/W Word		
0xFE05	MFR_SVID_PWRSTATE	R/W Byte		
0xFE06	MFR_SVID_OFFSET	R/W Byte	0x00	
0xFE07	MFR_START_THREAD	R/W Block3		
0xFE08	MFR_SVID_ICCMAX	R/W Byte	0x00	
0xFE09	MFR_SVID_TEMPMAX	R/W Byte	0x00	
0xFE0A	MFR_SVID_SRFAST	R/W Byte	0x00	
0xFE0B	MFR_SVID_SRSLOW	R/W Byte	0x00	
0xFE0C	MFR_SVID_MULTI_VR_CONFIG	R/W Byte		
0xFE0D	MFR_SVID_VOUTMAX	R/W Byte	0x01	1 V
0xFE0E	MFR_SVID_SLOW_SR_SELECTOR	R/W Byte	0x84	
0xFE0F	MFR_SVID_PIN_MAX	R/W Byte	0x00	
0xFE10	MFR_SVID_PIN_ALERT_THR	R/W Byte	0x00	
0xFE11	MFR_SVID_WP0	R/W Byte		
0xFE12	MFR_SVID_WP1	R/W Byte		
0xFE13	MFR_SVID_WP2	R/W Byte		

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 481 X021/002 R1	
0xFE14	MFR_SVID_WP3	R/W Byte		
0xFE15	MFR_SVID_WP4	R/W Byte		
0xFE16	MFR_RD_TEMPERATURE_PHASE1	Read Word		
0xFE17	MFR_RD_TEMPERATURE_PHASE2	Read Word		
0xFE18	MFR_RD_TEMPERATURE_PHASE3	Read Word		
0xFE19	MFR_RD_TEMPERATURE_PHASE4	Read Word		
0xFE1A	MFR_RD_TEMPERATURE_PHASE5	Read Word		
0xFE1B	MFR_RD_TEMPERATURE_PHASE6	Read Word		
0xFE1C	MFR_CTRL_ID	Read Word		
0xFE1E	MFR_SVID_REGLOCK	R/W Byte		
0xFE20	MFR_SECT_L	R/W Block8		
0xFE21	MFR_SECT_H	R/W Block8		
0xFE24	MFR_SECT_RD	Write Byte		
0xFE25	MFR_SECT_WR	Write Byte		
0xFE26	MFR_MEMORY_WORD	R/W Block8		
0xFE27	MFR_MEMORY_RD	Write Block3		
0xFE28	MFR_MEMORY_WR	Write Block4		
0xFE29	MFR_READ_BLACKBOX	Send Byte		
0xFE2A	MFR_BLACKBOX	Read Block16		
0xFE2B	MFR_CLEAR_BB	Send Byte		
0xFE2C	MFR_CONFIG_BBR	R/W Word	0x0000	
0xFE2E	MFR_PROTECT_DEFAULT	R/W Byte	0x00	
0xFE2F	MFR_POUT_THREAD	Read Block4		
0xFE30	MFR_PMBUSCFG_REVISION	R/W Word	0000	
0xFE31	MFR_PMBUSCFG_TIMESTAMP	Read Block8	Unit Specific	
0xFE32	MFR_PEAK_FAULT_RESPONSE	R/W Byte	0x00	
0xFE33	MFR_PMBUSCFG_USERID	R/W Word	0000	

System Registers

Offset	Name	Factory Default Value Standard Configuration BMR 481 X021/002 R1
0xA408	CURRENT_SHARING_RESET	0x66
0xA40B	HIGH_CURR_PROT_EN	0x16
0xA40D	AVS_CONFIG	0x28
0xA418	HIZ_HALFB_SYMMETRIC	0x34
0xB006	CTRL_PFM_ENA_PS	0x03
0xB007	DPM_HYSTERESIS	0x0E
0xB00C	DVID_SR_FAST_STEP	0x1F
0xB00D	DVID_SR_SLOW_STEP	0x1F
0xB00E	DVID_VAR_OFFSET_PARAM	000000800000
0xB018	TEL_GAIN_VIN	0x80
0xB01A	THERMAL_GAIN	0x73
0xB01B	TEL_IOUT_FSR	0x002B
0xB027	TEL_OFFSET_VIN	0x0000
0xB029	TEL_GAIN_IMON	0x98
0xB02B	SVI_ADDITIONAL_OFFSET	0x09
0xB038	VIN_FEED_FWD_SOURCE	0x01
0xB039	VIN_MONITORING_SOURCE	0x01
0xB03C	IOUT_VR125_PERC_EN	0x01
0xB040	VR13_TIME_FRAME	0x00
0xB041	CTRL_VERR_CLAMP	0x00
0xB044	DISABLE_DPM_PROT	0x00
0xB046	TGB_CONFIG	0x00
0xB047	VDROOP_CONFIG	0x00
0xB04A	TON_RED_CONFIG	0x08
0xB04B	EN_DROOP_START	0x00
0xB04E	CS_OVERFLOW_DISABLE_IRQ	0x01
0xB051	VR_READY_FAST_DISABLE	0x00
0xB057	MULTIFUNCTION_PIN_MUX	0x04
0xB05E	MONITOR_OFFSET	Unit Specific
0xB063	EXTRA_OFFSET	0x00
0xB064	DPM_OFFSET	0x0E

PMBus Command Details

OPERATION (0x01)
Description: Sets the desired PMBus enable and margin operations.

Bit	Function	Description	Value	Function	Description
7:6	Enable	Make the device enable or disable.	00	Immediate Off	Disable immediately without controlled ramp-down or sequencing.
			01	Soft Off	Disable by controlled ramp-down timings or sequencing.
			10	Enable	Enable device to the set voltage or margin state, using ramp up timings / sequencing.
5:4	Output Voltage Source	Select between margin high/low states or nominal output, and control by AVSBus.	00	Nominal	Operate at nominal output voltage given by VOUT_COMMAND.
			01	Margin Low	Operate at margin low voltage set in VOUT_MARGIN_LOW.
			10	Margin High	Operate at margin high voltage set in VOUT_MARGIN_HIGH.
			11	AVSBus	Operate at voltage set by AVSBus.
3:2	Act on Fault	Set 10b to act on fault or set to 01b to ignore fault.	10	Act on Faults	Act on Faults when in a margined state. The device will handle appropriate overvoltage/under voltage warnings and faults and respond as programmed by the warning limit or fault response command.
1	AVSBus to PMBus transition	Controls how the nominal output voltage command is updated, or not, when control is passed from the AVSBus to the PMBus.	1	VOUT_COMMAND updated	VOUT_COMMAND value is updated upon transfer of control from AVSBus to the PMBus
			0	VOUT_COMMAND not updated	VOUT_COMMAND value is not updated upon transfer of control from AVSBus to the PMBus

ON_OFF_CONFIG (0x02)
Description: Configures how the device is controlled by the CTRL pin and the PMBus.

Bit	Function	Description	Value	Function	Description
4	Powerup Operation	Sets the default to either operate any time power is present or for the on/off to be controlled by CTRL pin and PMBus commands.	0	Enable Always	Unit powers up any time power is present regardless of state of the CTRL pin.
			1	CTRL pin and/or PMBus	Unit does not power up until commanded by the CTRL pin and/or OPERATION command.
3	PMBus Enable Mode	Controls how the unit responds to commands received via the PMBus.	0	Ignore PMBus command	Unit ignores the on/off portion of the OPERATION command from serial bus.
			1	Use PMBus command	To start, the unit requires that the on/off portion of the OPERATION command is instructing the unit to run.
2	Enable Pin Mode	Controls how the unit responds to the CTRL pin.	0	Ignore CTRL pin	Unit ignores the CTRL pin.
			1	Use CTRL pin	Unit requires the CTRL pin to be asserted to start the unit.
1	Enable Pin Polarity	Polarity of the CTRL pin.	1	Active High	CTRL pin will cause device to enable when driven high.

CLEAR_FAULTS (0x03)
Description: Clears all fault status bits

WRITE_PROTECT (0x10)
Description: The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. This command is stored in NVM but not included in a MFR_STORE_MAP operation (STORE_DEFAULT_ALL must be used).

Bit	Description	Value	Function	Description
7:0	All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.	0x80	Disable all writes	Disable all writes except to the WRITE_PROTECT command.
		0x40	Enable operation	Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands.
		0x20	Enable control and Vout commands	Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands.
		0x00	Enable all commands	Enable writes to all commands.

STORE_DEFAULT_ALL (0x11)
Description: Commands the device to store its configuration into the Default Store.

RESTORE_DEFAULT_ALL (0x12)
Description: Commands the device to restore its configuration from the Default Store.

CAPABILITY (0x19)
Description: Reads back the supported SMBus features

Bit	Description	Format
7:0	Reads back the supported SMBus features	Byte Array

SMBALERT_MASK (0x1B)
Status Registers: STATUS_BYTE (0x78), STATUS_VOUT (0x7A), STATUS_IOUT (0x7B), STATUS_INPUT (0x7C), STATUS_TEMPERATURE (0x7D), STATUS_CML (0x7E), STATUS_MFR_SPECIFIC (0x80)
Description: The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Mask Bit 7		0	Pull SALERT	
			1	Ignore	
6	Mask Bit 6		0	Pull SALERT	
			1	Ignore	
5	Mask Bit 5		0	Pull SALERT	
			1	Ignore	
4	Mask Bit 4		0	Pull SALERT	
			1	Ignore	
3	Mask Bit 3		0	Pull SALERT	
			1	Ignore	
2	Mask Bit 2		0	Pull SALERT	
			1	Ignore	
1	Mask Bit 1		0	Pull SALERT	
			1	Ignore	
0	Mask Bit 0		0	Pull SALERT	
			1	Ignore	

VOUT_MODE (0x20)
Description: Controls how future VOUT-related commands parameters will be interpreted.

Bit	Function	Description	Value	Function	Description
7:5	Vout mode	Selection of mode for representation of output voltage parameters.	000	Linear	Linear Mode Format.
			001	VID	VID Mode.
			010	Direct	Direct Mode.
4:0	VID code identifier	Five bit VID code identifier. See SVID_IFC_CONF description.	00000	AVSBus	AVSBus Vout mode.
			00011	Intel	Intel Vout mode.

VOUT_COMMAND (0x21)
Description: Commands the device to transition to a new output voltage.

Bit	Description	Format	Unit
9:0	Sets the nominal output voltage value [VID] - Data need to be compliant with format specified in VOUT_MODE. In AVS domain see specifications of OPERATION command. In SVI domain, the command is acknowledged and information stored.	Fixed Point Unsigned	V

VOUT_MAX (0x24)
Description: Configures the maximum allowed output voltage.

Bit	Description	Format	Unit
9:0	Sets the maximum possible value setting of VOUT.	Fixed Point Unsigned	V

VOUT_MARGIN_HIGH (0x25)
Description: Configures the target for margin-up commands.

Bit	Description	Format	Unit
9:0	Sets the value of the VOUT during a margin high.	Fixed Point Unsigned	V

VOUT_MARGIN_LOW (0x26)
Description: Configures the target for margin-down commands.

Bit	Description	Format	Unit
9:0	Sets the value of the VOUT during a margin low.	Fixed Point Unsigned	V

VOUT_DROOP (0x28)
Description: Sets the effective load line (V/I slope) for the rail in which the device is used. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -6 (0b11010).

Bit	Description	Format	Unit
7:0	LSB = 0.015625 mV/A.	Fixed Point Unsigned	mV/A

VIN_ON (0x35)
Description: Input voltage must be above this level before the output can be enabled. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -3 (0b11101).

Bit	Description	Format	Unit
9:0	LSB = 0.125 V	Fixed Point Unsigned	V

VOUT_OV_FAULT_LIMIT (0x40)
Description: Reads the absolute Vout over-voltage fault threshold computed as: Vout target - MFR_OV_LIMIT_OFFSET The returned value is valid only when regulation of Vout is enabled. To change the threshold, MFR_OV_LIMIT_OFFSET should be changed.

Bit	Description	Format	Unit
15:0	LSB = 0.00390625 V.	Linear	V

VOUT_OV_FAULT_RESPONSE (0x41)
Description: Sets the VOUT OV fault response. Always set to 0x80 (thus cannot be ignored).

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

VOUT_UV_FAULT_LIMIT (0x44)
Description: Reads the absolute Vout under-voltage fault threshold computed as: Vout target - MFR_UV_LIMIT_OFFSET - VOUT_DROOP*Iout The returned value is valid only when regulation of Vout is enabled. To change the threshold, MFR_UV_LIMIT_OFFSET should be changed.

Bit	Description	Format	Unit
15:0	LSB = 0.00390625 V.	Linear	V

VOUT_UV_FAULT_RESPONSE (0x45)
Description: Sets the VOUT UV LIMIT Response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

IOUT_OC_FAULT_LIMIT (0x46)
Description: Sets the output over-current fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

IOUT_OC_FAULT_RESPONSE (0x47)
Description: Sets the IOUT OC LIMIT Response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

IOUT_OC_WARN_LIMIT (0x4A)
Description: Sets the output over-current warning limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

OT_FAULT_LIMIT (0x4F)
Description: Sets the over-temperature fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110).

Bit	Description	Format	Unit
9:0	LSB = 0.25 Celsius Degrees.	Fixed Point Unsigned	°C

OT_FAULT_RESPONSE (0x50)
Description: Sets the over-temperature fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

OT_WARN_LIMIT (0x51)
Description: Sets the over-temperature warning limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110).

Bit	Description	Format	Unit
9:0	LSB = 0.25 Celsius Degrees.	Fixed Point Unsigned	°C

VIN_OV_FAULT_LIMIT (0x55)
Description: Sets the input over-voltage fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -3 (0b11101).

Bit	Description	Format	Unit
9:0	LSB = 0.125 V.	Fixed Point Unsigned	V

VIN_OV_FAULT_RESPONSE (0x56)
Description: Sets the input over-voltage fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

VIN_UV_FAULT_LIMIT (0x59)
Description: Sets the input under-voltage fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -3 (0b11101).

Bit	Description	Format	Unit
9:0	LSB = 0.125 V.	Fixed Point Unsigned	V

VIN_UV_FAULT_RESPONSE (0x5A)
Description: Sets the input under-voltage fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

TON_DELAY (0x60)
Description: Sets the turn-on delay time

Bit	Description	Format	Unit
7:0	Sets the delay time from ENABLE to start of the rise of the output voltage. The time can range from 0 ms up to 127.5 ms. For a current sharing group this range is valid if PMBus enable or CTRL pin enable is used. LSB = 0.5 ms.	Fixed Point Unsigned	ms

POUT_OP_FAULT_LIMIT (0x68)
Description: Sets the Output power over-power fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = 1 (0b00001).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	W

POUT_OP_FAULT_RESPONSE (0x69)
Description: Sets the output power Over-Power fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

STATUS_BYTE (0x78)
Description: Returns a brief fault/warning status byte.

Bit	Function	Description	Value	Description
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No fault
			1	Fault
6	Off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	0	No fault
			1	Fault
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No fault
			1	Fault
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No fault
			1	Fault
3	Vin under voltage Fault	An input under voltage fault has occurred.	0	No fault
			1	Fault
2	Temperature	A temperature fault or warning has occurred.	0	No fault
			1	Fault
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault
			1	Fault
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred.	0	No fault
			1	Fault

STATUS_WORD (0x79)
Description: Returns an extended fault/warning status byte.

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has occurred.	0	No fault
			1	Fault
14	Iout/Pout	An output current or output power fault or warning has occurred.	0	No Fault.
			1	Fault.
13	Input	An input voltage, input current, or input power fault or warning has occurred.	0	No Fault.
			1	Fault.
12	Mfr	A manufacturer specific fault or warning has occurred.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No Fault.
			1	Fault.
6	Off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	0	No Fault.
			1	Fault.
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No Fault.
			1	Fault.
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No Fault.
			1	Fault.
3	Vin under voltage Fault	An input under voltage fault has occurred.	0	No Fault.
			1	Fault.
2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault.
			1	Fault.
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred.	0	No fault.
			1	Fault.

STATUS_VOUT (0x7A)
Description: Returns Vout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vout Overvoltage Fault	Vout Overvoltage Fault.	0	No Fault.
			1	Fault.
4	Vout under voltage Fault	Vout under voltage Fault.	0	No Fault.
			1	Fault.
3	Vout Max Warning	Vout Max Warning (An attempt has been made to set the output voltage to value higher than allowed by the Vout Max command (Section 13.5).	0	No Warning.
			1	Warning.

STATUS_IOUT (0x7B)
Description: Returns Iout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Iout Overcurrent Fault	Iout Overcurrent Fault.	0	No Fault.
			1	Fault.
5	Iout Overcurrent Warning	Iout Overcurrent Warning.	0	No Fault.
			1	Fault.
3	Current Sharing Unbalance Warning	Triggered when difference in monitored current from two phases is higher than the limit set by MFR_CS_CELL_WARN_LIMIT.	0	No Fault.
			1	Fault.
1	Pout Over Power Fault	Pout Over Power Fault.	0	No Fault.
			1	Fault.

STATUS_INPUT (0x7C)
Description: Returns VIN/IIN-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vin Overvoltage Fault	Vin Overvoltage Fault.	0	No Fault.
			1	Fault.
4		Vin under voltage Fault.	0	No Fault.

Bit	Function	Description	Value	Description
	Vin under voltage Fault		1	Fault.

STATUS_TEMPERATURE (0x7D)
Description: Returns the temperature-related fault/warning status bits

Bit	Function	Description	Value	Description
7	Overtemperature Fault	Overtemperature Fault.	0	No Fault.
			1	Fault.
6	Overtemperature Warning	Overtemperature Warning.	0	No Warning.
			1	Warning.

STATUS_CML (0x7E)
Description: Returns Communication/Logic/Memory-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	0	No Invalid Command Received.
			1	Invalid Command Received.
6	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	0	No Invalid Data Received.
			1	Invalid Data Received.
5	Packet Error Check Failed	Packet Error Check Failed.	0	No Failure.
			1	Failure.
4	Memory Fault Detected	Memory Fault Detected. Set if CRC check fails at boot-up.	0	No Fault.
			1	Fault.
0	Other Memory Or Logic Fault	Other Memory Or Logic Fault has occurred.	0	No Fault.
			1	Fault.

STATUS_MFR_SPECIFIC (0x80)
Description: Returns manufacturer specific status information.

Bit	Function	Description	Value	Description
7	Black box full	Black box full	0	No Fault.
			1	Fault.
6	Catastrophic fault precursor	Catastrophic fault precursor	0	No Fault.
			1	Fault.
5	NVM status(1)	NVM status(1)	0	No Fault.
			1	Fault.
4	NVM status(0)	NVM status(0)	0	No Fault.
			1	Fault.
3	VSRMON peak fault	VSRMON peak threshold reached.	0	No Fault.
			1	Fault.
2	Patch code download (from I2C)	Patch code download (from I2C)	0	No Fault.
			1	Fault.
1	Feedback disconnection	Feedback disconnection fault = +S vs VOUT voltage difference is too high.	0	No Fault.
			1	Fault.
0	PUC CRC Fault	PUC CRC Fault	0	No Fault.
			1	Fault.

READ_VIN (0x88)
Description: Returns the input voltage reading, value averaged over configured MFR_AVERAGE_TIME_SCALE. Input voltage source configured by System Register VIN_MONITORING_SOURCE.

Bit	Description	Format	Unit
15:0	LSB=0.125 V.	Linear	V

READ_VOUT (0x8B)
Description: Returns the measured output voltage, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	VID code, see section Output Voltage Format.	Fixed Point Unsigned	V

READ_IOUT (0x8C)
Description: Returns the measured output current, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	LSB weight is given by System Register IOUT_EXP.	Linear	A

READ_TEMPERATURE_1 (0x8D)
Description: Returns the max temperature read from Main/Satellites (and from primary reporting through PuC, if enabled).

Bit	Description	Format	Unit
15:0	LSB=0.25 degree C.	Linear	°C

READ_POUT (0x96)
Description: Returns the computed output power, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	LSB weight is given by System Register IOUT_EXP.	Linear	W

PMBUS_REVISION (0x98)
Description: Returns the PMBus revision number for this device.

Bit	Description	Format
7:0	Returns the PMBus revision number for this device. Returns 0x22, formatted as per PMBus specification.	ASCII

MFR_ID (0x99)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
23:0		ASCII

MFR_MODEL (0x9A)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
63:0		ASCII

MFR_REVISION (0x9B)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
23:0		ASCII

MFR_DATE (0x9D)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
31:0		ASCII

USER_DATA_00 (0xB0)
Description: Contains serial # from production, together with USER_DATA_01. Complete serial #, e.g. DL5A123456, contains: Factory code ("DL5", represented as enum by 4 bits). Letter ("A", represented by ASCII 8 bits). Number with 6 digits (123456, represented by 20 bits).

Bit	Description	Format
15:0	Least 16 bits of number being part of serial #.	Integer Unsigned

USER_DATA_01 (0xB1)
Description: Contains serial # from production, together with USER_DATA_00. Complete serial #, e.g. DL5A123456, contains: Factory code ("DL5", represented as enum by 4 bits). Letter ("A", represented by ASCII 8 bits). Number with 6 digits (123456, represented by 20 bits).

Bit	Function	Description	Format
11:4	Letter of serial #	Letter after factory code in serial #. For example "A" in serial #: DL5A123456.	ASCII
3:0	Number of serial # - Addend 1	Most 4 bits of number being part of serial #.	Fixed Point Unsigned

Bit	Function	Description	Value	Function	Description
15:12	Factory code of serial #	Factory code being part of serial #. 0x00=DL5. 0x01=CB6, 0x02=DL6, 0x03=DL7. Other values may be used in the future.	0x00	DL5	
			0x01	CB6	
			0x02	DL6	
			0x03	DL7	

MFR_AVERAGE_TIME_SCALE (0xD1)
Description: Used to sets the time period between two measurements.

Bit	Description	Format
3:0	Manufacture specific average time scale. Used to sets the time period between two measurements. [3:0]: Averaging time = 1.2 * 2^MFR_AVERAGE_TIME_SCALE [ms].	Integer Unsigned

MFR_READ_VOUT (0xD2)
Description: Returns the output voltage, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	Linear format. LSB = 3.90625 mV.	Linear	V

MFR_IOUT_CAL_OFFSET (0xD3)
Description: Mfr output current calibration Offset.

Bit	Description	Format	Unit
15:0	Used to add a calibration offset for READ_IOUT monitoring. # of ADC Steps. ADC step = TEL_IOUT_FSR / 2^9.	Integer Signed	ADC steps

MFR_VOUT_CAL_OFFSET (0xD4)
Description: Mfr output voltage calibration Offset.

Bit	Description	Format	Unit
10:0	Used to add a calibration offset for READ_VOUT monitoring. # of ADC Steps. ADC step = 2.5V / (2^9) = 4.8828 mV.	Fixed Point Signed	mV

MFR_PID (0xD6)
Description: Configures the linear control loop filter coefficients.

Bit	Function	Description	Format
50:32	PID C1 PD	Contains PID coefficient PID_C1_PD. PID_C1_PD = 8 * (kP + kD / 25nSec) - max 0x7FFFF	Integer Unsigned
31:16	PID C1 F	Contains PID coefficient PID_C1_F. PID_C1_F = kI * 25nSec * 2^16 - max 0xFFFF	Integer Unsigned
15:0	PID C3	Contains PID coefficient PID_C3. PID_C3 = kD / 25nSec - max 0xFFFF	Integer Unsigned

MFR_FILT_PRE_POST (0xD7)
Description: Configures the linear control loop low-pass filter coefficients.

Bit	Function	Description	Format
14:7	PID pre filter	PID_LP_PRE = 25nSec/(25nSec + tPRE)*2^8. E.g. tPRE = 50 ns => PID_LP_PRE = 85.	Integer Unsigned
6:0	PID post filter	PID_LP_POST = 25nSec/(25nSec + tPOST)*2^7; max 0x7F. E.g. tPOST = 50 ns => PID_LP_POST = 43.	Integer Unsigned

MFR_DUTY_PARAMETER (0xD9)
Description: Used to configure TSTART Correction to control average Duty Cycle for the regulation in case of low VIN value. Through System register TON_RED_CONFIG[6], it is possible to disable phase shedding and enable all phases when input voltage is below the threshold (VOLTAGE_DUTY_ENABLE). Note. KDUTY duty cycle threshold is 8 bit wide and split between this command and MFR_KK_FEEDFRWD_GAIN_CTRL. Only for resonant topology.

Bit	Function	Description	Format	Unit
23:14	Vin voltage threshold (VOLTAGE_DUTY_ENABLE)	Input voltage value below which the correction engages. [#of 0.125V steps]; max 127.875V.	Fixed Point Unsigned	V
13:9	KDUTY Proportional coeff	Contains PID coefficient KDUTY_PROPORTIONAL. Max value is 0x1F.	Integer Unsigned	
8:3	KDUTY Integrative coeff	Contains PID coefficient KDUTY_INTEGRATIVE. Max value is 0x3F.	Integer Unsigned	
2:0	KDUTY Duty cycle threshold [2:0]	kDUTY duty cycle [# of 0.195% Steps]; max = 50%, 0d = OFF. Duty cycle value above which the correction engages. 5 remaining bits are stored into MFR_KK_FEEDFRWD_CTRL.	Integer Unsigned	

MFR_UNLOCK (0xDA)
Description: Unlocks write AND read access to critical PMBus commands. Takes password as an argument. Needs WRITE_PROTECT to be set accordingly. Password can be changed by modifying UNLOCK_PWD SysReg and NVM accordingly. Unlocks the following PMBus commands: MFR_BODY_BRAKE_CONFIG, MFR_CS_PROP_INTEGR, MFR_DUTY_PARAMETER, MFR_FILT_PRE_POST, MFR_FSWITCH_PROTECT_COEFF, MFR_KK_FEEDFRWD_GAIN_CTRL, MFR_PID, MFR_T_START_PH_SHIFT_DELTA_DELAY, MFR_VEXT_NVM, MFR_SECT_L, MFR_SECT_H, MFR_SECT_RD, MFR_SECT_WR, MFR_MEMORY_WORD, MFR_MEMORY_RD, MFR_MEMORY_WR.

Bit	Description	Format
39:0		Byte Array

MFR_LOCK (0xDB)
Description: Locks the access to Low Level commands. Needs WRITE_PROTECT to be set accordingly.

MFR_FAULT_CONFIG (0xDC)
Description: Used to set up the FAULT# pin behavior. 0b = The event do NOT trigger the FAULT# pin assertion. 1b = The event triggers the FAULT# pin assertion.

Bit	Function	Description	Value	Description
10	PUC Error	PUC Error.	1	Trigger enabled
			0	Trigger blocked

Bit	Function	Description	Value	Description
9	Vin Over-Voltage Fault	Vin Over-Voltage Fault.	1	Trigger enabled
			0	Trigger blocked
8	VSRMON peak fault	VSRMON pin peak fault.	1	Trigger enabled
			0	Trigger blocked
7	Vout Over-Voltage Fault (HW)	Vout Over-Voltage Fault (HW).	1	Trigger enabled
			0	Trigger blocked
6	Iout Over-Current Fault (HW)	Iout Over-Current Fault (HW)	1	Trigger enabled
			0	Trigger blocked
5	Catastrophic Fault	Catastrophic Fault.	1	Trigger enabled
			0	Trigger blocked
4	Vput Over-Voltage Fault (HW)	Vput over-voltage Fault (HW).	1	Trigger enabled
			0	Trigger blocked
3	Pout Over-power Fault	Pout Over-power Fault.	1	Trigger enabled
			0	Trigger blocked
2	Feedback disconnection fault	Feedback disconnection fault.	1	Trigger enabled
			0	Trigger blocked
1	Vin Under-voltage Fault	Vin under voltage Fault.	1	Trigger enabled
			0	Trigger blocked
0	Over-Temperature Fault	Over-temperature fault.	1	Trigger enabled
			0	Trigger blocked

MFR_IMON (0xDE)
Description: Mfr Imon.

Bit	Description	Format
5:0	Used to define RIMON/RG ratio from 2.678 to 174.120 in 64 steps; RIMON/RG = 2.678571 * (MFR_IMON + 1), RG=~560 Ohm. Peak OCP limit is impacted as PEAK_OCP = 2.1 / IMONx2 / DCReq / (RIMON/RG) where IMONx2 is given by System Register IMONX2 (OCP is triggered when the drop across RIMON reaches 2.1V). Impacts also READ_IOUT reporting.	Fixed Point Unsigned

MFR_STORE_MAP (0xDF)
Description: Copies the entire RAM content (PMBus commands and system Register values) into NVM, calculating CRC accordingly. The payload data reflects the settings of WRITE_PROTECT and MFR_PROTECT_DEFAULT registers that the stored map will feature (in order to store a map write-protected).

Bit	Function	Description	Format
3:0	MFR_PROTECT_DEFAULT payload		Fixed Point Unsigned
7:4	WRITE_PROTECT payload		Fixed Point Unsigned

MFR_RESTORE_MAP (0xE0)
Description: Restores the NVM content into RAM, as happens during device initial startup.

MFR_CELL_CONFIG (0xE4)
Description: Used to define the number of phases in design.

Bit	Description	Value	Function	Description
2:0	Number of phases/modules in design.	000	1 phase	Main only
		001	2 phases	1 Main + 1 Satellite.
		010	3 phases	1 Main + 2 Satellites.
		011	4 phases	1 Main + 3 Satellites.
		100	5 phases	1 Main + 4 Satellites.
		101	6 phases	1 Main + 5 Satellites.

MFR_OV_LIMIT_OFFSET (0xE5)
Description: MFR_OV_LIMIT_OFFSET.

Bit	Description	Format	Unit
2:0	Used to program the VOUT over voltage threshold as positive offset from 50mV (0x00) to 400mV (0x07) in 50mV steps. OV threshold is set above the commanded Vout setpoint, regardless of the voltage positioning offset (droop).	Fixed Point Unsigned	ΔmV

MFR_UV_LIMIT_OFFSET (0xE6)
Description: MFR_UV_LIMIT_OFFSET.

Bit	Description	Format	Unit
2:0	Used to program the VOUT under voltage threshold as negative offset from 50mV (0x00) to 400mV (0x07) in 50mV steps. UV threshold is set below the commanded setpoint considering the voltage positioning offset (droop).	Fixed Point Unsigned	ΔmV

MFR_VBOOT_SET (0xE7)
Description: MFR_VBOOT_SET.

Bit	Description	Format	Unit
9:0	Used to define VBOOT to which the device regulate after receiving valid enable. [VID] data need to be compliant with format specified in VOUT_MODE. This is the default boot voltage in SVI Mode (Reg26h) and AVS Mode (when OPERATION is set accordingly).	Fixed Point Unsigned	V

MFR_SVI_PMBUS_SELECT (0xE8)
Description: Switch ON (0x01) or OFF (0x00) the Vout control on PMBus domain. In AVS mode this command is NACKed.

Bit	Description	Value	Function	Description
0	[0]: 0b0 = CPU-Link / 0b1 = PMBus"	0	SVID Bus	SVID CPU-Link
		1	PMBus	PMBus

MFR_ICC_MAX_ADD (0xE9)
Description: Additional bytes to standard SVID commands. Formatted per CPU-link definition. LSB = 2A. Check HC_SUPPORT for further info.

Bit	Description	Format
7:0	MFR_ICC_MAX_ADD [A].	Integer Unsigned

MFR_PWR_IN_MAX_ADD (0xEA)
Description: Additional bytes to standard SVID commands. Formatted per CPU-link definition. LSB = 4W. Check HC_SUPPORT for further info.

Bit	Description	Format
7:0	MFR_PWR_IN_MAX_ADD [W].	Integer Unsigned

MFR_PWR_IN_ALERT_ADD (0xEB)
Description: Additional bytes to standard SVID commands. Formatted per CPU-link definition. LSB = 4W. Check HC_SUPPORT for further info.

Bit	Description	Format
7:0	MFR_PWR_IN_ALERT_ADD [W].	Integer Unsigned

MFR_READ_PIN_PUC (0xEF)
Description: Used to read the Input Power communicated through PuC interface, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	LSB=1W.	Linear	W

MFR_READ_VIN_PUC (0xF0)
Description: Used to read the Input voltage communicated through PuC interface, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	LSB=0.125 V.	Linear	V

MFR_DPM1_THR (0xF1)
Description: Sets the phase shedding; phase 1 to 2 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM2_THR (0xF2)
Description: Sets the phase shedding; phase 1 to 2 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM3_THR (0xF3)
Description: Sets the phase shedding; phase 1 to 2 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM4_THR (0xF4)
Description: Sets the phase shedding; phase 1 to 2 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM5_THR (0xF5)
Description: Sets the phase shedding; phase 1 to 2 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_FSWITCH_PROTECT_COEFF (0xF6)
Description: Resonant Loop Only. Used to configure FSW protection during ACLL. Enabled/Disabled through sys reg DISABLE_DPM_PROT

Bit	Description	Format
3:0	FSW_AVG computed as the average frequency of the previous [16 - FSW_AVGd] cycles. 0x01 = 15 cycles; 0x0F = 1 cycles; 0x00 = 0 cycles.	Integer Unsigned

MFR_CS_PROP_INTEGR (0xF7)
Description: Sets Proportional (Kp) and Integral (Ki) correction for Active Current Sharing. In resonant topologies: In order to enable the feature you need to set Ki to 1 or more. The higher value, the faster the regulator recovers current balancing after a load (or number of turned on phases) change. Leave Kp=0. Algorithm: when a phase current is less than average value of load/number of phases, then PWMx to START delay is increased. In non-resonant topologies (PSFB): In order to enable the feature you need to set Kp to 1 or more. The higher value, the faster the regulator recovers current balancing after load (or number of turned on phases) change. Leave Ki=0. Algorithm: when a phase current is less than average value of load/number of phases, then PWMx to PWMy time width is increased.

Bit	Function	Description	Format
13:7	Current Sharing Loop - Ki	Integral correction for active current sharing	Integer Unsigned
6:0	Current Sharing Loop - Kp	Proportional correction for active current sharing	Integer Unsigned

MFR_KK_FEEDFRWD_GAIN_CTRL (0xF9)
Description: Setups Input Voltage Feed-Forward Compensation. It also allow to setup other parameters. K Feed Forward: It is the input voltage FeedForward Gain for resonant topologies. As default value, it is an integer number which value is =(Tsw_noload*VOUT/VIN*1000) where Tsw_noload is the switching period of one secondary phase at no load in uSeconds. KDUTY sets the duty cycle value above which the TSTART correction applies (See MFR_DUTY_PARAMETER). Note. kDUTY is 8 bit wide and split between this command and MFR_KK_FEEDFRWD_GAIN_CTRL. Enable Ph Order: Enables/disables phase order memory during load transients. V_ERR_CLAMP_SOFTSTART: Used to override ErrorClamp setting (active only during SoftStart). Enable Memory: Enables Pulse memory during ACLL. If the VCO drives more pulses during the current Pulse, these are memorized and fired after the current Pulse has elapsed. K_GAIN_CTRL. Defines the bandwidth of the feed forward loop.

Bit	Function	Description	Format	Unit
42:24	Feed Forward Constant	Feed forward constant, integer. As default value, calculate it as (Tsw_noload*VOUT/VIN*1000) where Tsw_noload is the switching period of one secondary phase at no load in useconds. For resonant topology only.	Integer Unsigned	
23:19	KDUTY Duty cycle threshold [7:3]	kDUTY duty cycle [# of 0.195% Steps]; max = 50%, 0d = OFF. Duty cycle value above which the correction engages. 3 remaining bits are stored in MFR_DUTY_PARAMETER.	Integer Unsigned	
15:10	Error clamp threshold at soft-start	During soft-start (Vout ramp-up) this setting overrides the error clamp setting by CTRL_VERR_CLAMP. LSB = 2mV. Error clamp threshold = 2mV * (63 - set value). Max 126mV (0x01). Set 128mV (0x00) to disable function.	Integer Unsigned	mV
7:0	Feed Forward Gain	Sets K_GAIN_CTRL, the FeedForward Gain. Set to 0x01.	Integer Unsigned	

Bit	Function	Description	Value	Function	Description
18	Enable Ph Order On	Phase Order On Enable. 0x01 = Enable sequential; 0x00 = Disables Sequential (=Shuffle).	0xb1		Enabled.
			0xb0		Disabled.
17	Enable Err Clamp Pre	Error Clamp Pre. Reserved, need to be 1 (enabled).	0xb1	Enabled	Enabled.
16	Enable Integrative During Phase Memory On	Integrative During Phase Memory On Enable. Reserved, need to be 1 (enabled).	0xb1	Enabled	Enabled.
9	Secure Off Enable	Secure Off Enable. Reserved, need to be 1 (enabled).	0xb1	Enable	Secure Off enabled.
8	Enable Memory	Enables pulse memory during ACLL.	0xb1		Pulse memory during ACLL enabled.
			0xb0		Pulse memory during ACLL disabled.

MFR_VOUT_TRIM (0xFA)
Description: Mfr Vout Trim

Bit	Description	Format	Unit
7:0	Sets Mfr VOUT trim value. Applies a fixed offset voltage to the value set by VOUT_COMMAND (in # of VID steps). [# of VID]. Applied only in PMBus Domain. # of VID steps to add or remove from setpoint. In AVS mode, if applied, need to be in tracking with EXTRA_OFFSET.	Integer Signed	VID steps

MFR_MANUAL_CELL_SHED (0xFB)
Description: Sets DPM_NPH_PS00, DPM_NPH_PS01 and DPM_NPH_PS02 which are the minimum # of phases for Intel VR power states PS00, PS01 and PS02. Unless otherwise commanded by SVID interface, PS00 power state is used. If trying to set a min # phases higher than # of phases set by MFR_CELL_CONFIG, the write will have no effect and the Unsupported Data bit in STATUS_CML is set.

Bit	Function	Description	Format
9:6	OFFSET_FRACT	Optimizes PSKIP behavior	Integer Unsigned

Bit	Function	Description	Value	Function	Description
12:10	Min # of phases (PS02-SVID)	Minimum # of phases for power state PS02 (Intel VR/SVID only).	001	Min 1 phase	
			010	Min 2 phases	
			011	Min 3 phases	
			100	Min 4 phases	
			101	Min 5 phases	
			110	Min 6 phases	
5:3	Min # of phases (PS01-SVID)	Minimum # of phases for power state PS01 (Intel VR/SVID only).	001	Min 1 phase	
			010	Min 2 phases	
			011	Min 3 phases	
			100	Min 4 phases	
			101	Min 5 phases	
			110	Min 6 phases	
2:0	Min # of phases (PS00)	Minimum # of phases for power state PS00 (default).	001	Min 1 phase	
			010	Min 2 phases	
			011	Min 3 phases	
			100	Min 4 phases	
			101	Min 5 phases	
			110	Min 6 phases	

MFR_SVID_TEMPZONE (0xFE02)
Description: SVID Temperature Zone Register (reg12h). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_IOUT (0xFE03)
Description: SVID Output Current Register (reg15h). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_VIDSETTING (0xFE04)
Description: Last VID code commanded, i.e. actial regulation setpoint. Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
9:0		Integer Unsigned

MFR_SVID_PWRSTATE (0xFE05)
Description: Last PWRState Commanded. Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_OFFSET (0xFE06)
Description: SVID Commanded Offset (reg33h). See System Register CRC_SPI_EN for additional information. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_START_THREAD (0xFE07)
Description: When sent, IC starts to compute the total power delivered. Average Power delivered in 1.2 mSec interval is progressively added until the max time programmed T_THREAD = 1.2mSec * MFR_START_THREAD"

Bit	Description	Format	Unit
19:0	Number of 1 mSec interval to collect the measure on. Max 1,048,576 => 20.97min. Unit in ms.	Fixed Point Unsigned	ms

MFR_SVID_ICCMAX (0xFE08)
Description: ICCMAX Register (reg21h). This is not linked to OC protection in any way. Write unlocked by MFR_SVID_REGLOCK

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_TEMPMAX (0xFE09)
Description: TMAX Register (reg22h). This is not linked to OT protection in any way. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_SRFAST (0xFE0A)
Description: Slew Rate Fast (reg24h). Write unlocked by MFR_SVID_REGLOCK. This is for CPU-Link reading only. Actual slew rate is set through System Register DVID_SR_FAST_STEP.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_SRSLOW (0xFE0B)
Description: Slew Rate Slow (reg25h). Write unlocked by MFR_SVID_REGLOCK. This is for CPU-Link reading only. Actual slew rate is set through System Register DVID_SR_SLOW_STEP.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_MULTI_VR_CONFIG (0xFE0C)
Description: SVID Multi VR Config (reg34h). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
1:0		Integer Unsigned

MFR_SVID_VOUTMAX (0xFE0D)
Description: VOUTMAX (reg30h). Write unlocked by MFR_SVID_REGLOCK

Bit	Description	Format	Unit
7:0	Formatted as per CPU-Link definition	Integer Unsigned	V

MFR_SVID_SLOW_SR_SELECTOR (0xFE0E)
Description: Select SVID SR Slow range as fraction of SVID SR Fast range. Write unlocked by MFR_SVID_REGLOCK. It affects real slew rate as programmed by System Registers DVID_SR_FAST_STEP and DVID_SR_SLOW_STEP. Setting of VR13.1 HC options.

Bit	Function	Description	Value	Function	Description
7	Enable HC support	Configures VR13.HC support Can only be written directly to NVM, read-only in RAM! 0b0: VR13 Protocol support. Exponent for Iout and Pout read/settings and TEL_IOUT_FSR is set by IOUT_EXP. Registers PWR_IN_MAX_ADD and PWR_IN_ALERT_ADD are ignored. 0b1: VR13.HC Protocol support. Iout exponent = -1 (LSB=0.5A), Pout exponent = 1 (LSB=2W), TEL_IOUT_FSR exponent = 1 (LSB=2A), regardless of HC active or not. Registers PWR_IN_MAX_ADD and PWR_IN_ALERT_ADD are supported according to VR13.HC specs. The following commands are affected by the exponent setting: IOUT_OC_FAULT_LIMIT. IOUT_OC_WARN_LIMIT. POUT_OP_FAULT_LIMIT. READ_IOUT. READ_POUT. MFR_DPM1_THR. MFR_DPM2_THR. MFR_DPM3_THR. MFR_DPM4_THR. MFR_DPM5_THR. MFR_READ_PIN_POUT. TEL_IOUT_FSR. DPM_HYSTERESIS.	1	HC supported	HC supported
6	Activate HC		1		HC activated

Bit	Function	Description	Value	Function	Description
		Pre-sets the HC_ACTIVE bit supposed to be commanded through the SVI interface. Can only be written directly to NVM, read-only in RAM! 0b0: HC mode not active. The device behaves as a VR13 controller. -> DEFAULT. ICCMAX = MFR_SVID_ICCMAX [A]. PIN_MAX = MFR_SVID_PIN_MAX*2 [W]. PIN_ALERT_THRESHOLD = MFR_SVID_PIN_ALERT_THR*2 [W]. 0b1: HC mode active. ICCMAX = MFR_SVID_ICCMAX + MFR_ICC_MAX_ADD*2 [A]. PIN_MAX = MFR_SVID_PIN_MAX*2 + MFR_PWR_IN_MAX_ADD*4 [W]. PIN_ALERT_THRESHOLD = MFR_SVID_PIN_ALERT_THR*2 + MFR_PWR_IN_ALERT_ADD*4 [W].	0		HC not activated
3:0	Slow vs fast slew rate range FRACTION	0x01 = 1/2; 0x02 = 1/4; 0x04 = 1/8; 0x08 = 1/16 Others are rejected"	0x01	1/2	
			0x02	1/4	
			0x04	1/8	
			0x08	1/16	

MFR_SVID_PIN_MAX (0xFE0F)
Description: PINMAX (reg2Eh). Used to set the PIN protection threshold. Set threshold to max allowable to disable the protection. Write unlocked by MFR_SVID_REGLOCK. Formatted per CPU-link definition. LSB = 2W.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_PIN_ALERT_THR (0xFE10)
Description: Used to set the PIN protection ALERT threshold. Set threshold to max allowable to disable the warning signal. Write unlocked by MFR_SVID_REGLOCK. Formatted per CPU-link definition. LSB = 2W.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP0 (0xFE11)
Description: SVID Working point #0 (reg3Ah). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP1 (0xFE12)
Description: SVID Working point #1 (reg3Bh). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP2 (0xFE13)
Description: SVID Working point #2 (reg3Ch). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP3 (0xFE14)
Description: SVID Working point #3 (reg3Dh). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP4 (0xFE15)
Description: SVID Working point #4 (reg3Eh). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_RD_TEMPERATURE_PHASE1 (0xFE16)
Description: Reads the temperature for Phase 1. Reporting is active only when Phase 1 is switching.

Bit	Description	Format	Unit
15:0	Phase 1 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE2 (0xFE17)
Description: Reads the temperature for Phase 2. Reporting is active only when Phase 2 is switching.

Bit	Description	Format	Unit
15:0	Phase 2 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE3 (0xFE18)
Description: Reads the temperature for Phase 3. Reporting is active only when Phase 3 is switching.

Bit	Description	Format	Unit
15:0	Phase 3 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE4 (0xFE19)
Description: Reads the temperature for Phase 4. Reporting is active only when Phase 4 is switching.

Bit	Description	Format	Unit
15:0	Phase 4 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE5 (0xFE1A)
Description: Reads the temperature for Phase 5. Reporting is active only when Phase 5 is switching.

Bit	Description	Format	Unit
15:0	Phase 5 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE6 (0xFE1B)
Description: Reads the temperature for Phase 6. Reporting is active only when Phase 6 is switching.

Bit	Description	Format	Unit
15:0	Phase 6 temperature.	Linear	°C

MFR_CTRL_ID (0xFE1C)
Description: Used to read controller internal reference code.

Bit	Description	Format
15:0	Used to read controller internal reference code.	Byte Array

MFR_SVID_REGLOCK (0xFE1E)
Description: CPU-Link registers are by default accessible only with read operations (locked). This command allows to lock (0x01) or unlock (0x00) access to these registers. This command is not stored in NVM but will be set to lock state (0x01) efter a RESTORE from NVM command (e.g. MFR_RESTORE_MAP).

Bit	Description	Value	Description
0		1	Protects SVID Registers
		0	Unprotects SVID Registers

MFR_SECT_L (0xFE20)
Description: 8 bytes low sector image data - Used to access read NVM data after writing MFR_SECT_RD or to write NVM data before writing MFR_SECT_WR. [63..56] = byte 00 ... [7..0] = byte 07.

Bit	Description	Format
63:0		Integer Unsigned

MFR_SECT_H (0xFE21)
Description: 8 bytes high sector image data - Used to access read NVM data after writing MFR_SECT_RD or to write NVM data before writing MFR_SECT_WR. [63..56] = byte 08 ... [7..0] = byte 15.

Bit	Description	Format
63:0		Integer Unsigned

MFR_SECT_RD (0xFE24)
Description: Copy from specified NVM sector (0x01 to 0x0E) into a register accessible by PMBus commands MFR_SECT_L and MFR_SECT_H.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SECT_WR (0xFE25)
Description: Copy from register written by PMBus commands MFR_SECT_L and MFR_SECT_H into specified NVM sector (0x01 to 0x0E).

Bit	Description	Format
7:0		Integer Unsigned

MFR_MEMORY_WORD (0xFE26)
Description: 8 bytes - Data for read/write of specified RAM memory location (used by MFR_MEMORY_RD or MFR_MEMORY_WR). [63..56] = Base Address +7 ... [7..0] = Base Address as specified into MFR_MEMORY_RD, MFR_MEMORY_WR.

Bit	Description	Format
63:0		Integer Unsigned

MFR_MEMORY_RD (0xFE27)
Description: 3 bytes - Used to copy 8 bytes of the specified RAM memory location into PMBusTM accessible register, read by MFR_MEMORY_WORD. Byte 1 [7:0] : RAM address low byte. Byte 2 [15:8]: RAM address high byte. Byte 3 [23:16]: Source. 0x00 to read from RAM. Other combinations are reserved. Protected by MFR_UNLOCK.

Bit	Description	Format
23:0		Integer Unsigned

MFR_MEMORY_WR (0xFE28)
Description: "4 bytes - Used to copy the content of PMBusTM accessible registers, written to MFR_MEMORY_WORD, into the specified RAM memory location. Byte 1 [7:0] : RAM address low byte. Byte 2 [15:8] : RAM address high byte. Byte 3 [23:16]: Source. 0x00 to read from RAM. Other combinations are reserved. Byte 4 [31:24]: Number of bytes to be written, 1 to 8. Other combinations are reserved. Protected by MFR_UNLOCK.

Bit	Description	Format
31:0		Integer Unsigned

MFR_READ_BLACKBOX (0xFE29)
Description: NVM BBR Access. Used to copy the content of NVM that contains BBR data into accessible PMBusTM register MFR_BLACKBOX.

MFR_BLACKBOX (0xFE2A)
Description: NVM BBR Access - Shadow register containing the BBR NVM Sector being read. Status Register array is reported before and after the BBR trigger.

Bit	Function	Description	Value	Description
125	After trigger - VSRMON peak fault		0	
			1	
124	After trigger - PATCH_DOWNLOAD		0	
			1	
123	After trigger - MEM_FAULT		0	
			1	
122	After trigger - POUT_OP_FAULT		0	
			1	
121	After trigger - DATACMD_RCV_FAULT		0	
			1	
120	After trigger - IOUT_OC_WARN		0	
			1	
115	After trigger - CATASTROPHIC_FAULT		0	
			1	
114	After trigger - VIN_UV_FAULT		0	
			1	
113	After trigger - VIN_OV_FAULT		0	
			1	
112	After trigger - PUC_CRC_FAULT		0	
			1	
110	After trigger - CURR_SHARE_WARN		0	
			1	
103	After trigger - OFF		0	
			1	
102	After trigger - VOUT_OV_FAULT		0	
			1	
101	After trigger - VOUT_UV_FAULT		0	
			1	
100	After trigger - IOUT_OC_FAULT		0	
			1	
99	After trigger - Feedback disconnection		0	
			1	
98	After trigger - VOUT_MAX_WARNING		0	
			1	
97	After trigger - OT_FAULT		0	
			1	
96			0	

Bit	Function	Description	Value	Description
	After trigger - OT_WARNING		1	
93	Before trigger - VSRMON peak fault		0	
			1	
92	Before trigger - PATCH_DOWNLOAD		0	
			1	
91	Before trigger - MEM_FAULT		0	
			1	
90	Before trigger - POUT_OP_FAULT		0	
			1	
89	Before trigger - DATACMD_RCV_FAULT		0	
			1	
88	Before trigger - IOUT_OC_WARN		0	
			1	
83	Before trigger - CATASTROPHIC_FAULT		0	
			1	
82	Before trigger - VIN_UV_FAULT		0	
			1	
81	Before trigger - VIN_OV_FAULT		0	
			1	
80	Before trigger - PUC_CRC_FAULT		0	
			1	
78	Before trigger - CURR_SHARE_WARN		0	
			1	
71	Before trigger - OFF		0	
			1	
70	Before trigger - VOUT_OV_FAULT		0	
			1	
69	Before trigger - VOUT_UV_FAULT		0	
			1	
68	Before trigger - IOUT_OC_FAULT		0	
			1	
67	Before trigger - Feedback disconnection		0	
			1	
66	Before trigger - VOUT_MAX_WARNING		0	
			1	
65	Before trigger - OT_FAULT		0	
			1	
64	Before trigger - OT_WARNING		0	
			1	

MFR_CLEAR_BB (0xFE2B)
Description: Clear the content of NVM that contains BBR data.

MFR_CONFIG_BBR (0xFE2C)
Description: "Select which events trigger the writing of the BBR in NVM. Set 1b to enable event to trigger BBR, 0b to disable."

Bit	Function	Description	Value	Description
11	PUC_CRC_FAULT		0	Do not trigger on fault
			1	Trigger event on fault
10	Feedback disconnection fault		0	Do not trigger on fault
			1	Trigger event on fault
9	VSRMON peak fault		0	Do not trigger on fault
			1	Trigger event on fault

Bit	Function	Description	Value	Description
8	VOUT_OV		0	Do not trigger on fault
			1	Trigger event on fault
7	IOUT_OC		0	Do not trigger on fault
			1	Trigger event on fault
6	CATASTROFIC FAULT		0	Do not trigger on fault
			1	Trigger event on fault
5	VOUT Under Voltage Fault		0	Do not trigger on fault
			1	Trigger event on fault
4	Over Output Power Fault		0	Do not trigger on fault
			1	Trigger event on fault
3	Current Sharing Unbalance Warning		0	Do not trigger on fault
			1	Trigger event on fault
2	VIN OV Fault	VIN Over Voltage Fault	0	Do not trigger on fault
			1	Trigger event on fault
1	VIN UV Fault	VIN Under Voltage Fault	0	Do not trigger on fault
			1	Trigger event on fault
0	Over Temperature Fault	Over Temperature Fault	0	Do not trigger on fault
			1	Trigger event on fault

MFR_PROTECT_DEFAULT (0xFE2E)
Description: Protects non volatile memory from writing by inhibiting commands STORE_DEFAULT_ALL and MFR_STORE_MAP. In case, the PMB_ALRT# signal is asserted and “other ML flag” bit is STATUS_CML register is set. 0x00 = Unprotected; 0x01 = Protected.

Bit	Description	Value	Description
0	[7:1]: Don't Care [0]: 0b0 = Unprotected; 0b1 = Protected	0	Unprotected
		1	Protected

MFR_POUT_THREAD (0xFE2F)
Description: When sent, stops the computation started with MFR_START_THREAD and returns the total energy delivered in the programmed time (max 1GW).

Bit	Description	Format	Unit
31:0	LSB weight is given by System Register IOUT_EXP.	Integer Unsigned	Wms

MFR_PMBUSCFG_REVISION (0xFE30)
Description: Can be used for user/custom data.

Bit	Description	Format
15:0	Can be used for user/custom data.	Byte Array

MFR_PMBUSCFG_TIMESTAMP (0xFE31)
Description: Contains product number and revision information. Example: For product number BMR 481 0021/031B R2C the fields will be: BMR number = 4810021031. Preliminary revision = Not = 0. Product revision number = 2. Product revision letter = C.

Bit	Function	Description	Format
63:24	BMR number	Number 1-999 9999 999.	Integer Unsigned
22:16	Product revision number	Number 1-127	Integer Unsigned
15:8	Product revision letter	Letter ASCII coded	ASCII
7:0	Configuration revision	Letter ASCII coded	ASCII

Bit	Function	Description	Value	Description
23	Preliminary revision	0=Non-preliminary revision (e.g. R1A), 1=Preliminary revision (e.g. P1A)	0	Non-preliminary revision (e.g. R1A)
			1	Preliminary revision (e.g. P1A)

MFR_PEAK_FAULT_RESPONSE (0xFE32)
Description: Used to configure how to respond to a peak fault read through VSRMON pin. When enabled, fault is set if VSRMON pin > 3.045V.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

MFR_PMBUSCFG_USERID (0xFE33)
Description: Can be used for user/custom data.

Bit	Description	Format
15:0	Can be used for user/custom data.	Byte Array

System Registers Details

CURRENT_SHARING_RESET (0xA408)

Bit	Function	Description	Format
5:0	Activation threshold	Activation threshold for current sharing reset. 0x00=126mV, 0x01=124mV, 0x02=122mV, ... , 0x26=50 mV, ... , 0x3D=4mV, 0x3E=2mV, 0x3F=0 mV.	Byte Array

Bit	Function	Description	Value	Function	Description
7	Enable current sharing Reset	For resonant mode only. Enable Current sharing Reset. Needed in case of heavy load transient release to suddenly reduce the TSTART signal delay vs PWMx, in order to avoid secondary phases overvoltage. Adjusts the current sharing correction (dividing its correction /2 or /4) when the current sharing error exceeds a programmable threshold in order to optimize load release.	0		Disable
			1		Enabled
6	Correction division	Dividing correction for current sharing reset.	0	Divide with 2	Divide with 2.
			1	Divide with 4	Divide with 4.

HIGH_CURR_PROT_EN (0xA40B)

Bit	Function	Description	Value	Function	Description
7	Add 12.5 ns to base Tshift correction	Adds 12.5 ns to the base Tshift correction set by MFR_T_START_PH_SHIFT_DELTA_DELAY[35:31].	0		Do not add 12.5 ns
			1		Add 12.5 ns
6	Add 12.5 ns to base Tshift	Adds 12.5 ns to the base Tshift set by MFR_T_START_PH_SHIFT_DELTA_DELAY[8:0]. Cannot be 0 (do not add 12.5 ns) in Resonant application if NCHECKS = 0x00. Cannot be 1 (add 12.5 ns) in NonResonant PSFB if TPHASE_SHIFT = 0nSec or 25nSec.	0		Do not add 12.5 ns
			1		Add 12.5 ns
5	Enable one Phase gain reduction	GAIN_REDU_1PH_EN. Reduces by 1/2 the control loop gain when working in single phase.	0		Disable
			1		Enabled
4	Enable soft start gain reduction	GAIN_REDU_SS_EN. Reduces by 1/2 the control loop gain during SoftStart.	0		Disable
			1		Enabled
3	Enable TGB hysteresis		0		Disable
			1		Enabled
2	Current sharing correction storage.	Enables/disables current sharing correction to be memorized when shedding phases. Reserved, set to 0x01 (not stored).	0	Correction stored	
			1	Correction not stored	
1	AVSBus current monitor	0b0: EXP = -2; 0b1: EXP = -1	0	EXP = -2	EXP = -2
			1	EXP = -1	EXP = -1
0	Enable High Current Protection	Reserved, set to 0 (disabled).	0		Disable
			1		Enabled

AVS_CONFIG (0xA40D)

Bit	Function	Description	Value	Function	Description
3	SDATA release method	Controls when SDATA is released (open) at the end of a frame. 0x00: As per protocol at CLK edge (rising). 0x01: Data line release 1/2 CLK in advance (CLK falling edge).	0	At CLK edge (per protocol)	
			1	1/2 CLK in advance	
2	Do not produce response to wrong address	Controls the response to command with address that doesn't match VRM address. 0x00: Response is produced; 0x01: No Response.	0		Disable
			1		Enabled
1	Do not produce status response	Controls the production of status response frame and response to broadcast commands. 0x00: Response is produced; 0x01: No Response.	0		Disable
			1		Enabled
0	Do not produce interrupt over data line	Controls interrupt produced from the interface in case of OC OT on DAT line of the interface. 0x00: Interrupt is produced over data line; 0x01: No interrupt is produced.	0		Disable
			1		Enabled

HIZ_HALFB_SYMMETRIC (0xA418)

Bit	Function	Description	Value	Function	Description
5	SFAS displacement	Current reading Chopper Amplifiers Control. Configures which phase shift is applied once enabled by SFAS. Reserved, set to 0x01.	0	12.5 ns	_
			1	25 ns	_
4	SFAS enable	Current reading Chopper Amplifiers Control. Enables phase shifting between the clock of the six chopper amplifiers. Reserved, set to 0x01.	0		Disabled
			1		Enabled
3	HiZ mode for PWM		0	PWMX/PWMY never HiZ	_
			1	PWMX/PWMY HiZ @ no operation	_
2	Symmetric mode		0	Asymmetric	_
			1	Symmetric	_
1	Bridge functionality		0	Full bridge	_
			1	Half bridge	_
0			0	Soft-off	Use the configured fall time (slew rate).

Bit	Function	Description	Value	Function	Description
	Immediate (HiZ) or soft-off	When set, immediate off (HiZ) is used rather than soft-off when the output voltage is disabled. When set, also forces immediate off for all protection shutdowns. Because, in some cases, even if the immediate OFF is configured by OPERATION, the device is defaulting the behavior to soft-off. Vout OVP and OV peak protections by default always make a soft-off even if the OPERATION configures immediate OFF. This removes these default; it overrides and forces a real HiZ when stopping the operations after a FAULT event. For Vin UV/OV, Vout UV, Iout OC, over power and over temperature protections immediate off (HiZ) is always used and this bit has no impact.	1	Immediate off	Turn off the output and stop transferring energy to the output as fast as possible.

CTRL_PFM_ENA_PS (0xB006)

Bit	Description	Value	Function	Description
1:0	Enable the PFM working mode vs power state.	00	PFM enabled in any PS	
		01	PFM enabled in PS01-03	
		10	PFM enabled in PS02-03	
		11	PFM disabled	

DPM_HYSTERESIS (0xB007)

Bit	Description	Format	Unit
7:0	Used to define the hysteresis for Phase Shedding. DPM_OFFSET may optimize the hysteresis settings. LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

DVID_SR_FAST_STEP (0xB00C)

Bit	Description	Value	Function	Description
5:0	Programs the [# of 25nSec] to step VOUT by 5mV. This setting actively drives the reference slew. dV/dt = 5mV / (SR_FAST_STEP * 25nSec) Actual fast slew rate (mV/us) = 200 / DVID_SR_FAST_STEP[5:0]. [7:6]: Don't Care [5:0]: SR_FAST_STEP. Values accepted from 0x01 to 0x3F. If 0x00, wraps to 0x3F.	0x01	200 mV/us	
		0x02	100 mV/us	
		0x03	66.67 mV/us	
		0x04	50.00 mV/us	
		0x05	40.00 mV/us	
		0x06	33.33 mV/us	
		0x07	28.57 mV/us	
		0x08	25.00 mV/us	
		0x09	22.22 mV/us	
		0x0A	20.00 mV/us	
		0x0B	18.18 mV/us	
		0x0C	16.67 mV/us	
		0x0D	15.38 mV/us	
		0x0E	14.29 mV/us	
		0x0F	13.33 mV/us	
		0x10	12.50 mV/us	
		0x11	11.76 mV/us	
		0x12	11.11 mV/us	
		0x13	10.53 mV/us	
		0x14	10.00 mV/us	

Bit	Description	Value	Function	Description
		0x15	9.52 mV/us	
		0x16	9.09 mV/us	
		0x17	8.70 mV/us	
		0x18	8.33 mV/us	
		0x19	8.00 mV/us	
		0x1A	7.69 mV/us	
		0x1B	7.41 mV/us	
		0x1C	7.14 mV/us	
		0x1D	6.90 mV/us	
		0x1E	6.67 mV/us	
		0x1F	6.45 mV/us	
		0x20	6.25 mV/us	
		0x21	6.06 mV/us	
		0x22	5.88 mV/us	
		0x23	5.71 mV/us	
		0x24	5.56 mV/us	
		0x25	5.41 mV/us	
		0x26	5.26 mV/us	
		0x27	5.13 mV/us	
		0x28	5.00 mV/us	
		0x29	4.88 mV/us	
		0x2A	4.76 mV/us	
		0x2B	4.65 mV/us	
		0x2C	4.55 mV/us	
		0x2D	4.44 mV/us	
		0x2E	4.35 mV/us	
		0x2F	4.26 mV/us	
		0x30	4.17 mV/us	
		0x31	4.08 mV/us	
		0x32	4.00 mV/us	
		0x33	3.92 mV/us	
		0x34	3.85 mV/us	
		0x35	3.77 mV/us	
		0x36	3.70 mV/us	
		0x37	3.64 mV/us	
		0x38	3.57 mV/us	
		0x39	3.51 mV/us	
		0x3A	3.45 mV/us	
		0x3B	3.39 mV/us	
		0x3C	3.33 mV/us	
		0x3D	3.28 mV/us	
		0x3E	3.23 mV/us	
		0x3F	3.17 mV/us	

DVID_SR_SLOW_STEP (0xB00D)

Bit	Description	Value	Function	Description
5:0	Programs the [# of 25nSec] to step VOUT by 5mV. This setting actively drives the reference slew. Data computed over MFR_SVID_SLOW_SR_SELECTOR. Actual slow slew rate (mV/us) = FRACTION x 200 / DVID_SR_SLOW_STEP[5:0] where FRACTION = 2 x MFR_SVID_SLOW_SR_SELECTOR[3:0]. [7:6]: Don't Care. [5:0]: SR_SLOW_STEP. Values accepted from 0x01 to 0x3F. If 0x00, wraps to 0x3F.	0x01	FRACTION x 200 mV/us	
		0x02	FRACTION x 100 mV/us	
		0x03	FRACTION x 66.67 mV/us	
		0x04	FRACTION x 50.00 mV/us	
		0x05	FRACTION x 40.00 mV/us	
		0x06	FRACTION x 33.33 mV/us	
		0x07	FRACTION x 28.57 mV/us	

Bit	Description	Value	Function	Description
		0x08	FRACTION x 25.00 mV/us	
		0x09	FRACTION x 22.22 mV/us	
		0x0A	FRACTION x 20.00 mV/us	
		0x0B	FRACTION x 18.18 mV/us	
		0x0C	FRACTION x 16.67 mV/us	
		0x0D	FRACTION x 15.38 mV/us	
		0x0E	FRACTION x 14.29 mV/us	
		0x0F	FRACTION x 13.33 mV/us	
		0x10	FRACTION x 12.50 mV/us	
		0x11	FRACTION x 11.76 mV/us	
		0x12	FRACTION x 11.11 mV/us	
		0x13	FRACTION x 10.53 mV/us	
		0x14	FRACTION x 10.00 mV/us	
		0x15	FRACTION x 9.52 mV/us	
		0x16	FRACTION x 9.09 mV/us	
		0x17	FRACTION x 8.70 mV/us	
		0x18	FRACTION x 8.33 mV/us	
		0x19	FRACTION x 8.00 mV/us	
		0x1A	FRACTION x 7.69 mV/us	
		0x1B	FRACTION x 7.41 mV/us	
		0x1C	FRACTION x 7.14 mV/us	
		0x1D	FRACTION x 6.90 mV/us	
		0x1E	FRACTION x 6.67 mV/us	
		0x1F	FRACTION x 6.45 mV/us	
		0x20	FRACTION x 6.25 mV/us	
		0x21	FRACTION x 6.06 mV/us	
		0x22	FRACTION x 5.88 mV/us	
		0x23	FRACTION x 5.71 mV/us	
		0x24	FRACTION x 5.56 mV/us	
		0x25	FRACTION x 5.41 mV/us	

Bit	Description	Value	Function	Description
		0x26	FRACTION x 5.26 mV/us	
		0x27	FRACTION x 5.13 mV/us	
		0x28	FRACTION x 5.00 mV/us	
		0x29	FRACTION x 4.88 mV/us	
		0x2A	FRACTION x 4.76 mV/us	
		0x2B	FRACTION x 4.65 mV/us	
		0x2C	FRACTION x 4.55 mV/us	
		0x2D	FRACTION x 4.44 mV/us	
		0x2E	FRACTION x 4.35 mV/us	
		0x2F	FRACTION x 4.26 mV/us	
		0x30	FRACTION x 4.17 mV/us	
		0x31	FRACTION x 4.08 mV/us	
		0x32	FRACTION x 4.00 mV/us	
		0x33	FRACTION x 3.92 mV/us	
		0x34	FRACTION x 3.85 mV/us	
		0x35	FRACTION x 3.77 mV/us	
		0x36	FRACTION x 3.70 mV/us	
		0x37	FRACTION x 3.64 mV/us	
		0x38	FRACTION x 3.57 mV/us	
		0x39	FRACTION x 3.51 mV/us	
		0x3A	FRACTION x 3.45 mV/us	
		0x3B	FRACTION x 3.39 mV/us	
		0x3C	FRACTION x 3.33 mV/us	
		0x3D	FRACTION x 3.28 mV/us	
		0x3E	FRACTION x 3.23 mV/us	
		0x3F	FRACTION x 3.17 mV/us	

DVID_VAR_OFFSET_PARAM (0xB00E)

Bit	Function	Description	Format
47:42	RISE_FAST offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed
41:36	RISE_SLOW offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed

Bit	Function	Description	Format
35:30	FALL_FAST offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed
29:24	FALL_SLOW offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed
23:10	Offset expiration TauDVID	Offset application/removal time constant. LP_CONST = (25 * 2^14) / (25 + TauDVID[nSec]). [# of non-linear steps -> value[ns]= 25 *(1-(LP_CONST/2^14)) / (LP_CONST/2^14)].	Integer Unsigned
9:0	OC mask after DVID ends	[9..0] = OCP_TAU = (TOCP-25nSec) / 100nSec. OC Disable TOCP after DVID ends. [# of 100nSec steps +25ns internal offset].	Integer Unsigned

TEL_GAIN_VIN (0xB018)

Bit	Description	Format
7:0	VSRMON ADC: Used to define the Gain correction for VIN monitoring over VSRMON when Opto Mode is Enabled. Ranges linearly from 0 (0x00) to 2 (0xFF). 0x80 = Gain = 1 shall be used for a 1/40 divider, which is the recommended configuration. VSRMON ADC range is 0 to 3.2V and VSRMON pin has an internal 10k pull-down resistor, thus a 1/40 divider is achieved by a 390k resistance to VIN.	Integer Unsigned

THERMAL_GAIN (0xB01A)

Bit	Description	Format
7:0	Used to set T_COMP variable for Thermal Compensation of output current sense. T_COMP makes an adjustment of the correction factor that is ideal for copper, according to: Iinfo_TC = Iinfo x Kcorr = Iinfo x 1 / (1 + alfa x deltaT_DCR) = Iinfo x 1 / (1 + alfa x deltaT_NTC x T_COMP / 128) where alfa = 0.0039 and deltaT_NTC is calculated difference from Tmin, given by TEL_NTC_MAP_Q6. Thus, T_COMP is used to compensate for the temp difference between NTC-resistor and output inductor DCR. T_COMP = 128 means ideal correction alfa is used. Note that Kcorr must always be in the range 0.67 to 1.0, which limits the maximum deltaT_NTC that can be handled.	Fixed Point Unsigned

TEL_IOUT_FSR (0xB01B)

Bit	Description	Format	Unit
8:0	Defines the READ_IOUT monitoring ADC Full scale. Shall be set to match the peak OCP limit as defined by MFR_IMON. LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

TEL_OFFSET_VIN (0xB027)

Bit	Function	Description	Format	Unit
10	Sign	1 = Positive 0 = Negative	Integer Unsigned	
9:0	Number of 0.125V steps	VSRMON ADC: Used to define the Offset correction for VIN monitoring over VSRMON when Opto Mode is Enabled.	Integer Unsigned	V

TEL_GAIN_IMON (0xB029)

Bit	Description	Format
7:0	Sets the gain correction to be applied to IMON reading (both PMBus and CPU-Link). Computed at controller startup as TEL_GAIN_IMON_RAM adjusted per trimming calibration. Ranges linearly from 0 (0x00) to 2 (0xFF). Note. If modified, when MFR_STORE_MAP is issued, IC automatically stores into TEL_GAIN_IMON_RAM the RAW value adjusted per trimming calibration.	Fixed Point Unsigned

SVI_ADDITIONAL_OFFSET (0xB02B)

Bit	Function	Description	Format
1:0	DPM # of phases PS2	0x01 = NCELL=1 through 0x06 = NCELL=6. Other combinations are not supported. Configures the minimum number of operating phases in PS02.	Integer Unsigned

Bit	Function	Description	Value	Function	Description
7			0		Disable hiccup mode

Bit	Function	Description	Value	Function	Description
	Enable hiccup mode	Enable hiccup fault response mode. When enabled, after a fault occurred, the controller re-attempts to startup Vout after 1 mSec. When enabled, the hiccup fault response mode applies for the fault types that are enabled in MFR_FAULT_CONFIG. After a restart due to hiccup, the fault flag set in STATUS_WORD will be cleared.	1		Enable hiccup mode
6	IMON divider @ dynamic VID	IMON divider in dynamic VID condition. Delivers reduced IMON current to the IMON resistor to prevent from false OC being trip.	0	IMON/2	Divide by 2.
			1	IMON/4	Divide by 4.
5:4	IMON divider @ soft start	IMON divider in soft start transitions. Delivers reduced IMON current to the IMON resistor to prevent from false OC being trip.	00	IMON	Divide by 1.
			01	IMON/2	Divide by 2.
			10	IMON/4	Divide by 4.
			11	IMON/8	Divide by 8.
3	Enable soft bias current sense	Enable soft bias to allow current sense below Vout 0.7V. Prevent damage at startup with short circuit for full bridge. Optimizes current reading amplifier biasing at low output voltages preventing saturation. Reserved, need to be 0b1 (enabled).	0		Disable
			1		Enable

VIN_FEED_FWD_SOURCE (0xB038)

Bit	Description	Value	Function	Description
0	Used to define which input to be used for VIN FeedForward Compensation. 0x00 = Uses data from PuC. 0x01 = Uses data from VSRMON at secondary. Other combinations are not supported.	00	PuC	
		01	VSRMON at secondary	

VIN_MONITORING_SOURCE (0xB039)

Bit	Description	Value	Function	Description
0	Used to define which input to be used for VIN monitoring and Protection between PuC and VSRMON. VSRMON needs to be further configured. 0x00 = Uses data from PuC. 0x01 = Uses data from VSRMON at secondary. Other combinations are not supported.	00	PuC	
		01	VSRMON at secondary	

IOUT_VR125_PERC_EN (0xB03C)

Bit	Description	Value	Function	Description
0	Used to define whether the IOUT reporting on reg15h is to be in percentage of ICCMAX (given by MFR_SVID_ICCMAX) or absolute value in Amperes.	0	Absolute in [A]	
		1	% of ICCMAX	

VR13_TIME_FRAME (0xB040)

Bit	Description	Value	Function	Description
0	Used to define averaging interval for VR1xx IMON reporting register. Update interval is always 100uSec while averaging can be programmed.	0	Averaging on 200 us	
		1	Averaging on 100 us	

CTRL_VERR_CLAMP (0xB041)

Bit	Description	Format	Unit
5:0	When the voltage regulation error increases above the “Unload” threshold, integrator stops to limit the overshoot at load release. LSB = 2mV. Error clamp threshold = 2mV * (63 - set value). Max 126mV (0x01). Set 128mV (0x00) to disable function.	Fixed Point Unsigned	mV

DISABLE_DPM_PROT (0xB044)

Bit	Description	Value	Description
0	Used to disable DPM Protection that, during ACLL, increases the # of phases by 1 if instantaneous FSW gets greater than averaged FSW_AVG. FSW_AVG set by MFR_FSWITCH_PROTECT_COEFF in Resonant Loop while in Non Resonant Loop the comparison is made over the nominal FSW set. Trigger threshold changes with the number of active phases: # of active phases = 1 => Fthreshld = 2.00*FSW_AVG. # of active phases = 2 => Fthreshld = 1.50*FSW_AVG. # of active phases = 3 => Fthreshld = 1.33*FSW_AVG. # of active phases = 4 => Fthreshld = 1.25*FSW_AVG. # of active phases = 5 => Fthreshld = 1.20*FSW_AVG.	0	DPM Protection Enabled - # of phases reset in load transient
		1	DPM Protection Disabled - # of phases NOT reset in load transient

TGB_CONFIG (0xB046)

Bit	Function	Description	Format	Unit
7:2	TGB/NLR Load Threshold	LSB = 2mV, max 126mV (0b111111)	Fixed Point Unsigned	mV

Bit	Function	Description	Value	Function	Description
1:0	TGB/NLR Load Mode	Used to configure Transient Gain Boost to improve transient response. When the voltage regulation error decreases below the “Load” threshold, the control loop gain is doubled to limit the undershoot during load application.	00	Disabled	
			01	Enabled when # of phases >= 2	
			10	Enabled	
			11	Enabled with 2x threshold when # of phases=1	

VDROOP_CONFIG (0xB047)

Bit	Function	Description	Format	Unit
5:2	Virtual Droop Error Threshold	Activation threshold over Control Error (+/-). LSB = 4mV.	Fixed Point Unsigned	mV

Bit	Function	Description	Value	Function	Description
1:0	Virtual Droop Timeframe	Duration of Virtual Droop. Expires after this time has elapsed.	00	0.8 us	
			01	1.6 us	
			10	2.4 us	
			11	3.2 us	
1:0	Virtual Droop Mode	Virtual Droop slows the load transient response in order to keep the control loop (PID) in linear region, avoiding control loop saturation. Typically used in applications without voltage positioning (droop) since it adds a virtual voltage positioning. Virtual Droop reduces the regulation error (when overcoming the set threshold) for the programmed timeframe. Enabling Virtual Droop provides a load transient response worse than without Virtual Droop but it ensures a better response at high frequency load transients.	00	Disabled	
			01	Enabled for load release	
			10	Enabled for load apply + release	
			11	Enabled for load apply + release with half timeframe	

TON_RED_CONFIG (0xB04A)

Bit	Function	Description	Format
1:0	ZCDM offset	Used to set an offset on ZCD to optimize PFM (not for Phase 1 which uses ZCD1_OFFSET). Offset in [uA], how this is translated into [A] on inductor ripple depends on the real application implemented. 0x03 = 2.4uA ; 0x02 = 4uA; 0x01 = 5.6uA; 0x00 = 7.2uA. Other combinations are not supported.	Fixed Point Unsigned

Bit	Function	Description	Value	Function	Description
7	Boost on Phase number change	Reserved, disable/set to 0.	0	Disabled	Disabled
6	Enable all phases at low Vin	If enabled, all phases will be turned on if duty cycle is high and input voltage is lower than the threshold (VOLTAGE_DUTY_ENABLE) set by MFR_DUTY_PARAMETER[23:14] . This will improve transient response at low input voltage. Only for resonant topology.	0		Disabled
			1		Enabled
5	Force VR_READY	When set/enabled, VRREADY = 0 regardless of regulation. Reserved bit #4 need to be set to 0b.	0		Disabled
			1		Enabled
3	Prevent spec patterns	NO_PINTA: Prevents issuing special patterns in case of primary driver replacement.	1	Enabled	Enabled
2	Enable all phases Vin hysteresis	Adds 1V hysteresis on the All phases enable activation Vin threshold. See TON_RED_CONFIG[6] and MFR_DUTY_PARAMETER[23:14] . Only for resonant topology.	0		Disabled
			1		Enabled

EN_DROOP_START (0xB04B)

Bit	Description	Value	Description
0	Enables fake droop effect at startup to keep Control-ADC Error negative to avoid bumps on VOUT at start-up. Other combinations than 0x00 and 0x01 are not supported.	0	Disable startup droop
		1	Enable startup droop

CS_OVERFLOW_DISABLE_IRQ (0xB04E)

Bit	Description	Value	Function	Description
0	Used to disable current sharing overflow fault. 0x00 = Current Sharing FAULT Enable. 0x01 = Current Sharing FAULT Disable. Other combinations are not supported.	00	Enable Current Sharing FAULT	
		01	Disable Current Sharing FAULT	

VR_READY_FAST_DISABLE (0xB051)

Bit	Description	Value	Function	Description
0	Used to allow immediate VR_RDY signal de-assertion in case of disable from EN pin. If not set, VR_RDY may be delayed from EN de-assertion up to 400 us.	00	Disable fast de-assertion	
		01	Enable fast de-assertion	

MULTIFUNCTION_PIN_MUX (0xB057)

Bit	Function	Description	Value	Function	Description
2	Enable IMON filtering	Enable additional analog filtering on IMON (800nSec time constant) to prevent from false OC tripping and to reduce overall ripple noise. Should always be enabled.	1	Enable	Enable IMON filtering
1:0	Configure droop effect at startup	Configure droop effect at startup, see EN_DROOP_START.	00	Regulation error only (standard)	Use regulation error only.
			01	Regulation error and Droop	Use regulation error + droop value by VOUT_DROOP.
			10	Regulation error and 2 x Droop	Use regulation error + 2 x droop value by VOUT_DROOP
			11	Regulation error and 3 x Droop	Use regulation error + 3 x droop value by VOUT_DROOP

MONITOR_OFFSET (0xB05E)

Bit	Description	Format	Unit
4:0	Vout monitoring offset applied to READ_VOUT (not applied to MFR_READ_VOUT). LSB depends on the table used (10mV or 5mV by VR_TAB_RAIL). Signed. It is an additional contribute to MFR_VOUT_CAL_OFFSET which is usually tuned to compensate internal ADC VSS (0.5V).	Fixed Point Signed	mV

EXTRA_OFFSET (0xB063)

Bit	Description	Format	Unit
7:0	Additional offset for SVID and AVSBus domain (does not apply to PMBus) In AVSBus mode, if applied, need to be in tracking with MFR_VOUT_TRIM. # of VID LSB to add to setpoint (unsigned, always positive).	Fixed Point Unsigned	mV

DPM_OFFSET (0xB064)

Bit	Description	Format	Unit
7:0	DPM threshold offset. Always Negative. Used to offset phase shedding thresholds in order to compensate for each phase current ripple without playing with DPM_HYSTERESYS. LSB weight based on IOUT_EXP and HC support enabled or disabled.	Fixed Point Unsigned	A