STANDARD MICROSYSTEMS CORPORATION

HDC 9224

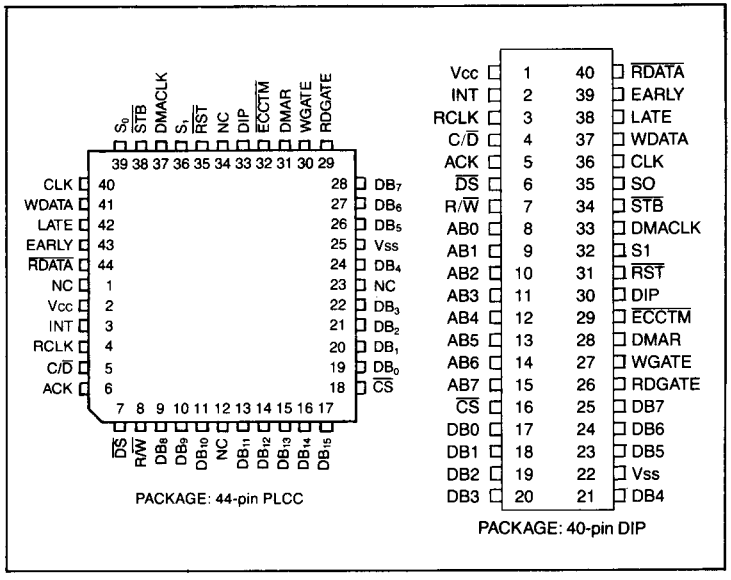
Universal Disk Controller

FEATURES

Programmable Disk Drive Interface and Formats

- ☐ Seagate (ST506) or user definable Hard Disk Formats
- ☐ IBM Compatible Single or Double Density Floppy Disk Formats
- ☐ Controls 8", 5.25", and 3.5" drives
- ☐ Controls tape drives for tape backup of disks
- ☐ Full CRC generation and checking
- ☐ Internal or External Error detection
- ☐ Programmable user-transparent Error correction
- ☐ Programmable automatic retry option
- ☐ Programmable internal write precompensation logic
- ☐ Read/Write commands with automatic seek
- ☐ Multiple sector read/write transfers
- ☐ Sector interleave capability
- ☐ Internal address mark generation and detection
- ☐ Programmable track step rates
- ☐ Supports both buffered and unbuffered seeks
- ☐ Polling command allows overlapping seeks
- ☐ Powerful, high level command set
- ☐ Controls up to 4 drives with
  - ☐ up to 16 heads per drive
  - ☐ up to 2048 cylinders per drive
  - ☐ up to 256 sectors per track

PIN CONFIGURATION



Flexible System Interface

- ☐ Built-in DMA controller capable of addressing up to 16 MBytes
- ☐ Supports either private or virtual buffer memory addressing schemes
- ☐ User readable Interrupt, Chip Status, and Drive Status registers
- ☐ Programmable Interrupt Mask
- ☐ TTL compatible
- ☐ Standard 40 pin DIP package
- ☐ Single +5 volt supply

GENERAL DESCRIPTION

The HDC 9224 Universal Disk Controller (UDC) is a 40 pin, n-channel MOS/LSI device capable of interfacing up to 4 Winchester-type hard disks and/or industry standard floppy disks to a processor. The chip is programmable to support both the Seagate (ST506) and user defined hard disk formats, as well as IBM compatible 8", 5.25" and 3.5" single and double density formats.

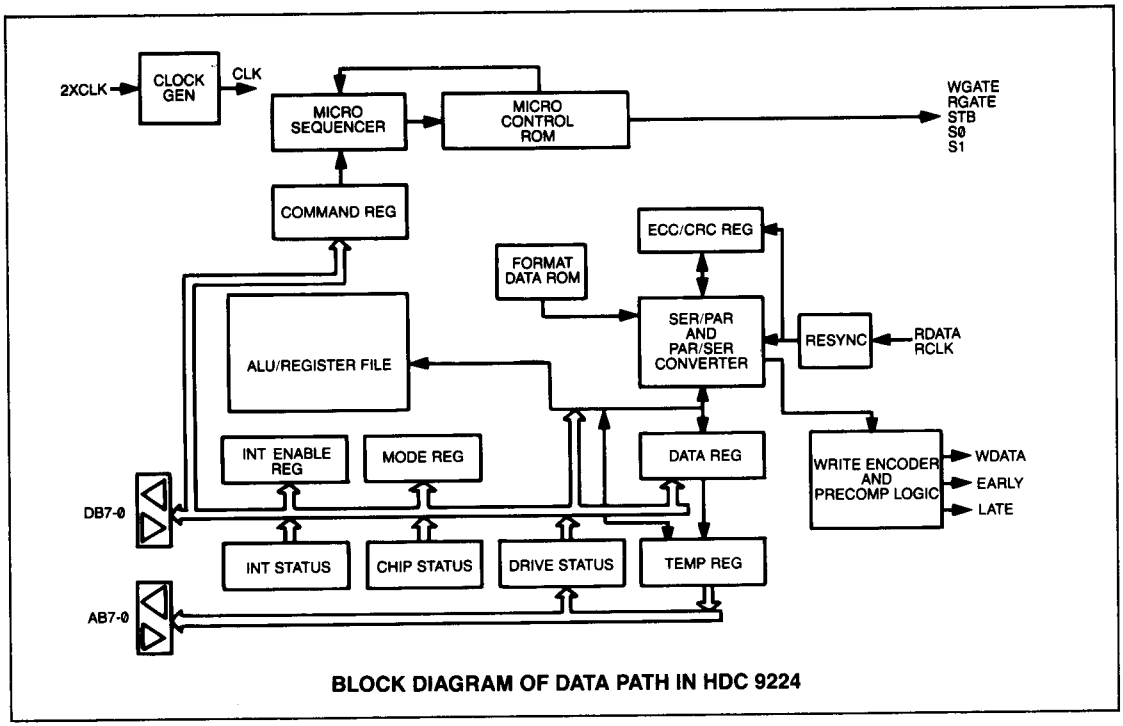
A powerful and sophisticated command set reduces the software overhead required to implement a combined hard disk/floppy disk controller. These commands include:

Drive Select	Seek to cylinder and read ID
Step out 1 cylinder	Step in 1 cylinder
Restore Drive	Read Logical Sectors
Read Physical Sectors	Read Entire Track
Write Logical Sectors	Write Physical Sectors
Chip Reset	Deselect Drive
Poll Drives for Ready	Set Register Pointer
Tape Back-up	Format current track

The HDC 9224 can use both private memory or shared memory buffers with the chip's internal DMA controller providing up to 24 bit addresses over an 8 bit data bus. This enables the HDC 9224 to address up to 16 megabytes of memory, and allows the hardware designer tremendous flexibility in system design.

Several techniques of error detection and correction are implemented on the HDC 9224. One user selected method allows the chip to detect and transparently correct a read error in the data-stream, without external logic. Another technique allows the designer complete control over the ECC algorithm, by using external logic or system software to detect and correct the error. As a further aid in error handling, the HDC 9224 allows the user to specify the number of read retries to be attempted before an error is reported to the host processor by the HDC 9224.

The HDC 9224 features a versatile track format command which allows formatting with interleaved sectors. The chip needs only 3 or 4 bytes of external memory space per sector (depending on format selected). This feature allows the designer to optimize sector interleaving for optimum throughput.



BLOCK DIAGRAM OF DATA PATH IN HDC 9224

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1	Power	V_{CC}	+5 volt power supply pin
22	Ground	V_{SS}	System ground
16	Chip Select	$\overline{CS}$	This signal (when active) selects the HDC 9224 for communications with the host processor. This signal is normally derived by decoding the high order address bits. It is active low.
17,18 19,20 21,23 24,25	Data Bus 7-0	DB7-0	All system processor reads and writes, (including status reads, initialization, disk parameters, and commands) are 8 bit transfers which utilize these lines. When the UDC is accessing memory, data is input or output on these lines. Data on these lines is valid only when DATA STROBE ($\overline{DS}$) is active low.
8-15	Aux Bus 7-0	AB7-0	These 8 pins are used to output drive control signals and DMA Address information. Additionally, these pins are used to input drive status information.
4	Command/$\overline{Data}$	C/$\overline{D}$	During processor to UDC communications, this input is used to indicate whether a command or data transfer will follow. If this pin is low, data may be written to, or read from, the internal data registers. If this pin is high, the processor may write commands or read command results from the UDC.
7	Read/$\overline{Write}$	R/$\overline{W}$	When the processor is communicating to the UDC, a high on this input line indicates a (processor) request for a UDC read operation, and a low indicates a (processor) request for a write operation. R/$\overline{W}$ C/$\overline{D}$ Operation 0 0 Write to register file 0 1 Write to command reg. 1 0 Read from register file 1 1 Read Interrupt Status Register During UDC initiated operations, this pin becomes an output, and is used to indicate a read operation (logic 1) or write operation (logic 0) to external memories.

PIN NO.	NAME	SYMBOL	DESCRIPTION
6	Data Strobe	$\overline{DS}$	This active low pin functions as both an input and output. When the processor is writing to the UDC, the trailing edge of an active (low) signal applied to this pin indicates that the data on DB7-0 is valid, and the data is latched into the appropriate UDC register on the rising edge. When the processor is reading from the UDC, the trailing edge of an active (low) signal applied to this pin is used to clock out the desired UDC register on to DB7-0. During UDC initiated DMA operations, the UDC drives this pin low to either read or write data from memory. On DMA read cycles, data is clocked in on the trailing edge. On DMA write operations, the data on DB7-0 is valid anytime this pin is active (low). When this pin is high (logic 1), DB7-0 return to a high impedance state.
2	Interrupt	INT	This active high output is used by the UDC whenever it wants to interrupt the processor. The interrupt pin is reset to its inactive (low) state when the UDC interrupt status register is read.
30	DMA In Progress	DIP	This active high output becomes active whenever the UDC is actually performing a DMA operation.
28	DMA Request	DMAR	This active high output becomes active whenever the UDC requires the system bus to perform a memory cycle, and ACK is inactive. During hard disk operations, it remains active until the sector transfer is complete. During floppy disk operations, it is active for 1 byte transfer time. The UDC shows that is has released the system bus by resetting this signal to its inactive (low) state.
5	Acknowledge	ACK	This active high signal from the processor tells the UDC that the processor has released the system bus and the UDC may access system memory.
37	Write Data	WDATA	This pin is used to output serial data from the UDC to the drive, in either FM or MFM format. In both cases, data is output with the most significant bit first.
38	Late	LATE	This output (when active high) indicates that the current flux transition appearing on WDATA is to be written late.
39	Early	EARLY	This output (when active high) indicates that the current flux transition appearing on WDATA is to be written early.
27	Write Gate	WGATE	This output (when active high) indicates the drive should allow a write operation.
40	Read Data	$\overline{RDATA}$	This input pin contains the serial bit stream read from the drive, in either FM or MFM format. Media flux reversals are indicated by a negative transition.
3	Read Clock	RCLK	This input is generated by the external data separator. Its frequency should self-adjust to the variations in bit width in the data stream from the drive. This clock supplies a window to indicate half-bit-cell boundaries.
26	Read Gate	RDGATE	This output pin is used to enable the external data separator, compensate for write to read recovery time of the drive, and filter out the write splice in gaps 2 and 3. The timing of this signal is dependent upon the type of drive (hard or floppy) being used. RDGATE is inactive at all times except when the UDC is actually performing a read operation or an internal ECC operation.
29	ECC Time	$\overline{ECCTM}$	When the UDC is used in external ECC mode, this output pin becomes active (low) during the time the UDC is reading the ECC bytes from memory or external ECC chip, when executing a WRITE command. It is also active during internal ECC correction operations, and for either one (write) or two (read) byte times after DIP (pin 30) becomes inactive following a sector transfer. This shows the system processor when it should service the UDC buffer.
32,35	Select 1,0	S1,S0	These active high outputs are used by external logic to select either the source or destination for data transfers occuring via AB7-0. The following table defines the specific transfer being called for by the UDC. (Note that S1-0 are valid only when $\overline{STB}$ is active low.)

$\overline{STB}$	S1	S0	AB7-0 Activity
1	X	X	S1,S0 Invalid
0	0	0	UDC inputs Drive Status Signals
0	0	1	UDC outputs DMA address bytes
0	1	0	UDC outputs OUTPUT 1 signals
0	1	1	UDC outputs OUTPUT 2 signals

PIN NO.	NAME	SYMBOL	DESCRIPTION
34	Strobe	$\overline{STB}$	This active low output indicates when the host processor should read or write to AB7-0, as indicated by S1-0. When AB7-0 are used as outputs from the UDC, data is valid anytime this signal is active (low). When AB7-0 are used as inputs to the UDC, data is clocked in on the rising edge of this signal.
36	DEVICE CLOCK	CLK	This input is the double frequency clock used by the UDC for all internal timing operations. Eight inch hard disk drives (with a nominal bit time of 230 ns) require an input of 8.696 MHz (115 ns period). 5.25" hard disks (with a nominal bit time of 200 ns) require a 10 MHz input (100 ns period). Eight inch, 5.25" and 3.5" floppy drives all require a 10 MHz clock, which is internally prescaled by the UDC to the correct frequency, as determined from the Drive Select command and MODE register. This input requires an external pull-up resistor, as it is not TTL-level compatible. See figure 2.
31	Reset	$\overline{RST}$	This active low input will force the UDC into the following known state: INT–Inactive low WDATA–Inactive low $\overline{ECCTM}$–Inactive high DMAR–Inactive low EARLY–Inactive low C/$\overline{D}$–Input AB7-0–Input LATE–Inactive low R/$\overline{W}$–Input DB7-0–Input WGATE–Inactive low DIP–Inactive low RDGATE–Inactive low $\overline{DS}$–Input An active low on this pin has the same effect as a RESET Command.
33	DMA Clock	DMACLK	All UDC DMA operations will be synchronized to this clock input. Three DMACLK periods are required for each DMA byte transfer.

OVERVIEW OF UDC REGISTERS

The HDC 9224 has three types of internal, processor addressable registers; Read/Write, Read Only, and Write Only. These registers are addressed by an internal register pointer that is set by the SET REGISTER POINTER command.

All register data is passed to and from the UDC via the data bus (DB7-0).

The internal register pointer is automatically incremented with each register access until it points to the DATA Register. This insures that all subsequent register accesses will address the DATA register.

PROCESSOR ACESSIBLE REGISTERS

REGISTER ADDR	WRITE	READ
0	DMA7-0	DMA7-0
1	DMA15-8	DMA15-8
2	DMA23-16	DMA23-16
3	Desired Sector	Desired Sector
4	Desired Head	Current Head
5	Desired Cylinder	Current Cylinder
6	Sector Count	Temporary Storage
7	Retry Count	Temporary Storage
8	Mode	Chip Status
9	Interrupt/Command Terminator	Drive Status
A	Data/Delay	Data
COMMAND	Current Command	Interrupt Status

Three internal registers (OUTPUT 1, OUTPUT 2, and INPUT DRIVE STATUS) which are not directly addressable by the processor are accessed by the UDC. The information contained in these registers is used in disk interfacing and is input or output on UDC Pins AB7-0. The following table describes these registers and the signals they output or input on AB7-0.

UDC ADDRESSABLE REGISTERS

DRIVE STATUS REGISTER (input)	**Select Pins S1 = 0, S0 = 0**
AB7—ECC Error	AB6—Index Pulse
AB5—Seek Complete	AB4—Track 00
AB3—User Defined	AB2—Write Protect
AB1—Drive Ready	AB0—Write Fault

OUTPUT 1 (Output)	**Select Pins S1 = 1, S0 = 0**
AB7—Drive Select 3	AB6—Drive Select 2
AB5—Drive Select 1	AB4—Drive Select 0
AB3—Programmable Outputs (see text)	AB2—Programmable Outputs
AB1—Programmable Outputs	AB0—Programmable Outputs

OUTPUT 2 (Output)	**Select Pins S1 = 1, S0 = 1**
AB7—$\overline{\text{Drive Select 3}}$	AB6—Reduce Write Current
AB5—Step Direction	AB4—Step Pulse
AB3—Desired Head (Bit 3)	AB2—Desired Head (Bit 2)
AB1—Desired Head (Bit 1)	AB0—Desired Head (Bit 0)

Additionally, several registers (DMA7-0, DMA15-8, DMA23-16, DESIRED SECTOR, DESIRED CYLINDER, SECTOR COUNT, and RETRY COUNT) serve an alternate purpose. These registers are used by the FORMAT TRACK command to hold parameters. This alternate register utilization is described in detail under the FORMAT TRACK command.

DESCRIPTION OF UDC REGISTERS

DMA 7-0 (R/W Register; Address 0)
This 8-bit read/write register is loaded with the low order byte (MSB in bit 7) of the DMA buffer memory starting address.

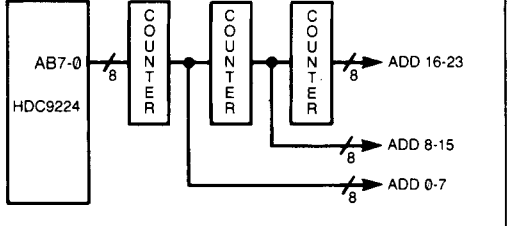
DMA 15-8 (R/W Register; Address 1)
This 8-bit read/write register is loaded with the middle order byte (MSB in bit 7) of the DMA buffer memory starting address.

DMA 23-16 (R/W Register; Address 2)
This 8 bit read/write register is loaded with the high order byte (MSB in bit 7) of the DMA buffer memory starting address.

Prior to the data transfer portion of a read or write command, the UDC writes the contents of the DMA registers to an external counter. This transfer (from the registers to the external counter) is accomplished by the UDC with 3 separate outputs on AB7-0, with the contents of DMA 24-16 being transfered first. (In memory areas that require less than 24 bit addressing, the higher order bits are overwritten. The external counter must be incremented with the UDC's $\overline{DS}$ signal after each byte transfer.

If, during read operations, an error is detected during the data transfer, a retry will occur (if so programmed), and the three DMA registers will re-initialize the external counter to the original starting address.

During multiple sector read/write operations, the DMA address contained in the DMA registers will be incremented by the size of the sector selected at each sector boundary. This ensures that during read operations the address contained in the DMA registers always corresponds to the proper memory starting address of the sector currently being read.



DMA COUNTER OPERATION

DESIRED SECTOR REGISTER (R/W Register; Address 3)
This 8-bit read/write register is loaded with the starting sector number of a multiple sector read/write operation. Except for the last sector of the operation, this register is incremented after each sector is written or read without error.

If the UDC terminates a command because of an error, this register will normally contain the bad sector number, and may be read by the processor.

DESIRED HEAD REGISTER (Write Register; Address 4)
This 8-bit write only register is loaded with the 4-bit head number, and the upper 3 bits of the desired cylinder number.
BIT 7 ALWAYS 0
BITS 6-4 MSBs of the Desired Cylinder number
BITS 3-0 Desired Head Number.
The desired head number is output on AB3-0 during OUTPUT 2 times.

DESIRED CYLINDER REGISTER (Write Register; Address 5)
This 8-bit write only register is loaded with the 8 low order bits of the desired cylinder (MSB in Bit 7). Combined with the 3 high order bits loaded into the DESIRED HEAD REGISTER, these 11 bits form the desired cylinder number, which is checked by read and write operations during the Check ID portion of the command.

SECTOR COUNT REGISTER (Write Register; Address 6)
This 8-bit write only register is loaded with the number of sectors to be operated on by the read or write command. This allows multiple sectors on the same cylinder to be either written or read.

RETRY COUNT REGISTER (Write Register; Address 7)
This 8-bit write only register is loaded with the number of times the UDC should retry to read a data field before reporting an error. Additionally, this register is loaded with the user programmable output signals that the UDC outputs on AB0-3 during OUTPUT 1 times.
The retry count is loaded (in 1's complement format) into the 4 most significant bits of this register.
The user programmable output signals are loaded into the 4 least significant bits of the register.
BITS 7-4 Desired Retry Count (in 1's complement format)
BITS 3-0 User Programmable Output Signals

MODE REGISTER (Write Register; Address 8)
This 8-bit write only register defines the operating mode of the UDC as follows:
BIT 7 (DRIVE DATA TYPE)
This bit determines how the UDC decodes data from the drive.
BIT 7 = (1): UDC configured for hard disk use. (Level transitions)
BIT 7 = (0): UDC configured for floppy use. (Pulse inputs)
BITS 6,5 (CRC/ECC Enable Code)
These bits determine the error detection/correction code generated and checked by the UDC.

DB6	DB5	CODE GENERATED/CHECKED
0	0	CRC
0	1	External ECC
1	0	Internal 32 bit ECC without correction
1	1	Internal 32 bit ECC with correction

With internal ECC selected the UDC will transfer 4 extra bytes during reads and writes. Normal CRC checking is still done on all ID fields.

With external ECC selected the UDC will flag an ECC error via BIT 7 of the DRIVE STATUS REGISTER. Normal CRC checking is still done on all ID fields.

If neither internal or external ECC is selected, then the UDC will perform CRC checks on both data and ID fields.

STEP RATES FOR DOUBLE DENSITY (MFM) OPERATION **(Mode Bit 4 = 0)**

DRIVE TYPE			5.25" HARD DISK	8" FLOPPY	5.25" FLOPPY
DB2	DB1	DB0	STEP RATE	STEP RATE	STEP RATE
1	1	1	12.8 ms	128 ms	256 ms
1	1	0	6.4 ms	64 ms	128 ms
1	0	1	3.2 ms	32 ms	64 ms
1	0	0	1.6 ms	16 ms	32 ms
0	1	1	0.8 ms	8 ms	16 ms
0	1	0	0.4 ms	4 ms	8 ms
0	0	1	0.2 ms	2 ms	4 ms
0	0	0	17.6 us *	176 us *	352 us *
0	0	0	21.8 us **	218 us **	436 us **
Pulse Width:			11.2 us	112 us	224 us

*This rate applies for SEEK commands only
**This rate applies for RESTORE commands only

(DOUBLE ALL OF THE ABOVE TIMES FOR SINGLE DENSITY (FM) OPERATIONS.)

BIT 4 (Single or Double Density)
This bit determines whether the UDC will perform its operations in either single or double density.

BIT 4 = (1) Single Density (FM) Format
BIT 4 = (0) Double Density (MFM) Format

BIT 3 (ALWAYS 0)

BITS 2,1,0 (Step Rate Select)
These bits are programmed to select the desired drive step rate. Note that all step rates are determined by the type of drive and density selected, and are scaled from the CLK input.

The UDC can output extremely rapid step rate pulses if these bits are set to 000. This is useful when the UDC is controlling drives which support buffered seeks. For other speeds, please refer to the table above.

INTERRUPT/COMAND TERMINATION REGISTER (Write Register; Address 9)

This 8-bit write only register allows the programmer to mask out a number of conditions that would cause termination of a command. (Such termination occurs when the DONE bit in the INTERRUPT STATUS register is set.) One bit in this register also controls the generation of interrupts when either the DONE bit or the READY CHANGE bit in the INTERRUPT STATUS register go active.

BIT 7 (CRC PRESET)
Setting this bit to "1" will cause the CRC register to preset to 1 for CRC generation and checking. Setting this bit to "0" will cause the CRC register to preset to 0 for CRC generation and checking.

ID field CRC and data field CRC or ECC are generated and tested from the first A1 HEX byte in the ID field.

BIT 6 (ALWAYS "0")
This bit should always be set to "0" by the user. Failure to do this may result in unreliable operation.

BIT 5 (INT ON DONE)
If this bit is set (to "1"), an interrupt will occur when the DONE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

BIT 4 (DELETED DATA MARK)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the DELETED DATA MARK bit in the CHIP STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 3 (USER DEFINED)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the USER DEFINED status bit in the DRIVE STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 2 (WRITE PROTECT)
If this bit is set to (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE PROTECT bit in the DRIVE STATUS register goes active.

BIT 1 (READY CHANGE)
If this bit is set (to "1"), an interrupt will occur when the READY CHANGE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

The user should note that as a drive is selected or deselected, it is possible for the ready line from the drive to change state, and care should be taken in the design of the interrupt handler.

BIT 0 (WRITE FAULT)
If this bit is set (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE FAULT status bit in the DRIVE STATUS register is set. The command in progress will terminate when the current sector operation is completed.

DATA/DELAY REGISTER (R/W Register; Address 0AH)

This 8-bit read /write register serves a dual purpose. During UDC writes, data is placed in this register for recording to the disk. During UDC reads, recovered data is fetched from this register for storage into memory. All transfers occur via DB7-0, under DMA control.

Additionally, this register is loaded with the HEAD LOAD TIMER COUNT when the Drive Select command is issued. (Note that the actual amount of head load time is this value, times a value predetermined by the UDC, based on the type of drive selected. For more information, please see the Drive Select command description.)

COMMAND REGISTER (Write Register)

This 8-bit write only register is used to pass commands to the UDC. Valid commands are given to the UDC by setting C/$\overline{D}$ high and R/$\overline{W}$ active high, while strobing $\overline{DS}$ active (low).

CURRENT HEAD REGISTER Read Register; Address 4)

This 8-bit read only register is updated from the disk when a valid ID field sync mark is found while executing a read ID field command sequence. This register contains the actual head number, bad sector flag, and the 3 most significant bits of the cylinder number, as specified during formatting.

BIT 7 = (1) Last sector read had BAD SECTOR bit set
BIT 7 = (0) Last sector read had BAD SECTOR bit reset.

BITS 6-4 Three most significant bits of the current cylinder. (Most significant bit in Bit 6.)

BITS 3-0 Current Head Number (MSB in bit 3).

CURRENT CYLINDER REGISTER (Read Register; Address 5)

This 8-bit read only register is updated from the disk when a valid ID field sync mark is found while executing a read ID field command sequence. This register will contain the 8 least significant bits of the cylinder ID number, as specified during formatting. (The 3 most significant bits of the 11 bit cylinder ID number are contained as part of the CURRENT HEAD REGISTER.)

INTERRUPT STATUS REGISTER (Read Register)

This 8-bit read only register contains status information associated with interrupt conditions and errors that occur during disk operation. This register is read by setting C/$\overline{D}$ high, and R/$\overline{W}$ high.

When the Interrupt Status register is read, the INT output signal from the UDC will be reset (to an inactive low level).

BIT 7 (INTERRUPT PENDING)
A "1" indicates that either DONE bit or READY CHANGE bit has gone active. The user may disable these interrupts by setting the appropriate bits in the INTERRUPT/COMMAND TERMINATION, REGISTER. This bit is reset (to "0") by reading the Interrupt Status register.

BIT 6 (DMA REQUEST)
A "1" indicates that the UDC requires a data transfer either to or from its data register. This bit is reset (to "0") by the data transfer.

BIT 5 (DONE)
A "1" indicates that the current command is completed. This bit is reset (to "0") when a new command is issued.

BIT 4,3 (COMMAND TERMINATION CODE)
(Valid only when DONE is set)
These two bits indicate the command termination conditions:

BIT 4	BIT 3	CONDITIONS
0	0	Successful command termination
0	1	Execution error in READ ID Sequence
1	0	Execution error in SEEK Sequence
1	1	Execution error in DATA field

More detailed command termination error information is obtained by reading the Chip Status register.

BIT 2 (READY CHANGE)
A "1" indicates that the "ready" signal from the drive has experienced a low-to-high or high-to-low transition. (This shows that the drive has either become ready or become not ready.) This bit is reset (to "0") by reading the Interrupt Status register.

BIT 1 (OVERRUN/UNDERRUN)
A "1" indicates that a overrun or underrun condition has occured during a read or write command. These conditions occur when the UDC does not receive an acknowledge (to a DMA request) by the time a byte is ready for transfer to or from the processor.

This bit can only be reset (to "0") with a RESET command or a high on the RESET pin.

BIT 0 (BAD SECTOR)
A "1" indicates that a bad sector (as indicated from the MSB of the head ID byte in the ID field) has been encountered. This bit is reset when a new command is issued, or a good sector is read.

CHIP STATUS REGISTER (Read Register; Address 8)

This 8-bit read only register supplies additional chip status information. The information in this register is only valid between the time that the DONE bit is set in the INTERRUPT STATUS register and the time when the next command is issued to the UDC.

BIT 7 (RETRY REQUIRED)
If a retry was attempted by the UDC during the execution of any read or write command, this bit is set (to "1").

BIT 6 (ECC CORRECTION ATTEMPTED)
If the internal ECC circuitry has attempted to correct a bad sector, this bit is set (to "1").

BIT 5 (CRC/ECC ERROR)
If the UDC detects a CRC error or an ECC error, this bit is set (to "1").

BIT 4 (DELETED DATA MARK)
If the UDC reads a deleted data mark in the ID field, this bit is set (to "1"), otherwise it is reset (to "0").

BIT 3 (SYNC ERROR)
If the UDC does not find a sync mark when it is attempting to read either an ID or data field, then this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 2 (COMPARE ERROR)
If the information contained in the DESIRED HEAD and DESIRED CYLINDER registers does not match that contained in an ID field on the disk, this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 1,0 (PRESENT DRIVE SELECTED)
These two binary encoded bits represent the drive currently selected and correspond to the Drive Select bits set in the Output 1 and Output 2 latches.

BIT 1	BIT 0	DRIVE SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

DRIVE STATUS REGISTER (Read Register; Address 9)

This 8-bit read only register contains status information generated by the drives, external ECC Chip (if any), and a user definable input to the UDC from the drive.

To save pins on the UDC, the 8 status lines are input on AB7-0 and are latched in this internal register. The UDC will update this register whenever it is not using AB7-0 to output DMA counter values, OUTPUT 1, or OUTPUT 2 data. When configured as described below, the UDC will input drive status signals and interpret them as follows. In all cases, a logic "1" is considered the active input.

BIT 7 (ECC ERROR)
This bit is set (to "1") when the ECC ERROR signal is generated by an external ECC chip. This signal is input to the UDC on AB7.

BIT 6 (INDEX)
This bit is set (to "1") when the INDEX signal from the selected drive is active. Typically, index pulses from the drives are active for 10us-100us for each disk revolution. This signal is input to the UDC on AB6.

BIT 5 (SEEK COMPLETE)
This bit is set (to "1") when the SEEK COMPLETE signal from the selected drive is active. This bit will go active when the heads of the selected drive have settled over the desired track (at the completion of a seek).

When a drive supplies this signal, reading and writing should not be attempted until SEEK COMPLETE is set (to "1"). This signal is input on AB5.

For floppy disk operation, where the drives normally do not provide this signal, a retriggerable one shot could be used to generate a SEEK COMPLETE signal (if desired).

BIT 4 (TRACK 00)
This bit is set (to "1") when the TRACK 00 signal from the selected drive is active. This indicates that the heads on the selected drive are positioned over track 0. This signal is input on AB4.

BIT 3 (USER DEFINED)
This bit is set (to "1") when the USER DEFINED signal is active. This signal is input on AB3.

BIT 2 (WRITE PROTECT)
This bit is set (to "1") when the WRITE PROTECT signal from the selected drive is active. When set, this bit indicates that the disk in the selected drive is write protected. This signal is input on AB2.

BIT 1 (READY)
This bit is set (to "1") when the READY signal from the selected drive is active. When set, this bit indicates that the drive is ready to execute commands. This signal is input on AB1.

BIT 0 (WRITE FAULT)
This bit is set (to "1") when the WRITE FAULT signal from the selected drive is active. This signal, when active, indicates that a condition exists at the drive that would cause improper writing on the disk. This signal is input to the UDC on AB0.

TEMPORARY STORAGE REGISTERS

The UDC contains two temporary storage registers, used by the UDC for internal operations. The host processor should not attempt to read or modify these registers, as unpredictable results may occur.

UDC COMMAND OVERVIEW

The HDC 9224 has 16 high-level commands that provide the user with a high degree of flexibility and control. All of the commands for the UDC can be thought of as falling into one of two basic groups.

The first group handles the "housekeeping" required by the drives and the UDC itself. These commands are:

RESET	STEP OUT 1 CYLINDER
STEP IN 1 CYLINDER	SET REGISTER POINTER
DRIVE SELECT	RESTORE DRIVE
DESELECT DRIVES	POLL DRIVES

The second group comprises the "READ/WRITE" functions required in a magnetic disk subsystem. These commands are:

SEEK/READ ID	TAPE BACKUP (READ/
FORMAT TRACK	WRITE)
READ TRACK	READ SECTORS LOGICAL
READ SECTORS PHYSICAL	
WRITE SECTORS LOGICAL	

An internal status byte, which contains the BAD SECTOR, DELETED DATA and OVER/UNDER RUN bits, along with the current state of the READY, WRITE PROTECT, WRITE FAULT, and USER DEFINED lines, is checked at various times during command execution.

This internal status byte is examined before the execution of all READ/WRITE commands, and is also checked just prior to the completion of all commands (except for RESET, where its values would be meaningless.)

This byte is also checked by the UDC between sector operations during the execution of READ LOGICAL, READ PHYSICAL, WRITE LOGICAL and WRITE PHYSICAL commands.

The UDC makes decisions regarding command termination and interrupt generation based on the contents of this status byte, and the state of the bits in the INTERRUPT/COMMAND TERMINATION register. (Note that "write protect" and "write fault" status may cause command termination only during write and format operations.)

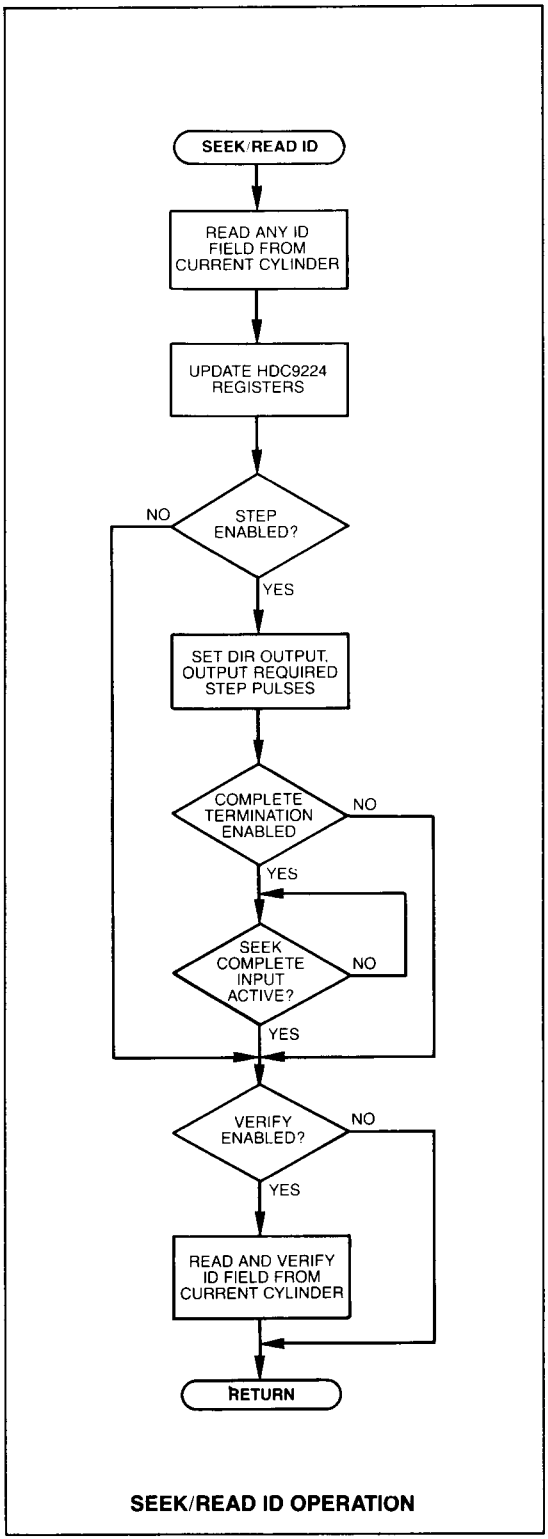
All commands (except RESET) terminate with the DONE bit in the INTERRUPT STATUS register being set. This bit may also be considered to be an inverted "busy" line, as the UDC resets it upon receipt of a valid command.

During all READ/WRITE group commands (except FORMAT TRACK and BACKUP), the UDC utilizes some common command execution sequences. Prior to entering each sequence the UDC sets the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to a known state. If a command fails to execute properly, these bits may then be used to determine where the command aborted.

The sequences common to the READ/WRITE group commands are as follows:

1. READ ID FIELD (Command Termination Code = 0-1)
   First, the UDC attempts to find an ID Field Sync mark. If no sync mark is found within 33,792 byte times (byte time = time to read one byte from the type of drive selected), the SYNC ERROR bit (in the CHIP STATUS register) is set (to "1"), and the command is terminated.

   During this phase, the UDC will raise and drop RDGATE up to 256 times (as it attempts to read each sector on the cylinder).



SEEK/READ ID OPERATION

After the ID Field is found, the UDC reads it and updates it CURRENT HEAD and CURRENT CYLINDER registers. This information was written to the disk during formatting.

Next, the UDC checks the CRC of the ID field which was read. If it is incorrect, the UDC sets (to "1") the CRC ERROR status bit (in the CHIP STATUS register) and terminates the command.

If the CRC is correct, the UDC then calculates the direction and number of step pulses required to move the head from the current cylinder to the cylinder specified in the DESIRED HEAD REGISTER. These pulses, and the direction bit are output during the OUTPUT 2 times.

If a command should terminate while in the sequence, the COMMAND TERMINATION bits will be set to 0-1.

2. VERIFY (Command Termination Code = 1-0)

After the UDC has read the ID Field, it attempts to verify that it has found the correct cylinder. To do this, the UDC tries to find an ID Field sync mark on the selected disk. If the UDC is unable to find an ID Field sync mark within 33,792 byte times, the SYNC ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

The UDC, after finding the ID Field sync mark, then reads the ID field and compares the information on the disk to the information contained in the DESIRED CYLINDER, DESIRED HEAD and DESIRED SECTOR registers.

The UDC will hunt for sync marks and read ID fields until the desired sector is found. If the desired sector is not located within 33,792 byte times, then the COMPARE ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

After the correct sector is found, the UDC checks the CRC for the sector ID Field. If this is found to be incorrect, the UDC sets to "1" the CRC/ECC ERROR bit in the CHIP STATUS register, and the command is terminated.

(When the UDC is executing a READ PHYSICAL or WRITE PHYSICAL command, ID Fields are checked only until the first sector to be transfered is found. No ID Field checking is performed on subsequent sectors, although CRC checking is done.)

If a command should terminate while in this sequence, the COMMAND TERMINATION bits will be set to 1-0.

3. DATA TRANSFER (Command Termination Code = 1-1)

If a READ PHYSICAL or READ LOGICAL command is being executed, the UDC will try to find a data sync mark (FBhex or F8hex) on the disk. If the sync mark found is F8h, then the UDC will set the DELETED DATA MARK bit in the CHIP STATUS register.

After a data sync mark is found, the UDC then updates its CURRENT HEAD and CURRENT CYLINDER registers from the information found on the disk and initiates a DMA request. If the host processor does not respond to the request within 1 byte time, then the UDC will set to "1" the OVER/UNDERRUN status bit in the INTERRUPT STATUS register, and the command will terminate.

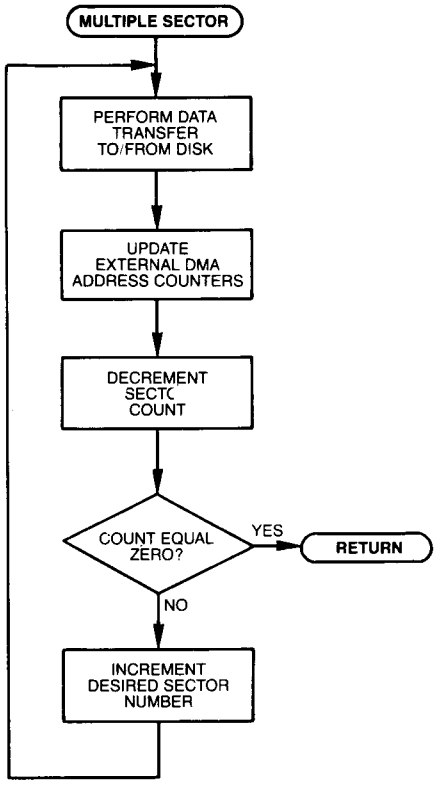
Using DMA, the UDC transfers a sector's worth of data, and then reads the ECC and/or CRC bytes. If a CRC error or uncorrectable ECC error is detected, the UDC will decrement the RETRY REGISTER, set the RETRY REQUIRED status bit (in the CHIP STATUS

register), and return to the VERIFY sequence.

If the UDC cannot read the sector, and the count in the ENTRY COUNT register has expired, then the CRC/ECC Error bit (in the CHIP STATUS register) is set, and the command terminates.

During a multi-sector transfer, the UDC updates the DMA registers after all sector operations, including the last one, and the SECTOR COUNT register is decremented. If the SECTOR COUNT register equals 0, then the command is terminated. If the SECTOR COUNT register is not equal to 0, then the UDC will increment the DESIRED SECTOR register, re-initialize the RETRY COUNT register (to its original value) and return to the VERIFY sequence.

If a command should terminate while in this sequence, the command termination bits will be set to 1-1.



MULTIPLE SECTOR READ OPERATIONS

COMMAND DESCRIPTION

RESET **(Hex Value = 00)**

This command causes the UDC to return to a known state. This command allows the system software to reset the chip, and has the same effect as $\overline{RST}$ input becoming active.

DESELECT DRIVE **(Hex Value = 01)**

This command causes all of the drive select bits (Drive Select 0-3) in the OUTPUT 1 and OUTPUT 2 registers to become inactive.

RESTORE DRIVE **(Hex Values = 02, 03)**

This command will cause the HDC 9224 to output step pulses to the selected drive, so as to move the head back to Track 00. Before each step pulse, the UDC first checks the TRK00 and READY bits in the DRIVE STATUS register. If TRK00 is active (high) or READY is inactive (low), then the UDC will terminate the command.

The UDC will output up to 4096 step pulses. If the drive does not respond with an active (high) TRK00 signal within this period, the UDC will terminate the command with the DONE bit set (to "1") and the COMMAND TERMINATION CODE bits set to 1-0. (These bits are contained in the INTERRUPT STATUS register.)

This command takes two forms:

COMMAND BYTE	RESULT
02	The command will terminate, and an interrupt generated after the UDC has issued the step pulses.
03	The command will terminate, and an interrupt generated after the drive has provided a SEEK COMPLETE signal to the UDC. (This is useful in systems with "buffered seek" drives.)

This command uses the step rate value loaded into the MODE register.

STEP IN 1 CYLINDER **(Hex Values = 04, 05)**

This command will cause the HDC 9224 to issue one step pulse towards the inner most track. This command is generally used during track formatting, and takes two forms:

COMMAND BYTE	RESULT
04	The command will terminate, and an interrupt generated after the UDC issues the step pulse.
05	The command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of SEEK COMPLETE the UDC will generate an interrupt.

This command uses the step rate value programmed into the MODE register.

STEP OUT 1 CYLINDER **(Hex Values = 06, 07)**

This command will cause the HDC 9224 to issue one step pulse towards the outer most track (Track 00). This command is generally used during track formatting, and takes two forms:

COMMAND BYTE	RESULT
06	This command will terminate, and an interrupt generated after the UDC issues the step pulse.
07	This command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of the SEEK COMPLETE, the UDC will generate an interrupt.

This command uses the step rate value programmed into the MODE Register.

POLL DRIVES (Hex Values = 10 thru 1F)

This command polls the drives for a SEEK COMPLETE signal allowing the user to perform simultaneous seeks on up to four drives. Polling is enabled by setting (to 1) the appropriate bit in the command word: bit 0 for drive 0 thru to bit 3 for drive 3.

This command executes as follows:

The UDC will output a drive select for the first drive in the polling sequence and look for a SEEK COMPLETE status input from the polled drive. If the polled drive has not completed a seek, then this line remains low (logic 0), and the UDC selects the next drive in the polling sequence. This continues until the UDC detects a SEEK COMPLETE signal from a drive, which causes the DONE bit in the Interrupt Status register to be set, and the command terminates.

The UDC will continue to select the drive that produced the SEEK COMPLETE signal, allowing the user to read the DRIVE STATUS register to determine which drive caused the command termination.

The POLL DRIVES command must be preceeded by DESELECT.

DRIVE SELECT (Hex Values = 20 thru 3F)

This command will cause one of (up to) four drives to be selected for operation. Any previously selected drive is deselected by this command. Bits 0 and 1 in the command word indicate (in binary form) which of the (up to) four drives has been selected.

COMMAND WORD		DRIVE SELECTED
DB1	DB0	
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

Decoded drive select signals are then placed on the data bus (via AB7-AB4) during OUTPUT 1 times and should be latched externally.

Since the HDC 9224 can interface both hard disks and floppy disks to a processor, the Drive Select command needs to also specify the type of drive being selected. Bits 2 and 3 in the command word are used to pass this information to the chip, and take the following form:

COMMAND WORD		TYPE OF DRIVE
DB3	DB2	
0	0	Hard disk with ST506 (Seagate) compatible format—256 byte data field and 3 byte ID field per sector. No internal clock prescaling performed.
0	1	Hard disk with user defineable format. This format allows a data field length of 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes with 4 byte ID field per sector. No internal clock pre-scaling is performed.
1	0	8 inch floppy disk, with standard 4 byte ID field. An internal divider creates a 1 MHz clock to be compatible with standard disk data rates.
1	1	5.25 inch floppy disk, with standard 4 byte ID field. An internal divider creates a 500 KHz clock to be compatible with standard disk data rates.

NOTE: Microfloppy system designers should determine whether the drive they have chosen to use in the system is compatible with 8" floppy drives or 5.25" floppy drives, and use the appropriate values from the table above.

Note that eight inch Winchester-type drives require an 8.696 MHz system clock. All other drives require a 10 MHz system clock. It is not possible for the UDC to derive internally the clocks required for floppy disk operation from the 8.696 MHz clock required by 8 inch Winchester drives.

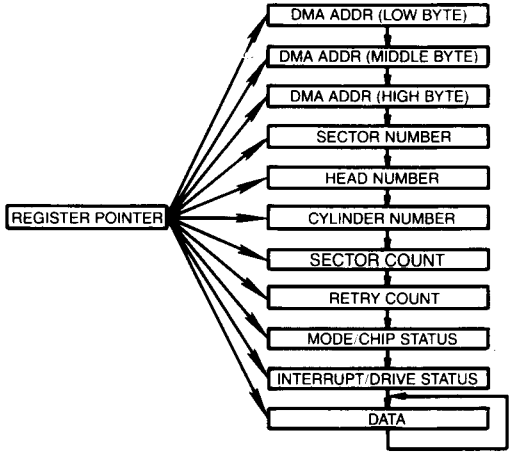
To insure compatibility with various drives, the HDC 9224 features a programmable head load timer. Head load delay may be inhibited by resetting the Delay Bit (Bit 4) in the Drive Select command word to 0. If Bit 4 is set (to 1), then the head load delay timer is configured with the value in the DATA/DELAY register (Register A), multiplied by value shown below:

DRIVE AND FORMAT SELECTED	HEAD LOAD TIMER INCREMENT (BIT 4 = 1 = Delay Enabled)	
5.25" HARD DISK (Double Density)	200 usec	(The HEAD LOAD TIMER is set to a value equal to this increment times the number in the DATA/DELAY register.)
5.25" HARD DISK (Single Density)	400 usec	
8" FLOPPY (Double Density)	2 msec	
8" FLOPPY (Single Density)	4 msec	
5.25" FLOPPY (Double Density)	4 msec	
5.25" FLOPPY (Single Density	8 msec	

The Drive Select command also optimizes certain characteristics of the HDC 9224 for the type of drive selected.

IF HARD DISK SELECTED:

- –DMA mechanism works in burst mode and the bus is held for the entire sector transfer.
- –The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.
- –The GAP lengths are as shown in Table 1.



SET REGISTER POINTER COMMAND

IF FLOPPY DISK SELECTED:

–DMA mechanism transfers an 8-bit byte, and releases the bus.

–The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.

–The GAP lengths are as shown in Table 1.

–The CLK input clock is prescaled (internally) to create an internal clock compatible with the floppy disk data rates.

SET REGISTER POINTER (Hex Values = 40 to 4A)
This command causes the register pointer to point to a register. The desired register number is loaded into the 4 least significant bits of the command word. (MSB in BIT 3).

The register pointer is incremented by the UDC on each register access, until it points to the DATA register. This reduces the number of times the user must set the register pointer during read and write operation.

Care should be taken to ensure that only valid register values are loaded into the command word. (Valid register numbers are 0 thru OAH.)

SEEK/READ ID (Hex Values = 50 to 57)
This command will cause the UDC to read the first sector ID field found from the currently selected drive, head, and cylinder. The MODE register should contain the correct value for step rate and density options.

After reading the ID field the UDC will examine the command word and execute the specified options. Bits 2 thru 0 in the command word are used to specify the following options:

BIT 2 = 1 STEP ENABLE. The UDC will execute the step sequence, and position the head on the track specified by the DESIRED CYLINDER register.

BIT 2 = 0 STEP DISABLE. No step pulses will be issued by the UDC.

BIT 1 = 1 WAIT FOR COMPLETE. The UDC will proceed to the verify sequence only after the drive has issued a SEEK COMPLETE signal.

BIT 1 = 0 DO NOT WAIT FOR COMPLETE. The UDC will proceed to the verify sequence after the last step pulse has been issued.

BIT 0 = 1 VERIFY ID. The UDC will execute the VERIFY sequence after operations selected by the previous options have finished.

BIT 0 = 0 DISABLE VERIFY ID. The UDC will not enter the VERIFY sequence. Instead, the command will terminate.

The order in which these options execute is: STEP, COMPLETE, VERIFY ID. Any combination of these option bits may be specified in the command word.

READ SECTORS PHYSICAL (Hex Values = 58 and 59)
This command will cause the UDC to read up to a full track from the disk. The user specifies the MODE, DESIRED CYLINDER, DESIRED HEAD, and DESIRED SECTOR along with the SECTOR COUNT. The UDC will find the requested cylinder and sector and set up to begin the data transfer.

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

If a BAD SECTOR bit is read (from the sector ID field) the UDC will set the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to 1-0, and set the DONE bit (in the INTERRUPT STATUS register) to 1, and terminate the command.

After each sector is successfully read, the SECTOR COUNT register is decremented. If the SECTOR COUNT register is not yet equal to 0 the process is repeated for the next physical sector on the track. This command also will terminate if the Index pulse is received from the drive.

(Note that after the first sector is found, no further comparison is made against sector numbers found on the disk as the DESIRED SECTOR register value may not correspond to the next physical sector on the disk because of sector interleaving.)

This command takes two forms allowing the user to specify the desired transfer option. The options are specified by Bit 0 in the command word, and are:

BIT 0 = 1 TRANSFER ENABLE. The UDC will transfer the data fields to (external) memory, using DMA.

BIT 0 = 0 TRANSFER DISABLE. The UDC will NOT transfer any data to (external) memory, but all error detection circuitry will be enabled and errors reported. This is useful in detecting bad sectors and tracks on the disk.

Before executing this command, the user must set the RETRY COUNT to 0. This is done by loading the high order nybble in the RETRY COUNT register to "1111" (zero in 1's complement format). Failure to do this will result in unpredictable performance because the DESIRED SECTOR register value may not correspond to the next physical sector on the disk.

READ TRACK (Hex Values = 5A and 5B)
When this command is issued, the UDC will read the data from the entire track on which the selected drive is currently sitting: The UDC will begin reading when it detects the leading edge of an index mark signal from the drive, and terminate reading when it detects the next leading edge of an index mark signal. Sync detect is performed for the ID field, but no error checking is done on the data field.

This command allows the user to specify a data transfer option, using Bit 0 in the command word. These options are:

BIT 0 = 1 TRANSFER ALL DATA. The UDC will transfer the ID field and data fields to (external) memory.

BIT 0 = 0 TRANSFER ONLY IDs. The UDC will transfer only ID fields to the (external) memory. This is useful during tape backup operations.

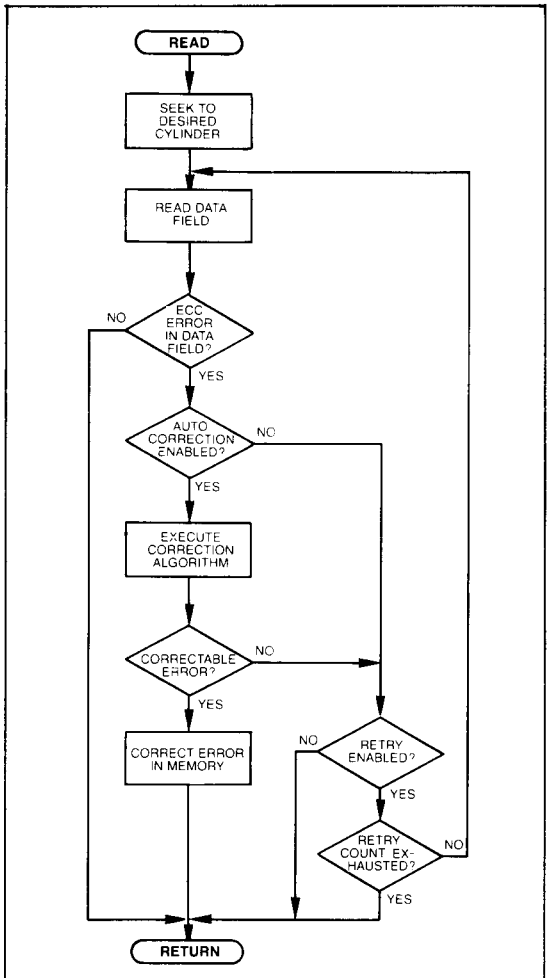
READ SECTORS LOGICAL (Hex Values = 5C to 5F)
When this command is issued, the UDC will read up to a full track from the selected drive. Prior to reading the data from the disk, the UDC will use the information in the MODE, DESIRED CYLINDER, DESIRED SECTOR and DESIRED HEAD registers to locate the correct track, sector and drive surface (using the previously described VERIFY sequence).

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

Before the command is issued, the system processor must also load the desired values into the MODE, SECTOR COUNT, RETRY COUNT and the three DMA registers.

When reading multiple sectors, the read command must be configured with ECC correction disabled. If a hard error is detected, the sector count must be set to one, retry count to zero, and ECC correction enabled. The sector can then be read and corrected. After the error has been corrected, ECC correction can be disabled, retry can be re-enabled, and the remainder of the data can be read.

After the desired track and sector is found and verified, the DATA TRANSFER sequence begins. After each successful sector transfer, the UDC increments the DESIRED SECTOR register (except after the last sector is transferred), decrements the SECTOR COUNT register, and reenters the VERIFY sequence. This process continues until



READ SECTORS OPERATION

the SECTOR COUNT register is equal to 0 (or an error occurs).

This command has four options, which are specified by Bit 1 and Bit 0 of the command word. The four options are:

BIT 1 = 1 BAD SECTOR BYPASS. If, during the read, the UDC finds a sector with the BAD SECTOR bit set (from the sector ID field on the disk), the sector be skipped, the sector count will not be decremented, and the sector number will not be changed.

BIT 1 = 0 BAD SECTOR TERMINATE. If, during a read, the UDC finds a sector with the BAD SECTOR bit set, the UDC will set the COMMAND TERMINATION CODE to 1-0, set the BAD SECTOR status bit and the DONE status bit, and terminate the command (with an interrupt, if enabled). All of the above named status bits are contained in the INTERRUPT STATUS register.

BIT 0 = 1 TRANSFER ENABLED. The UDC will transfer data from the disk to the system. The DMA REQUEST status bit (in the INTERRUPT STATUS register) will be set when the UDC requires servicing.

BIT 0 = 0 TRANSFER DISABLED. The UDC will not transfer data read from the disk, but all error checking circuitry will be enabled.

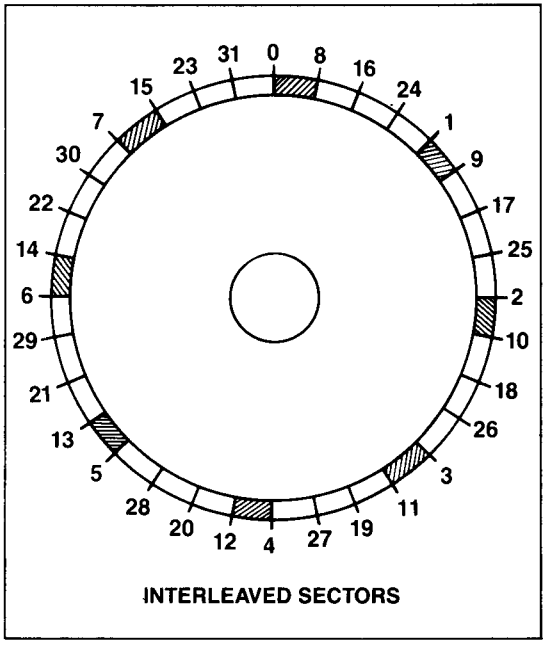
FORMAT TRACK (Hex Values 60 to 7F)

This command causes the UDC to format the current cylinder from the leading edge of one index mark to the leading edge of the next index mark. The format chosen is dependent on the Drive Select command.

During execution of the FORMAT TRACK command, the UDC will fetch all required ID field data from external memory, and write it to the disk, along with format constants supplied automatically by the UDC. This reduces the number of bytes required to format a sector to 3 or 4, depending on the format chosen.

Before the FORMAT TRACK command can be given, the system processor must:

1. Generate an ID Field table for the track in UDC memory area. This ID Field Table consists of:
   CYLINDER BYTE
   HEAD BYTE
   SECTOR NUMBER BYTE
   SECTOR SIZE/ECC SIZE BYTE (not required for ST-506 formats) repeated for each sector on the track.



INTERLEAVED SECTORS

The UDC can format a track with interleaved sectors by staggering the sector numbers. For example, to format a 32 sector track, with a sector interleave factor of 4, the system processor would set up the ID Field table sector numbers as follows:
0,8,16,24,1,9,17,25,2,10,18,26,3,11,19,
27...7,15,23,31.

(Note that when formatting in ST506 mode, only three bytes are required for each sector, while four bytes are needed for IBM or user defineable formats. Also note that sector numbers start with zero (0) on ST506 compatible format, and start with one (1) on IBM formatted floppy diskettes.)

2. Load the UDC DMA registers with the starting address of the external memory buffer containing the ID Field data just created.

3. Issue the DRIVE SELECT command, which moves the DMA registers to the CURRENT HEAD, CURRENT CYLINDER, and a TEMPORARY REGISTER. (This is necessary because the UDC will now re-use the DMA registers to hold format parameters).

   When formatting multiple cylinders, the system processor does not need to re-issue DRIVE SELECT between cylinders as the STEP IN and STEP OUT commands preserve the DMA addresses and format parameters. It is necessary, however, to update the ID Field table, described in #1, above.

4. Load the DESIRED HEAD register with the proper value.
5. Load the following values (in the format shown) into the registers indicated below:

PARAMETER	FORMAT	REGISTER
GAP 0 Size	two's complement format	DMA 7-0
GAP 1 Size	two's complement format	DMA 15-8
GAP 2 Size	two's complement format	DMA 23-16
GAP 3 Size	two's complement format	Desired Sector
Sync Size	one's complement format	Desired Cylinder
Sector Count	one's complement format	Sector Count
Sector Size Mult.	one's complement format	Retry Count

FORMAT PARAMETERS TABLE

When using ST506/PC (fixed length) hard disk format, the values for GAP 0 and GAP 1 must both be set to the same number, and loaded into the appropriate DMA register.

The Sector Size Multiple programs the UDC to format with a sector size that is a multiple of 128 data field bytes. For example, to format a track with a sector data field size of 512 bytes, then the Sector Size Multiple would be set to FB hex, which is "4" in one's complement notation.

In ST506/PC format, the sector size is fixed at 512 bytes. In IBM floppy disk format, the sector sizes allowed are 128, 256, 512, or 1024 bytes. With user defineable hard disk formats, allowed sector sizes are 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes.

6. Load the MODE register to specify the step rate, single or double density option, and CRC/ECC options.
7. Step to the desired track. For the first track, this is normally done by issuing a RESTORE DRIVE command, to return the heads to Cylinder 000, then use the STEP IN 1 or STEP OUT 1 commands to move the head to subsequent cylinders on the disk.
8. Issue the FORMAT TRACK command. All data fields on the disk will be filled with E5 hex. In double density recording (MFM) all gaps will be filled with 4E hex, while in single density (FM) all gaps will be filled with FF hex. This format is compatible for IBM specifications for floppy disks.
9. To Format additional tracks, it is only necessary to update the ID Field table (step 1) and repeat steps 7 and 8. Do NOT modify the DESIRED HEAD register when formatting additional tracks with the same head. If it is necessary to change the DESIRED HEAD register, the system processor must repeat all steps described above.

   The FORMAT TRACK command allows the user to specify several options. These options are specified by setting the appropriate low order bits in the command word. The bit mapping for these options are:

BIT 4 = 1 Write Deleted Data Mark. During the format process, the UDC will write the deleted data mark (F8 hex) for the data address field.

BIT 4 = 0 Write Normal Data Mark. During the format process, the UDC will write the normal data field address mark (FB hex).

BIT 3 = 1 Write with Reduced Current. When this bit is set, the Reduced Write Current Output will go high (active) during the Output 2 time slot.

BIT 3 = 0 Write with Normal Current. When this bit is reset, the Reduced Write Current Output wil remain low (inactive) during the Output 2 time slot.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during the format of disks. The following table specifies these values:

SECTOR SIZE FIELD BITS

DB2	DB1	DB0	IBM FD FORMAT	HD FORMAT
0	0	0	128 bytes/sector	128 bytes/sector
0	0	1	256 bytes/sector	256 bytes/sector
0	1	0	512 bytes/sector	512 bytes/sector
0	1	1	1024 bytes/sector	1024 bytes/sector
1	0	0	not used	2048 bytes/sector
1	0	1	not used	4096 bytes/sector
1	1	0	not used	8192 bytes/sector
1	1	1	not used	16,384 bytes/sector

FORMAT ECC TYPE FIELD

DB7	DB6	DB5	DB4	HD FORMAT
0	0	0	0	4 ECC bytes generated/checked
1	1	1	1	5 ECC bytes generated/checked (1)
1	1	1	0	6 ECC bytes generated/checked (1)
1	1	0	1	7 ECC bytes generated/checked (1)

note 1: WITH EXTERNAL ECC

IBM FLOPPY DISK FORMAT:

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	track number							
HEAD	side number							
SECTOR	sector number							
SECTOR SIZE								(2 bits)

HARD DISK FORMAT: ST506 PC FORMAT (512 BYTES)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	cylinder number (8 LSB's)							
HEAD	bad sector flag	cyl # bit 10	cyl # bit 9	cyl # bit 8	hd # bit 3	hd # bit 2	hd # bit 1	hd # bit 0
SECTOR	sector number							

HARD DISK FORMAT: (USER SELECTABLE SECTOR SIZE)

ID FIELD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CYLINDER	cylinder number (8 LSB's)							
HEAD	bad sector flag	cyl # bit 10	cyl # bit 9	cyl # bit 8	hd # bit 3	hd # bit 2	hd # bit 1	hd # bit 0
SECTOR	sector number							
SECTOR SIZE	ECC type			X				sector size (3 bits)

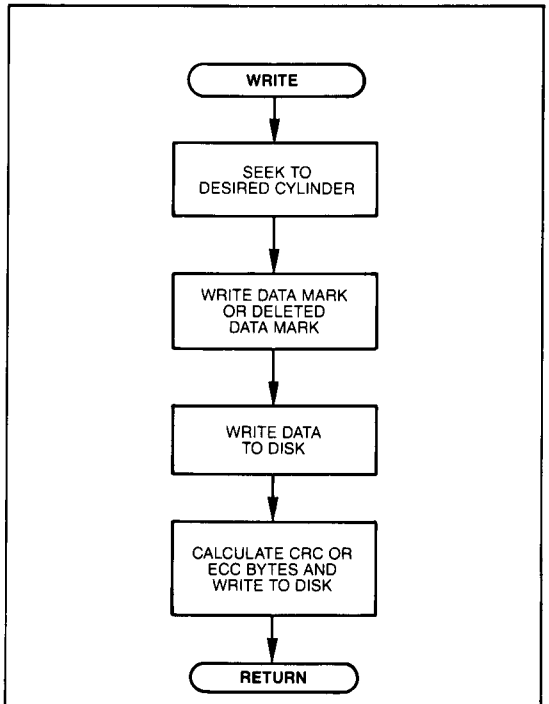
BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

WRITE SECTORS LOGICAL (Hex Values A0 thru BF, E0 thru FF)

This command will cause the UDC to write logically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

DESIRED SECTOR	DESIRED CYLINDER
DESIRED HEAD	SECTOR COUNT
DMA 7-0	DMA 15-8
DMA 23-16	MODE
RETRY COUNT	

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).



WRITE DATA OPERATION

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder and verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register.

Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next logical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 BAD SECTOR BYPASS. The UDC will bypass the sectors with the BAD SECTOR FLAG set in the ID field.

BIT 6 = 0 BAD SECTOR TERMINATION. The UDC will terminate the command when it locates a sector with the BAD SECTOR FLAG flag set in the ID field. In addition, the COMMAND TERMINATION CODE Status bits will be set to 1-0, the BAD SECTOR status bit will be set, the DONE status bit will be set, and if not masked, an interrupt will be generated.

BIT 5 = 1 WRITE LOGICAL COMMAND BIT (Always set to "1" for Write logical command).

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to disks. The table below specifies these values.

BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

NOTE: For hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

WRITE SECTORS PHYSICAL (Hex Values 80 thru 9F, C0 thru DF)

This command will cause the UDC to write physically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

DESIRED SECTOR	DESIRED CYLINDER
DESIRED HEAD	SECTOR COUNT
DMA 7-0	DMA 15-8
DMA 23-16	MODE
RETRY COUNT	

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder and

verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register. Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next physical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 BAD SECTOR BYPASS. The UDC will bypass the sectors with the BAD SECTOR FLAG set in the ID field.

BIT 6 = 0 BAD SECTOR TERMINATION. The UDC will terminate the command when it locates a sector with the BAD SECTOR FLAG flat set in the ID field. In addition, the COMMAND TERMINATION CODE Status bits will be set to 1-0, the BAD SECTOR status bit will be set, the DONE status bit will be set, and if not masked, an interrupt will be generated.

BIT 5 = 0 WRITE PHYSICAL COMMAND BIT (Reset to "0" for Write Physical Command).

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to floppy disks. The table below specifies these values.

BIT 2	BIT 1	BIT 0	Precompensation (For Floppy Disks)
0	1	0	None, enable EARLY and LATE Outputs
1	0	1	600 nsec, Minifloppy only
0	1	1	500 nsec, Minifloppy only
1	1	1	400 nsec, Minifloppy only
1	1	0	300 nsec
1	0	0	200 nsec
0	0	1	100 nsec
0	0	0	None, suppress EARLY and LATE Outputs

NOTE: for hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

TAPE BACK-UP (Hex Values = 08 to 0F)

The TAPE BACK-UP command set provides the system with the capability of transferring data to and from a tape drive in continuous blocks. TAPE BACK-UP utilizes the UDC's DMA, data conversion, error detection/correction and sector count circuitry.

Because of the mechanical and electronic differences between tape drives and disk drives, some of the register bits described earlier in this data sheet change functions when the UDC is executing the TAPE BACKUP COMMAND. In many cases, the CLK input to the UDC will also need to be changed to compensate for the slower data rate from tape drives.

TAPE BACKUP REGISTER DESCRIPTION

The following bits in the UDC's register file assume the functions listed below when executing the BACK-UP command and should be programmed accordingly.

The following tables describe the differences in register usage when the UDC is executing the TAPE BACKUP command. (Complete TAPE BACKUP register bit maps are located in rear of the data sheet.)

MODE REGISTER

Bit 2 = 1 16 byte sync detect delay enable
= 0 16 byte sync detect delay disabled

Bit 1 = 1 TAPE BACKUP Write Enable (writing)
= 0 TAPE BACKUP Write Disable (reading)

Bit 0 = 1 Tape mark enable (short block)
= 0 Tape mark disable (long block)

RETRY COUNT REGISTER

Bits 7-4 Retry should be disabled, by setting these bits to "1". (Retry Disabled)

Bits 3-0 program outputs (user controlled). Bit 3 is typically used for write enable to the tape drive.

Bits 0 and 1 are typically used for tape driven motion control as per drive manufacturer's specification.

DESIRED CYLINDER

Bits 7-4 ECC Type Field:

DB7	DB6	DB5	DB4	ECC TYPE
0	0	0	0	4 ECC bytes generated/ checked
1	1	1	1	5 ECC bytes generated/ checked
1	1	1	0	6 ECC bytes generated/ checked
1	1	0	1	7 ECC bytes generated/ checked

note: 5, 6, 7 byte ECCs are generated and checked by hardware external to the UDC.

DESIRED CYLINDER

Bit 3 Always 1

Bits 2-0 Data Block Size:

DB2	DB1	DBO	DATA BLOCK SIZE
0	0	0	128 bytes
0	0	1	256 bytes
0	1	0	512 bytes
0	1	1	1024 bytes
1	0	0	2048 bytes
1	0	1	4096 bytes
1	1	0	8192 bytes
1	1	1	16,384 bytes

Remember that the UDC internal ECC code can correct up to a 4K byte long Data Block, but that the larger the Data Block the greater the probability of a miscorrection.

Also, when executing the TAPE BACKUP command, the DRIVE SELECT command is altered slightly, as illustrated below:

DRIVE SELECT COMMAND								
Bit #	7	6	5	4	3	2	1	0
Drive Select	0	0	1	Ramp Up/Down delay enable	1	CLK divisor	1	1

DB2	CLOCK DIVISOR FOR TAPE
0	CLK is divided by 10 (similar to 8" floppy divisor).
1	CLK is divided by 20 (similar to 5.25" floppy divisor).

These bits, in conjunction with Bits 4 and 7 of the MODE register, will allow selection of both FM and MFM recording on tape, with a tape format that resembles IBM compatible floppy disk formats.

Setting the Drive Type bits to 1,0 or 1,1 will also cause the UDC to take on the following characteristics:

- –DMA mechanism transfers a byte (8 bits) and relinquishes the bus.
- –The RDGATE and WRGATE output signals have timing characteristics as shown in Figures 12A and 12B of the UDC spec.
- –The gap lengths are as illustrated in Table 1 or the UDC spec.
- –Tape format parameters will be as per Table 1 of the UDC spec.

COMMAND EXECUTION OVERVIEW

The tape backup command allows the user a convenient method of backing up either floppy or hard disks to tape. The UDC may be interfaced to either cartridge or cassette type tape drives, working in either streaming or start/stop mode.

Read and Write functions of TAPE BACKUP share a common command byte. The three LSB's of the MODE register are also used by the TAPE BACKUP command to specify user options, and to select between tape read or tape write mode.

Two kinds of blocks may be specified when reading or writing dependent on the state of the TAPE MARK ENABLE bit in the MODE register:

1. DATA BLOCK. The length of the data block (also called a long block) is equal to:

   2^n* 128 bytes where n is an integer between 0 and 7 inclusive. The desired length of the data block (2^n) is programmed into the desired cylinder register.

2. TAPE MARK. The minimum length of the tape mark (also called a short block) is 3 bytes. The maximum length of the tape mark is 257 bytes. The desired length is programmed into the sector count register.

Multiple data block transfers are accomplished by programming the 1's complement of the desired number of data blocks to be transferred into the sector count register.

The three LSB's of the MODE register function as part of the BACK-UP command word. The WRITE ENABLE bit determines whether loading the BACK-UP command into the UDC will initiate execution of a BACK-UP READ or BACK-UP WRITE sequence. The TAPE MARK ENABLE bit determines whether the UDC will write a short or long block of data on the tape and the DELAY ENABLE bit determines whether or not the RDGATE signal is stretched when it coincides with a sync mark when reading the tape. The remaining bits in the command word are as follows:

COMMAND	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BACK-UP (READING)	0	0	0	0	1	0	0	xfer enable
BACK-UP (WRITING)	0	0	0	0	1	precomp value		

BACK-UP READ

When reading a short block, only CRC is checked. When reading a long block, CRC or ECC will be checked, depending on the CRC/ECC bits in the Mode register.

Bit 0 = 1 Data transfer enabled, error checking enabled
= 0 Data transfer disabled, error checking enabled

BACK-UP WRITE

When writing, the precompensation value is derived from the CLK frequency as follows:

Bit 2	Bit 1	Bit 0	Precompensation
0	1	0	None, enable EARLY and LATE
1	0	1	6 CLK cycle periods
0	1	1	5 CLK cycle periods
1	1	1	4 CLK cycle periods
1	1	0	3 CLK cycle periods
1	0	0	2 CLK cycle periods
0	0	1	1 CLK cycle period
0	0	0	None, suppress EARLY and LATE

PRECOMPENSATION SELECT FOR BACK-UP COMMAND

TAPE BACKUP SYSTEM CONFIGURATION NOTES

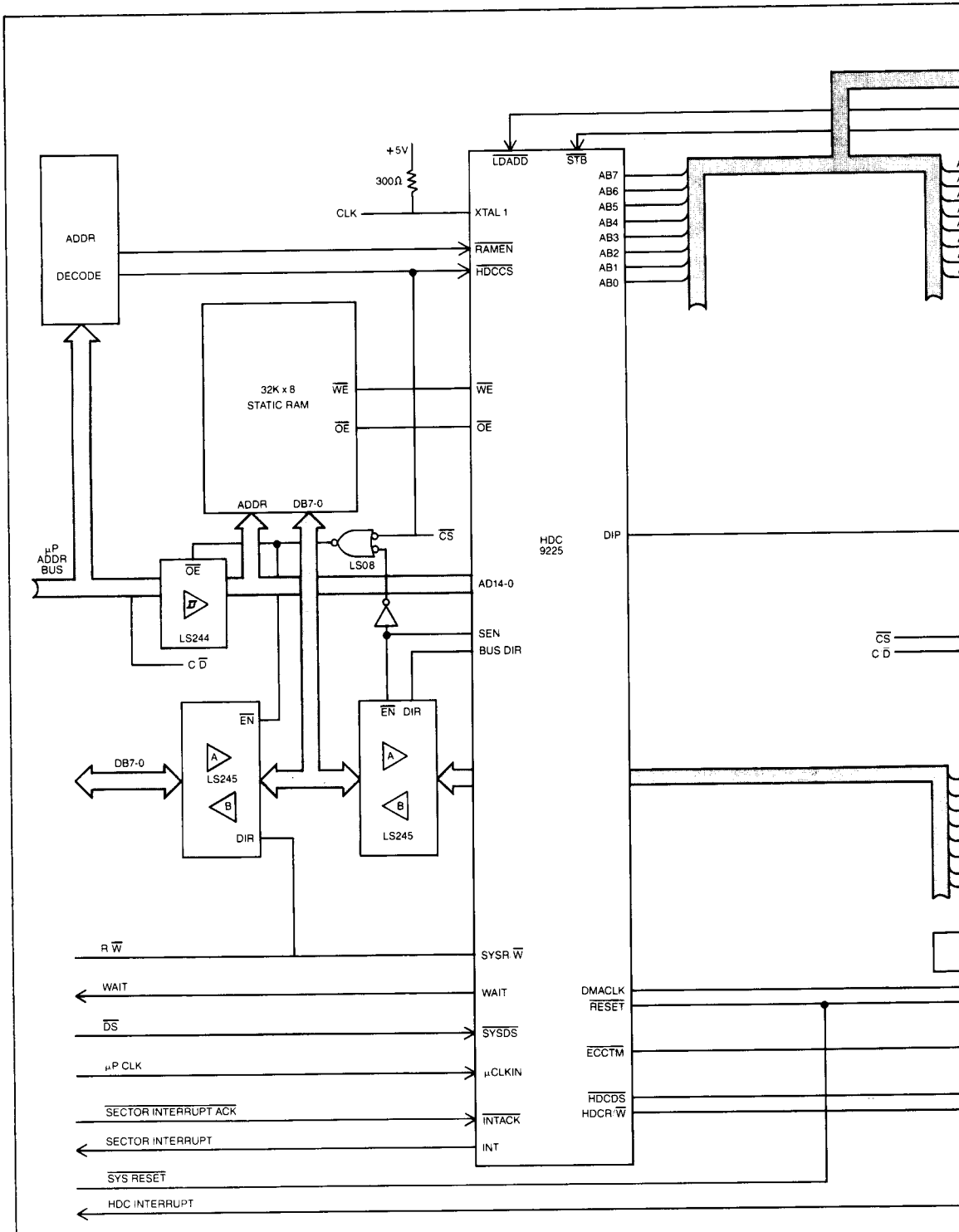
(A schematic showing a typical system implementation using the TAPE BACKUP feature is contained in Schematic Diagram 2.)

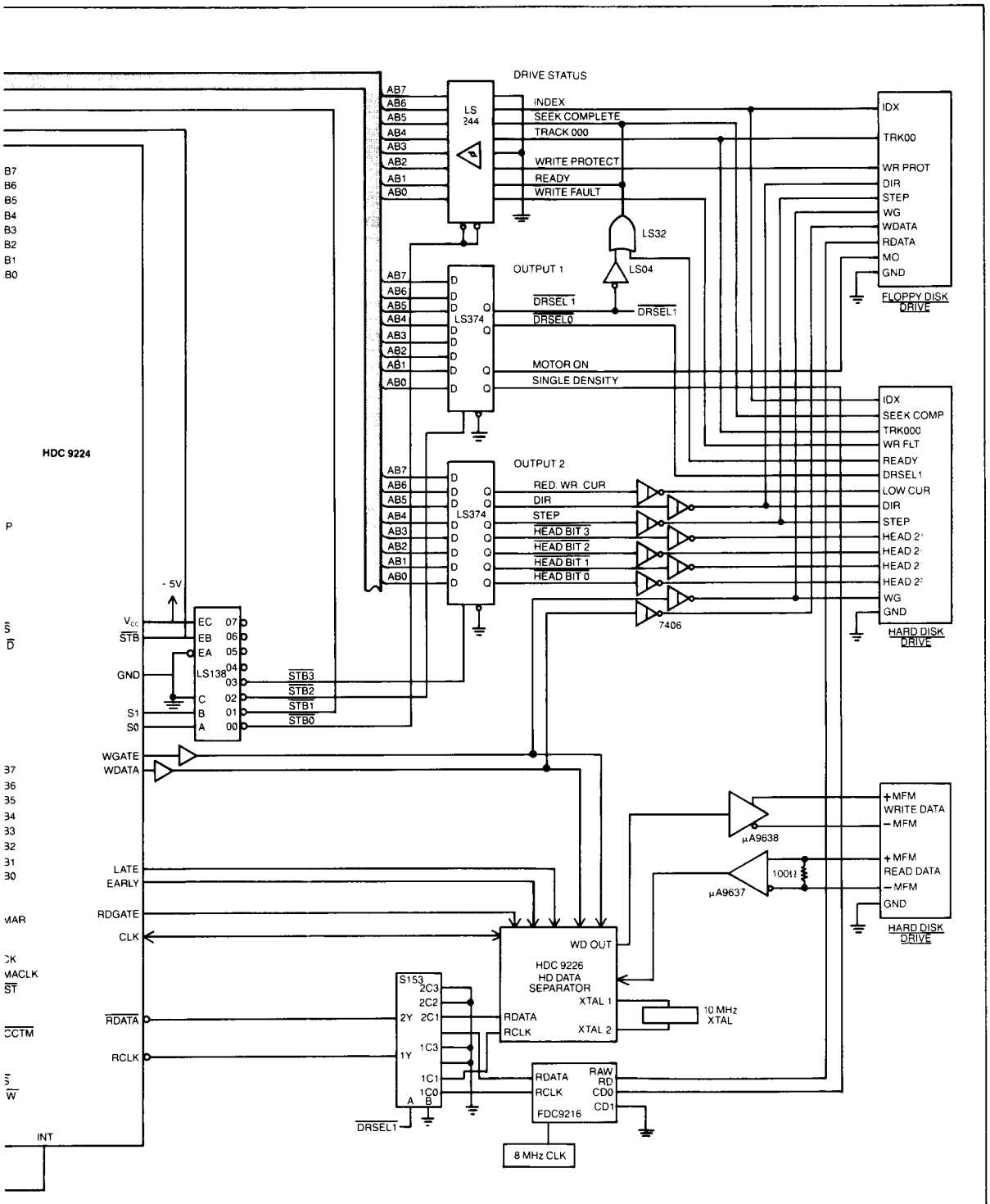
1. Proper operation of the TAPE BACKUP command requires that the tape drive be addressed as DRIVE #3 by the UDC.
2. During the UDC's OUTPUT 2 period external circuitry must enable a separate latch to receive the user defined IO bits and tape track number bits. This latch should use the DRIVE SELECT 3 signal (output during the OUTPUT 2 period) so that the contents of the latch may only be changed when the tape drive is selected.

   Four additional drive control signals may be loaded into the four LSB's of the RETRY COUNT register. These additional outputs are latched externally during OUTPUT 1 times for use by the tape drive. These outputs would normally be used to control tape drive Write Enable logic (bit 3) and tape motion (bits 0 and 1), and tape motor on and off (bit 2).

3. It is important to consider the time required for a tape drive to come up to operating speed when using the TAPE BACKUP command. Also, to insure adequate spacing between tape blocks, a delay is frequently required before stopping tape motion. The UDC has a programmable Ramp Up and Ramp Down timer to allow for easier implementation. The desired delay is programmed into the DATA/DELAY register before issuing the DRIVE SELECT "3" command.

CLOCK DIVISOR BIT	DENSITY BIT MODE REGISTER BIT 4	TIME IN SECONDS PER DELAY REGISTER COUNT
1	1 (Single)	1 CLK Cycle * 80000
1	0 (Double)	1 CLK Cycle * 40000
0	1 (Single)	1 CLK Cycle * 40000
0	0 (Double)	1 CLK Cycle * 20000


+5V
300Ω
CLK
XTAL 1
LDADD
STB
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
ADDR
DECODE
RAMEN
HDCCS
32K x 8
STATIC RAM
WE
OE
ADDR
DB7-0
CS
HDC
9225
DIP
μP
ADDR
BUS
LS08
AD14-0
LS244
SEN
BUS DIR
C D
EN
DIR
DB7-0
LS245
DIR
R W
SYSR W
WAIT
DS
SYSDS
μP CLK
μCLKIN
SECTOR INTERRUPT ACK
INTACK
SECTOR INTERRUPT
INT
SYS RESET
HDC INTERRUPT
DMACLK
RESET
ECCTM
HDCDS
HDCR W


DRIVE STATUS
LS 244
INDEX
SEEK COMPLETE
TRACK 000
WRITE PROTECT
READY
WRITE FAULT
LS32
LS04
OUTPUT 1
LS374
DRSEL 1
DRSEL0
MOTOR ON
SINGLE DENSITY
OUTPUT 2
RED. WR. CUR
DIR
STEP
HEAD BIT 3
HEAD BIT 2
HEAD BIT 1
HEAD BIT 0
7406
IDX
TRK00
WR PROT
DIR
STEP
WG
WDATA
RDATA
MO
GND
FLOPPY DISK DRIVE
SEEK COMP
TRK000
WR FLT
READY
DRSEL1
LOW CUR
HEAD 2
HEAD 2
HEAD 2
HEAD 2
HARD DISK DRIVE
HDC 9224
- 5V
LS138
STB3
STB2
STB1
STB0
WGATE
WDATA
LATE
EARLY
RDGATE
CLK
RDATA
RCLK
INT
WD OUT
HDC 9226
HD DATA SEPARATOR
XTAL 1
XTAL 2
10 MHz XTAL
RDATA
RCLK
S153
DRSEL1
RAW RD
CD0
CD1
FDC9216
8 MHz CLK
µA9638
µA9637
1001Ω
+MFM WRITE DATA
−MFM
+MFM READ DATA
−MFM
GND
HARD DISK DRIVE

The UDC will issue a normal interrupt (with the command termination code set to 0-0) when the RAMP UP or RAMP DOWN timer has expired.

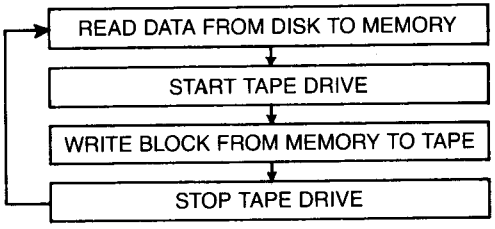
4. BACK-UP WRITE. The user will first request the UDC to perform a disk READ TRACK command, with the TRANSFER ENABLE bit in the command word reset. This will cause the UDC to transfer only the ID field information to memory.

   The TAPE BACKUP command will then be issued causing the UDC to write this ID information to the tape as a tape mark (typically 96 bytes for a drive formatted with a 3 byte/sector ID field or 128 bytes for a drive formatted with a four byte/sector ID field. The data fields should then be transferred to the tape in a similar manner.

   The UDC may be used with either "Streaming" or "Start/Stop" type tape drives. This is illustrated by the following examples:

   A. START/STOP TAPE DRIVE:

   typically transfers ½ or 1 disk track at a time as illustrated by the following flow chart:



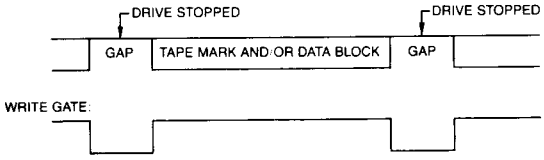
   When controlling a start/stop tape drive, the UDC will write the data "block by block". The system will issue a Drive Select command to the UDC with the Tape Motion, Motor On and Write Enable bits set to start and write data to the tape.

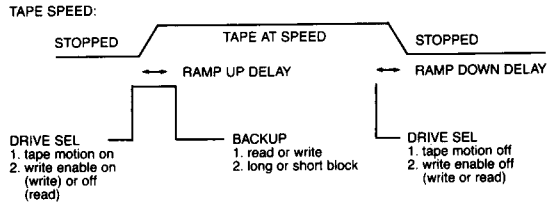
   The UDC will interrupt the system after the completion of the Ramp Up Delay indicating that the tape drive is up to speed. This interrupt is distinguished by the Command Termination Code of 0-0 (normal completion of command).

   The System then outputs the Write command (for a long or short block) and waits for the command termination interrupt. The UDC will write the Sync mark and tape mark or data block on the tape.

   When the System receives the interrupt indicating completion of the Write command, it will issue another drive select command with the Motor On and Write Enable bits set to stop the drive. The UDC will interrupt the system after completion of the Ramp Down Delay indicating that the tape has stopped moving.

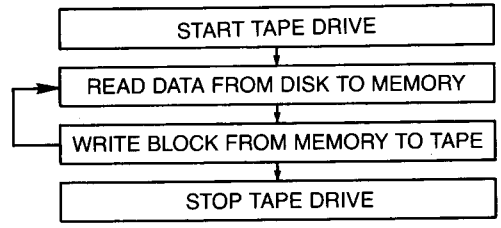
   The UDC will turn the Write Gate signal on when it is writing data and off when it is not, without regard to the tape motion. The Write Gate signal is used to generate "gaps" on the tape between the data blocks. This is done by externally forcing the two Data outputs with the Write Gate signal such that the Data + signal is high and the Data − signal is low when the UDC is not writing data to the tape (Write Gate is off):





   B. STREAMING TAPE DRIVE:

   typically transfers 1 sector at a time as illustrated by the following flow chart:



   Control of a streaming tape drive is similar to that of a start/stop drive. The tape is started at the beginning of the data transfer and stopped after the last block is written to the tape. The tape is not stopped in between blocks. The UDC will however turn the Write Gate signal on when it is writing data and off when it is not so that gaps will be written (with external hardware) on the tape between the data blocks.

5. BACK-UP READ. The data is read from the tape (in either start/stop or streamer mode) and buffered in memory. The disk track is then reconstructed from the data.

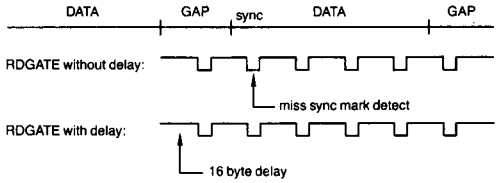
   The start/stop drive typically has a track (or half a track) of disk data stored as a block. It is therefore expedient to read in the data "block by block". When reading data from a streamer drive use can be made of the SECTOR COUNT register and a track's worth of data blocks may be read from the tape before generating the track on the disk.

   Tape motion control is similar to that described above except that the Write Enable Bit is off to inhibit writing to the tape. The UDC reads the tape until it detects a sync mark. After detecting a sync mark the UDC will transfer the data found on the tape to memory.

6. The search count is used when reading the tape. It specifies a maximum number of blocks of 128 bytes between adjacent data blocks. If the search count expires before sync is detected, the command is terminated.

   For example, if a search count of two is specified by loading the Desired Sector register with FD (hex), the UDC will search for 256 byte times before terminating the command. This will prevent the UDC from accidentally skipping a block. The search count is typically about the size of one block length. In the following figure, TM1 and TM2 are two tape marks and DB1, DB2, DB3 etc. are their associated Data Blocks:

7. 16 BYTE DELAY. Provision is made to shift the RDGATE pulse in the event that it coincides with the data block sync mark. If a tape cannot be read (sync is never detected) the tape can be re-read with the 16 byte delay enabled.



8. The DRIVE STATUS bits may be used by the tape drive if they are enabled (on the drive) by DRIVE SELECT 3. The ready change interrupt is especially handy for detecting start of tape (SOT) and end of tape (EOT) as a UDC command can be terminated by a change in state of the READY input.
9. The DATA FORMAT is as follows:

PRE	TMSYNC	TAPE MARK	POST GAP	PRE	DBSYNC	DATA BLOCK	POST GAP

The Tape Mark sync mark (TMSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FE (Hex). The Data Block sync mark (DBSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FB (Hex). A1 (Hex) is encoded with the standard missing clock pattern.

The sync mark is preceeded by a "preamble" consisting of bytes of 00 as per figure 2 of the UDC spec (this is required to synchronize the data separator when reading the tape). The Tape Mark and Data Block (including CRC or ECC bytes) are followed by a "postamble" consisting of one byte of 00.

Note that the postamble is not included in the Floppy Disk formats. The GAP sizes are dependent on the type of drive (start/stop or streamer) and the specific mechanical tape drive specifications.

10. Use can be made of the Sector Count register when doing a "file" (versus a "mirror image") backup on a start/stop tape drive. Instead of transferring the entire disk track to the tape in one long block, the data is moved file by file.

    If, for example, it is desired to back up a file consisting of five 256 byte long Hard Disk sectors, a 2048 byte long Data Block would have to be used for an image backup (the Data Block size is specified as $2^n * 128$ restricting blocks to 128, 256, 512 etc.). This would result in a lot of wasted space on the tape.

    If file backup is used and the Sector Count is set to five, 256 byte long Data Blocks can be used. Gaps will be generated on the tape corresponding to the time required to get the data from the disk drive (corresponding to DMA delays and the disk interleave factor).

    The tape will not be stopped until the entire file is transferred. When using sector count, the UDC internal programming will create inter-block gaps of about 30 to 32 bytes on the tape in both single (FM) and double (MFM) density modes.

SYSTEM CONFIGURATION NOTES

A simplified UDC schematic is shown in Schematic 1. The following notes may be helpful in implementation of the UDC.

1. In systems using a private memory area, it is important to know when the buffer needs servicing from the host processor. A second interrupt signal (INT2) signals the processor that servicing is needed. INT2 is generated by externally ANDING the ECCTM signal with STB1 signal. (The STB1 signal is active when the UDC is outputing the DMA address data, and occurs when STB is active (low), S0 is active (high) and S1 is inactive (low)).

   This "interrupt" occurs only when the UDC needs the system processor to either read from or write to the buffer memory. When reading from the disk, the system processor should empty the memory buffer each time this signal becomes active. (If an ECC error is detected, and error correction is enabled, this signal will not become active until the UDC has attempted to correct the error.)

   When writing data to the disk, the system processor must fill the buffer each time this signal becomes active.
2. The DIP (DMA in Progress) signal is used to isolate the buffer memory from the main system memory. If 74LS244 and 74LS245 address buffers are used in the memory addressing circuits, then this signal should be used to enable or disable the address buffers, as required. This eliminates the possibility of memory contention problems.
3. Write precompensation (for floppy disks) is handled internally by the UDC. For hard disks, the LATE and EARLY signals are connected to a multiplexer which, in turn is connected to a 24 ns delay line. The EARLY and LATE signals will toggle in response to the data pattern being written. This will allow the data being written to the shifted ± 12 ns from the nominal 12 ns delay specified by hard disk manufacturers.
4. The interface to the hard disk drive data inputs and outputs requires RS-422 data tranceivers. Other disk drive interface circuits (including floppy disk data inputs and outputs) may be 74LS series devices.
5. Since the UDC uses its Aux Bus for multiple functions, the system designer must be able to determine which function is occuring on the Aux Bus at any given time. The S0 and S1 signals, when combined with STB signal are decoded (using a 74LS138 or equivalent) to provide STB0-3 signals.

   These generated signals and their respective functions are:

STB0	Drive Status Input Time Slot
STB1	External DMA Address Counters Time Slot
STB2	Output 1 Time Slot
STB3	Output 2 Time Slot

6. The clocks required by the UDC are not TTL-level compatible. Pullup resistors (typically 390 ohms) should be used with Schottky drivers to insure that the clock signals reach the proper input (high) level, with acceptable rise and fall times.
7. The UDC features a built-in DMA controller that requires connection to external counters. These counters are configured so that they are incremented after each byte is transferred. (The UDC's internal DMA circuits transfer the starting memory address for each read or write operation.) 74LS161 Counters are typically used in this area.
8. The DMACLK input should be tied to the master system clock, through a bus buffer. It is important to remember that three DMACLK periods are required for each DMA transfer.
9. The system design may be simplified, and costs reduced, by using the FDC 9216B Floppy Disk Data Separator, to separate raw data from the floppy disk drive into RDATA and RCLK.

ERROR CHECKING AND CORRECTION CIRCUIT (ECC) OPERATING PRINCIPLES

The UDC will automatically detect and correct errors in the data read from the disk. Error checking may be done using industry standard CRC or ECC encoding. Error correction may be done using either internal or external ECC encoding. This section will explain ECC operation, as implemented on the UDC.

The UDC contains two 16-bit registers used by the CRC/ECC circuits. CRC logic uses only one of these registers, while the logic for ECC uses both registers, implementing a full 32-bit algorithm.

These registers may be preset to either one or zero, using the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION register. (This allows compatibility with existing disk controllers and external ECC chips.) Both ECC and CRC are calculated beginning with the sync mark of the address (CRC) or data (ECC) field.

CRC/ECC GENERATION

The UDC uses the following industry standard polynomials in computing the CRC and ECC check bytes:

CRC: $x^{16} + x^{12} + x^5 + 1$

ECC: $x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$

As the UDC writes data to the disk drive, it first passes this data thru the CRC (and, if enabled, ECC) registers. After all data has been written, the remaining two (CRC) or four (ECC) bytes remaining in these registers are written to the appropriate address or data field.

CRC/ECC CHECKING

When CRC or ECC checking is initiated, the internal CRC/ECC registers are set to either zero or one, as required by the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION REGISTER. Data read from the disk is simultaneously shifted thru the CRC/ECC registers, and transferred to external memory.

After the CRC or ECC check bytes have been shifted thru the CRC/ECC registers, the remainder in these registers should be zero, else an error has occurred in the address or data block.

If CRC or ECC (without correction) is enabled, automatic retry (if enabled) or command termination will occur. If internal ECC with automatic correction is enabled, the correction algorithm will be executed. If the internal ECC algorithm is unable to correct the error (in one attempt), then automatic retry (if enabled) or command termination will occur.

ECC CORRECTION

Error Correction consists of three distinct parts:

1. The CRC/ECC registers are normalized by shifting zeros thru the register. This sets up a data block which is 42,987 bits long, which corresponds to the "natural message length" of the generation polynomial. The actual number of zeros shifted through the registers depends on the difference between the natural message length of the generator polynomial and the actual length of the data block being checked. The longest data block that can be corrected (using the internal ECC algorithm) is 4K bytes.
2. The data input to the CRC/ECC registers is then disabled and the DMA counters are re-initialized to the starting address for this data block. The contents of the CRC/ECC registers are then "ring-shifted" until 21 consecutive zeros are detected. The remaining bits in the CRC/ECC registers compose the error syndrome. As the CRC/ECC registers are shifted, the UDC generates $\overline{DS}$ signals, causing the external DMA counters to be incremented. When the 21 consecutive zeros are detected, the DMA counters are pointing to the corrupt data.

   If the error syndrome is not found within the data block the error is judged to be uncorrectable and the correction algorithm is terminated. (The data block is the length of the data field in the sector and the 4 ECC bytes. A format with a sector size of 256 bytes would have a data block size of 260 bytes.)
3. When the error syndrome is detected, the UDC will enable its $\overline{ECCTM}$ output, read the next byte from memory, exclusive-or it with the first byte of the three byte error syndrome, disable the $\overline{ECCTM}$ output and write the corrected byte back to memory. The correction process is then repeated for the next two bytes in memory.

   When using internal ECC (with correction enabled), the $\overline{ECCTM}$ output is used by the external DMA counters to inhibit the counters from incrementing their addresses when correcting the erroneous bytes. When using external ECC, the $\overline{ECCTM}$ output goes active (low) when the UDC is requesting the ECC Check Bytes from the external ECC chip prior to writing them to the disk.

   After a correction is completed, the UDC will then attempt to read the next sector on the disk (if the SECTOR COUNT register is still greater than zero). Anytime ECC correction has been attempted, (even if unsuccessful), the CORRECTION ATTEMPTED bit in the CHIP STATUS register will be set.

The maximum time required for one ECC Correction Cycle (using the internal algorithm) is:

1) $\frac{\text{(Natural Message Length [Bits])}}{8} + 4 =$ ECC Cycle Time (in Byte times)

2) Maximum ECC Time = ECC Cycle Time + 30 byte times

Since the internal algorithm has a natural message length of 42,987 bits the ECC Cycle time is 5,377 byte times. Since a period of about 30 byte times must be allowed for the read-modify-write operations, the Maximum ECC Time equals 5,407 byte times.

One byte time equals the amount of time required to read one byte for the type of drive selected. For Hard Disks, this is about 1 microsecond. This equates to approximately 1 revolution (maximum) for either 8" floppy disk (running in double density) or 5.25" hard disk.

During the entire operation, the RDGATE signal is kept active.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0 to +70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec.) ..... +325 C
Positive Voltage on any Pin, with respect to ground ..... +8 V
Negative Voltage on any Pin, with respect to ground ..... −0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

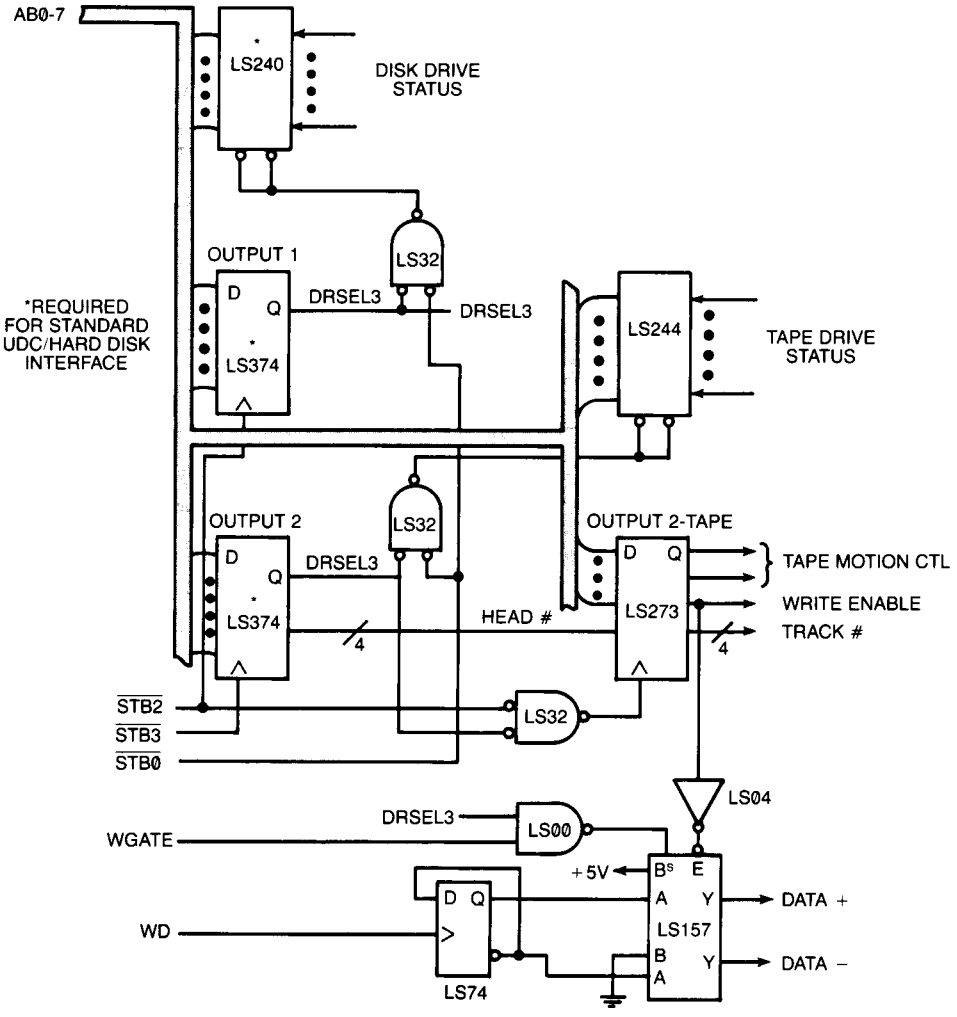
DC ELECTRICAL CHARACTERISTICS Ta = 0 C to +70 C, Vcc = 5.0V ±5%

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
Input Voltage						
V_{IL} Low			0.8	V		
V_{IH1} High	2.0			V	all inputs except CLK and DMACLK	
V_{IH2} High	4.2			V	CLK and DMACLK input	
Output Voltage						
V_{OL1} Low			0.4	V	all outputs except WDATA, Early and Late. (Drive 1 TTL load into 50 pf)	I_{OL1} = 1.6 mA
V_{OH1} High	2.4			V		I_{OH1} = 40μA
V_{OL2} Low			0.5	V	WDATA, EARLY and LATE outputs. (Will drive 1 Schottky load into 15 pf.)	I_{OL2} = 2mA
V_{OH2} High	2.7			V		I_{OH2} = 50μA
V_{OL3} Low			0.4	V	DMAR and INT	I_{OL3} = 0.4 mA
V_{OH3} High	2.4			V	DMAR and INT	I_{OH3} = 20μA
Input Leakage Current					0.4V to 3.5V	
I_L			±10	uA		
I_{LC} (Clock)			−600	μA	0V	
Input Capacitance						
C_{IN}			25	pf		
Power Supply Current						
Icc			200	ma		

AC ELECTRICAL CHARACTERISTICS Ta = 0 C to +70 C, Vcc = 5.0V ±5%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
PROCESSOR WRITE CYCLE						
C/$\overline{D}$, R/$\overline{W}$, $\overline{CS}$ Setup time to DS↓	T_{DSB}	110			ns	FIGURE 3
C/$\overline{D}$, R/$\overline{W}$, $\overline{CS}$ Hold time to DS↑	T_{DSB}	0			ns	
$\overline{DS}$ Pulse Width	T_{DSL}	150			ns	
$\overline{DS}$ Pulse High Time	T_{DSH}	850			ns	
Data Bus In Setup time to $\overline{DS}$↑	T_{DIB}	100			ns	
Data Bus In Hold time to $\overline{DS}$↑	T_{DIA}	0			ns	
PROCESSOR READ CYCLE						
Data Access time from $\overline{DS}$↓	T_{DOB}	75			ns	FIGURE 3
Data Hold time from $\overline{DS}$↑	T_{DOA}	10			ns	
UDC TO MEMORY TIMING (BUS MASTER)						
(based on 10 Mhz DMACLK Input)						
Write Setup time to $\overline{DS}$↓	T_{WB}	110			ns	FIGURE 4
Write Data Strobe Width	T_{WDS}	180			ns	
Write Hold time from $\overline{DS}$↑	T_{WA}	110			ns	
Data Strobe Falling Edge	T_{DSF}			15	ns	
Data Strobe Rising Edge	T_{DSR}			20	ns	
Write Data Valid before $\overline{DS}$↑	T_{WDB}			90	ns	
Write Data Hold time after $\overline{DS}$↑	T_{WDA}	10			ns	
Memory Access Time	T_W		200		ns	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
Read Setup time to $\overline{DS}\downarrow$	T_{RB}	110			ns	FIGURE 4
Read Hold time after $\overline{DS}\uparrow$	T_{RA}	110			ns	
Read Data Strobe Pulse Width	T_{RDS}	180			ns	
Read Data Setup time to $\overline{DS}\uparrow$	T_{RDB}	50			ns	
Read Data Hold time from $\overline{DS}\uparrow$	T_{RDA}	0			ns	
DMACLK$\uparrow$ to $\overline{DS}\downarrow$	T_{DDD}			100	ns	
DMACLK$\uparrow$ to $\overline{DS}\uparrow$	T_{DDA}			100	ns	
S0, S1, AND $\overline{STB}$ TIMING						
$\overline{STB}$ Width	T_{SW}	800			ns	FIGURE 7
S0, S1 Hold time after $\overline{STB}\uparrow$	T_{SD}	100			ns	
Data In Setup time to $\overline{STB}\uparrow$	T_{DIS}	700			ns	
Data In Hold time after $\overline{STB}\uparrow$	T_{DIH}	0			ns	
S0, S1 Setup time to $\overline{STB}\downarrow$	T_{SST1}	100			ns	
Aux Bus Setup time to $\overline{STB}\downarrow$	T_{SST2}	100			ns	
Aux Bus Hold time after $\overline{STB}\uparrow$	T_{SST3}			100	ns	
INPUT CLOCK TIMING (10 MHz Input)						
Clock Rise Time	T_{RT}			10	ns	FIGURE 2
Clock Fall Time	T_{RF}			10	ns	
Clock Cycle High Time	T_{CH}	40			ns	
Clock Cycle Low Time	T_{CL}	40			ns	
Clock Cycle Time	T_{CYC}	95	100	105	ns	
PRECOMPENSATION TIMING						
Early, Late Setup time (Before WDATA$\uparrow$)	T_{PB}	0			ns	FIGURE 9
Early, Late Hold Time (after WDATA$\downarrow$)	T_{PB}	50			ns	
FLOPPY INPUT DATA TIMING						
Window Setup time to RDCLK	T_{FRB}	50			ns	FIGURE 10
Window Hold time from $\overline{RDDATA}\uparrow$	T_{FRA}	50			ns	
HARD DISK INPUT DATA TIMING						
Data Setup time to RCLK$\downarrow$	T_{HRB}	60			ns	FIGURE 10
Data Hold time after RCLK$\downarrow$	T_{HRA}	10			ns	
Clock Setup time to RCLK$\uparrow$	T_{HCB}	60			ns	
Clock Hold time from RCLK$\uparrow$	T_{HCA}	10			ns	
ECCTIM TIMING						
$\overline{ECCTM}$ Setup to $\overline{DS}\downarrow$	T_{EDS}	50				FIGURE 10
$\overline{ECCTM}$ Hold after $\overline{DS}\uparrow$	T_{EDH}	100			ns	
RESET TIMING						
$\overline{RST}$ Pulse Width		1			µs	



SCHEMATIC 2: UDC/TAPE DRIVE INTERFACE CIRCUIT

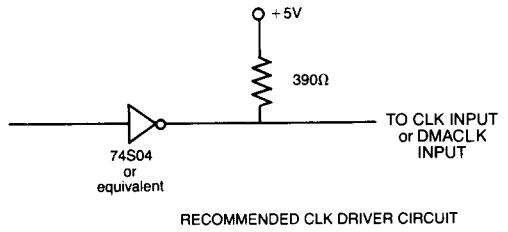


FIGURE 1: RECOMMENDED CLK/DMACLK INPUT

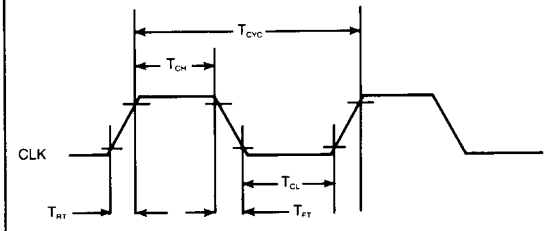


FIGURE 2: INPUT CLOCK TIMING (10MHz)

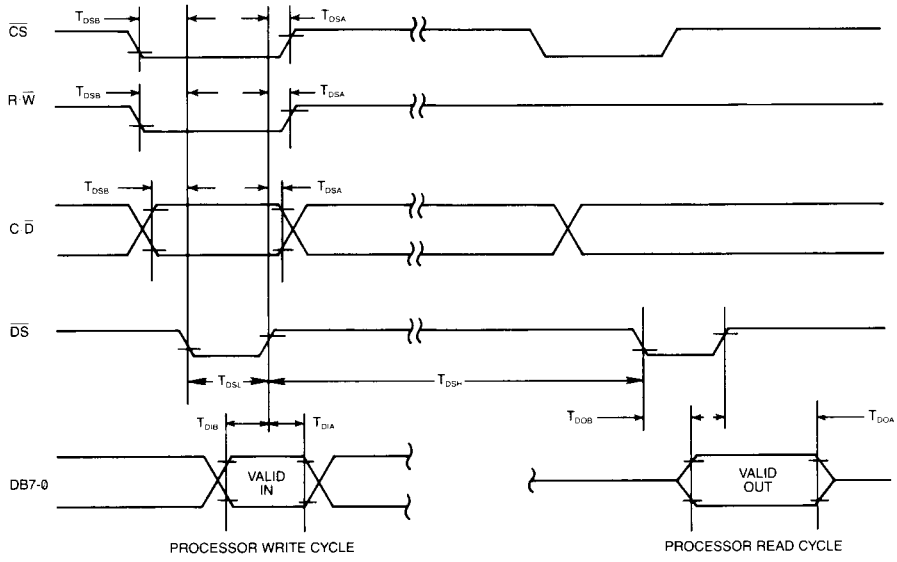


FIGURE 3: SYSTEM PROCESSOR TO UDC TIMING

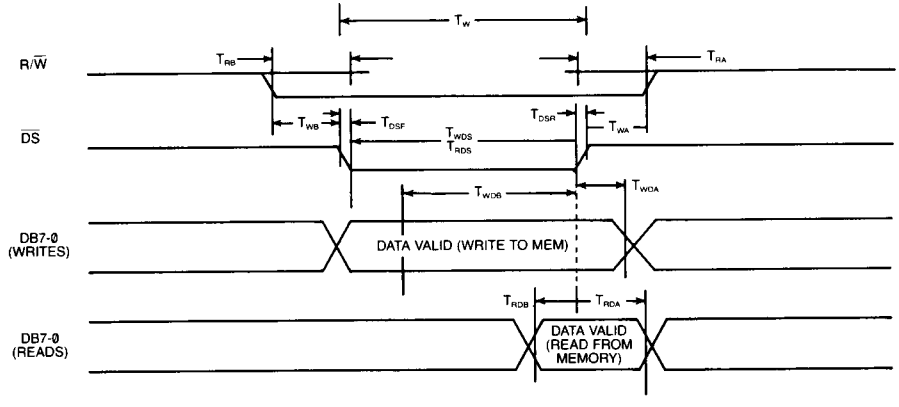


FIGURE 4: UDC TO MEMORY TIMING (BUS MASTER)

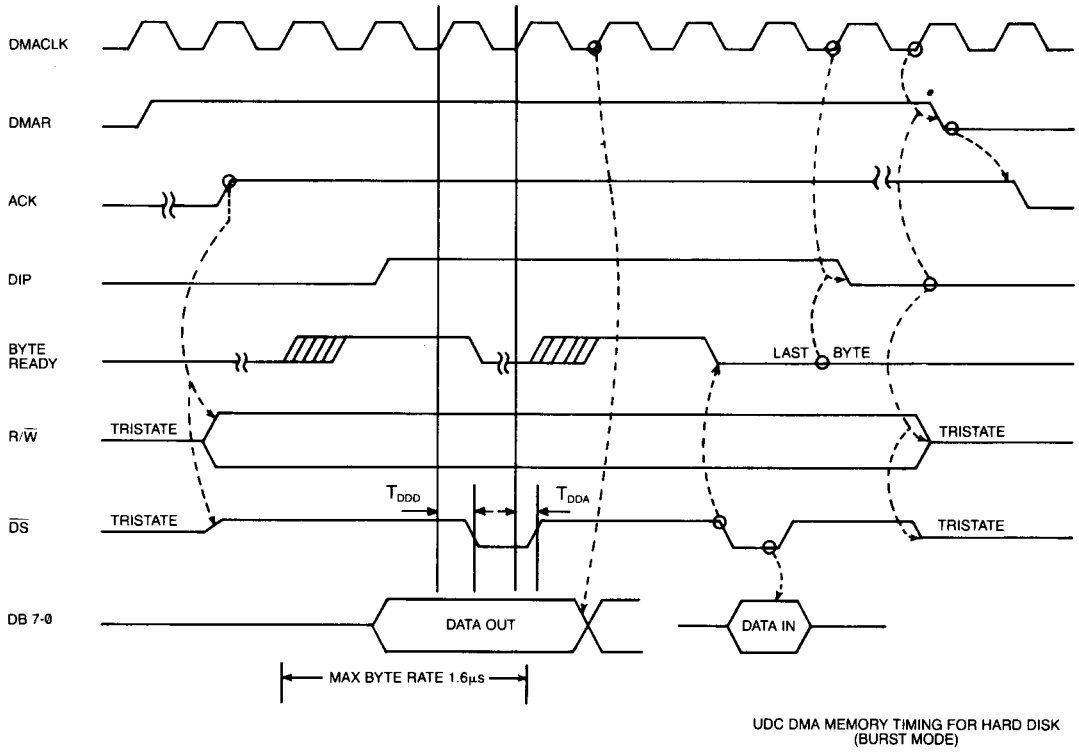


FIGURE 5: UDC DMA MEMORY TIMING FOR HARD DISK (BURST MODE)

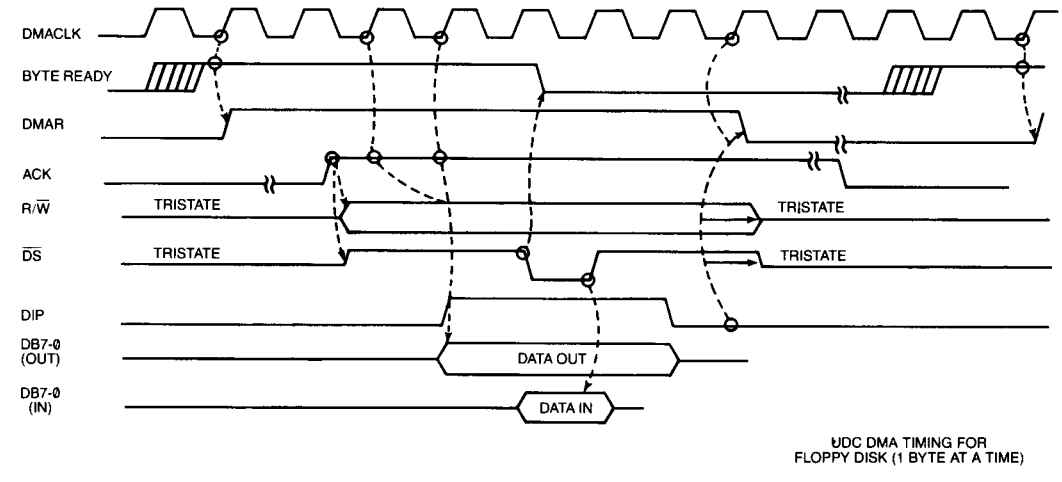


FIGURE 6: UDC DMA TIMING FOR FLOPPY DISK (1 BYTE AT A TIME)

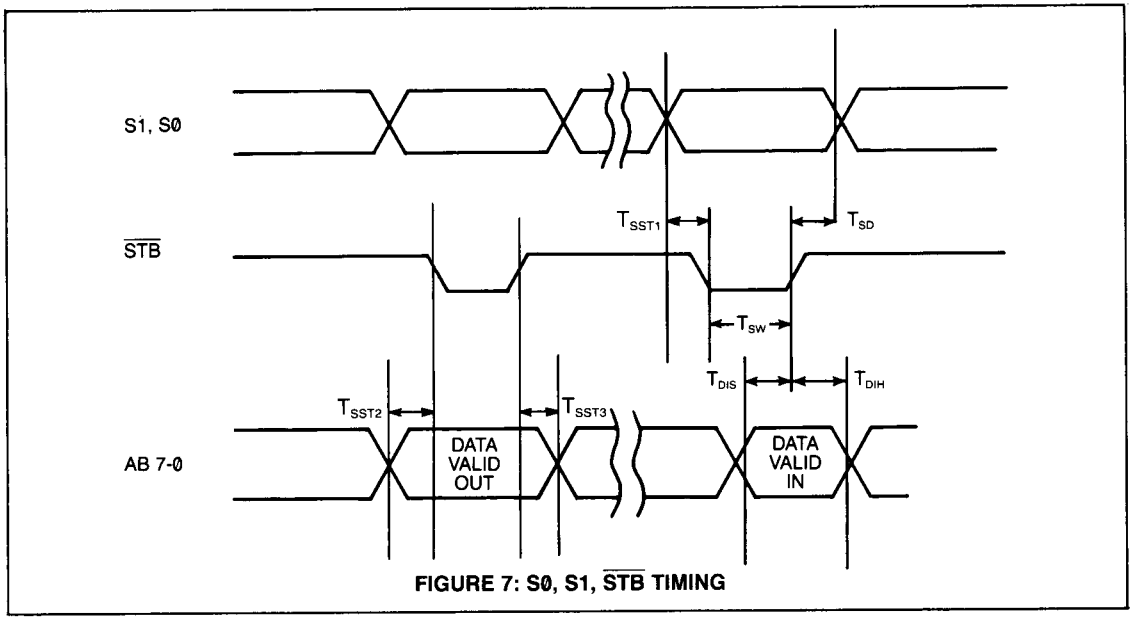


FIGURE 7: SØ, S1, STB TIMING

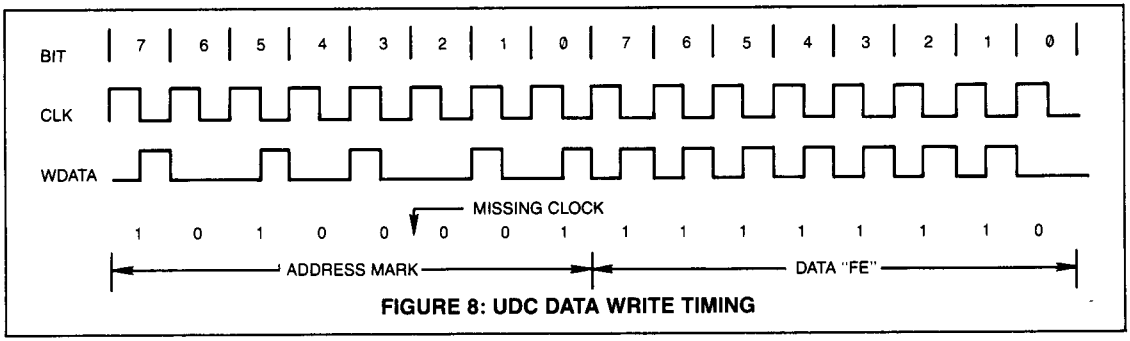
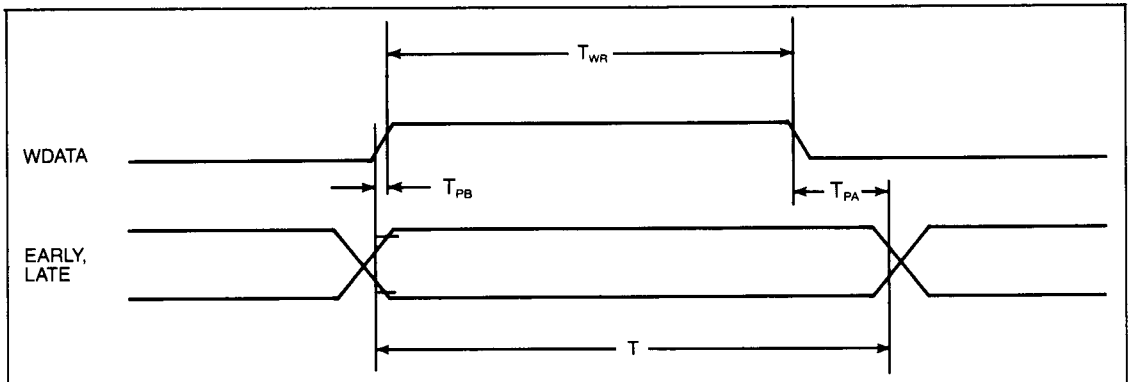
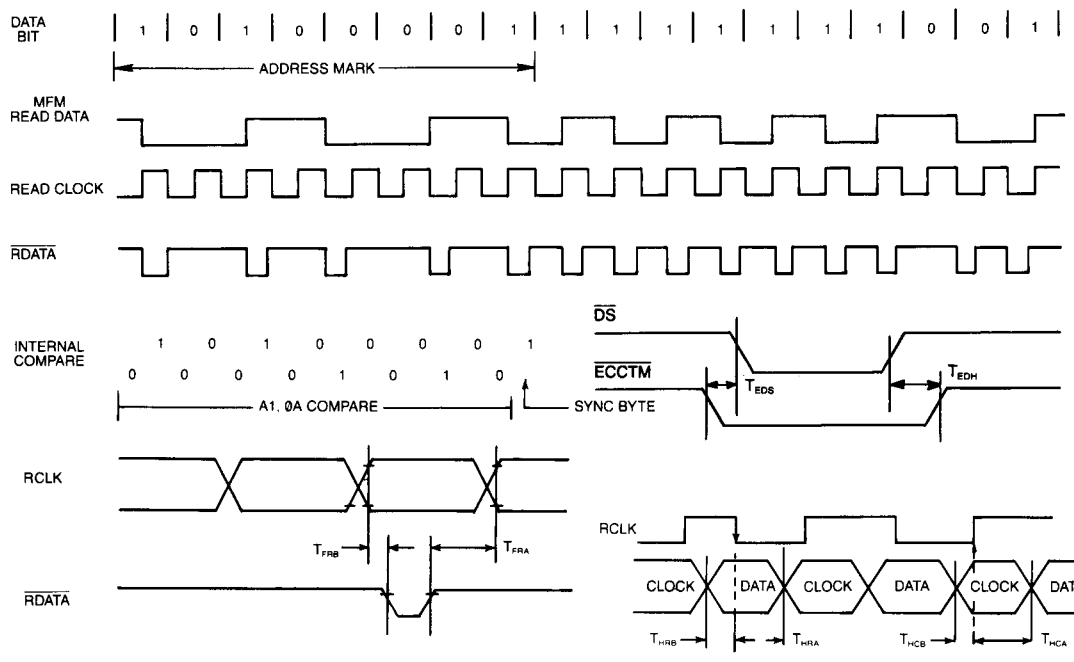


FIGURE 8: UDC DATA WRITE TIMING



DRIVE TYPE	T (typ)	T_{WR} (typ)
HARD DISK	200 NS	100 NS
8" MFM FLOPPY	2 µs	300 NS
8" FM FLOPPY	—	300 NS
5¼" MFM FLOPPY	4µs	300 NS
5¼" FM FLOPPY	—	300 NS

FIGURE 9: PRECOMPENSATION TIMING



FLOPPY INPUT DATA TIMING (HARD DISK BIT = Ø)

HARD DISK INPUT DATA TIMING (HARD DISK BIT = 1)

FIGURE 10

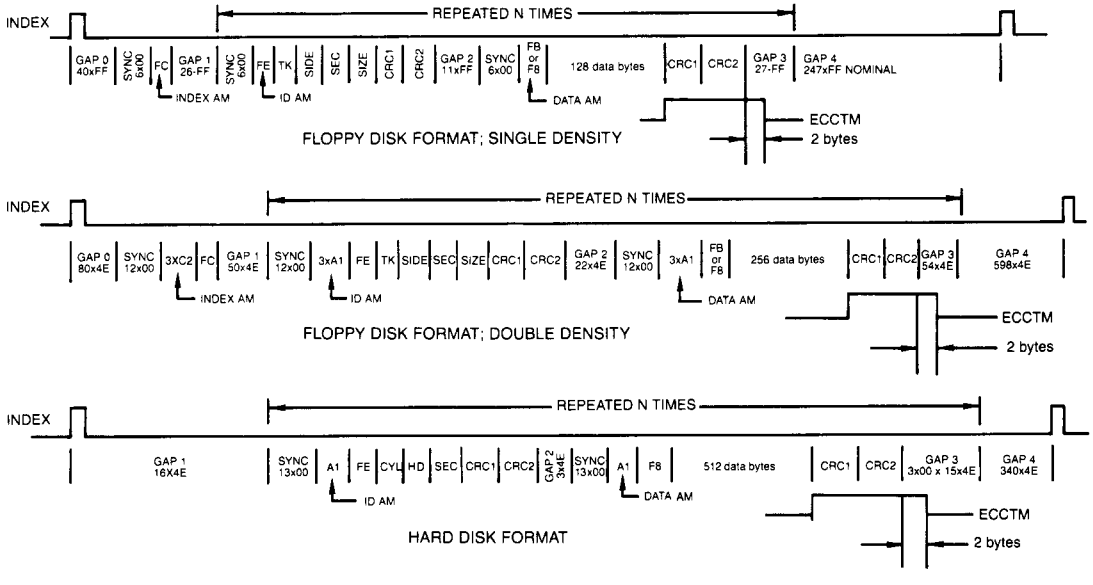


FIGURE 11: DISK FORMATS

SECTION VII

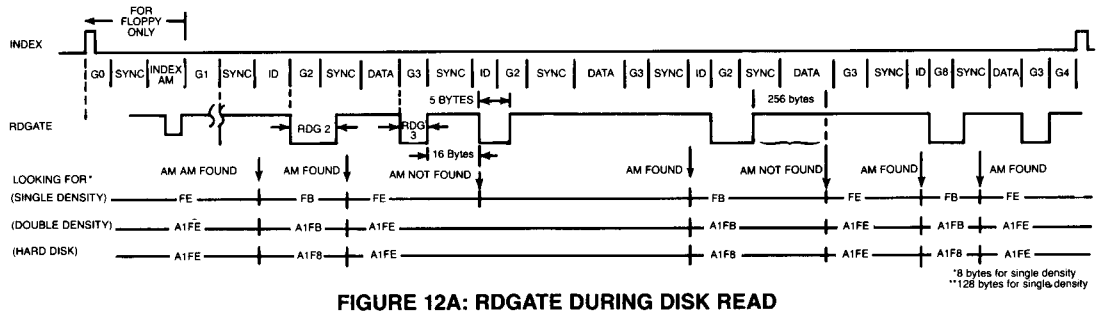


FIGURE 12A: RDGATE DURING DISK READ

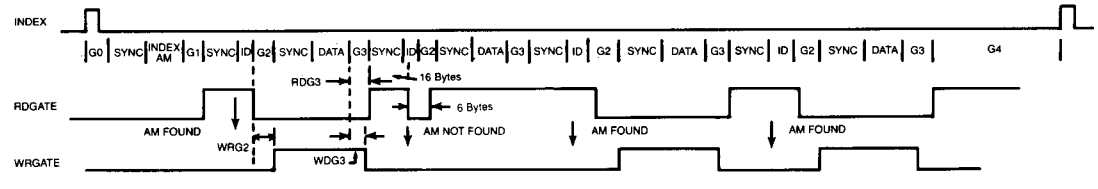


FIGURE 12B: RDGATE AND WRITE GATE TIMING

STANDARD FORMAT PARAMETERS			
PARAMETER	HARD DISK***	SINGLE DEN. FLOPPY	DOUBLE DEN. FLOPPY
GAP Ø *	16	40	80
GAP 1 *	16	26	50
GAP 2 *	3	11	22
GAP 3 *	18**	27	54
SYNC SIZE *	13	6	12
SECTOR COUNT *	user selectable	user selectable	user selectable
SECT. SIZE MULT *	user selectable	user selectable	user selectable
RDG 1	16	73	NA
RDG 2	6	13	24
RDG 3	25	27	24
WDG 2	5	11	23
WDG 3	3	11	3

* = PARAMETER USED BY FORMAT COMMAND
** = GAP 3 VARIES WITH SECTOR SIZE
*** = ALL VALUES APPLY TO 512 BYTES/SECTOR

TABLE 1: STANDARD FORMAT PARAMETERS

REGISTER BIT DEFINITIONS

	7	6	5	4	3	2	1	0
DMA 7-0 (REGISTER 0)	(MSB)			LOW ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 15-8 (REGISTER 1)	(MSB)			MIDDLE ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DMA 23-16 (REGISTER 2)	(MSB)			HIGH ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS				(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)			DESIRED SECTOR NUMBER				(LSB)
DESIRED HEAD (REGISTER 4)	ALWAYS 0		(MSB)	HIGH ORDER BITS OF DESIRED CYLINDER	(MSB)	DESIRED HEAD NUMBER		(LSB)
DESIRED CYLINDER (REGISTER 5)	(MSB)			LOW ORDER BITS OF DESIRED CYLINDER				(LSB)
SECTOR COUNT (REGISTER 6)	(MSB)			NUMBER OF SECTORS TO BE OPERATED ON BY COMMAND				(LSB)
RETRY COUNT (REGISTER 7)	RETRY COUNT (1'S COMPLEMENT)				PROGRAMMABLE OUTPUTS			
MODE (REGISTER 8)	HARD DISK	CRC/ECC	ENABLE	SINGLE DENSITY	ALWAYS 0	STEP	RATE	SELECT
INTERRUPT/ COMMAND TERM. (REGISTER 9)	CRC PRESET 1 = Set to 1 0 = Set to 0	ALWAYS 0	INTERRUPT ON DONE	FLAG DELETED DATA MARK	USER DEFINED FLAG	FLAG WRITE PROTECT	FLAG READY CHANGE	FLAG WRITE FAULT
DATA/DELAY (REGISTER A)	(MSB)			HEAD LOAD DELAY MULTIPLE IS LOADED INTO THIS REGISTER DATA IS LOADED TO OR READ FROM THIS REGISTER				(LSB)
CURRENT HEAD (READ REGISTER 4)	BAD SECTOR FLAG		(MSB)	HIGH ORDER BITS OF CURRENT CYLINDER	(MSB)	CURRENT HEAD NUMBER		(LSB)
CURRENT CYLINDER (READ REGISTER 5)	(MSB)			LOW ORDER BITS OF CURRENT CYLINDER NUMBER				(LSB)
CHIP STATUS (READ REGISTER 8)	RETRY REQUIRED	ECC CORRECTION ATTEMPTED	CRC/ECC ERROR	DELETED DATA MARK READ	SYNC ERROR	COMPARE ERROR	PRESENT DRIVE SELECTED	
DRIVE STATUS (READ REGISTER 9)	ECC ERROR	INDEX	SEEK COMPLETE	TRACK 00	USER DEFINED ACTIVE	WRITE PROTECT ACTIVE	DRIVE READY	WRITE FAULT
INTERRUPT STATUS (COMMAND READ)	INTERRUPT PENDING	DMA REQUEST	DONE	COMMAND TERMINATION CODE		READY CHANGE	OVERRUN/ UNDERRUN	BAD SECTOR

TABLE 2: REGISTER BIT MAPS

UDC WRITE REGISTERS (APPLIES DURING TAPE BACKUP ONLY)

REGISTER	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DMA 7-0 (REGISTER 0)	(MSB)	DMA BEGINNING ADDRESS BUTE (LOW ORDER BITS)						(LSB)
DMA 15-8 (REGISTER 1)	(MSB)	DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS)						(LSB)
DMA 23-16 (REGISTER 2)	(MSB)	DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS)						(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)	MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT) (1)						(LSB)
DESIRED HEAD (REGISTER 4)	0	0	0	0	TRK # BIT 3	TRK # BIT 2	TRK # BIT 1	TRK # BIT 0
DESIRED CYLINDER (REGISTER 5)	ECC TYPE				ALWAYS 1	DATA BLOCK SIZE		
SECTOR COUNT (REGISTER 6)	TAPE MARK BLOCK SIZE (IN 2'S COMPLEMENT + 1) (MODULO 256) (2)			OR	DATA BLOCK COUNT (IN 1'S COMPLEMENT) (3)			
RETRY COUNT (REGISTER 7)	1	1	1	1	USER DEFINED OUTPUTS			
MODE (REGISTER 8)	ALWAYS "0" FOR TAPE	CRC/ECC ENABLE CODE		SINGLE/ DOUBLE DENSITY	ALWAYS 0	SYNC DELAY ENABLE	WRITE ENABLE	TAPE MARK ENABLE
INTERRUPT/ COMMAND TERMINATOR (REGISTER 9)	CRC PRESET	ALWAYS 0	INTERRUPT ON DONE	ALWAYS 1	USER DEFINED	FLAG WRITE PROTECT	FLAG READY CHANGE	FLAG WRITE FAULT

NOTES: (1) The maximum search count is composed of:
130 byte inner loop (RDGATE high 128, 2 byte times)
times the number programmed (maximum of 33,150 byte times
(2) Tape mark operation
(3) Data block operation

TABLE 3: TAPE BACKUP REGISTER BIT MAPS

UDC READ REGISTERS (APPLIES TAPE BACKUP ONLY)

REGISTER	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DMA 7-0 (REGISTER 0)	(MSB)	DMA BEGINNING ADDRESS BYTE (LOW ORDER BITS)						(LSB)
DMA 15-8 (REGISTER 1)	(MSB)	DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS)						(LSB)
DMA 23-16 (REGISTER 2)	(MSB)	DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS)						(LSB)
DESIRED SECTOR (REGISTER 3)	(MSB)	MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT)						(LSB)
CURRENT HEAD (REGISTER 4)	X	X	X	X	X	X	X	X
CURRENT CYLINDER (REGISTER 5)	X	X	X	X	X	X	X	X
CHIP STATUS (REGISTER 8)	X	ECC CORRECTION ATTEMPTED	CRC/ECC ERROR	X	X	X	PRESENT DRIVE SELECTED	
DRIVE STATUS (REGISTER 9)	USER DEFINED	USER DEFINED	SEEK COMP	USER DEFINED	USER DEFINED	WRITE PROTECT	READY	WRITE FAULT
DATA (REGISTER A)	READ DATA							
INTERRUPT STATUS (COMMAND READ)	INT PENDING	DMA REG	DONE	COMMAND TERMINATION CODE (1)		READY CHANGE	OVER/ UNDER RUN	X

NOTES: (1) Command termination bits set to:
11 for data transfer error
10 for sync error
00 for successful termination
X Don't care

TABLE 4: TAPE BACKUP REGISTER BIT MAPS

COMMAND BIT DEFINITIONS

	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0
DESELECT DRIVES	0	0	0	0	0	0	0	1
RESTORE DRIVE	0	0	0	0	0	0	1	1 = Buffered Seek 0 = Normal Seek
STEP IN 1 CYLINDER	0	0	0	0	0	1	0	1 = Buffered Seek 0 = Normal Seek
STEP OUT 1 CYLINDER	0	0	0	0	0	1	1	1 = Buffered Seek 0 = Normal Seek
POLL DRIVES	0	0	0	1	1 = Poll Drive 3 0 = Don't Poll	1 = Poll Drive 2 0 = Don't Poll	1 = Poll Drive 1 0 = Don't Poll	1 = Poll Drive 0 0 = Don't Poll
SELECT DRIVE	0	0	1	1 = Head Load Delay Enabled 0 = Delay Disabled	TYPE OF DRIVE		DRIVE UNIT SELECTED	
SET REGISTER POINTER	0	1	0	0	REGISTER		NUMBER	
SEEK/READ ID	0	1	0	1	0	Step Enable	Wait For Complete	Verify ID
READ SECTORS PHYSICAL	0	1	0	1	1	0	0	Enable Transfer
READ TRACK	0	1	0	1	1	0	1	1 = Transfer All 0 = Transfer ID
READ SECTORS LOGICAL	0	1	0	1	1	1	1 = Bad Sector Bypass 0 = Bad Sector Terminate	Enable Transfer
FORMAT TRACK	0	1	1	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
WRITE SECTORS PHYSICAL	1	1 = Bad Sector Bypass 0 = Bad Sector Termination	0	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
WRITE SECTORS LOGICAL	1	1 = Bad Sector Bypass 0 = Bad Sector Terminate	1	Write Deleted Data	Write With Reduced Current	PRECOMPENSATION VALUE		
TAPE BACKUP	0	0	0	0	1	WRITE:	PRECOMPENSATION VALUE	
						READ:	0 0	Transfer Enable

TABLE 5: COMMAND WORD BIT MAPS

SECTOR SIZE FIELD BITS

DB2	DB1	DB0	IBM FD FORMAT	HD FORMAT
0	0	0	128 bytes/sector	128 bytes/sector
0	0	1	256 bytes/sector	256 bytes/sector
0	1	0	512 bytes/sector	512 bytes/sector
0	1	1	1024 bytes/sector	1024 bytes/sector
1	0	0	not used	2048 bytes/sector
1	0	1	not used	4096 bytes/sector
1	1	0	not used	8192 bytes/sector
1	1	1	not used	16,384 bytes/sector

FORMAT ECC TYPE FIELD

DB7	DB6	DB5	DB4	HD FORMAT
0	0	0	0	4 ECC bytes generated/checked
1	1	1	1	5 ECC bytes generated/checked (1)
1	1	1	0	6 ECC bytes generated/checked (1)
1	1	0	1	7 ECC bytes generated/checked (1)

note 1: WITH EXTERNAL ECC

IBM FLOPPY DISK FORMAT:

ID FIELD	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CYLINDER	track number
HEAD	side number
SECTOR	sector number sector size
SECTOR SIZE	(2 bits)

HARD DISK FORMAT: ST506 PC FORMAT (512 BYTES)

ID FIELD	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CYLINDER	cylinder number (8 LSB's)
HEAD	bad cyl # cyl # cyl # hd # hd # hd # hd # sector bit 10 bit 9 bit 8 bit 3 bit 2 bit 1 bit 0 flag
SECTOR	sector number

HARD DISK FORMAT: (USER SELECTABLE SECTOR SIZE)

ID FIELD	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
CYLINDER	cylinder number (8 LSB's)
HEAD	bad cyl # cyl # cyl # hd # hd # hd # hd # sector bit 10 bit 9 bit 8 bit 3 bit 2 bit 1 bit 0 flag
SECTOR	sector number
SECTOR SIZE	ECC type X sector size (3 bits)

DISK FORMATS

TABLE 6

For additional information, please consult the following:

- Technical Note 6-2 (9224 Overview)
- Technical Note 6-5 (Programmer's Reference Manual)
- HDC 9225 Data Sheet
- HDC 9226 Data Sheet
- HDC 9224 Programmer's Quick Reference Card

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