

54ABT652

Octal Transceivers and Registers with TRI-STATE® Outputs

General Description

The 'ABT652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

- Multiplexed real-time and stored data
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latching protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9324201

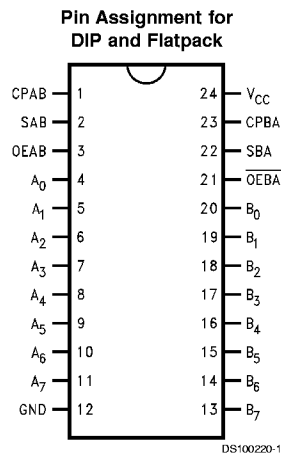
Features

- Independent registers for A and B buses

Ordering Code:

Commercial	Package Number	Package Description
54ABT652J-QML	J24A	24-Lead Ceramic Dual-in-line
54ABT652W-QML	W24C	24-Lead Cerpack
54ABT652E-QML	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

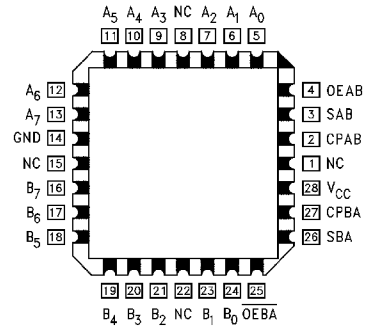
Connection Diagram



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Connection Diagram (Continued)

Pin Assignment for LCC

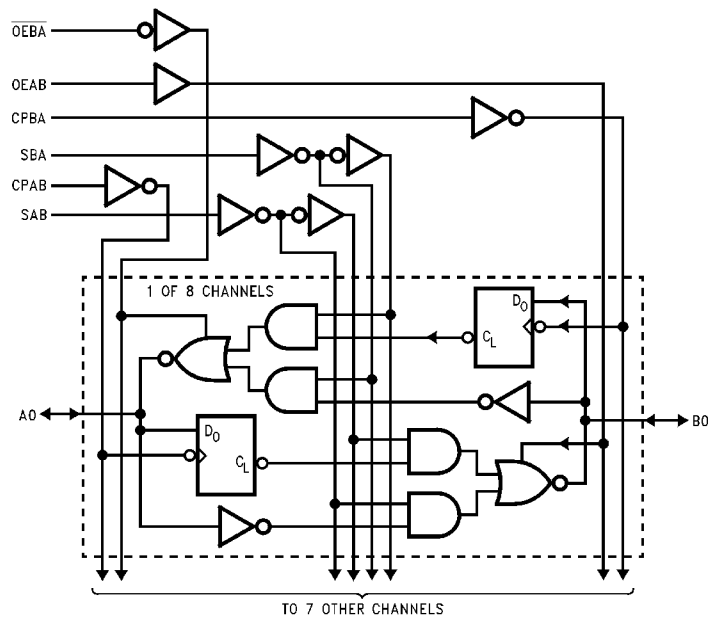


DS100220-48

Pin Descriptions

Pin Names	Description
A ₀ –A ₇	Data Register A Inputs/TRI-STATE Outputs
B ₀ –B ₇	Data Register B Inputs/TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, \overline{OEBA}	Output Enable Inputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

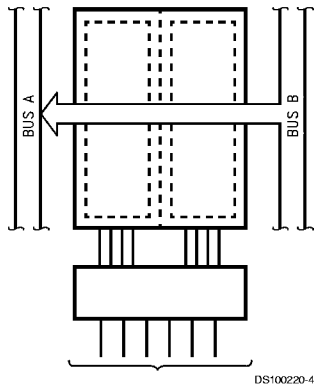
The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 'ABT652C.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropri-

ate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and \overline{OEBA} . In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

Functional Description (Continued)

Note A: Real-Time Transfer Bus B to Bus A

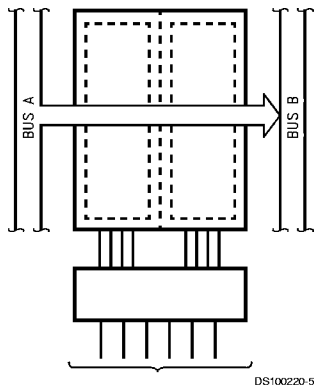


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OEAB	<u>OEBA</u>
L	L

CPAB	CPBA	SAB	SBA
X	X	X	L

Note B: Real-Time Transfer Bus A to Bus B

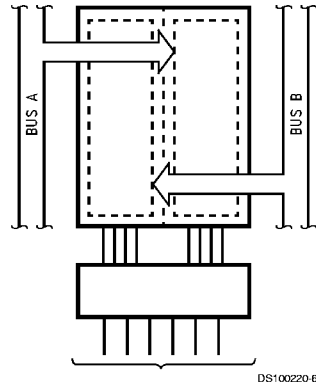


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OEAB	<u>OEBA</u>
H	H

CPAB	CPBA	SAB	SBA
X	X	L	X

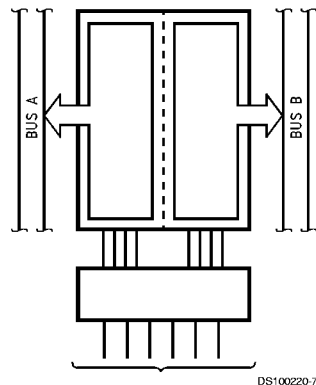
Note C: Storage



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OEAB	<u>OEBA</u>	CPAB	CPBA	SAB	SBA
X	H	N	X	X	X
L	X	X	N	X	X
L	H	N	N	X	X

Note D: Transfer Storage Data to A or B



DS100220-7

OEAB	<u>OEBA</u>	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FIGURE 1.

Functional Description (Continued)

Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	$\overline{\text{OEBA}}$	CPAB	CPBA	SAB	SBA	A ₀ thru A ₇	B ₀ thru B ₇	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	N	N	X	X			Store A and B Data
X	H	N	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	N	N	X	X	Input	Output	Store A in Both Registers
L	X	H or L	N	X	X	Not Specified	Input	Hold A, Store B
L	L	N	N	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

N = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or or Power-Off State in the HIGH State	-0.5V to +5.5V -0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA

Over Voltage Latchup (I/O)

10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT652			Units	V _{CC}	Conditions	
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal	
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal	
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA (Non I/O Pins)	
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA, (A _n , B _n)	
		54ABT	2.0		V	Min	I _{OH} = -24 mA, (A _n , B _n)	
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA, (A _n , B _n)	
I _{IH}	Input HIGH Current			2	μA	Max	V _{IN} = 2.7V (Non-I/O Pins) (Note 4) V _{IN} = V _{CC} (Non-I/O Pins)	
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)	
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V _{IN} = 5.5V (A _n , B _n)	
I _{IL}	Input LOW Current			-2	μA	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 4) V _{IN} = 0.0V (Non-I/O Pins)	
I _{IH} + I _{OZH}	Output Leakage Current			50	μA	0V-5.5V	V _{OUT} = 2.7V (A _n , B _n); OEBA = 2.0V and OEAB = GND = 2.0V	
I _{IL} + I _{OZL}	Output Leakage Current			-50	μA	0V-5.5V	V _{OUT} = 0.5V (A _n , B _n); OEBA = 2.0V and OEAB = GND = 2.0V	
I _{OS}	Output Short-Circuit Current			-50	-180	mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50		μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{CCH}	Power Supply Current			250		μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30		mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			250		μA	Max	Outputs TRI-STATE; All others at V _{CC} or GND
I _{CCIT}	Additional I _{CC} /Input			2.5		mA	Max	V _I = V _{CC} - 2.1V All others at V _{CC} or GND

Note 4: Guaranteed but not tested.

Note 5: For 8 outputs toggling, I_{CCD} < 1.4 mA/MHz.

Note 6: Guaranteed, but not tested.

DC Electrical Characteristics

Symbol	Parameter	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	1.2	V	5.0	T _A = 25°C (Note 7)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-1.8	V	5.0	T _A = 25°C (Note 7)

Note 7: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF			
		Min	Max		
f _{max}	Max Clock Frequency	125		MHz	
t _{PLH}	Propagation Delay	1.4	7.8	ns	Figure 5
t _{PHL}	Clock to Bus	1.2	8.4		
t _{PLH}	Propagation Delay	1.5	6.7	ns	Figure 5
t _{PHL}	Bus to Bus	1.5	6.7		
t _{PLH}	Propagation Delay	1.2	6.9	ns	Figure 5
t _{PHL}	SBA or SAB to A _n to B _n	1.2	7.7		
t _{PZH}	Enable Time	1.3	5.6	ns	Figure 7
t _{PZL}	$\overline{\text{OEBA}}$ or OEAB to A _n or B _n	2.0	7.8		
t _{PHZ}	Disable Time	1.5	8.2	ns	Figure 7
t _{PLZ}	$\overline{\text{OEBA}}$ or OEAB to A _n or B _n	1.5	7.3		

AC Operating Requirements

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF			
		Min	Max		
t _{S(H)}	Setup Time, HIGH	3.5		ns	Figure 8
t _{S(L)}	or LOW Bus to Clock				
t _{H(H)}	Hold Time, HIGH	1.5		ns	Figure 8
t _{H(L)}	or LOW Bus to Clock				
t _{W(H)}	Pulse Width, HIGH	4.0		ns	Figure 6
t _{W(L)}	HIGH or LOW				

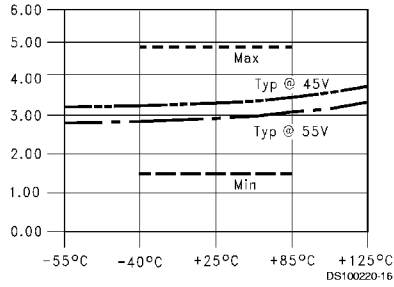
Capacitance

Symbol	Parameter	Max	Units	Conditions ($T_A = 25^\circ\text{C}$)
C_{IN}	Input Capacitance	14.0	pF	$V_{CC} = 0V$ (non I/O pins)
$C_{I/O}$ (Note 8)	I/O Capacitance	19.5	pF	$V_{CC} = 5.0V$ (A_n, B_n)

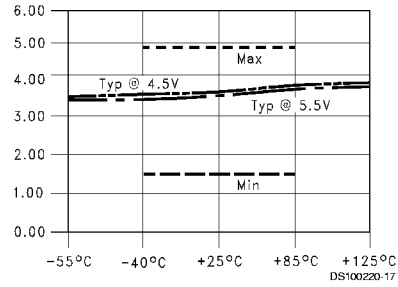
Note 8: $C_{I/O}$ is measured at frequency, $f = 1\text{ MHz}$, per MIL-STD-883D, Method 3012.

Capacitance (Continued)

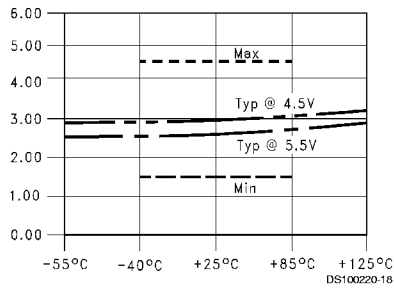
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Clock to Bus



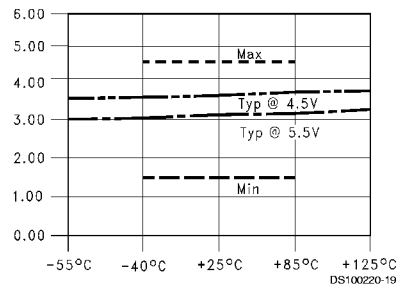
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Clock to Bus



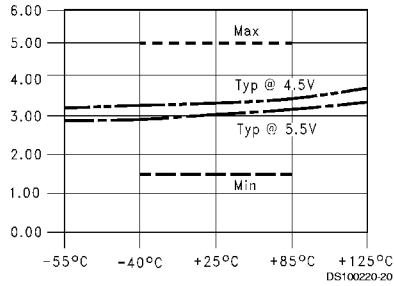
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Bus to Bus



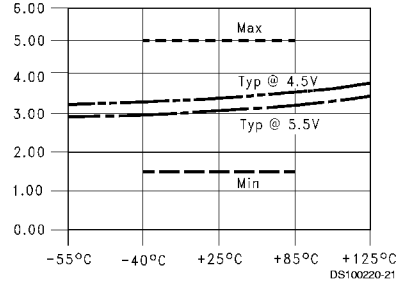
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 Bus to Bus



t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 SBA or SAB to A_n or B_n

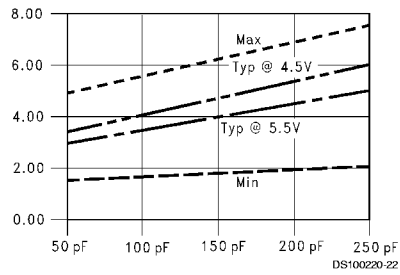


t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching
 SBA or SAB to A_n or B_n

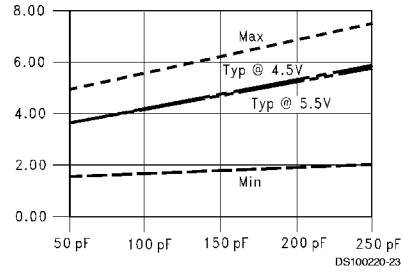


Capacitance (Continued)

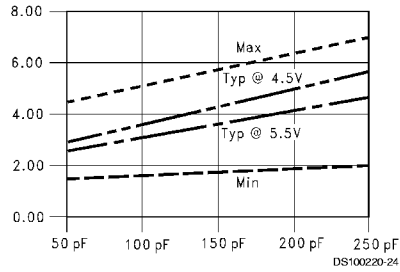
t_{PLH} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$
Clock to Bus



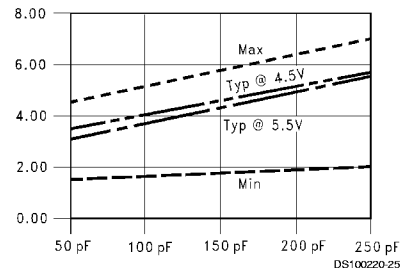
t_{PHL} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$
Clock to Bus



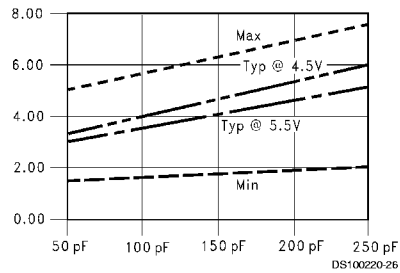
t_{PLH} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$
Bus to Bus



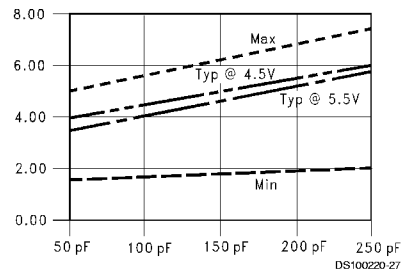
t_{PHL} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$
Bus to Bus



t_{PLH} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$
SBA or SAB to A_n or B_n

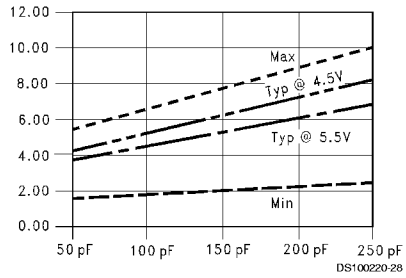


t_{PHL} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$
SBA or SAB to A_n or B_n

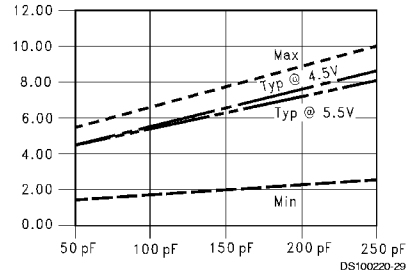


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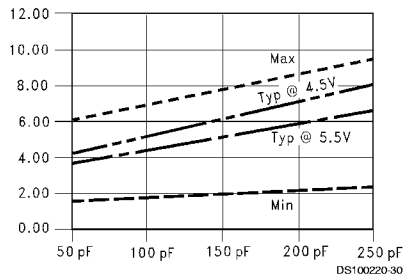
t_{PLH} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
Clock to Bus



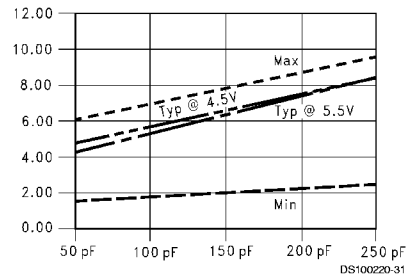
t_{PHL} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
Clock to Bus



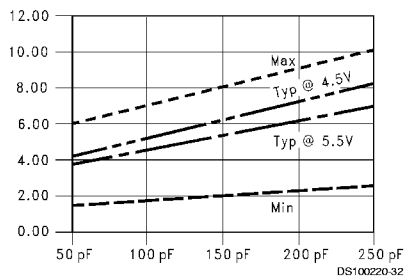
t_{PLH} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
Bus to Bus



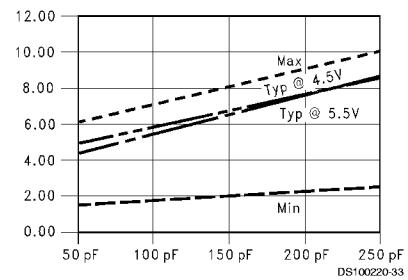
t_{PHL} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
Bus to Bus



t_{PLH} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
SBA or SAB to A_n or B_n

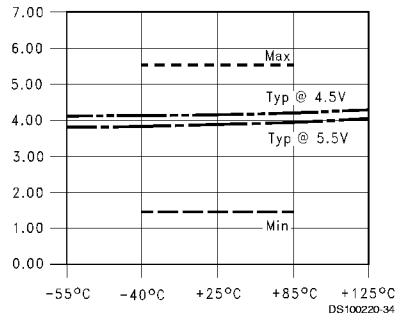


t_{PHL} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$
SBA or SAB to A_n or B_n

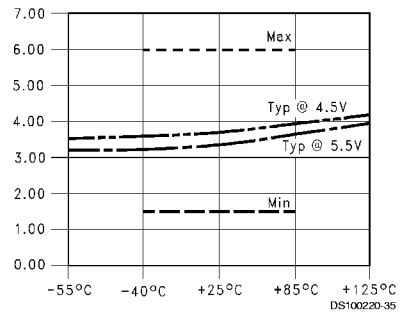


Capacitance (Continued)

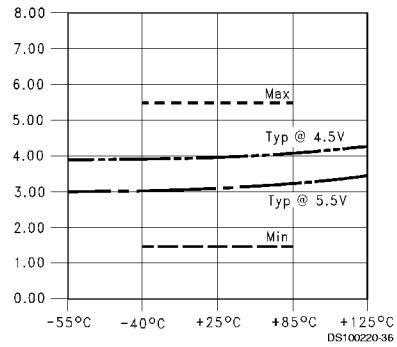
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



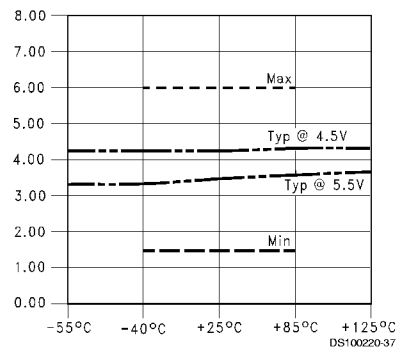
t_{PLZ} vs Temperature (T_A)
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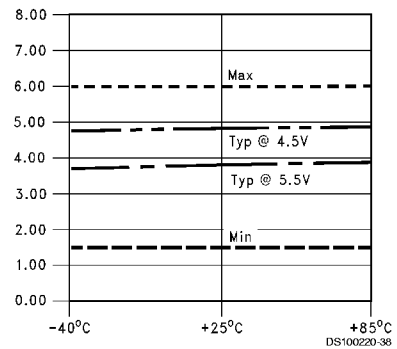
t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



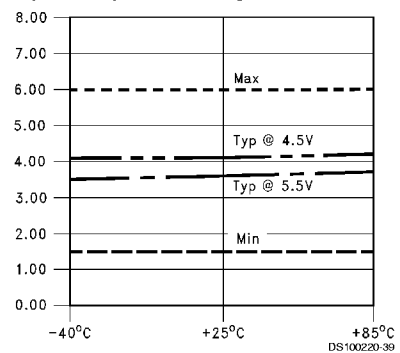
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching

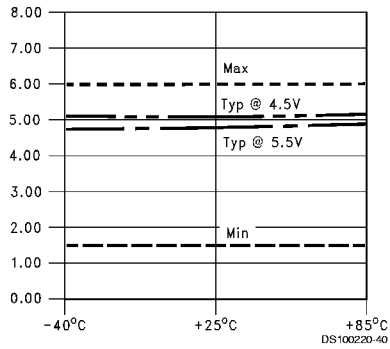


t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching

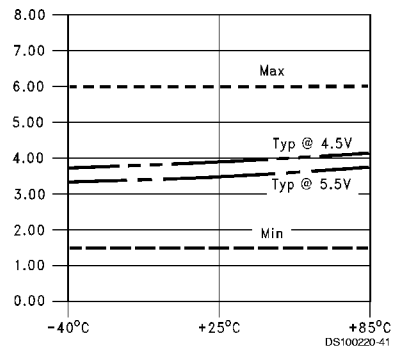


Capacitance (Continued)

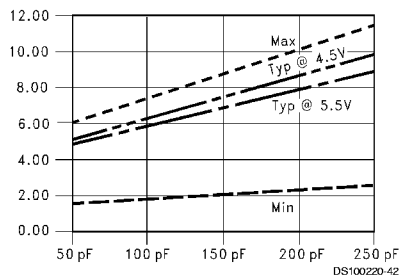
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



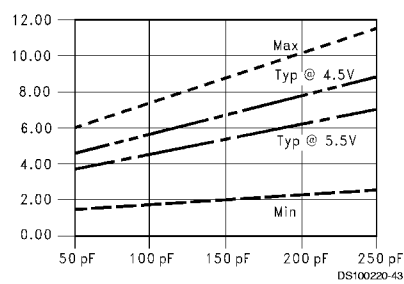
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



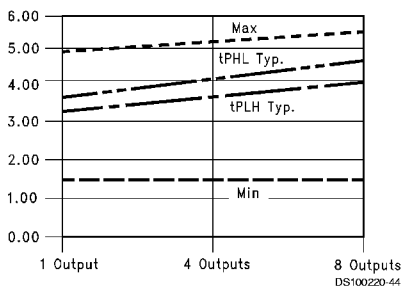
t_{PZL} vs Load Capacitance
 8 Outputs Switching
 $T_A = 25^\circ\text{C}$



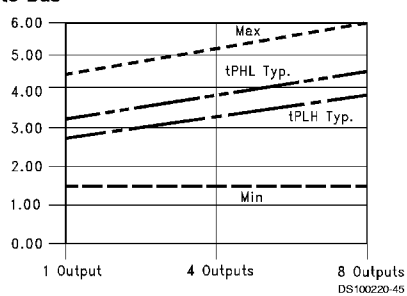
t_{PZH} vs Load Capacitance
 8 Outputs Switching
 $T_A = 25^\circ\text{C}$



t_{PLH} and t_{PHL} vs Number Output Switching
 $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, $C_L = 50$ pF
 Clock to Bus



t_{PLH} and t_{PHL} vs Number Output Switching
 $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, $C_L = 50$ pF
 Bus to Bus

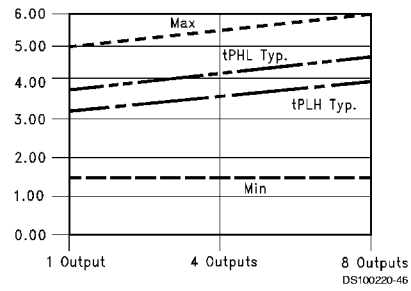


Capacitance (Continued)

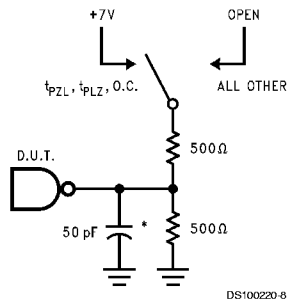
t_{PLH} and t_{PHL} vs Number Output Switching

$V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50 pF$

SBA or SAB to A_n or B_n



AC Loading



*Includes jig and probe capacitance

FIGURE 2. Standard AC Test Load

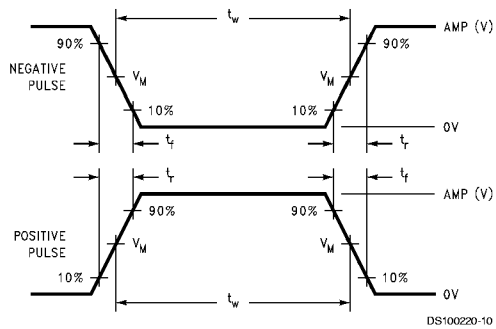


FIGURE 3. Test Input Signal Levels

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

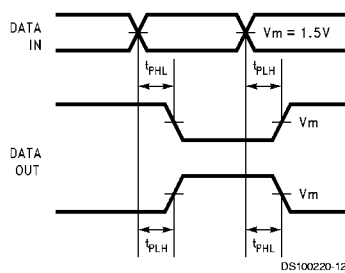


FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

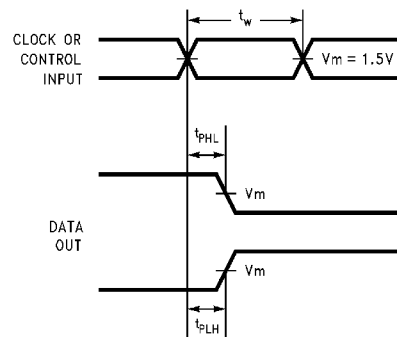


FIGURE 6. Propagation Delay, Pulse Width Waveforms

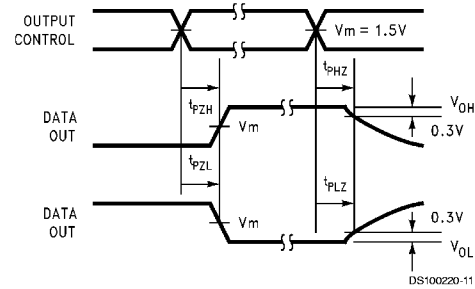


FIGURE 7. TRI-STATE Output HIGH and LOW Enable and Disable Times

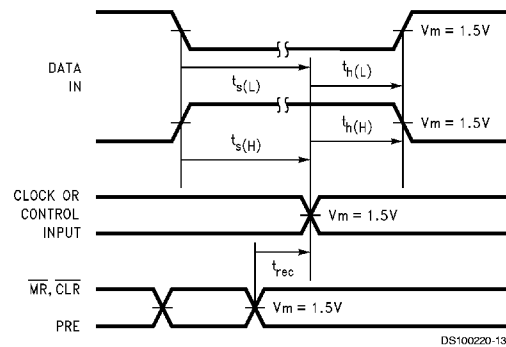
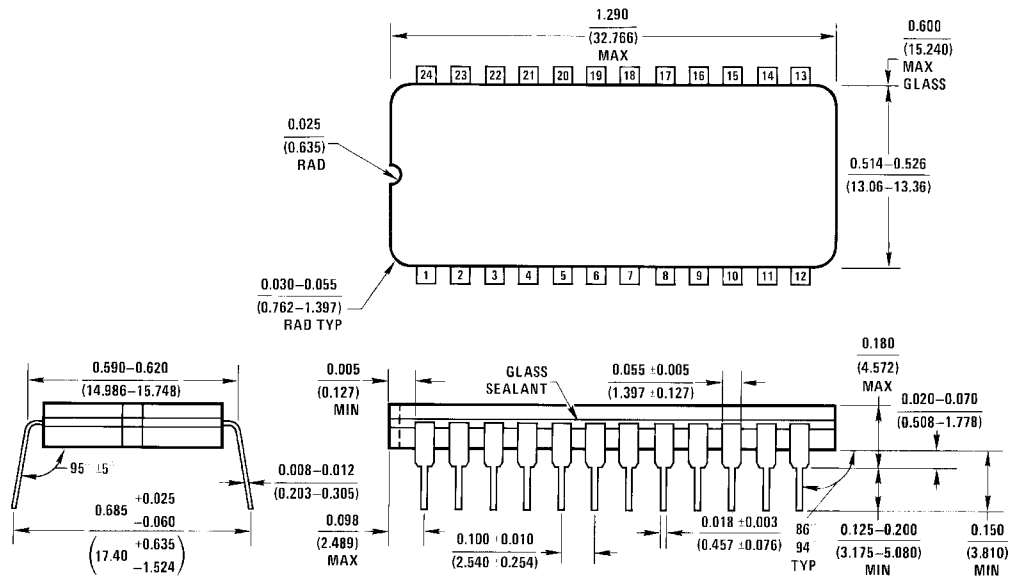


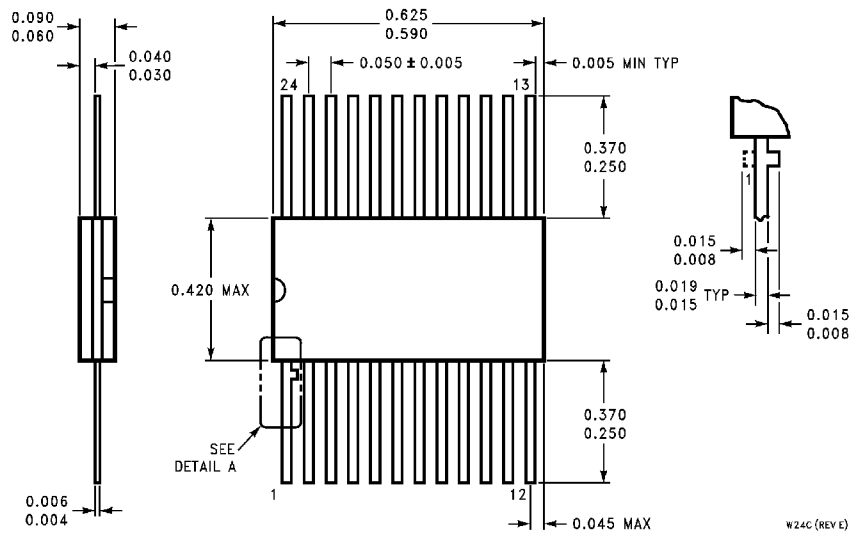
FIGURE 8. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



J24A (REV H)

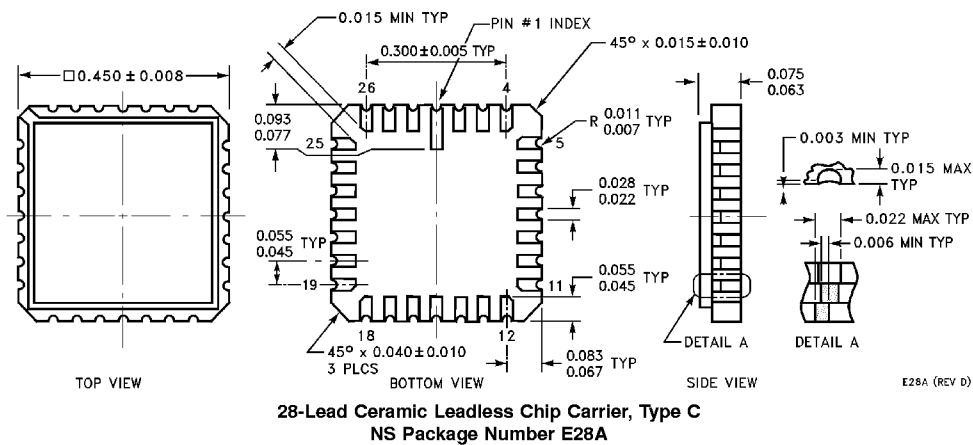
24-Lead Ceramic Dual-in-line
NS Package Number J24A



W24C (REV E)

24-Lead Cerpack
NS Package Number W24C

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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