UC2854B-EP Advanced High-Power Factor Preregulator

1 Features

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of −55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Controls Boost PWM to Near-Unity Power Factor
- Limits Line Current Distortion to <3%
- World-Wide Operation Without Switches
- Accurate Power Limiting
- Fixed-Frequency Average Current-Mode Control
- High Bandwidth (5 MHz), Low-Offset Current Amplifier
- Integrated Current- and Voltage Amplifier Output Clamps
- Multiplier Improvements: Linearity, 500 mV VAC Offset (Eliminates External Resistor), 0 V to 5 V Multout Common-Mode Range
- V_{REF} GOOD Comparator
- Faster and Improved Accuracy ENABLE Comparator
- UVLO Options (16 V/10 V or 10.5 V/10 V)
- 300-µA Start-Up Supply Current

2 Applications

Industrial Lighting

3 Description

The UC2854B products are pin compatible enhanced versions of the UC2854. Like the UC2854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the ac-input line current waveform to correspond to the ac-input line voltage. To do this the UC2854B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

A 1% 7.5-V reference, fixed frequency oscillator, PWM, voltage amplifier with soft-start, line voltage feedforward (VRMS squarer), input supply voltage clamp, and over current comparator round out the list of features.

The UC2854B is available in a DW (SOIC-wide) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC2854B-EP	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

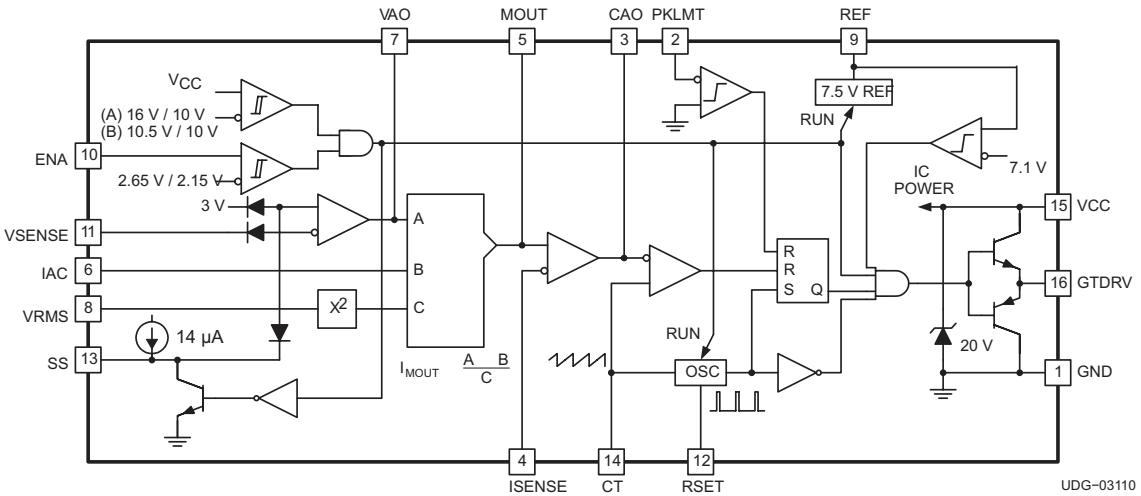


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2005) to Revision A **Page**

- Added *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated the max V_{CC} turn-on threshold voltage ... 6
- Updated the max enable threshold voltage ... 6

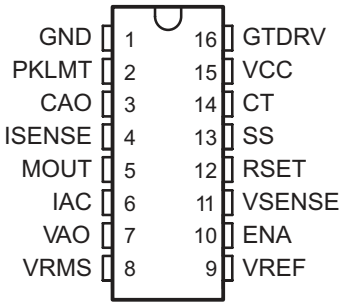
5 Description (continued)

The UC2854A/B products improve upon the UC2854 by offering a wide bandwidth, low offset current amplifier, a faster responding and improved accuracy enable comparator, a VREF GOOD comparator, UVLO threshold options (16 V/10 V for offline, 10.5 V/10 V for startup from an auxiliary 12-V regulator), lower startup supply current, and an enhanced multiply/divide circuit.

New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the multiplier output/current amplifier input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, RSET controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of 2 × IAC at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

6 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	J/N/DW	Q/L		
CAO	3	4	O	Output of the wide bandwidth current amplifier and one of the inputs to the PWM duty-cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1 V to 7.5 V.
CT	14	18	I	Capacitor from CT to GND sets the PWM oscillator frequency
ENA	10	13	I	A nominal voltage above 2.65 V on this pin allows the device to begin operating. Once operating, the device shuts off if this pin goes below 2.15 V nominal.
GND	1	2	—	All bypass and timing capacitors connected to GND should have leads as short and direct as possible. All voltages are measured with respect GND.
GTDRV	16	20	O	Output of the PWM is a 1.5-A peak totem-pole MOSFET gate driver on GTDRV. This output is internally clamped to 15 V so that the device can be operated with VCC as high as 35 V. Use a series gate resistor of at least 5 Ω to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load.
IAC	6	8	I	Current input to the multiplier, proportional to the instantaneous line voltage. This input to the analog multiplier is a current. The multiplier is tailored for low distortion from this current input (IAC) to MOUT, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on ac is 6 V, so in addition to a resistor from IAC to rectified 60 Hz, connect a resistor from IAC to VREF. If the resistor to VREF is one-fourth of the value of the resistor to the rectifier, then the 6-V offset is cancelled, and the line current has minimal cross-over distortion.
ISENSE	4	5	I	Switch current sensing input. This is the inverting input to the current amplifier. This input and the non-inverting input MOUT remain functional down to and below GND. Care should be taken to avoid taking these inputs below −0.5 V, because they are protected with diodes to GND.
MOUT	5	7	I/O	Multiplier output and current sense plus. The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MOUT. The cautions about taking ISENSE below −0.5 V also apply to MOUT. As the multiplier output is a current, this is a high-impedance input similar to ISENSE, so the current amplifier can be configured as a differential amplifier to reject GND noise.
PKLMT	2	3	I	Peak limit. The threshold for PKLMT is 0 V. Connect this input to the negative voltage on the current sense resistor. Use a resistor to REF to offset the negative current sense signal up to GND.
RSET	12	15	I	Oscillator charging current and multiplier limit set. A resistor from RSET to ground programs oscillator charging current. Multiplier output current does not exceed 3.75 V divided by the resistor from RSET to ground.
SS	13	17	I	Soft-start. SS remains at GND as long as the device is disabled or VCC is too low. SS pulls up to over 8 V by an internal 14-mA current source when both VCC becomes valid and the device is enabled. SS acts as the reference input to the voltage amplifier if SS is below VREF. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier rises slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.
VAO	7	9	I	Voltage amplifier input

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	J/N/DW	Q/L		
VCC	15	19	I	Positive supply rail
VREF	9	12	O	Used to set the peak limit point and as an internal reference for various device functions. This voltage must be present for the device to operate.
VRMS	8	10	I	One of the inputs into the multiplier. This pin provides the input RMS voltage to the multiplier circuitry.
VSENSE	11	14	I	This pin provides the feedback from the output. This input goes into the voltage error amplifier and the output of the error amplifier is another of the inputs into the multiplier circuit.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		22	V
Input voltage	VSENSE, VRMS, ISENSE MOUT		11	V
	PKLMT		5	V
I_{GTDRV}	GTDRV current, continuous		0.5	A
I_{GTDRV}	GTDRV current, 50% duty cycle		1.5	A
Input current	RSET, IAC, PKLMT, ENA		10	mA
T_J	Junction temperature	−55	150	°C
T_{sol}	Lead temperature, 1.6 mm (1/16 inch) from case for 10 seconds		300	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	10	20	V
T_J	Operating junction temperature	−55	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UC2854B-EP DW (SOIC) 16 PINS		UNIT
		HIGH	LOW	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	36.9	38.4	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	73.1	111.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) $R_{\theta JA}$ values are based on zero air flow.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
	Supply current, off	CAO = 0 V, VAO = 0 V, V_{CC} = V_{UVLO} − 0.3 V		250	400	µA
	Supply current, on			12	18	mA
	V_{CC} turn-on threshold voltage		8	10.5	11.3	V
	V_{CC} turn-off threshold voltage		9	10	12	V
	V_{CC} clamp	I_{VCC} = $I_{VCC(on)}$ + 5 mA	18	20	22	V
VOLTAGE AMPLIFIER						
	Input voltage		2.9	3	3.1	V
	V_{SENSE} bias current		−500	−25	500	nA
	Open loop gain	2 V ≤ V_{OUT} ≤ 5 V	70	100		dB
V_{OH}	High-level output voltage	I_{LOAD} = −500 µA		6		V
V_{OL}	Low-level output voltage	I_{LOAD} = 500 µA		0.3	0.5	V
I_{SC}	Output short-circuit current	V_{OUT} = 0 V		1.5	3.5	mA
	Gain bandwidth product(1)	f_{IN} = 100 kHz, 10 mV_{P-P}		1		MHz
CURRENT AMPLIFIER						
	Input offset voltage	V_{CM} = 0 V, T_A = 25°C	−4		0	mV
		V_{CM} = 0 V, overtemperature	−5.5		0	
	Input bias current, ISENSE	V_{CM} = 0 V	−500		500	nA
	Open loop gain	2 V ≤ V_{OUT} ≤ 6 V	80	110		dB
V_{OH}	High-level output voltage	I_{LOAD} = −500 µA		8		V
V_{OL}	Low-level output voltage	I_{LOAD} = 500 µA		0.3	0.5	V
	ISC Output short-circuit current	V_{OUT} = 0 V		1.5	3.5	mA
	CMRR Common mode rejection range		−0.3		5	V
	Gain bandwidth product(1)	f_{IN} = 100 kHz, 10 mV_{P-P}	3	5		MHz
REFERENCE						
	Output voltage	I_{REF} = 0 mA, T_A = 25°C	7.4	7.5	7.6	V
		I_{REF} = 0 mA	7.35	7.5	7.65	
	Load regulation	1 mA ≤ I_{REF} ≤ 10 mA	0	8	20	mV
	Line regulation	12 V ≤ V_{CC} ≤ 18 V	0	14	25	mV
	ISC Short circuit current	V_{REF} = 0 V	25	35	60	mA
OSCILLATOR						
	Initial accuracy	T_A = 25°C	85	100	115	kHz
	Voltage stability	12 V ≤ V_{CC} ≤ 18 V		1%		
	Total variation	Line, temperature	80		120	kHz
	Ramp amplitude (peak-to-peak)		4.9		5.9	
	Ramp valley voltage		0.8		1.3	V
ENABLE/SOFT-START/CURRENT LIMIT						
	Enable threshold voltage		2.35	2.55	2.90	V
	Enable hysteresis	V_{FAULT} = 2.5 V		500	600	mV
	Enable input bias current	V_{ENA} = 0 V		−2	−5	µA
	Propagation delay to disable time(1)	Enable overdrive = 100 mV		300		ns
	Soft-start charge current	V_{SS} = 2.5 V	10	14	24	µA
	Peak limit offset voltage		−15		15	mV
	Peak limit input current	V_{PKLMT} = −0.1 V	−200	−100		µA

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Peak limit propagation delay time(1)			150		ns
MULTIPLIER						
	Output current, I_{AC} limited	I_{AC} = 100 µA, V_{RMS} = 1 V, R_{SET} = 10 kΩ	−220	−200	−170	µA
	Output current, zero	I_{AC} = 0 µA, R_{SET} = 10 kΩ	−2	−0.2	2	µA
	Output current, power limited	V_{RMS} = 1.5 V, V_A = 6 V	−230	−200	−170	µA
	Output current	V_{RMS} = 1.5 V, V_A = 2 V		−22		µA
		V_{RMS} = 1.5 V, V_A = 5 V		−156		
		V_{RMS} = 5 V, V_A = 2 V		−2		
		V_{RMS} = 5 V, V_A = 5 V		−14		
	Gain constant(2)	V_{RMS} = 1.5 V, V_A = 6 V, T_A = 25°C	−1.1	−1	−0.9	A/A
GATE DRIVER						
V_{OH}	High-level output voltage	I_{OUT} = −200 mA, V_{CC} = 15 V	12	12.8		V
V_{OL}	Low-level output voltage	I_{OUT} = 200 mA		1	2.2	V
		I_{OUT} = 10 mA		300	500	mV
	Low-level UVLO voltage	I_{OUT} = 50 mA, V_{CC} = 0 V		0.9	1.5	V
	Output rise time(1)	C_{LOAD} = 1 nF		35		ns
	Output fall time(1)	C_{LOAD} = 1 nF		35		ns
	Output peak current(1)	C_{LOAD} = 10 nF		1		A

(2) Gain constant.

$$(K) = \frac{I_{IAC} \times (V_{VAO} - 1.5\ V)}{\left[(V_{VRMS})^2 \times I_{MOUT}\right]}$$

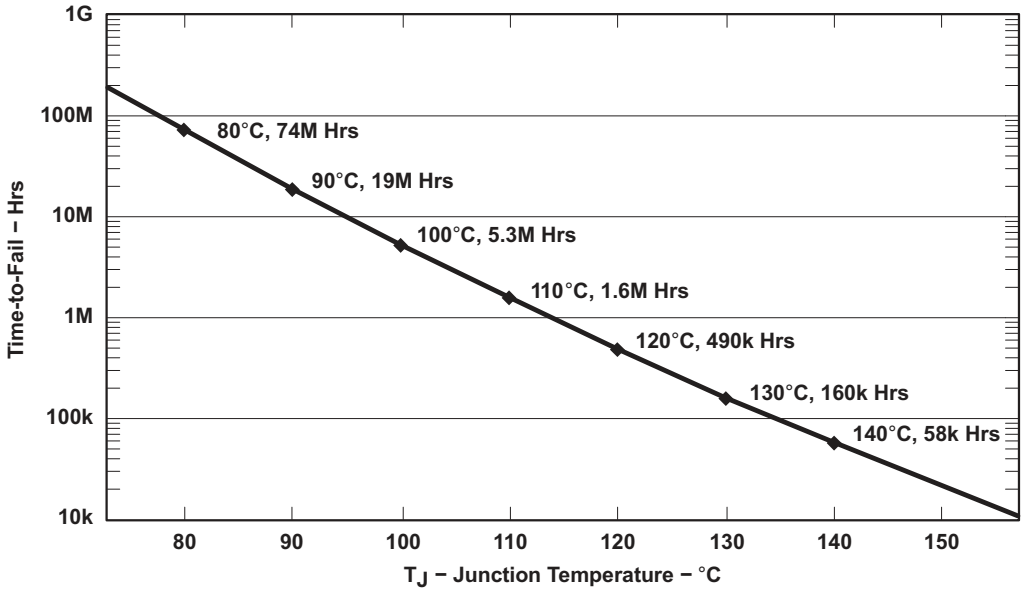


Figure 1. Wirebond Operating Life Derating Chart

7.6 Typical Characteristics

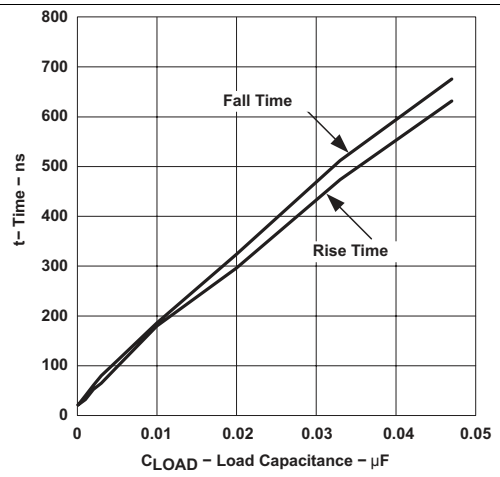


Figure 2. Gate Drive Timing vs Load Capacitance

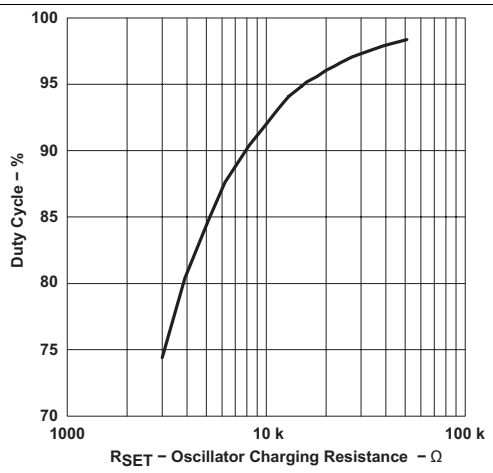


Figure 3. Gate Drive Maximum Duty Cycle vs Oscillator Charging Resistance

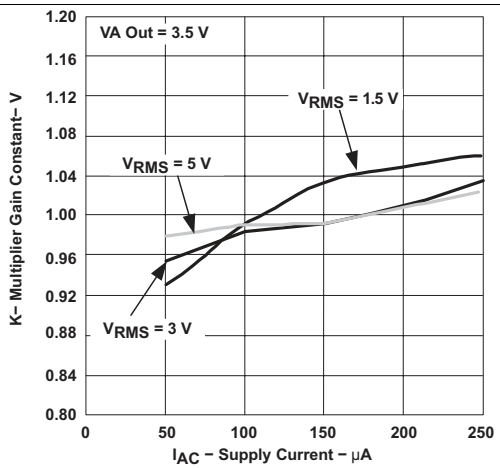


Figure 4. Multiplier Gain Constant vs Supply Current

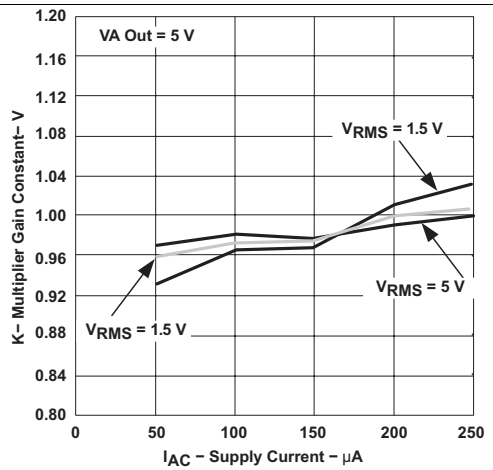


Figure 5. Multiplier Gain Constant vs Supply Current

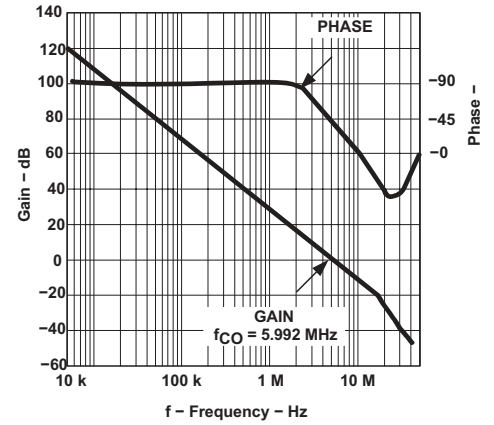


Figure 6. Current Amplifier Gain vs Frequency

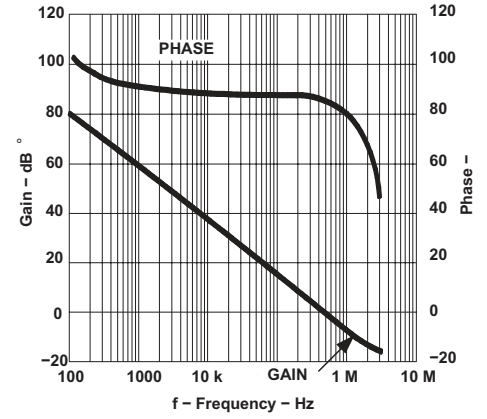


Figure 7. Voltage Amplifier Gain vs Frequency

Typical Characteristics (continued)

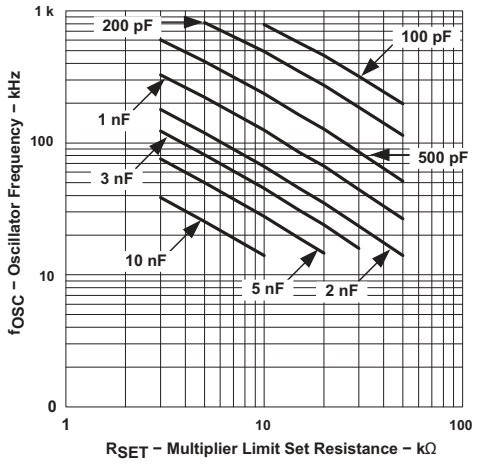


Figure 8. Oscillator Frequency vs Limit Set Resistance and Timing Capacitance

8 Detailed Description

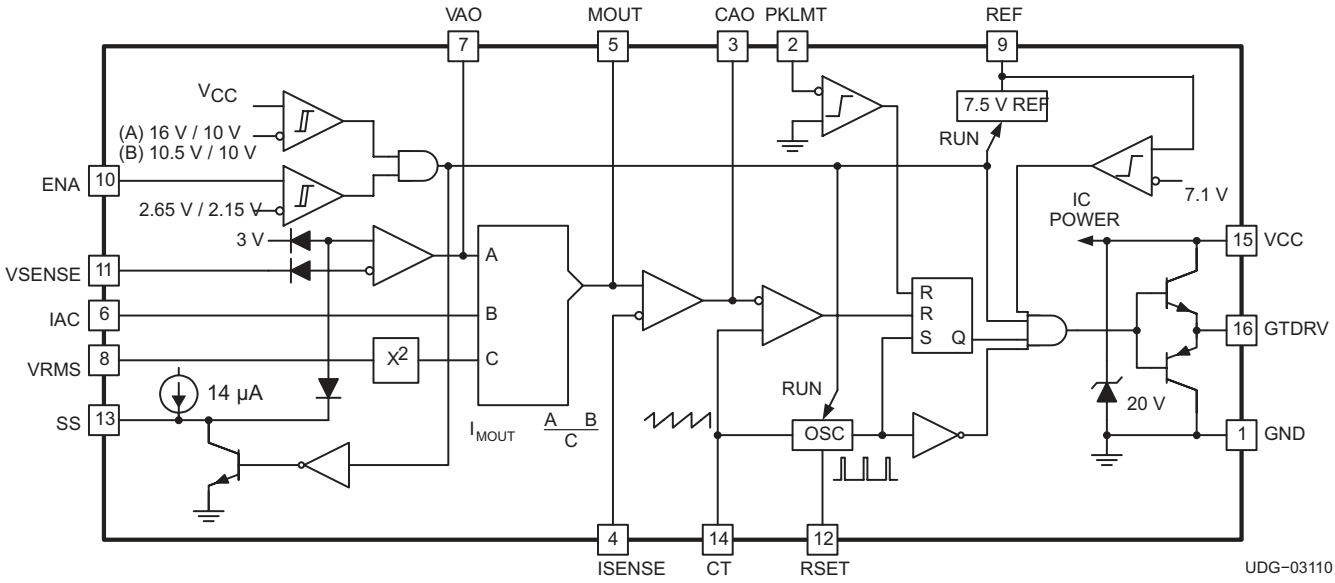
8.1 Overview

The objective of active power factor correction is to make the input to a power supply look like a simple resistor. An active power factor corrector does this by programming the input current in response to the input voltage. As long as the ratio between the voltage and current is a constant the input will be resistive and the power factor will be 1.0. When the ratio deviates from a constant the input will contain phase displacement, harmonic distortion or both and either one will degrade the power factor. UC3854 configured as a boost converter can be used to meet the system needs.

A boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantage of the boost regulator is the high output voltage required. The output voltage must be greater than the highest expected peak input voltage.

The boost regulator input current must be forced or programmed to be proportional to the input voltage waveform for power factor correction. Feedback is necessary to control the input current and either peak current mode control or average current mode control may be used. Both techniques may be implemented with the UC3854.

8.2 Functional Block Diagram



8.3 Feature Description

The UC2854B is designed as a pin compatible upgrade to the industry standard UC2854 active power factor correction circuits. The circuit enhancements allow the user to eliminate in most cases several external components currently required to successfully apply the UC2854. In addition, linearity improvements to the multiply, square and divide circuitry optimizes overall system performance. Detailed descriptions of the circuit enhancements are provided below. For in-depth design applications reference data see the application notes, *UC2854 Controlled Power Factor Correction Circuit Design* (SLUA144) and *UC2854A and UC2854B Advanced Power Factor Correction Control ICs* (SLUA177).

8.3.1 Multiply/Square and Divide

The UC2854B multiplier design maintains the same gain constant $\left(K = \frac{-1}{V}\right)$ as the UC2854. The relationship between the inputs and output current is given as:

Feature Description (continued)

$$R_{pk2} = \frac{V_{rs} \times R_{pk1}}{V_{ref}} \quad (1)$$

This is nearly the same as the UC2854, but circuit differences have improved the performance and application.

The first difference is with the IAC input. The UC2854B regulated this pin voltage to the nominal 500 mV over the full operating temperature range, rather than the 6 V used on the UC2854. The low offset voltage eliminates the need for a line zero crossing compensating resistor to VREF from IAC that UC2854 designs require. The maximum current at high line into Iac should be limited to 250 µA for best performance.

Therefore, if $V_{VAC(max)}$ = 270 V,

$$R_{IAC} = \frac{270 \times 1.414}{250\ \mu A} = 1.53\ M\Omega \quad (2)$$

The V_{RMS} pin linear operating range is improved with the UC2854B as well. The input range for VRMS extends from 0 V to 5.5 V. Since the UC2854A squaring circuit employs an analog multiplier, rather than a linear approximation, accuracy is improved, and discontinuities are eliminated. The external divider network connected to VRMS should produce 1.5 V at low line (85 VAC). This puts 4.77 V on VRMS at high line (27 VAC) which is well within its operating range.

The voltage amplifier output forms the third input to the multiplier and is internally clamped to 6 V. This eliminated an external zener clamp often used in UC2854 designs. The offset voltage at this input to the multiplier has been raised on the UC2854A/B to 1.5 V.

The multiplier output pin, which is also common to the current amplifier non-inverting input, has a −0.3 V to 5 V output range, compared to the −0.3 V to 2.5 V range of the UC2854. This improvement allows the UC2854B to be used in applications where the current sense signal amplitude is large.

8.3.2 Voltage Amplifier

The UC2854B voltage amplifier design is essentially similar to the UC2854 with two exceptions. The first is with the internal connection. The lower voltage reduces the amount of charge on the compensation capacitors, which provides improved recovery form large signal events, such as line dropouts, or power interruption. It also minimizes the dc current flowing through the feedback. The output of the voltage amplifier is also changes. In addition to a 6-V temperature compensated clamp, the output short circuit current has been lowered to 2 mA typical and an active pull down has replaced the passive pull down of the UC2854.

8.3.3 Current Amplifier

The current amplifier for an average current PFC controller needs a low offset voltage in order to minimize AC line current distortion. With this in mind, the UC2854B current amplifier has improved the input offset voltage from ±4 mV to 0 V to ±3 mV. The negative offset of the UC2854B assures that the PWM circuit will not drive the MOSFET is the current command is zero (both current amplifier inputs zero.) Previous designs required an external offset cancellation network to implement this key feature. The bandwidth of the current amplifier has been improved as well to 5 MHz typical. While this is not generally an issue at 50-Hz or 60-Hz inputs, it is essential for 400-Hz input avionics applications.

8.3.4 Miscellaneous

Several other important enhancements have been implemented in the UC2854B. A V_{CC} supply voltage clamp at 20 V allows the controller to be current fed if desired. The lower startup supply current (250 mA typical), substantially reduces the power requirements of an offline startup resistor. The 10.5 V/10 V UVLO option (UC2854B) enables the controller to be powered off of an auxiliary 12-V supply.

The VREF GOOD comparator assures that the MOSFET driver output remains low if the supply of the 7.5 V reference are not yet up. This improvement eliminates the need for external Schottky diodes on the PKLMT and Mult Out pins that some UC2854 designs require. The propagation delay of the disable feature has been improved to 300 ns typical. This delay was proportional to the size of the VREF capacitor on the UC2854 and is typically several orders of magnitude slower.

8.4 Device Functional Modes

Functional Block Diagram shows a block diagram of the UC2854. This integrated circuit contains the circuits necessary to control a power factor corrector. The UC2854 is designed to implement average current mode control but is flexible enough to be used for a wide variety of power topologies and control methods.

The top left corner of *Functional Block Diagram* contains the undervoltage lockout comparator and the enable comparator. The output of both of these comparators must be true to allow the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called Vsense. The diodes shown around the voltage error amplifier are intended to represent the functioning of the internal circuits rather than to show the actual devices. The diodes shown in the block diagram are ideal diodes and indicate that the non-inverting input to the error amplifier is connected to the 7.5Vdc reference voltage under normal operation but is also used for the slow start function. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and eliminates the turn-on overshoot which plagues many power supplies. The diode shown between pin 11 and the inverting input of the error amplifier is also an ideal diode and is shown to eliminate confusion about whether there might be an extra diode drop added to the reference or not. In the actual device, this is done with differential amplifiers. An internal current source is also provided for charging the slow start timing capacitor.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Section highlights the design of a boost preregulator for power factor correction. The boost power circuit design and the UC2854B integrated circuit which controls the converter. A complete design procedure is given which includes the tradeoffs necessary in the process. The design procedure is directly applicable to UC2854A/B as well as the UC2854.

9.2 Typical Application

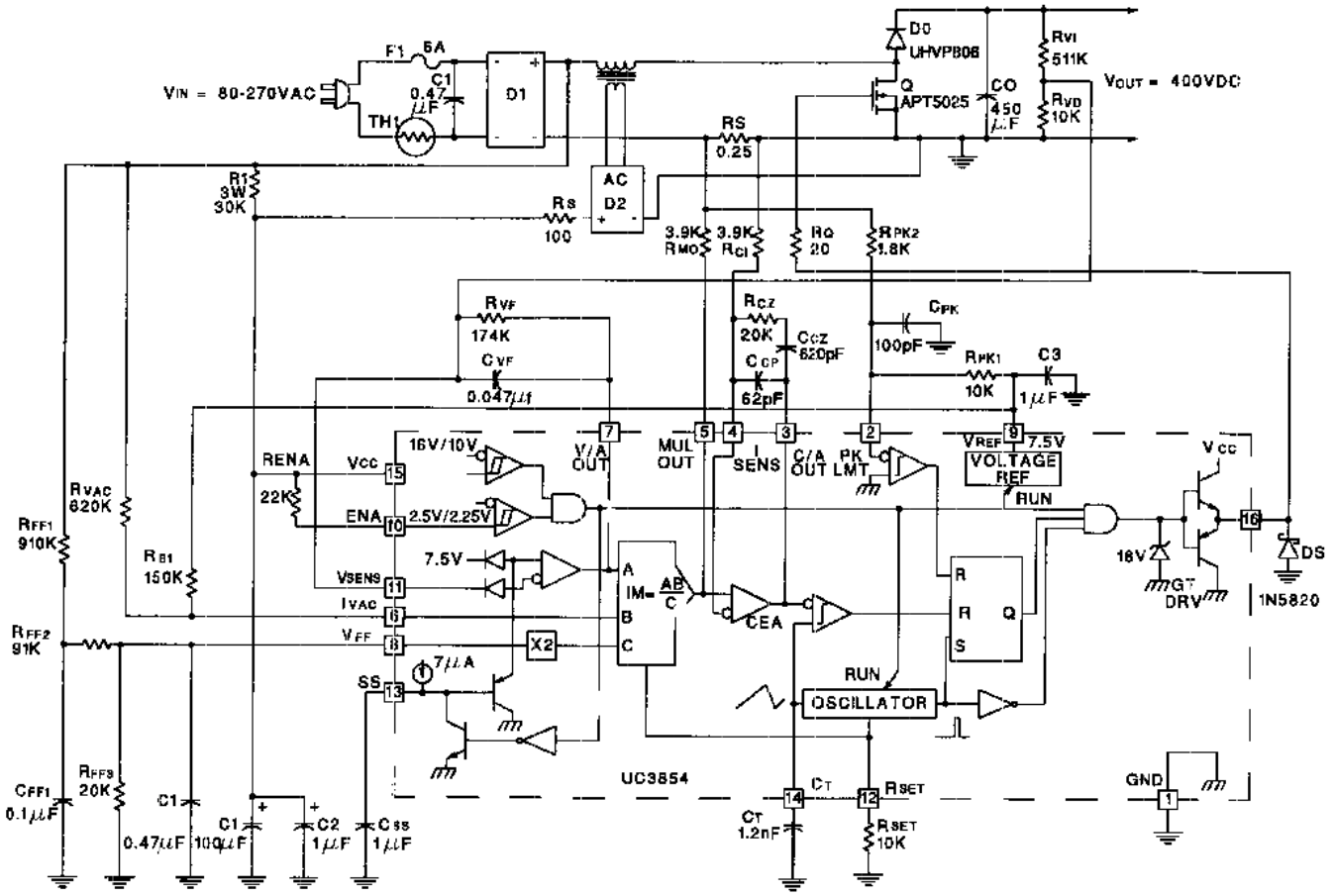


Figure 9. 250-W Power Factor Preregulator Schematic

9.2.1 Design Requirements

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency range must be specified. For the example circuit the specifications are:

- Maximum power output: 250 W
- Input voltage range: 80-270 Vac

Typical Application (continued)

- Line frequency range: 47-65 Hz

This defines a power supply which will operate almost anywhere in the world. The output voltage of a boost regulator must be greater than the peak of the maximum input voltage and a value 5% to 10% higher than the maximum input voltage is recommended so the output voltage is chosen to be 400 Vdc.

9.2.2 Detailed Design Procedure

9.2.2.1 Switching Frequency

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20 kHz to 300 kHz proves to be an acceptable compromise. The example converter uses a switching frequency of 100 kHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive. Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubbers for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very-high efficiency.

9.2.2.2 Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak current of the input sinusoid. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I_{line(pk)} = \frac{\sqrt{2} \times P}{V_{in(min)}} \tag{3}$$

For the example converter the maximum peak line current is 4.42 A at a V_{in} of 80Vac.

The maximum ripple current in a boost converter occurs when the duty factor is 50% which is also when the boost ratio M = V_o / V_{in} = 2. The peak value of inductor current generally does not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter. Figure 12 is a graph of the peak-to-peak ripple current in the inductor versus input voltage for the example converter.

The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. This is a somewhat arbitrary decision since this is usually not the maximum value of the high frequency ripple current. A larger value of ripple current will put the converter into the discontinuous conduction mode for a larger portion of the rectified line current cycle and means that the input filter must be larger to attenuate more high frequency ripple current. The UC3854, with average current mode control, allows the boost stage to move between continuous and discontinuous modes of operation without a performance change.

The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D at that input voltage and the switching frequency. The two equations necessary are given below:

$$D = \frac{V_O - Vin}{V_O} \tag{4}$$

$$L = \frac{V_{in} \times D}{f_s \times \Delta I} \tag{5}$$

where

- ΔI is the peak-to-peak ripple current.
- In the example 250-W converter:
  - D = 0.71
  - ΔI = 900 mA
  - L = 0.89 mH
- For convenience, the value of L is rounded up to 1.0 mH.

Typical Application (continued)

The high-frequency ripple current is added to the line current peak so the peak inductor current is the sum of peak line current and half of the peak-to-peak high frequency ripple current. The inductor must be designed to handle this current level. For our example the peak inductor current is 5.0 A. The peak current limit will be set about 10% higher at 5.5 A.

9.2.2.3 Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current. The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information.

The hold-up time of the output often dominates any other consideration in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up times of 15 to 50 ms are typical. In off-line power supplies with a 400 Vdc output the hold-up requirement generally works out to between 1 and 2 pF/W of output. In our 250-W example, the output capacitor is 450 pF. If hold-up is not required the capacitor will be much smaller, perhaps 0.2 pF/W, and then ripple current and ripple voltage are the major concern.

Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capacitance value in terms of the holdup time.

$$C_O = \frac{2 \times P_{out} \times \Delta t}{V_O^2 - V_{O(min)}^2}$$

where

- C_O is the output capacitor.
- P_{out} is the load power.
- Δt is the hold-up time
- V_o is the output voltage.
- $V_{o(min)}$ is the minimum voltage the load will operate at.
- For the example converter:
  - P_{out} is 250 W.
  - Δt is 64 ms.
  - V_O is 400 V.
  - $V_{O(min)}$ is 300 V.
  - So, C_o is 450 µF. (6)

9.2.2.4 Switch and Diode

The switch and diode must have ratings which are sufficient to ensure reliable operation. The switch must have a current rating at least equal to the maximum peak current in the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have some level of derating and this will vary depending on the application.

Typical Application (continued)

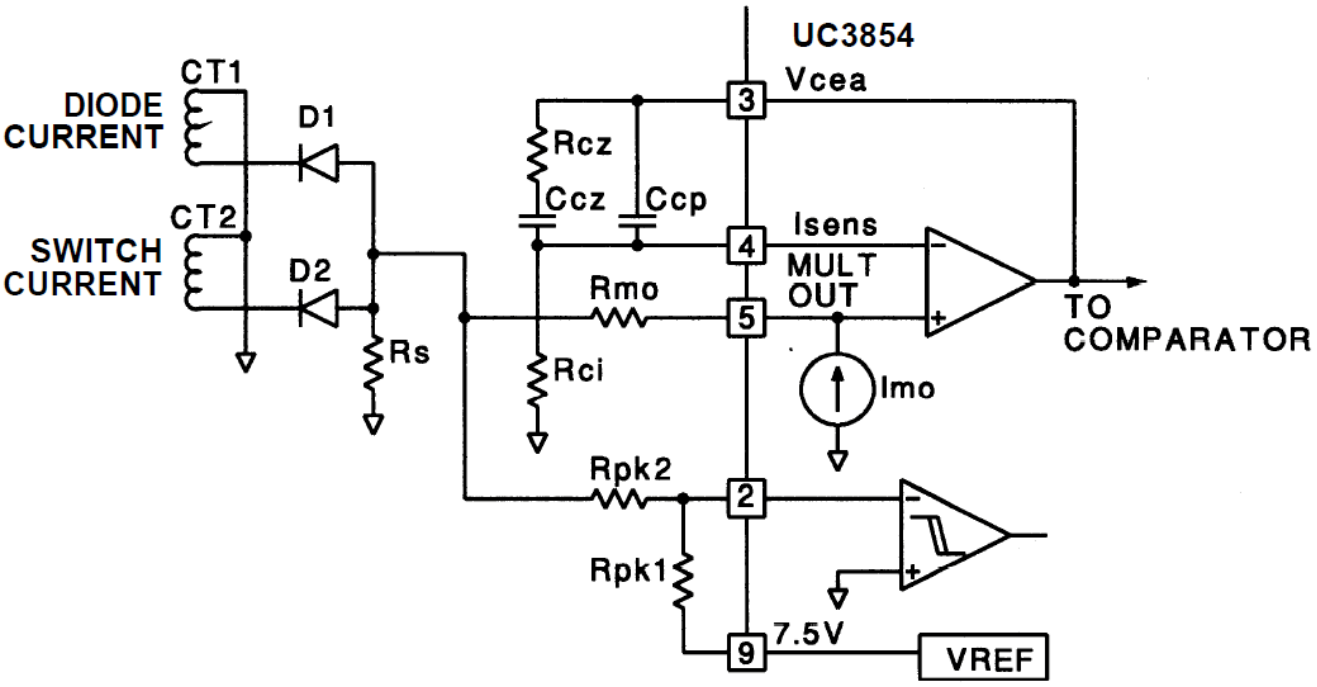


Figure 10. Current Transformers Used With Negative Output

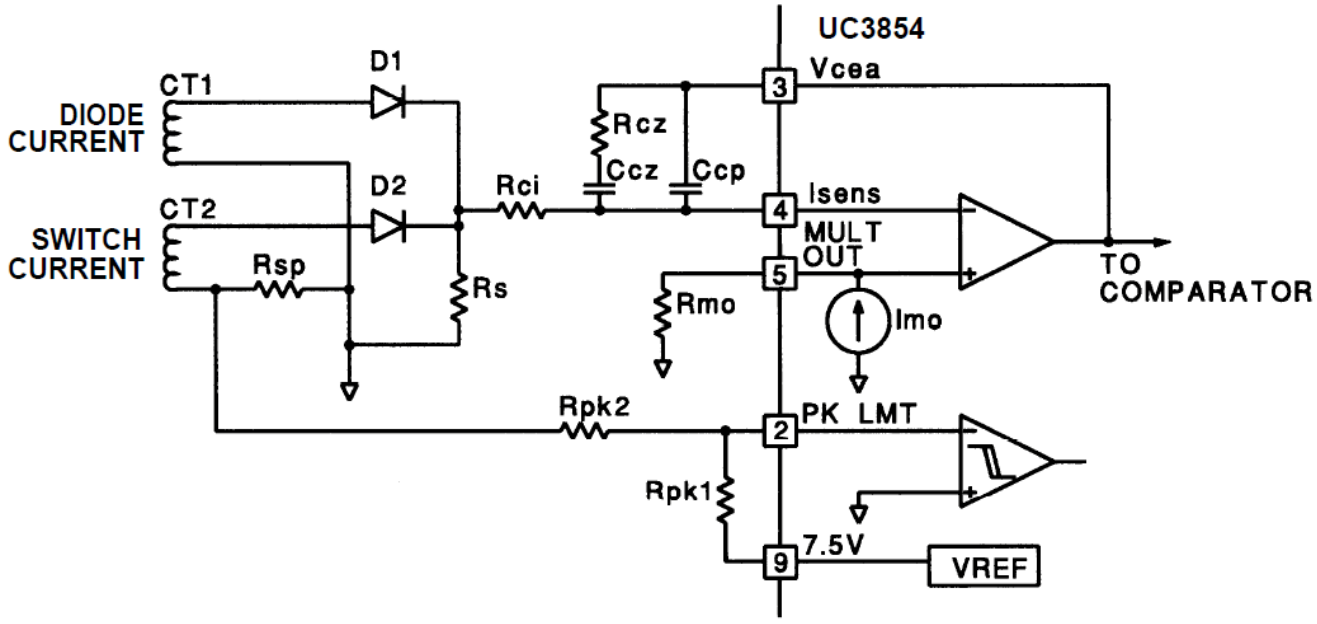


Figure 11. Current Transformers Used With Positive Output

Typical Application (continued)

For the example circuit the diode is a high speed, high voltage type with 35-ns reverse recovery, 600 Vdc breakdown, and 8-A forward current ratings. The power MOSFET in the example circuit has a 500 Vdc breakdown and 23 Adc current rating. A major portion of the losses in the switch are due to the turn-off current in the diode. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the example circuit was chosen for its fast turn off and the switch was oversized to handle the high peak power dissipation. A turn on snubber for the switch would have allowed a smaller switch and a slightly slower diode.

9.2.2.5 Current Sensing

There are two general methods for current sensing, a sense resistor in the ground return of the converter or two current transformers. The sense resistor is the least expensive method and is most appropriate at low power or current levels. The power dissipation in the resistor may become quite large at higher current levels and in that case the current transformers are more appropriate. Two current transformers are required, one for the switch current and one for the diode current, to produce an analog of the inductor current as is required for average current mode control. The current transformers must operate over a very-wide duty factor range and this can be difficult to achieve without saturating them. Current transformer operation is outside the scope of this paper but Unitrode has Design Note DN-41 which discusses the problem in some detail.

The current transformers may be configured for either a positive output voltage or a negative output voltage. In the negative output configuration, shown in Figure 10, the peak current limit on pin 2 of the UC3854 is easy to implement. In the positive output configuration, shown in Figure 11, this feature may be lost. It can be added back by putting another resistor in series with the ground leg of the current transformer which senses the switch current.

The configuration of the multiplier output and the current error amplifier are different depending on whether a resistor is used for current sensing or whether current transformers with positive output voltages are used for current sensing. Both work equally well and the configurations of the current error amplifier are shown in Figure 10 and Figure 11, respectively. The positive output current transformer configuration requires the inverting input to the integrator be connected to the sense resistor and the resistor at the output of the multiplier be connected to ground. (see Figure 11) The voltage at the output of the multiplier is not zero but is the programming voltage for the current loop and it will have the half sine wave shape which is necessary for the current loop.

The resistor current sense configuration is used in the example converter (Figure 9) so the inverting input to the current error amplifier (pin 4) is connected to ground through R_{ci}. The current error amplifier is configured as an integrator at low frequencies for average current mode control so the average voltage at the non-inverting input of the current error amplifier (pin 5, which it shares with the multiplier output) must be 0. The non-inverting input to the current error amplifier acts like a summing junction for the current control loop and adds the multiplier output current to the current from the sense resistor (which flows through the programming resistor R_{mo}). The difference controls the boost regulator. The voltage at the inverting input of the current error amplifier (pin 4) will be small at low frequencies because the gain at low frequencies is large. The gain at high frequencies is small so relatively large voltages at the switching frequency may be present. But, the average voltage on pin 4 must be 0 because it is connected through R_{ci} to ground.

The voltage across R_s, the current sense resistor in the example converter, goes negative with respect to ground so it is important to be sure that the pins of the UC3854 do not go below ground. The voltage across the sense resistor should be kept small and pins 2 and 5 should be clamped to prevent their going negative. A peak value of 1 V or so across the sense resistor provides a signal large enough to have good noise margin but which is small enough to have low power dissipation. There is a great deal of flexibility in choosing the value of the sense resistor. A 0.25-Ω resistor was chosen for R_s in the example converter and at the worst case peak current of 5.6 A gives a maximum voltage of 1.40-V peak.

9.2.2.6 Peak Current Limit

The peak current limit on the UC3854 turns the switch off when the instantaneous current through it exceeds the maximum value and is activated when pin 2 is pulled below ground. The current limit value is set by a simple voltage divider from the reference voltage to the current sense resistor. The equation for the voltage divider is given as follows:

Typical Application (continued)

$$R_{pk2} = \frac{V_{rs} \times R_{pk1}}{V_{ref}}$$

where

- R_{pk1} and R_{pk2} are the resistors of the voltage divider.
- V_{ref} is 7.5 V on the UC3854.
- V_{rs} is the voltage across the sense resistor R_s at the current limit point. (7)

The current through R_{pk2} should be around 1 mA. The peak current limit in the example circuit is set at 5.4 A with an R_{pk1} of 10 kΩ and R_{pk2} of 1.8 kΩ. A small capacitor, C_{pk}, has been added to give extra noise immunity when operating at low line and this also increases the current limit slightly.

9.2.2.7 Multiplier Set-up

The multiplier/divider is the heart of the power factor corrector. The output of the multiplier programs the current loop to control the input current to give a high power factor. The output of the multiplier is therefore a signal which represents the input line current.

Unlike most design tasks where the design begins at the output and proceeds to the input the design of the multiplier circuits must begin with the inputs. There are three inputs to the multiplier circuits: the programming current I_{ac} (pin 6) the feedforward voltage V_{ff} from the input (pin 8) and the voltage error amplifier output voltage V_{vea} (pin 7). The multiplier output current is Imo (pin 5) and it is related to the three inputs by the following equation:

$$I_{mo} = \frac{K_m \times I_{ac} \times (V_{vea} - 1)}{V_{ff}^2}$$

where

- Km is a constant in the multiplier and is equal to 1.0
- Iac is the programming current from the rectified input voltage
- Vvea is the output of the voltage error amplifier
- Vff is the feedforward voltage. (8)

9.2.2.8 Feedforward Voltage

V_{ff} is the input to the squaring circuit and the UC3854 squaring circuit generally operates with a V_{ff} range of 1.4 to 4.5 V. The UC3854 has an internal clamp which limits the effective value of V_{ff} to 4.5 V even if the input goes above that value. The voltage divider for the V_{ff} input has three resistors (R_{ff1}, R_{ff2}, and R_{ff3} – see Figure 9) and two capacitors (C_{ff1} and C_{ff2}) and so it filters as well as providing two outputs. The resistors and capacitors of the divider form a second order low pass filter so the DC output is proportional to the average value of the input half sine wave. The average value is 90% of the RMS value of a half sine wave. If the RMS value of the AC input voltage is 270 Vac the average value of a half sine will be 243 Vdc and the peak will be 382 V.

The V_{ff} voltage divider has two DC conditions to meet. At high- input line voltage V_{ff} should not be greater than 4.5 V. At this voltage the V_{ff} input clamps so the feedforward function is lost. The voltage divider should be set up so that V_{ff} is equal to 1.414 V when V_{in} is at its low line value and the upper node of the voltage divider, V_{ffc}, should be about 7.5 V. This allows V_{ff} to be clamped as described in Unitrode Design Note DN-39B. There is an internal current limit which holds the multiplier output constant if the V_{ff} input goes below 1.414 V. The V_{ff} input should always be set up so that V_{ff} is equal to 1.414 V at the minimum input voltage. This may cause V_{ff} to clip on the high end of the input voltage range if there is an extremely wide AC line voltage input range. However, it is preferable to have V_{ff} clip at the high end rather than to have the multiplier output clip on the low end of the range. If V_{ff} clips the voltage loop gain will change but the effect on the overall system will be small whereas the multiplier clipping will cause large amounts of distortion in the input current waveform.

The example circuit uses the UC3854 so the maximum value of V_{ff} is 4.5 V. If R_{ff1}, the top resistor of the divider, is 910 kΩ and R_{ff2}, the middle resistor, is 91 kΩ and R_{ff3}, the bottom resistor, is 20 kΩ the maximum value of V_{ff} will be 4.76 V when the input voltage is 270 Vac RMS and the DC average value will be 243 V. When the input voltage is 80 Vac RMS the average value is 72 V and V_{ff} is 1.41 Vdc. Also at V_{in} = 80 Vac the voltage at the upper node on the voltage divider, V_{ffc}, will be 7.83 V. Note that the high end of the range goes above 4.5 V so that the low end of the range will not go below 1.41 V.

Typical Application (continued)

The output of the voltage error amplifier is the next piece of the multiplier setup. The output of the voltage error amplifier, V_{vea}, is clamped inside the UC3854 at 5.6 V. The output of the voltage error amplifier corresponds to the input power of the converter. The feedforward voltage causes the power input to remain constant at given V_{vea} voltage regardless of line voltage changes. If 5.0 V is established as the maximum normal operating level then 5.6 V gives an overload power limit which is 12% higher.

The clamp on the output of the voltage error amplifier is what sets the minimum value of V_{ff} at 1.414 V. This can be seen by plugging these values into the equation for the multiplier output current given above. When V_{ff} is large the inherent errors of the multiplier are magnified because V_{vea}/V_{ff} becomes small. If the application has a wide input voltage range and if a very-low harmonic distortion is required then V_{ff} may be changed to the range of 0.7 to 3.5 V. To do this an external clamp **must** be added to the voltage error amplifier to hold its output below 2.00 V. In general, however, this is not a recommended practice.

9.2.2.9 Multiplier Input Current

The operating current for the multiplier comes from the input voltage through R_{vac}. The multiplier has the best linearity at relatively high currents, but the recommended maximum current is 0.6 mA. At high line the peak voltage for the example circuit is 382 Vdc and the voltage on pin 6 of the UC3854 is 6.0 Vdc. A 620 kΩ value for R_{vac} will give an lac of 0.6-mA maximum. For proper operation near the cusp of the input waveform when V_{in} = 0 a bias current is needed because pin 6 is at 6.0 Vdc. A resistor, R_{b1}, is connected from V_{ref} to pin 6 to provide the small amount of bias current needed. R_{b1} is equal to R_{vac} / 4. In the example circuit, a value of 150 kΩ for R_{b1} will provide the correct bias.

The maximum output of the multiplier occurs at the peak of the input sine wave at low line. The maximum output current from the multiplier can be calculated from the equation for I_{mo}, given above, for this condition. The peak value of I_{ac} will be 182 µA when V_{in} is at low line. V_{vea} will be 5.0 V and V_{ff} will be 2.0. Imo will then be 365 µA maximum. I_{mo} may not be greater than twice lac so this represents the maximum current available at this input voltage and the peak input current to the power factor corrector will be limited accordingly.

The I_{set} current places another limitation on the multiplier output current. I_{mo} may not be larger than 3.75 / R_{set}. For the example circuit this gives R_{set} = 10.27 kΩ maximum so a value of 10 kΩ is chosen.

The current out of the multiplier, Imo, must be summed with a current proportional to the inductor current to close the voltage feedback loop. R_{mo}, a resistor from the output of the multiplier to the current sense resistor, performs the function and the multiplier output pin becomes the summing junction. The average voltage on pin 5 will be 0 under normal operation but there will be switching frequency ripple voltage which is amplitude modulated at twice the line frequency. The peak current in the boost inductor is to be limited to 5.6 A in the example circuit and the current sense resistor is 0.25 Ω so the peak voltage across the sense resistor is 1.4 V. The maximum multiplier output current is 365 µA so the summing resistor, R_{mo}, must be 3.84 kΩ and a 3.9-kΩ resistor is chosen.

9.2.2.10 Oscillator Frequency

The oscillator charging current is I_{set} and is determined by the value of R_{set} and the oscillator frequency is set by the timing capacitor and the charging current. The timing capacitor is determined from:

$$C_t = \frac{1.25}{R_{set} \times f_s} \quad (9)$$

where

- C_t is the value of the timing capacitor
- f_s is the switching frequency in Hertz.

For the example converter:

- f_s is 100 kHz and R_{set} is 10K so C_t is 0.00125 pF.

9.2.2.11 Current Error Amplifier Compensation

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sense resistor (R_s) forming a low pass filter. The equation for the control to input current transfer function is:

Typical Application (continued)

$$\frac{V_{rs}}{V_{cea}} = \frac{V_{out} \times R_S}{V_S \times s_L}$$

where

- V_{rs} is the voltage across the input current sense resistor
- V_{cea} is the output of the current error amplifier.
- V_{out} is the DC output voltage
- V_s is the peak-to-peak amplitude of the oscillator ramp
- s_L is the impedance of the boost inductor (also jwL)
- R_s is the sense resistor (with a current transformer it will be R_s / N) (10)

This equation is only valid for the region of interest between the resonant frequency of the filter (LC_o) and the switching frequency. Below resonance the output capacitor dominates and the equation is different.

The compensation of the current error amplifier provides flat gain near the switching frequency and uses the natural roll off of the boost power stage to give the correct compensation for the total loop. A zero at low frequency in the amplifier response gives the high gain which makes average current mode control work. The gain of the error amplifier near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator. These two signals are the inputs of the PWM comparator in the UC3854.

The downslope of the inductor current has the units of amps per second and has a maximum value when the input voltage is zero. In other words, when the voltage differential between the input and output of the boost converter is greatest. At this point (V_{in} = 0) the inductor current is given by the ratio of the converter output voltage and the inductance (V_o / L). This current flows through the current sense resistor R_s and produces a voltage with the slope V_oR_s / L (with current sense transformers it will be V_oR_s/NL). This slope, multiplied by the gain of the current error amplifier at the switching frequency, must be equal to the slope of the oscillator ramp (also in volts per second) for proper compensation of the current loop. If the gain is too high the slope of the inductor current will be greater than the ramp and the loop can go unstable. The instability will occur near the cusp of the input waveform and will disappear as the input voltage increases.

The loop crossover frequency can be found from the above equation if the gain of the current error amplifier is multiplied with it and it is set equal to one. Then rearrange the equation and solve for the crossover frequency. The equation becomes:

$$f_{ci} = \frac{V_{out} \times R_S \times R_{CZ}}{V_S \times 2\pi L \times R_{ci}}$$

where

- f_{ci} is the current loop crossover frequency
- R_{cz} / R_{ci} is the gain of the current error amplifier. (11)

This procedure will give the best possible response for the current loop.

In the example converter the output voltage is 400 Vdc and the inductor is 1.0mH so the down slope of inductor current is 400 mA/µs. The current sense resistor is 0.25 Ω so the input to the current error amplifier is 100 mV/µs. The oscillator ramp of the UC3854 has a peak to peak value of 5.2 V and the switching frequency is 100 kHz so the ramp has a slope of 0.52 V/µs. The current error amplifier must have a gain of 5.2 at the switching frequency to make the slopes equal. With an input resistor (R_{ci}) value of 3.9K the feedback resistance (R_{cz}) is 20K to give the amplifier a gain of 5.2. The current loop crossover frequency is 15.9 kHz.

The placement of the zero in the current error amplifier response must be at or below the crossover frequency. If it is at the crossover frequency the phase margin will be 45°. If the zero is lower in frequency the phase margin will be greater. A 45° phase margin is very stable, has low overshoot and has good tolerance for component variations. The zero must be placed at the crossover frequency so the impedance of the capacitor at that frequency must be equal to the value of R_{cz}. The equation is: C_{cz} = 1 / (271 × f_{ci} × R_{cz}). The example converter has R_{cz} = 20K and f_{ci} = l5.9 kHz so C_{cz} = 500 pF. A value of 620 pF was chosen to give a little more phase margin.

Typical Application (continued)

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. If the pole is above half the switching frequency the pole will not affect the frequency response of the control loop. The example converter uses a 62-pF capacitor for C_{cp} which gives a pole at 128 kHz. This is actually above the switching frequency so a larger value of capacitor could have been used but 62 pF is adequate in this case.

9.2.2.12 Voltage Error Amplifier Compensation

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The loop bandwidth must be low enough to attenuate the second harmonic of the line frequency on the output capacitor to keep the modulation of the input current small. The voltage error amplifier must also have enough phase shift so that what modulation remains will be in phase with the input line to keep the power factor high.

The basic low frequency model of the output stage is a current source driving a capacitor. The power stage and the current feedback loop compose the current source and the capacitor is the output capacitor. This forms an integrator and it has a gain characteristic which rolls off at a constant 20 dB per decade rate with increasing frequency. If the voltage feedback loop is closed around this it will be stable with constant gain in the voltage error amplifier. This is the technique which is used to stabilize the voltage loop. However, its performance at reducing distortion due to the second harmonic output ripple is miserable. A pole in the amplifier response is needed to reduce the amplitude of the ripple voltage and to shift the phase by 90°. The distortion criteria is used to define the gain of the voltage error amplifier at the second harmonic of the line frequency and then the unity gain crossover frequency is found and is used to determine the pole location in the voltage error amplifier frequency response.

The first step in designing the voltage error amplifier compensation is to determine the amount of ripple voltage present on the output capacitor. The peak value of the second harmonic voltage is given by:

$$V_{opk} = \frac{P_{in}}{2\pi f_r \times C_O \times V_O}$$

where

- V_{opk} is the peak value of the output ripple voltage (the peak to peak value will be twice this)
- f_r is the ripple frequency which is the second harmonic of the input line frequency
- C_o is the value of the output capacitance and V_O is the DC output voltage. (12)

The example converter has a peak ripple voltage of 1.84 Vpk. The amount of distortion which the ripple contributes to the input must be decided next. This decision is based on the specification for the converter. The example converter is specified for 3% THD so 0.75% THD is allocated to this component. This means that the ripple voltage at the output of the voltage error amplifier is limited to 1.5%. The voltage error amplifier has an effective output range (ΔV_{vea}) of 1.0 to 5.0 V so the peak ripple voltage at the output of the voltage error amplifier is give by $V_{vea(pk)}$ = %Ripple × ΔV_{vea}. The example converter has a peak ripple voltage at the output of the voltage error amplifier of 60mVpk.

The gain of the voltage error amplifier, G_{va}, at the second harmonic ripple frequency is the ratio of the two values given above. The peak ripple voltage allowed on the output of the voltage error amplifier is divided by the peak ripple voltage on the output capacitor. For the example converter G_{va} is 0.0326.

The criteria for the choice of R_{vi}, the next step in the design process, are reasonably vague. The value must be low enough so that the operational amplifier bias currents will not have a large effect on the output and it must be high enough so that the power dissipation is small. In the example converter a 511-kΩ resistor was chosen for R_{vi} and it will have power dissipation of about 300 mW.

C_{vf}, the feedback capacitor sets the gain at the second harmonic ripple frequency and is chosen to give the voltage error amplifier the correct gain at the second harmonic of the line frequency. The equation is simply:

$$C_{vf} = \frac{1}{2\pi f_r \times R_{vi} \times G_{va}} \quad (13)$$

The example converter has a C_{vf} value of 0.08 µF. If this value is rounded down to C_{vf} = 0.O47pF the phase margin will be a little better with only a little more distortion so this value was chosen.

Typical Application (continued)

The output voltage is set by the voltage divider R_{vi} and R_{vd}. The value of R_{vi} is already determined so R_{vd} is found from the desired output voltage and the reference voltage which is 7.50Vdc. In the example R_{vd} = 10 kΩ will give an output voltage of 390 Vdc. This could be trimmed up to 400VDC with a 414-kΩ resistor in parallel with Rvd but for this application 390 Vdc is acceptable. R_{vd} has no effect on the AC performance of the active power factor corrector. Its only effect is to set the DC output voltage.

The frequency of the pole in the voltage error amplifier can be found from setting the gain of the loop equation equal to one and solving for the frequency. The voltage loop gain is the product of the error amplifier gain and the boost stage gain, which can be expressed in terms of the input power. The multiplier, divider and squarer terms can all be lumped into the power stage gain and their effect is to transform the output of the voltage error amplifier into a power control signal as was noted earlier. This allows us to express the transfer function of the boost stage simply in terms of power. The equation is:

$$G_{bst} = \frac{P_{in} \times X_{CO}}{\Delta V_{vea} \times V_O}$$

where

- G_{bst} is the gain of the boost stage including the multiplier, divider and squarer
- P_{in} is the average input power
- X_{CO} is the impedance of the output capacitor
- ΔV_{vea} is the range of the voltage error amplifier output voltage (4 V on the UC3854)
- V_O is the DC output voltage. (14)

The gain of the error amplifier above the pole in its frequency response is given by:

$$G_{va} = \frac{X_{cf}}{R_{vi}}$$

where

- G_{va} is the gain of the voltage error amplifier
- X_{cf} is the impedance of the feedback capacitance
- R_{vi} is the input resistance. (15)

The gain of the total voltage loop is the product of G_{bst} and G_{va} and is given by the this equation:

$$G_v = \frac{P_{in} \times X_{co} \times X_{cf}}{\Delta V_{vea} \times V_O \times R_{vi}} \quad (16)$$

Note that there are two terms which are dependent on f, X_{co}, and X_{cf}. This function has a second order slope (–40 dB per decade) so it must be a function of frequency squared. To solve for the unity gain frequency set G_v equal to one and rearrange the equation to solve for f_{vi}. X_{co} is replaced with 1 / ($2\pi f_r \times R_{vi} \times G_{va}$) and X_{cf} is replaced with 1 / ($2\pi f_r C_{vf}$).

The equation becomes:

$$f_{vi}^2 = \frac{P_{in}}{\Delta V_{vea} \times V_O \times R_{vi} \times C_O \times C_{vf} \times (2\pi)^2} \quad (17)$$

Solving for f_{vi} in the example converter gives f_{vi} = 19.14 Hz. The value of R_{vf} can now be found by setting it equal to the impedance of C_{vf} at f_{vi}. The equation is: R_{vf} = 1 I($2\pi f_{vi} C_{vf}$).

In the example converter a value of 177K is calculated and 174K is used.

9.2.2.13 Feedforward Voltage Divider Filter Capacitors

The percentage of second harmonic ripple voltage on the feedforward input to the multiplier results in the same percentage of third harmonic ripple current on the AC line. The capacitors in the feedforward voltage divider (C_{ff1} and C_{ff2}) attenuate the ripple voltage from the rectified input voltage. The second harmonic ripple is 66.2% of the input AC line voltage. The amount of attenuation required, or the *gain* of the filter, is simply the amount of third harmonic distortion allocated to this distortion source divided by 66.2% which is the input to the divider. The example circuit has an allocation of 1.5% total harmonic distortion from this input so the required attenuation is G_{ff} = 1.5 / 66.2 = 0.0227.

Typical Application (continued)

The recommended divider string implements a second order filter because this gives a much faster response to changes in the RMS line voltage. Typically, it is about six times faster. The two poles of the filter are placed at the same frequency for the widest bandwidth. The total gain of the filter is the product of the gain of the two filter section so the gain of each section is the square root of the total gain. The two sections of the filter do not interact much because the impedances are different so they can be treated separately. In the example converter the gain of each filter section at the second harmonic frequency is 0.0227 or 0.15 for each section. This same relationship holds for the cutoff frequency which is needed to find the capacitor values. These are simple real poles so the cutoff frequency is the section gain times the ripple frequency or:

$$f_p = \sqrt{G_{ff}} \times f_r \tag{18}$$

The example converter has a filter gain of 0.0227 and a section gain of 0.15 and a ripple frequency of 120 Hz so the cutoff frequency is $f_c = 0.15 \times 120 = 18$ Hz.

The cutoff frequency is used to calculate the values for the filter capacitors since, in this application, the impedance of the capacitor will equal the impedance of the load resistance at the cutoff frequency. The two equations given below are used to calculate the two capacitor values.

$$C_{ff1} = \frac{1}{2\pi \times f_p \times R_{ff2}} \tag{19}$$

$$C_{ff2} = \frac{1}{2\pi \times f_p \times R_{ff3}} \tag{20}$$

In the example converter R_{ff2} is 91 kΩ and R_{ff3} is 20 kΩ; so,

$C_{ff1} = ½\pi \times 18 \times 19k = 0.1\ \mu F$ (21)

$C_{ff2} = ½\pi \times 18 \times 20k = 0.44\ \mu F$ (22)

so choose $C_{ff2} = 0.47\ \mu F$

This completes the design of the major circuits of an active power factor corrector.

9.2.2.14 Design Procedure Summary

This section contains a brief, step-by-step summary of the design procedure for an active power factor corrector. The example circuit used above is repeated here.

1. Specifications: Determine the operating requirements for the active power factor corrector.

   Example:
   - Pout (max): 250 W
   - Vin range: 80 to 270 Vac
   - Line frequency range: 47 to 65 Hz
   - Output voltage: 400 Vdc
2. Select switching frequency:

   Example: 100 kHz
3. Inductor selection:

   (a) Maximum peak line current. $P_{in} = P_{out(max)}$

   $$I_{pk} = \frac{\sqrt{2} \times P_{in}}{V_{in(min)}} \tag{23}$$

   Example: $I_{pk} = 1.41 \times 250 / 80 = 4.42$ A

   (b) Ripple current.

   $$\Delta I = 0.2 \times I_{pk} \tag{24}$$

   Example: $\Delta I = 0.2 \times 4.42 = 0.2 \times 4.42 = 0.9$ A peak-to-peak

   (c) Determine the duty factor at I_{pk} where $V_{in(peak)}$ is the peak of the rectified line voltage at low line.

   $$D = \frac{V_O - V_{in(peak)}}{V_O} \tag{25}$$

Typical Application (continued)

Example: D = (400 – 113) / 400 = 0.71

(d) Calculate the inductance. f_S is the switching frequency.

$$L = \frac{V_{in} \times D}{f_S \times \Delta I} \tag{26}$$

Example:

L = (1113 × 0.71) / (100000 × 0.9) = 0.89 mH

Round up to 1.0 mH.

4. Select output capacitor. With hold-up time, use the equation below. Typical values for C_o are 1 µF to 2 µF per watt. If hold-up is not required use the second harmonic ripple voltage and total capacitor power dissipation to determine minimum size of the capacitor. At is the hold-up time in seconds and V_1 is the minimum output capacitor voltage.

$$C_O = \frac{2 \times P_{out} \times \Delta t}{V_O^2 - V_1^2} \tag{27}$$

Example:

$$C_O = (2 \times 250 \times 34\ \mu s) / (400 - 350) = 450\ \mu F \tag{28}$$

5. Select current sensing resistor. If current transformers are used then include the turns ratio and decide whether the output will be positive or negative relative to circuit common. Keep the peak voltage across the resistor low. 1.0 V is a typical value for V_{rs}.

(a) Find

$$T_{lpk(max)} = I_{pk} + \Delta I / 2 \tag{29}$$

Example: $I_{pk(max)} = 4.42 + 0.45 \approx 5.0$ A peak

(b) Calculate sense resistor value.

$$R_S = \frac{V_{rs}}{I_{pk(max)}} \tag{30}$$

Example: $R_S = 1.0 / 5.0 = 0.20\ \Omega$. Choose 0.25 Ω

(c) Calculate the actual peak sense voltage. $V_{rs(pk)} = I_{pk(max)} \times R_S$

Example: $V_{rs(pk)} = 5.0 \times 0.25 = 1.25$ V

6. Set independent peak current limit. R_{pk1} and R_{pk2} are the resistors in the voltage divider. Choose a peak current overload value, $I_{pk(ovld)}$. A typical value for R_{pk1} is 10 kΩ.

$V_{rs(ovld)} = I_{pk(olvd)} \times R_S$

Example: $V_{rs(ovld)} = 5.6 \times 0.25 = 1.4$ V

$$R_{pk2} = \frac{V_{rs(ovld)} \times R_{pk1}}{V_{ref}} \tag{31}$$

Example: $R_{pk2} = (1.4 \times 10k\Omega) / 7.5 = 1.87\ k\Omega$. Choose 1.8 kΩ

7. Multiplier setup. The operation of the multiplier is given by the following equation. Imo is the multiplier output current, $K_m = 1$, I_{ac} is the multiplier input current, V_{ff} is the feedforward voltage and V_{vea} is the output of the voltage error amplifier.

$$I_{mo} = \frac{K_m \times I_{ac} \times (V_{vea} - 1)}{V_{ff}^2} \tag{32}$$

(a) Feedforward voltage divider. Change V_{in} from RMS voltage to average voltage of the rectified input voltage. At $V_{in(min)}$ the voltage at V_{ff} should be 1.414 V and the voltage at V_{ffc}, the other divider node, should be about 7.5 V. The average value of V_{in} is given by the following equation where $V_{in(min)}$ is the RMS value of the AC input voltage:

$$V_{in(av)} = V_{in(min)} \times 0.9 \tag{33}$$

Typical Application (continued)

The following two equations are used to find the values for the V_{ff} divider string. A value of 1 MΩ is usually chosen for the divider input impedance. The two equations must be solved together to get the resistor values.

$$V_{ff} = 1.414\ V = \frac{V_{in(av)} \times R_{ff3}}{R_{ff1} + R_{ff2} + R_{ff3}} \tag{34}$$

$$V_{node} = 7.5\ V = \frac{V_{in(av)} \times (R_{ff2} + R_{ff3})}{R_{ff1} + R_{ff2} + R_{ff3}} \tag{35}$$

Example: R_{ff1} = 910 kΩ, R_{ff2} = 91 kΩ, and R_{ff3} = 20 kΩ

(b) R_{vac} selection. Find the maximum peak line voltage.

$$V_{pk(max)} = \sqrt{2} \times V_{in(max)} \tag{36}$$

Example: $V_{pk(max)} = 1.414 \times 270 = 382V_{pk}$

Divide by 600 µA, the maximum multiplier input current.

$$R_{vac} = \frac{V_{pk(max)}}{600E-6} \tag{37}$$

Example: $R_{vac} = (382) / 6e^{-4}$ = 637 kΩ. Choose 620 kΩ.

(c) R_{b1} selection. This is the bias resistor. Treat this as a voltage divider with V_{ref} and R_{vac} and then solve for R_{b1}. The equation becomes:

$$R_{b1} = 0.25\ R_{vac}$$

Example: $R_{b1} = 0.25R_{vac}$ = 155 kΩ. Choose 150 kΩ.

(d) R_{set} selection. I_{mo} cannot be greater than twice the current through R_{set}. Find the multiplier input current, I_{ac}, with $V_{in(min)}$. Then calculate the value for R_{set} based on the value of I_{ac} just calculated.

$$I_{ac(min)} = \frac{V_{in(pk)}}{R_{vac}} \tag{38}$$

Example:

$$R_{set} = \frac{3.75}{2 \times I_{ac(min)}} \tag{39}$$

Example:

$$R_{set} = \frac{3.75\ V}{2 \times 182\ \mu A} = 10.3\ k\Omega \tag{40}$$

Choose 10 kΩ.

(e) R_{mo} selection. The voltage across R_{mo} must be equal to the voltage across R_S at the peak current limit at low line input voltage.

$$R_{mo} = \frac{V_{rs(pk)} \times 1.12}{2 \times I_{ac(min)}} \tag{41}$$

Example: $R_{mo} = (l.25 \times 1.12) / (2 \times 182e^{-6})$ = 3.84 kΩ.

Choose 3.9 kΩ.

8. Oscillator frequency. Calculate C_t to give the desired switching frequency.

$$C_t = \frac{1.25}{R_{set} \times f_s} \tag{42}$$

Example:

$$C_t = \frac{1.25}{10k \times 100k} = 1.25\ nF \tag{43}$$

9. Current error amplifier compensation.

Typical Application (continued)

(a) Amplifier gain at the switching frequency. Calculate the voltage across the sense resistor due to the inductor current downslope and then divide by the switching frequency. With current transformers substitute (R_S / N) for R_S. The equation is:

$$\Delta V_{rs} = \frac{V_O \times R_S}{L \times f_S} \quad (44)$$

Example:

$$\Delta V_{rs} = \frac{400 \times 0.25}{0.001} = \frac{400 \times 0.25}{0.001 \times 100000} = 1.0\ V_{pk} \quad (45)$$

This voltage must equal the peak to peak amplitude of V_S, the voltage on the timing capacitor (5.2 V). The gain of the error amplifier is therefore given by:

$$G_{ca} = \frac{V_S}{\Delta V_{rs}} \quad (46)$$

Example: G_{ca} = 5.2 / 1.0 = 5.2

(b) Feedback resistors. Set R_{ci} equal to R_{mo}.

$R_{ci} = R_{mo}$

$R_{cz} = G_{ca} \times R_{ci}$

Example: R_{cz} = 5.2 × 3.9 kΩ =20 kΩ

(c) Current loop crossover frequency.

$$f_{ci} = \frac{V_{out} \times R_S \times R_{cz}}{V_S \times 2\pi L \times R_{ci}} \quad (47)$$

Example:

$$f_{ci} = \frac{400 \times 0.25 \times 20k}{5.2 \times 2\pi \times 0.001} = 15.7\ kHz \quad (48)$$

(d) C_{cz} selection. Choose a 45° phase margin. Set the zero at the loop crossover frequency.

$$C_{cz} = \frac{1}{2\pi \times f_{ci} \times R_{cz}} \quad (49)$$

Example:

$$C_{cz} = \frac{1}{2\pi \times 15.7k \times 20k} = 507\ pF \quad (50)$$

Choose 620 pF

(e) C_{cp} selection. The pole must be above f_S / 2.

$$C_{cp} = \frac{1}{2\pi \times f_S \times R_{cz}} \quad (51)$$

Example:

$$C_{cp} = \frac{1}{2\pi \times 1 \times 100k \times 20k} = 80\ pF \quad (52)$$

Choose 62 pF.

10. Harmonic distortion budget. Decide on a maximum THD level. Allocate THD sources as necessary. The predominant AC line harmonic is third. Output voltage ripple contributes 1/2% third harmonic to the input current for each 1% ripple at the second harmonic on the output of the error amplifier. The feedforward voltage, V_{ff}, contributes 1% third harmonic to the input current for each 1% second harmonic at the V_{ff} input to the UC3854.

Example:

3% third harmonic AC input current is chosen as the specification. 1.5% is allocated to the V_{ff} input and 0.75% is allocated to the output ripple voltage or 1.5% to V_{vao}. The remaining 0.75% is allocated to miscellaneous nonlinearities.

Typical Application (continued)

11. Voltage error amplifier compensation.

(a) Output ripple voltage. The output ripple is given by the following equation where f_r is the second harmonic ripple frequency:

$$V_{o(pk)} = \frac{P_{in}}{2\pi f_r \times C_O \times V_O} \quad (53)$$

Example:

$$V_{o(pk)} = \frac{250}{2\pi \times 120 \times 450E-6 \times 400} = 1.84\ V_{ac} \quad (54)$$

(b) Amplifier output ripple voltage and gain. $V_{o(pk)}$ must be reduced to the ripple voltage.

$$G_{va} = \frac{\Delta V_{vao} \times \%Ripple}{V_{o(pk)}} \quad (55)$$

For the UC3854 V_{vao} is 5 – 1 = 4 V

Example:

$$G_{va} = (4 \times 0.015) / 1.84 = 0.0326 \quad (56)$$

(c) Feedback network values. Find the component values to set the gain of the voltage error amplifier. The value of R_{vi} is reasonably arbitrary.

Example: Choose R_{vi} = 511 kΩ.

$$C_{vf} = \frac{1}{2\pi \times f_r \times R_{vi} \times G_{va}} \quad (57)$$

Example:

$$C_{vf} = \frac{1}{2\pi \times 120 \times 511k \times 0.0326} = 0.08\ \mu F \quad (58)$$

Choose 0.047 µF.

(d) Set DC output voltage.

$$R_{vd} = \frac{R_{vi} \times V_{ref}}{V_O - V_{ref}} \quad (59)$$

Example:

$$Rvd = \frac{511k \times 7.5}{400 \times 7.5} = 9.76k \quad (60)$$

Choose 10.0 kΩ.

(e) Find pole frequency. f_{vi} = unity gain frequency of voltage loop.

$$f_{vi}^2 = \frac{P_{in}}{\Delta V_{vao} \times V_O \times R_{vi} \times C_O \times C_{vf} \times (2\pi)^2} \quad (61)$$

Example:

$$fvi = \sqrt{\frac{250}{4 \times 400 \times 511k \times 450E-6 \times 47E-9 \times 39.5}} = 19.1\,Hz \quad (62)$$

(f) Find R_{vf}.

$$R_{vf} = \frac{1}{2\pi \times f_{vi} \times C_{vf}} \quad (63)$$

Example:

$$R_{vf} = \frac{1}{2\pi \times 19.1 \times 47E-9} = 177\ k\Omega \quad (64)$$

Choose 174 kΩ.

Typical Application (continued)

12. Feedforward voltage divider capacitors. These capacitors determine the contribution of Vff to the third harmonic distortion on the AC input current. Determine the amount of attenuation needed. The second harmonic content of the rectified line voltage is 66.2%. %THD is the allowed percentage of harmonic distortion budgeted to this input from step 10.

$$G_{ff} = \frac{\%THD}{66.2\%} \quad (65)$$

Example:

G_{ff} = 1.5 / 66.2 = 0.0227 (66)

Use two equal cascaded poles. Find the pole frequencies. fr is the second harmonic ripple frequency.

$$f_p = \sqrt{G_{ff}} \times f_r \quad (67)$$

Example:

f_p = 0.15 × l20 = 18 Hz

Select C_{ff1} and C_{ff2}.

$$C_{ff1} = \frac{1}{2\pi \times f_p \times R_{ff2}} \quad (68)$$

$$C_{ff2} = \frac{1}{2\pi \times f_p \times R_{ff3}} \quad (69)$$

Example:

$$C_{ff1} = \frac{1}{2\pi \times 18 \times 91k} = 0.097\ \mu F \quad (70)$$

Choose 0.10 µF.

$$C_{ff2} = \frac{1}{2\pi \times 18 \times 20k} = 0.44\ \mu F \quad (71)$$

Choose 0.47 µF.

9.2.3 Application Curve

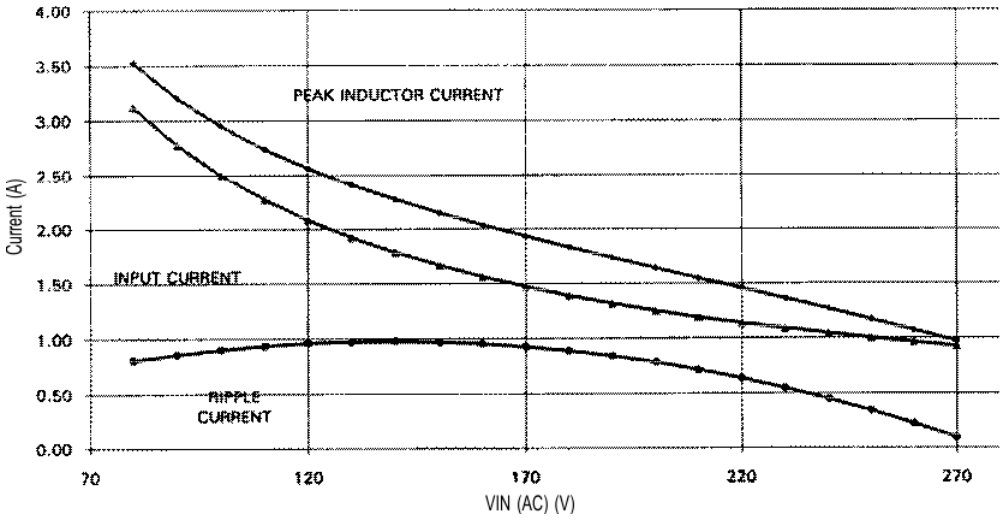


Figure 12. PFC Currents vs Input Voltage

10 Power Supply Recommendations

Power can be converted efficiently using any of several standard topologies. Design tradeoffs of cost, size, and performance generally narrow the field to one that is most appropriate. This demonstration application uses the off-line boost converter for the configuration.

11 Layout

11.1 Layout Guidelines

As in any converter design, Layout is a critical portion of good power supply design.

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

Several signals paths that conduct fast changing currents or voltages can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

• To help eliminate these problems, the Vcc pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.

• Care should be taken to minimize the loop area formed by the bypass capacitor connections, the Vcc pins, and the ground connections.

Try to run the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

External compensation components for stability should also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either.

Control circuitry and its associated components should be laid out minimizing the stray inductive loops.

11.2 Layout Example

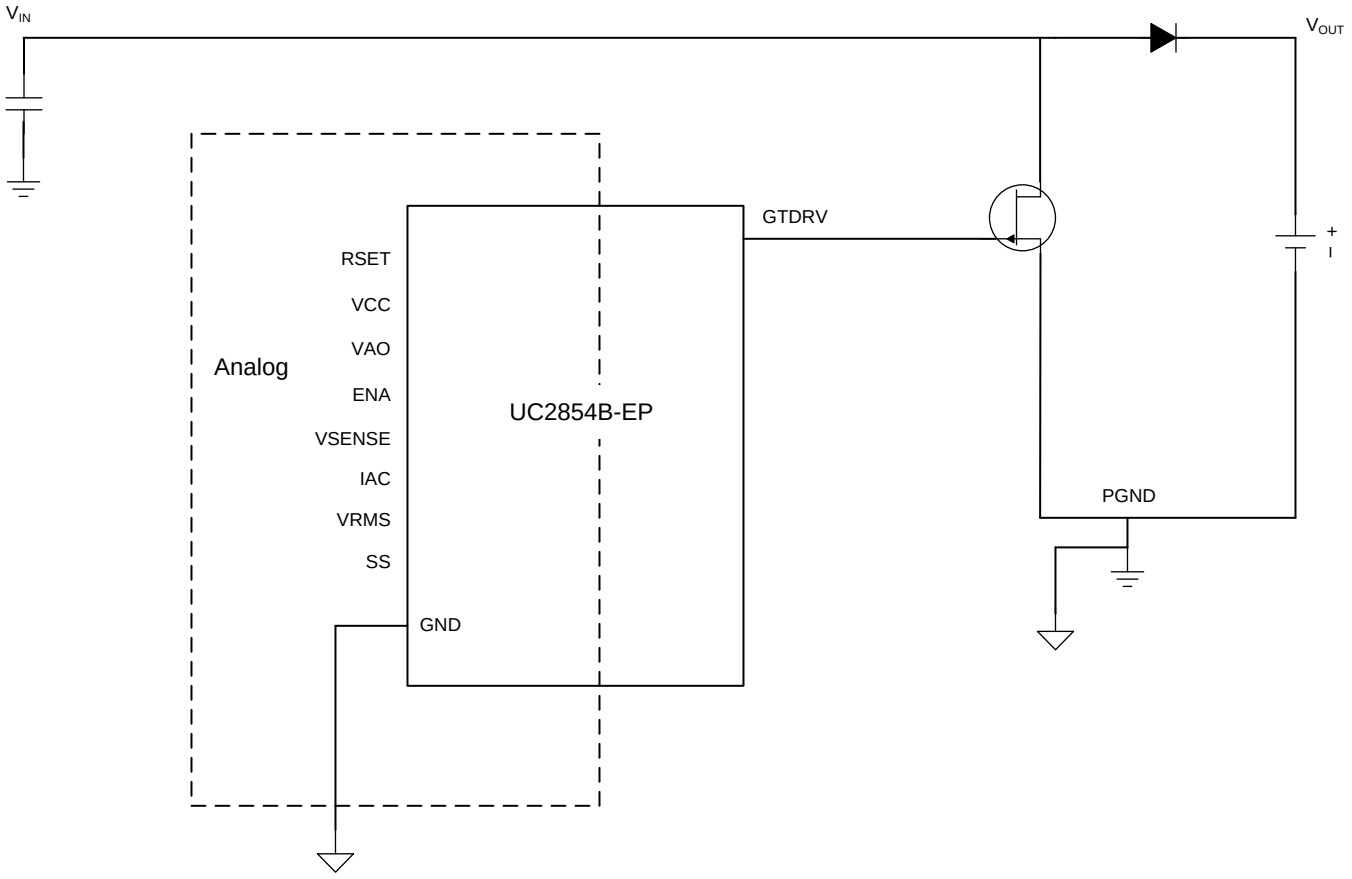


Figure 13. Layout Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2854BMDWREP	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC2854BMEP	Samples
UC2854BMDWREPG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC2854BMEP	Samples
V62/06612-01XE	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC2854BMEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC2854B-EP :

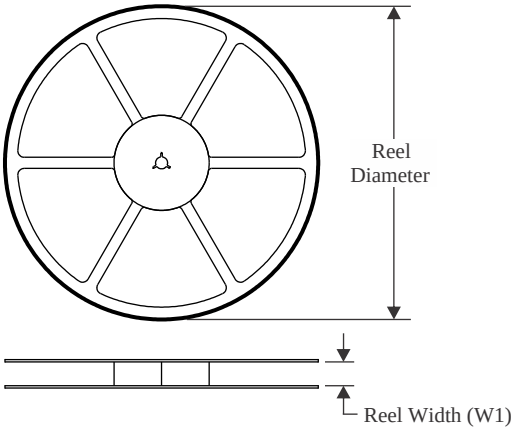
- Catalog: UC2854B
- Military: UC2854BM

NOTE: Qualified Version Definitions:

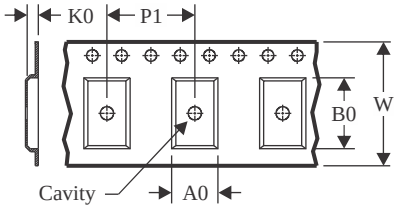
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

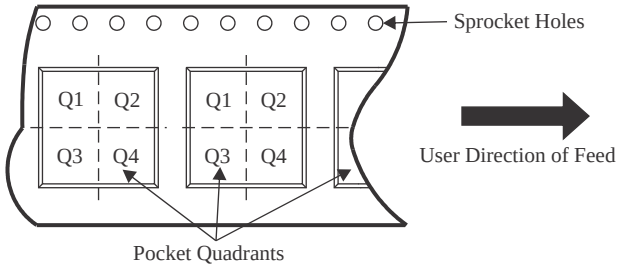


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

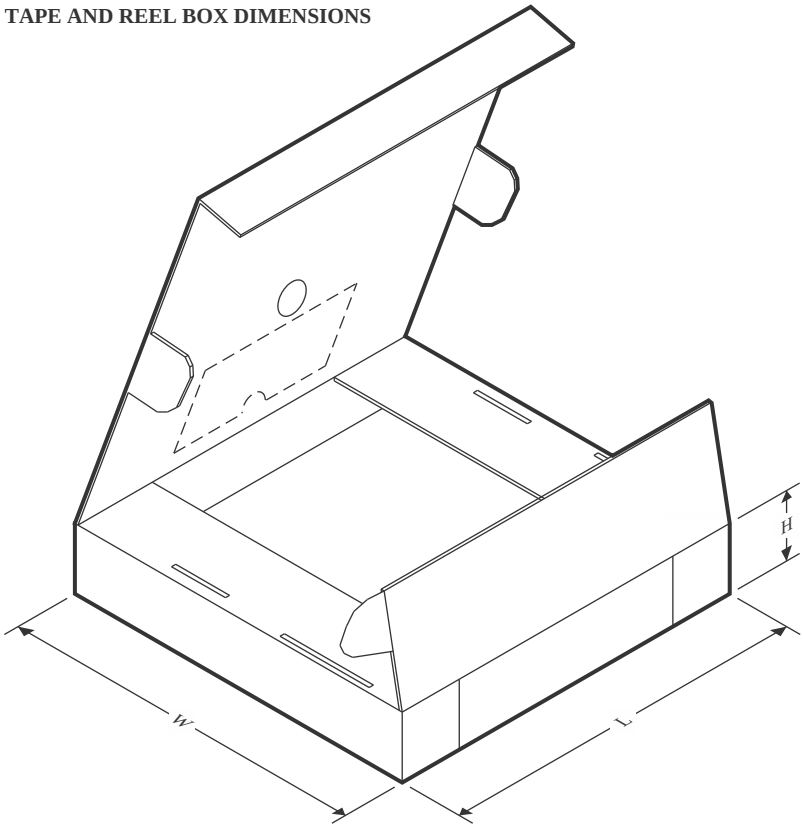
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2854BMDWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2854BMDWREP	SOIC	DW	16	2000	346.0	346.0	33.0

GENERIC PACKAGE VIEW

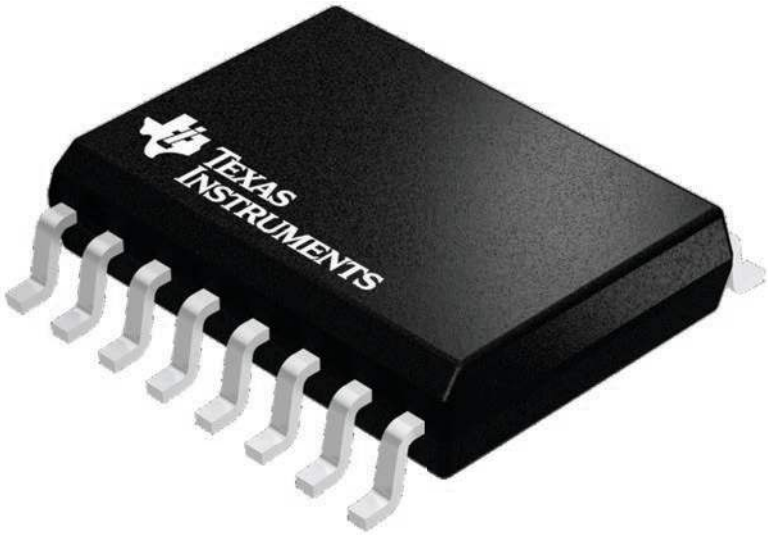
DW 16

SOIC - 2.65 mm max height

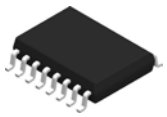
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

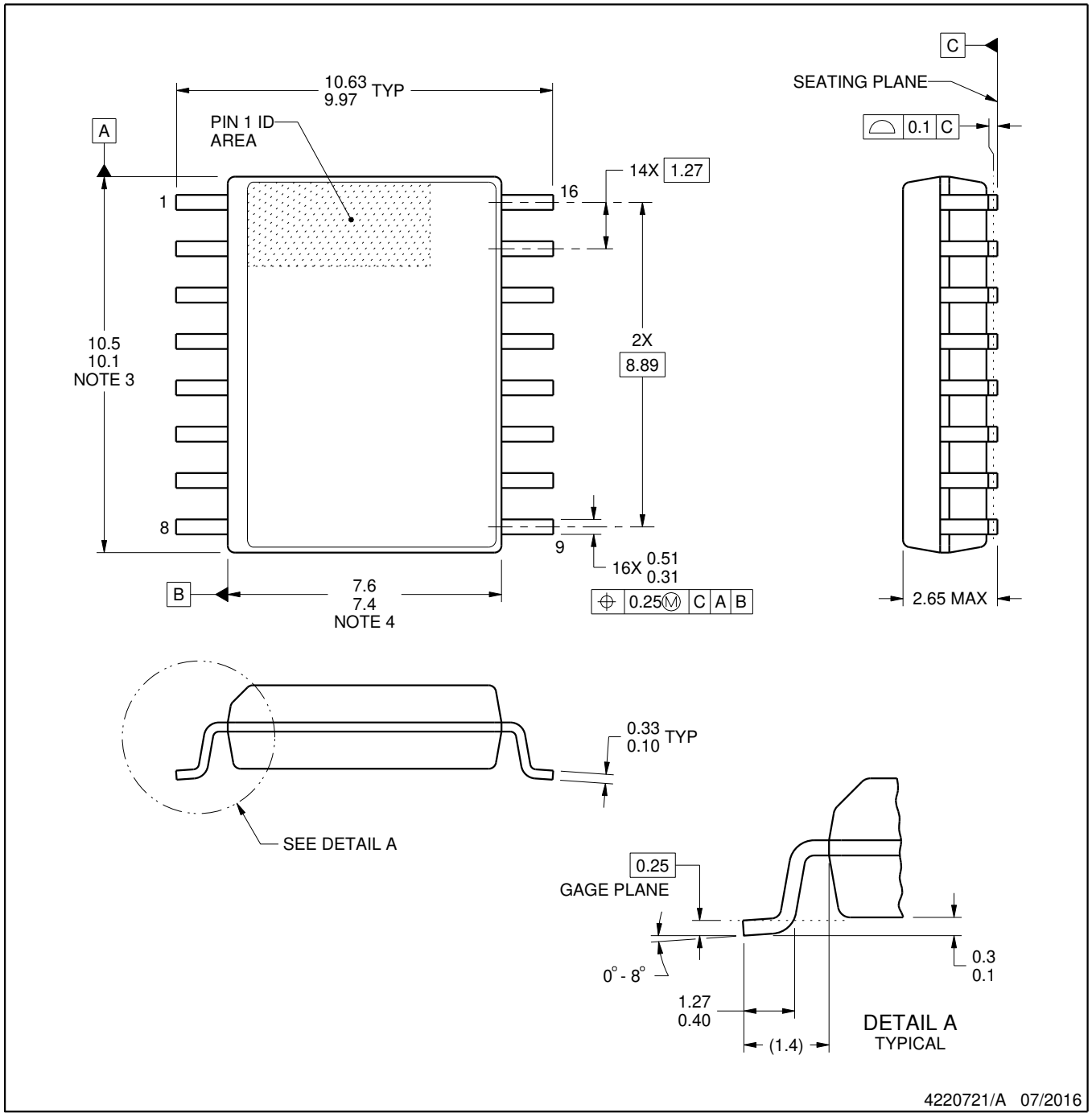


PACKAGE OUTLINE

DW0016A

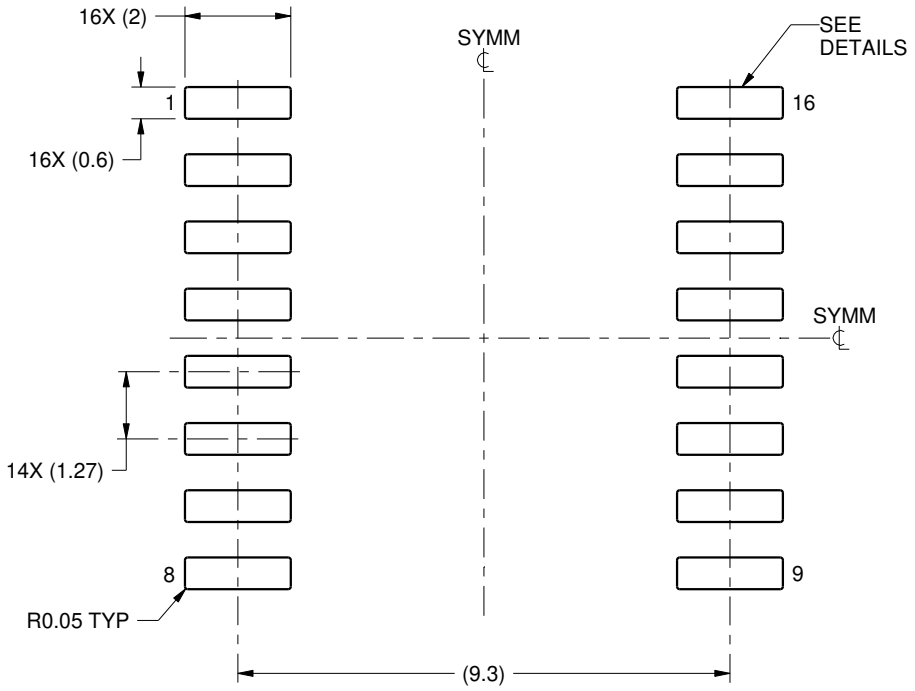
SOIC - 2.65 mm max height

SOIC

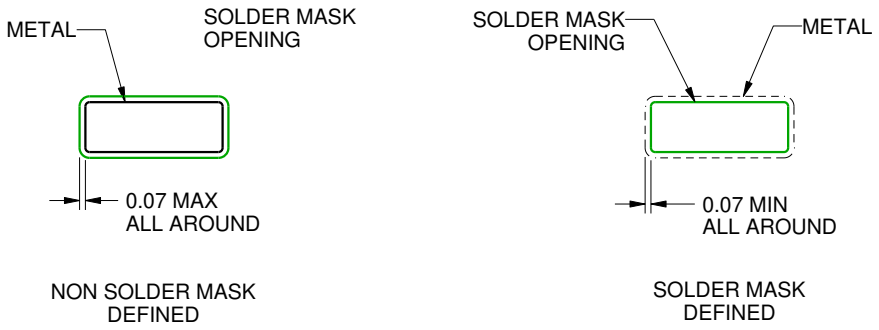


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

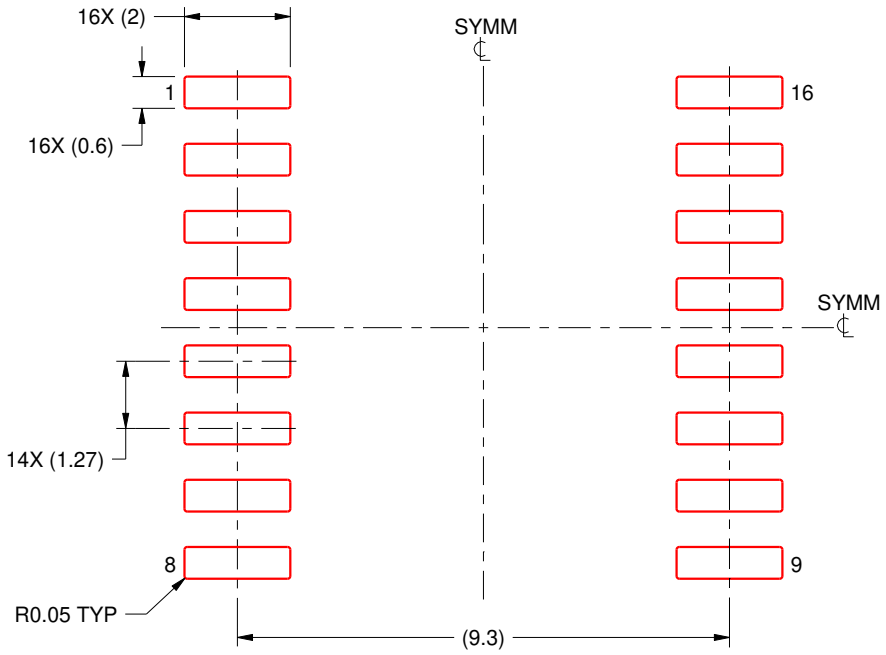


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265