



# BUK9Y8R8-60EL

Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LFPAK56 using Enhanced SOA technology

8 April 2022

Product data sheet

## 1. General description

Single, logic level, N-channel MOSFET in LFPAK56 using Application specific (ASFET) Enhanced SOA technology. This product has been designed and qualified to AEC-Q101 for use in linear mode in airbag applications.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Enhanced SOA technology for improved linear mode performance
- LFPAK copper clip package technology:
  - High robustness and current handling capability
  - Gull wing leads for easy AOI inspection and exceptional board level reliability

## 3. Applications

- 12 V automotive systems
- Airbag squib voltage regulator MOSFET

## 4. Quick reference data

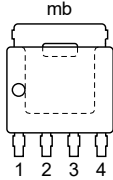
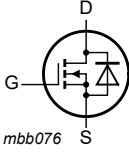
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	60	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	[1]	-	110	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	194	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 13</a>	3.1	4.4	5.6	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 4.5\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 15</a> ; <a href="#">Fig. 16</a>	-	18.2	36.4	nC

[1] 110 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y8R8-60EL	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y8R8-60EL	98E860L

## 8. Limiting values

Table 5. Limiting values

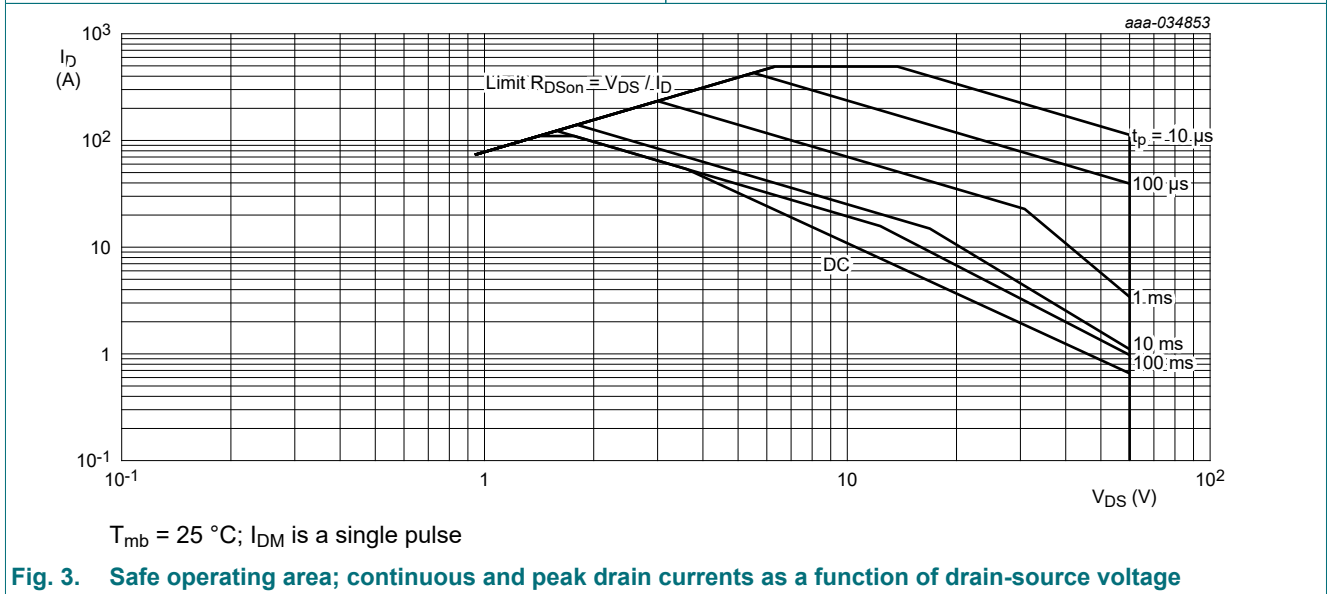
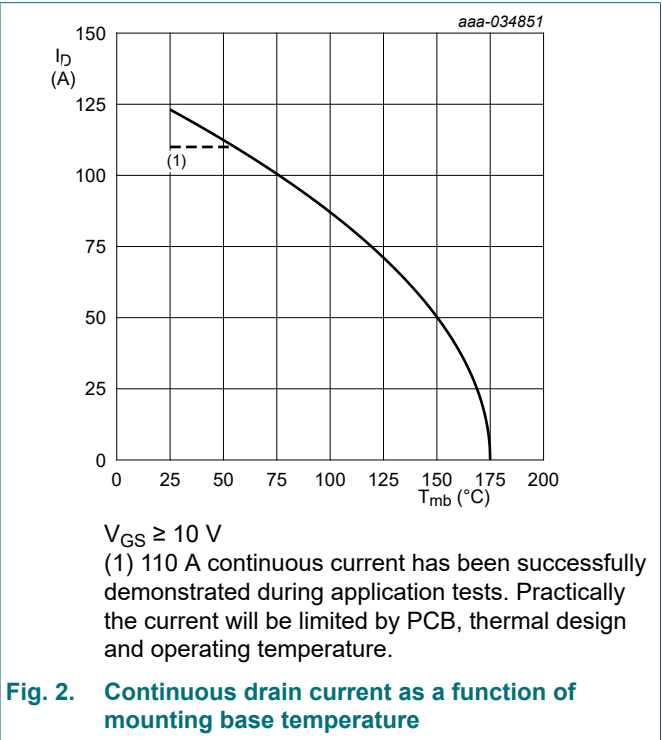
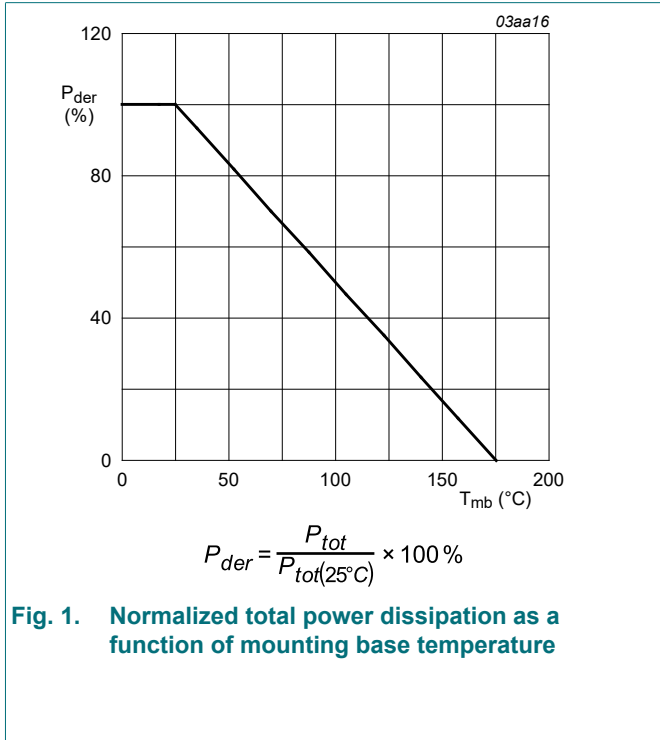
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	60	V
$V_{GS}$	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-10	10	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1		-	194	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	[1]	-	110	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2		-	87	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3; Fig. 4		-	493	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	110	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	493	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 62.3\text{ A}$ ; $V_{sup} \leq 60\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 76\text{ }\mu\text{s}$ ; Fig. 5	[2] [3]	-	195	mJ

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Symbol	Parameter	Conditions	Min	Max	Unit	
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 60\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $R_{GS} = 50\text{ }\Omega$ ; Fig. 5	[2] [3] [4]	-	62.3	A

- [1] 110 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test.



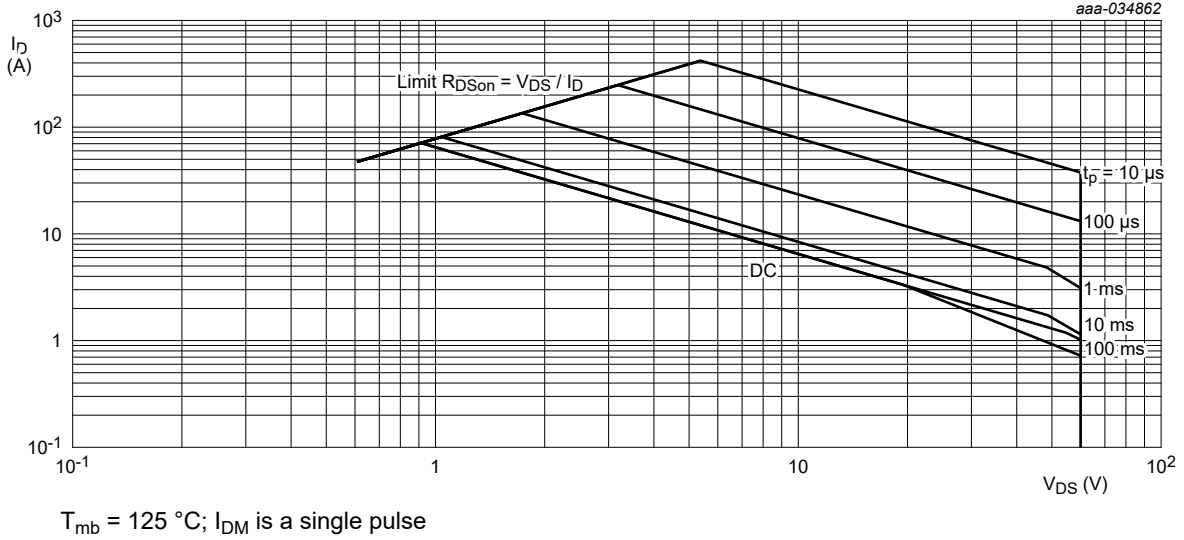
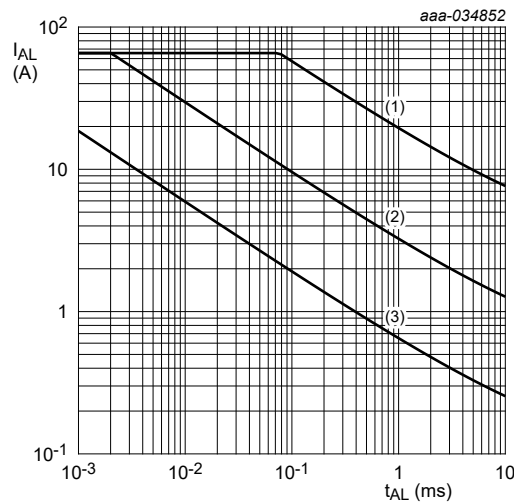


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1)  $T_{j (init)} = 25 \text{ }^\circ\text{C}$ ; (2)  $T_{j (init)} = 150 \text{ }^\circ\text{C}$ ; (3) Repetitive Avalanche

Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6	-	0.69	0.77	K/W

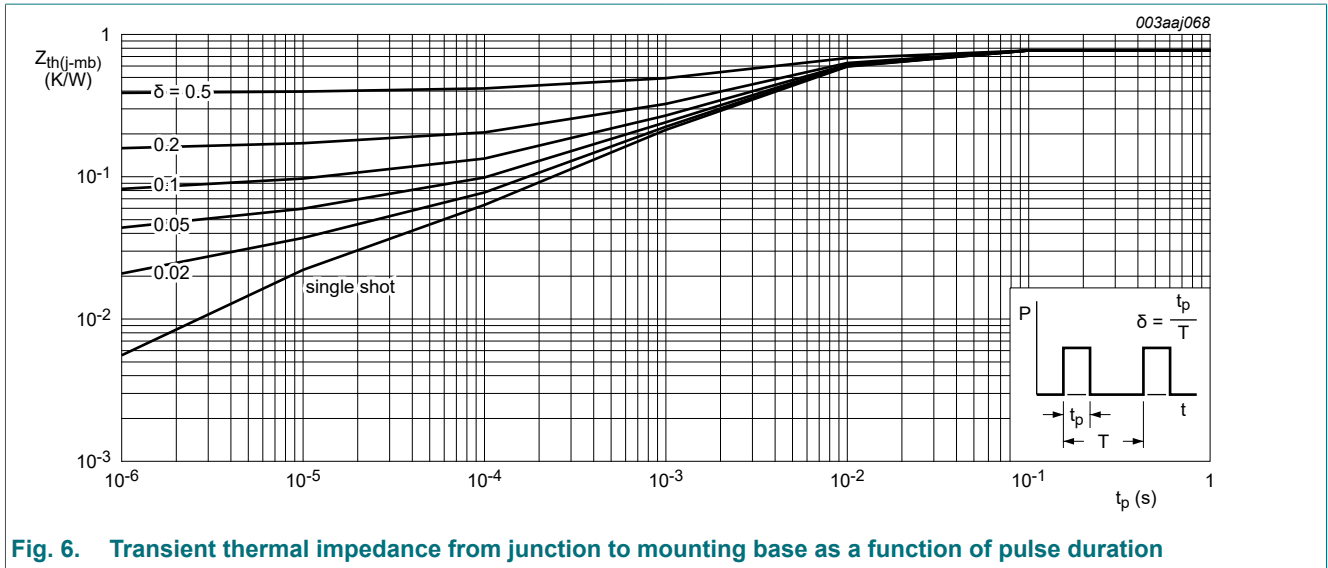


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

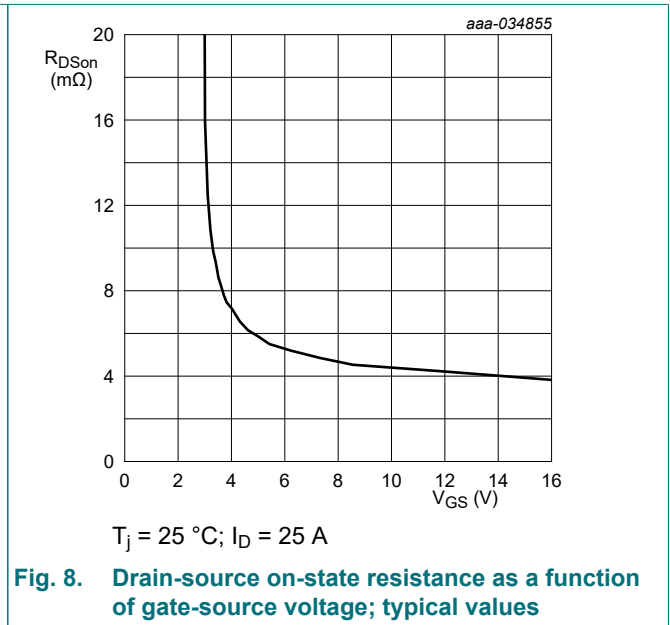
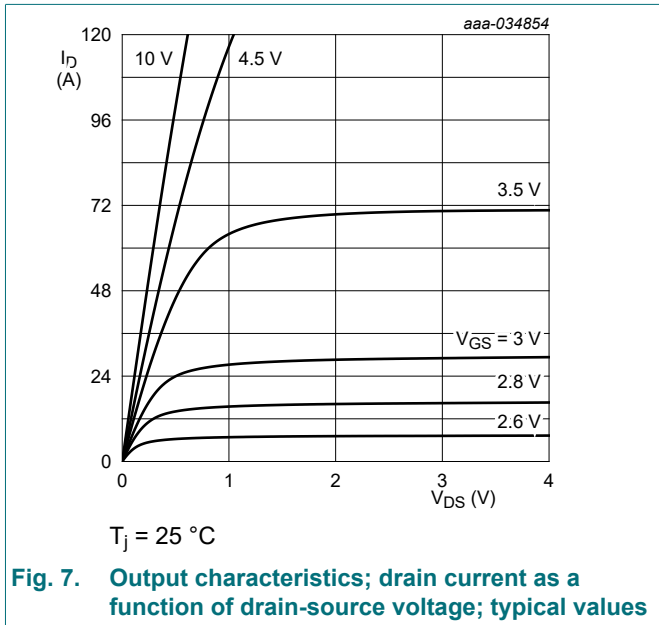
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	66	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	62.2	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	61.2	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	1.4	1.8	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 12</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.023	1	$\mu A$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	68	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 13</a>	3.1	4.4	5.6	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ C$ ; <a href="#">Fig. 14</a>	4.7	7	9	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ C$ ; <a href="#">Fig. 14</a>	5.2	7.7	10	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 14</a>	6.4	9.7	12.7	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 13</a>	4.5	6.5	8.6	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ C$ ; <a href="#">Fig. 14</a>	6.7	10	13.7	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ C$ ; <a href="#">Fig. 14</a>	7.3	11	15.2	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 14</a>	9	13.5	19.1	m $\Omega$

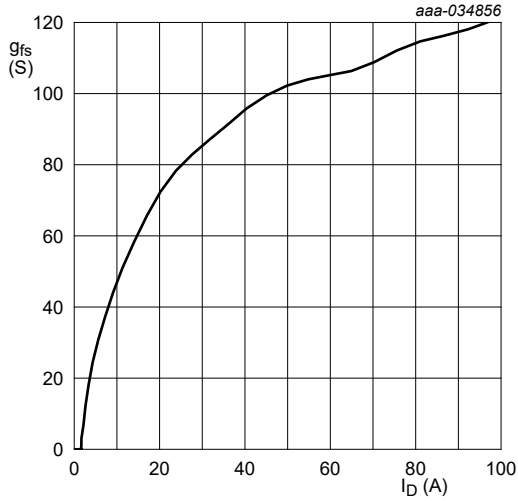
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	2.24	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 15}; \text{Fig. 16}$	-	43	60	nC
		$I_D = 25 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 15}; \text{Fig. 16}$	-	88	123	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 15}; \text{Fig. 16}$	-	12	18	nC
$Q_{GD}$	gate-drain charge		-	18.2	36.4	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 17}$	-	4782	6695	pF
$C_{oss}$	output capacitance		-	412	494	pF
$C_{rss}$	reverse transfer capacitance		-	224	307	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 48 \text{ V}; R_L = 1.92 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(\text{ext})} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	22	-	ns
$t_r$	rise time		-	55	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	56	-	ns
$t_f$	fall time		-	42	-	ns
$g_{fs}$	transfer conductance	$V_{DS} = 8 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 9}$	-	80	-	S
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 18}$	-	0.81	1	V
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 19}$	-	30	-	ns
$Q_r$	recovered charge		[1]	33	-	nC

[1] includes capacitive recovery

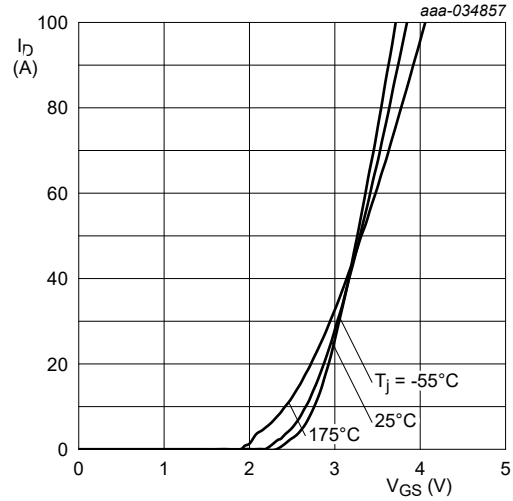


Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LPAK56 using Enhanced SOA technology



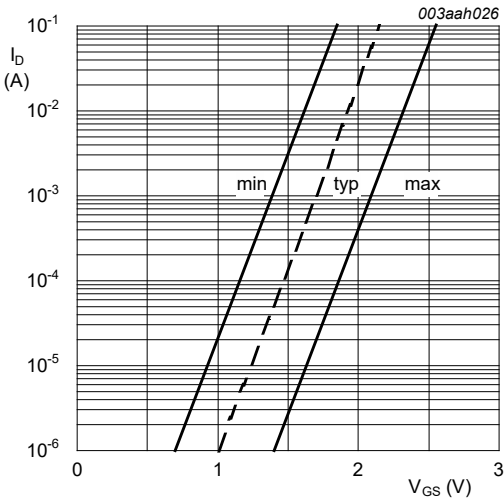
$T_j = 25\text{ °C}; V_{DS} = 8\text{ V}$

**Fig. 9. Forward transconductance as a function of drain current; typical values**



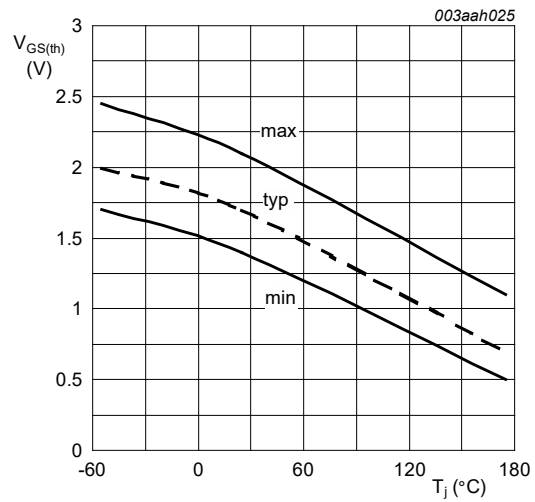
$V_{DS} = 8\text{ V}$

**Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

**Fig. 12. Gate-source threshold voltage as a function of junction temperature**

Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LPAK56 using Enhanced SOA technology

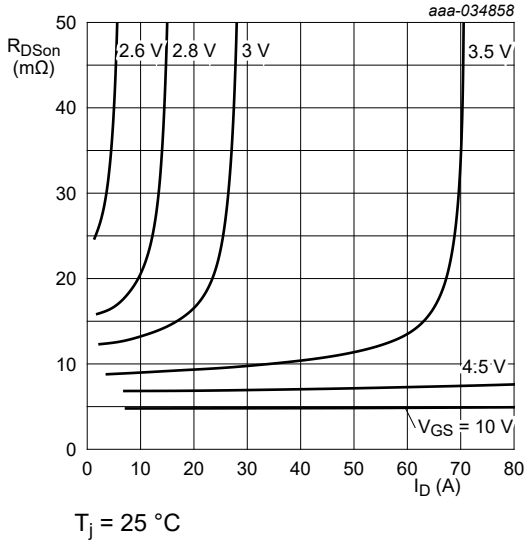
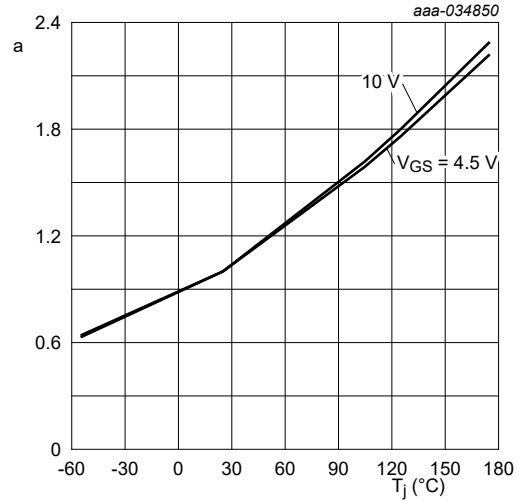


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 14. Normalized drain-source on-state resistance factor as a function of junction temperature

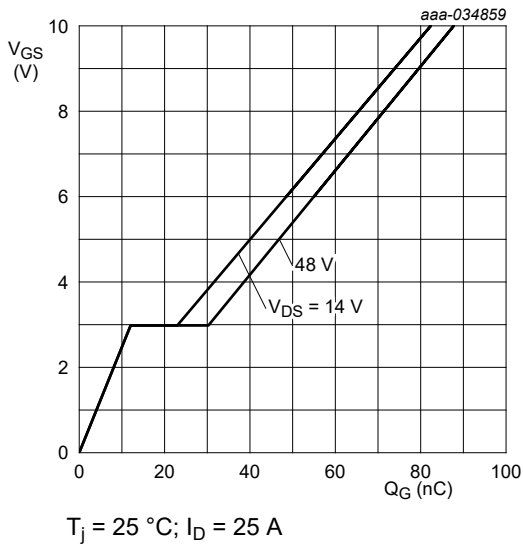


Fig. 15. Gate-source voltage as a function of gate charge; typical values

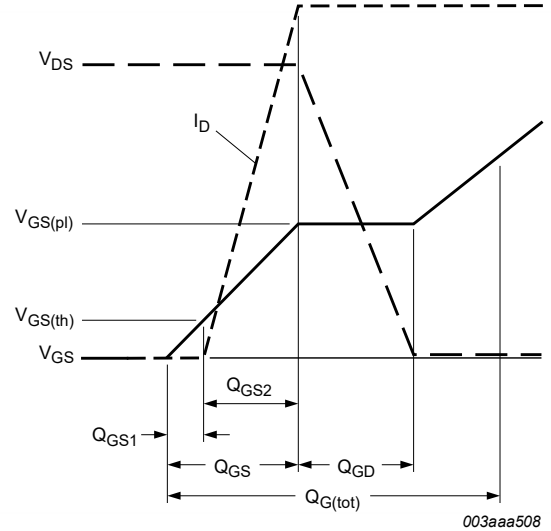


Fig. 16. Gate charge waveform definitions



Single N-channel 60 V, 5.6 mOhm logic level MOSFET in LPAK56 using Enhanced SOA technology

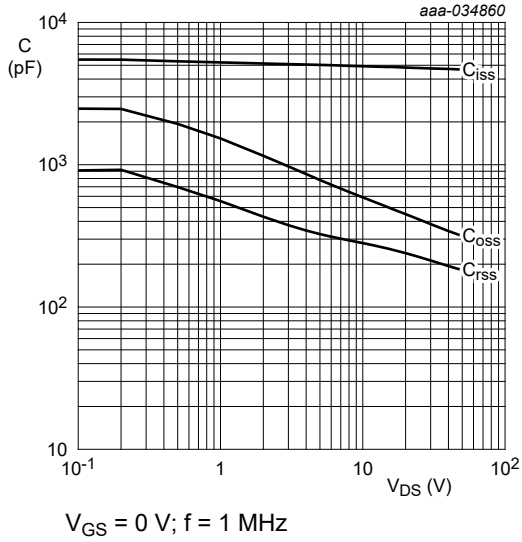


Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

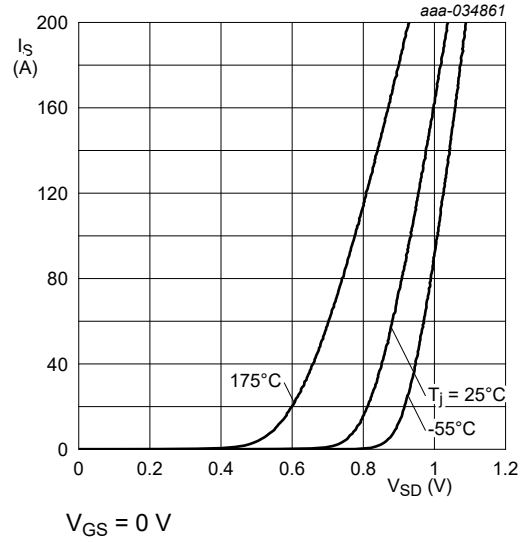


Fig. 18. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

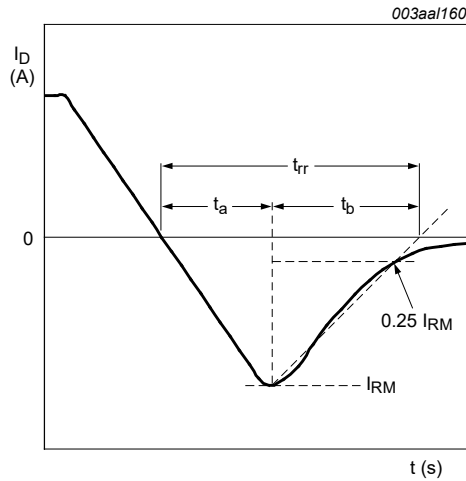


Fig. 19. Reverse recovery timing definition

### 11. Package outline

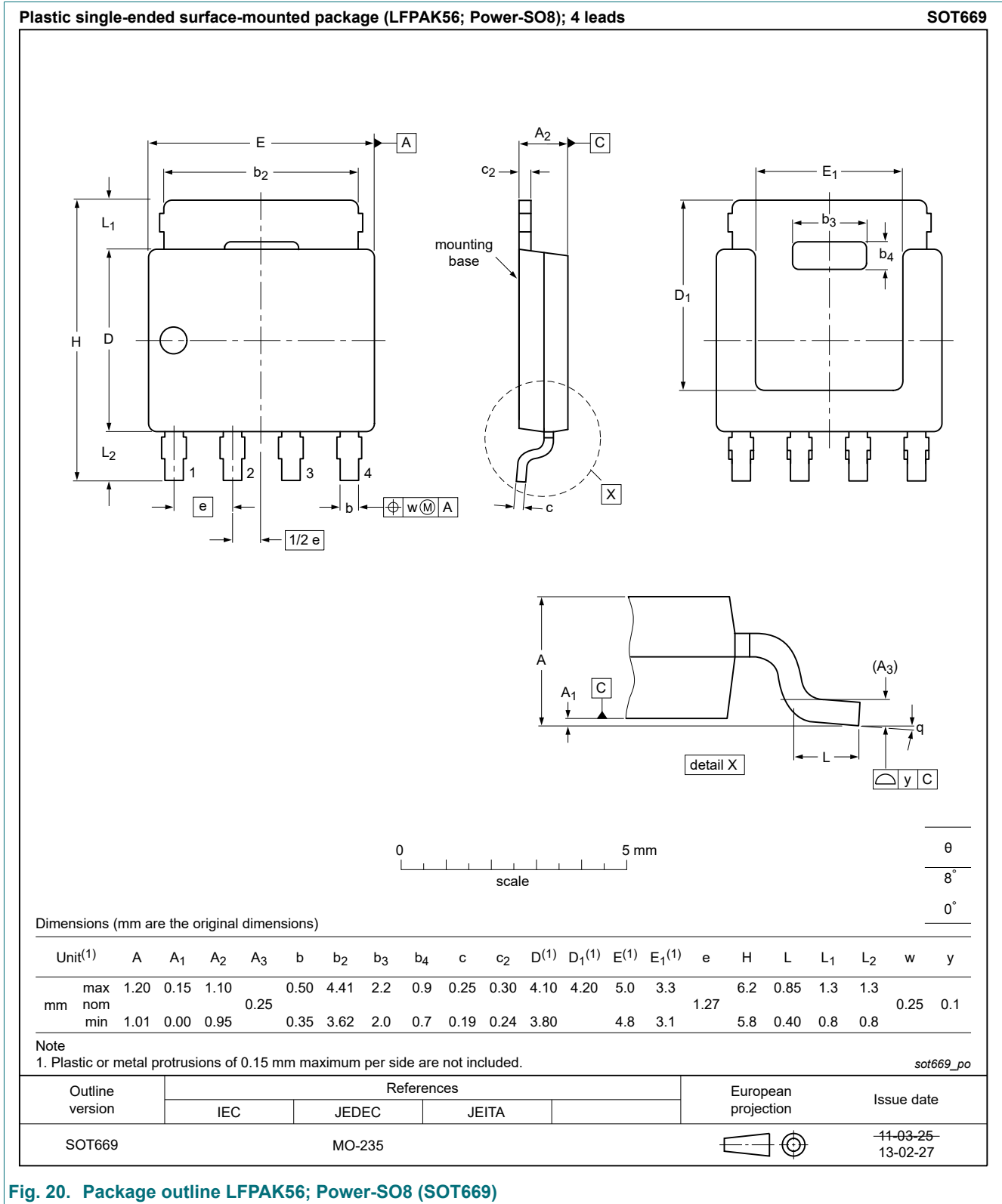


Fig. 20. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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