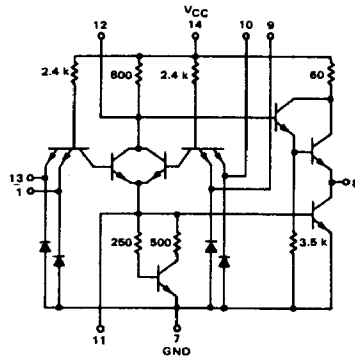


EXPANDABLE DUAL  
2-WIDE 2-INPUT  
"AND-OR-INVERT" GATE

MTTL III MC3100/3000 series

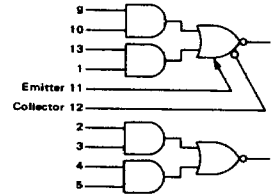
**MC3120F • MC3020F**  
**MC3120L • MC3020L,P**  
(54H50J) (74H50J,N)

1/2 OF CIRCUIT SHOWN †



†Other half of circuit omits expander inputs.

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORING nodes are available for expansion. Up to four AND gates can be ORed together using the MC3030 expander. Care should be taken to minimize the amount of capacitance on the expander terminals in order to maintain switching speeds.



Positive Logic:

$$B = (9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})$$

Negative Logic:

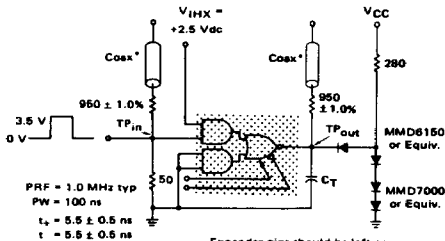
$$B = (9 + 10) \cdot (13 + 1) \cdot (\text{Expanders})$$

Input Loading Factor = 1

Output Loading Factor = 10

Total Power Dissipation = 62.5 mW typ/pkg  
Propagation Delay Time = 6.0 ns typ

SWITCHING TIME TEST CIRCUIT

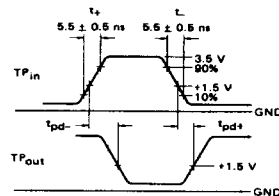


Expander pins should be left open when measuring switching times.

\*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C<sub>T</sub> = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



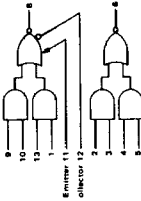
See General Information section for packaging.

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# MC3120F, MC3020F/MC3120L, MC3020L,P (continued)

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



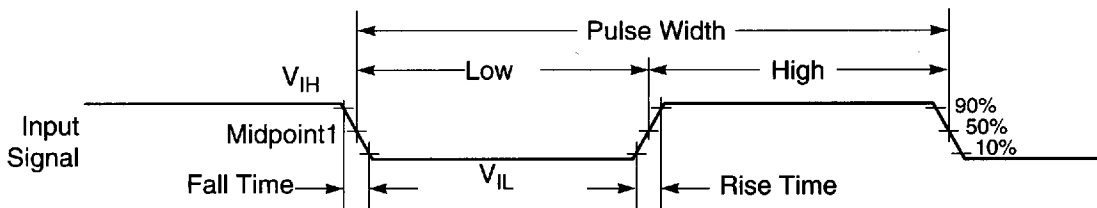
Characteristic	MC3120 Test limits			MC3020 Test limits			TEST CURRENT/VOLTAGE VALUES														Qual				
	Min	Max	Typ	Min	Max	Typ	Min	Max	Typ	Min	Max	Typ	Min	Max	Typ	Min	Max	Typ	Min	Max		Typ	Min	Max	Typ
Input																									
Forward Current	1	-3.0	-	-2.0	-	-1.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-
Leakage Current	I <sub>1</sub>	50	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-
Breakdown Voltage	BV <sub>1n</sub>	1	-	5.5	-	-	-	5.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Clamp Voltage	V <sub>D</sub>	1	-	-1.5	-	-	-	-1.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Output																									
Output Voltage	V <sub>OL</sub>	8	0.4	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-
	V <sub>OL</sub>	8	0.4	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-
	V <sub>OH</sub>	8	2.4	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-	2.5	-
Short-Circuit Current	I <sub>SC</sub>	8	40	100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100
Mean-Diameter Voltage	V <sub>BE (avg)</sub>	33	0.40	0.45	-	0.45	-	0.70	-	0.85	-	0.85	-	0.85	-	0.85	-	0.85	-	0.85	-	0.85	-	0.85	-
Power																									
Maximum Power (Total Device)	P <sub>max</sub>	16	-	24	-	-	-	24	-	24	-	24	-	24	-	24	-	24	-	24	-	24	-	24	-
Maximum Power (Per Gate)	P <sub>max/g</sub>	16	-	22	-	22	-	22	-	22	-	22	-	22	-	22	-	22	-	22	-	22	-	22	-
Power Supply Drain	I <sub>DD1</sub>	14	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-	14	-
Switching																									
Propagation Delay	t <sub>pd</sub>	1.8	-	-	-	12	-	-	-	12	-	-	-	12	-	-	-	12	-	-	-	12	-	-	-
Turn-Off Delay	t <sub>off</sub>	1.8	-	-	-	12	-	-	-	12	-	-	-	12	-	-	-	12	-	-	-	12	-	-	-

\*Typical data on switching delay is established by generating the inputs at given rate under test.

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## AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a  $V_{IL}$  maximum of 0.5 V and a  $V_{IH}$  minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine  $V_{OL}$  and  $V_{OH}$  reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is  $V_{IL} + (V_{IH} - V_{IL})/2$ .

AA0179

Figure 2-1 Signal Measurement Reference