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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Renesas

MOS FIELD EFFECT TRANSISTOR

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP110N04PUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rating
- Super low on-state resistance R_{DS(on)} = 1.8 mΩ MAX. (V_{GS} = 10 V, I_D = 55 A)
 Low C_{iss}: C_{iss} = 17100 pF TYP.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$)

•			
Drain to Source Voltage (VGS = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	±110	А
Drain Current (pulse) Note1	D(pulse)	±440	А
Total Power Dissipation (T _A = 25° C)	P _{T1}	1.8	W
Total Power Dissipation (Tc = 25° C)	Pt2	288	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	–55 to +175	°C
Repetitive Avalanche Current Note2	IAR	72	А
Repetitive Avalanche Energy Note2	Ear	518	mJ
Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%			
2. $T_{ch} \le 150^{\circ}C$, V_{DD} = 20 V, R_{G} = 25	Ω, V _{GS} =	$20 \rightarrow 0 V$	

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	0.52	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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ORDERING INFORMATION

PART NUMBER	PACKAGE
NP110N04PUG	TO-263 (MP-25ZP)



(TO-263)

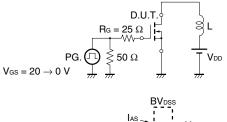
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	lgss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage Note	V _{GS(th)}	V_{DS} = V_{GS} , I_D = 250 μ A	2.0	3.0	4.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 55 A	45	89		S
Drain to Source On-state Resistance Note	RDS(on)	Vgs = 10 V, Id = 55 A		1.4	1.8	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V		17100	25700	pF
Output Capacitance	Coss	V _{GS} = 0 V		1420	2130	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		890	1610	pF
Turn-on Delay Time	td(on)	V _{DD} = 20 V, I _D = 55 A		54	120	ns
Rise Time	tr	V _{GS} = 10 V		140	350	ns
Turn-off Delay Time	td(off)	R _G = 0 Ω		130	260	ns
Fall Time	tr			21	60	ns
Total Gate Charge	QG	V _{DD} = 32 V		260	390	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		57		nC
Gate to Drain Charge	Qgd	I _D = 110 A		83		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 110 A, VGS = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	IF = 110 A, VGS = 0 V		60		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		80		nC

Note Pulsed

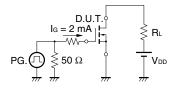
TEST CIRCUIT 1 AVALANCHE CAPABILITY

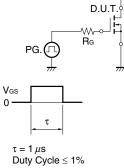
TEST CIRCUIT 2 SWITCHING TIME

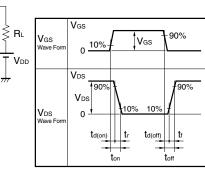




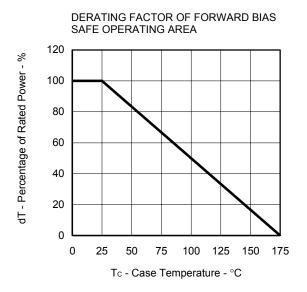
TEST CIRCUIT 3 GATE CHARGE

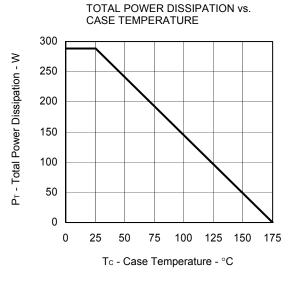




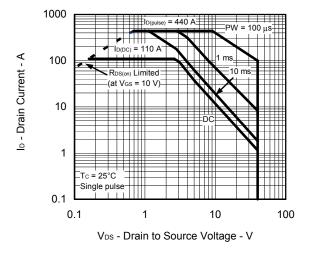


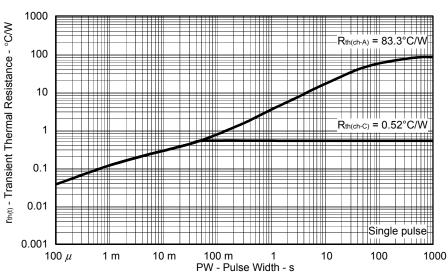
TYPICAL CHARACTERISTICS (T_A = 25°C)



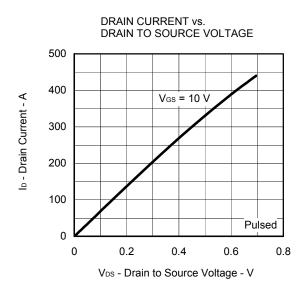


FORWARD BIAS SAFE OPERATING AREA

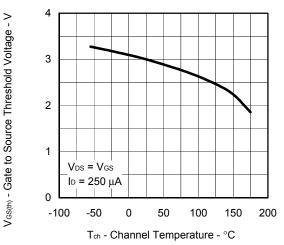


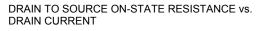


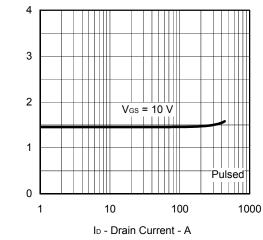
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



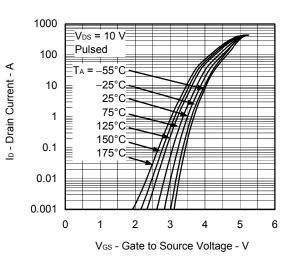




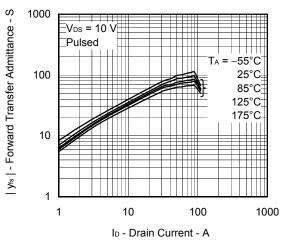




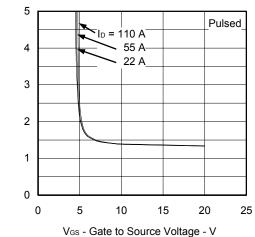
FORWARD TRANSFER CHARACTERISTICS



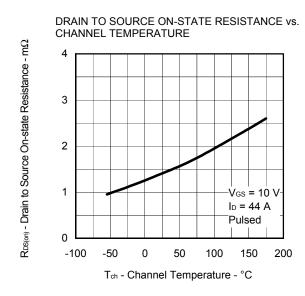
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



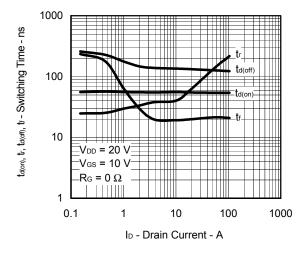
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



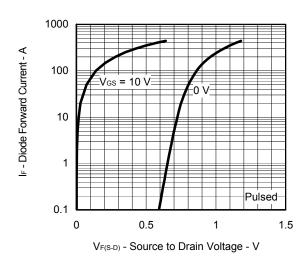
 $R_{DS(m)}$ - Drain to Source On-state Resistance - $m\Omega$



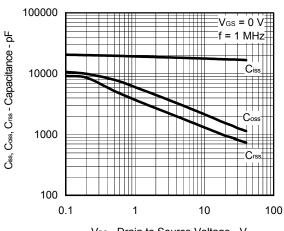




SOURCE TO DRAIN DIODE FORWARD VOLTAGE

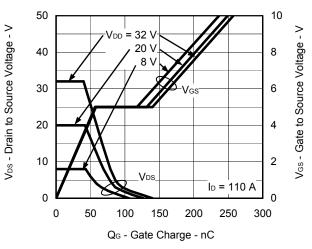


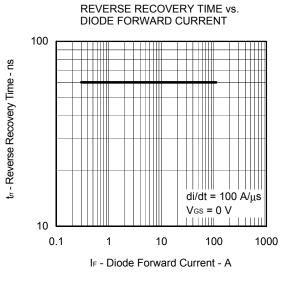
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



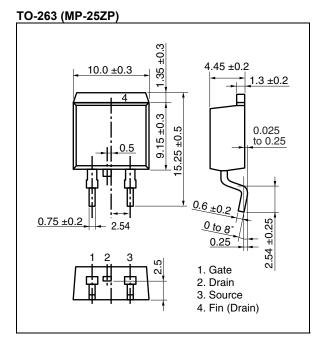
VDS - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS

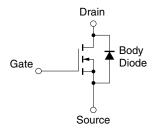




PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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