DATA SHEET

AAT1153: 2 A Step-Down Converter

Applications

- Cellular phones
- Digital cameras
- DSP core supplies
- PDAs
- Portable instruments
- Smart phones

Features

- Input voltage range: 2.5 V to 5.5 V
- Output voltages: 0.6 V to V_{IN}
- Output current: 2 A
- High efficiency: up to 95%
- 1.2 MHz constant switching frequency
- Low $R_{DS(ON)}$ internal switches: 0.15 Ω
- Allows use of ceramic capacitors
- Current mode operation for excellent line and load transient response
- Short-circuit and thermal fault protection
- Soft start
- Low dropout operation: 100% duty cycle
- Low shutdown current: $I_{SHDN} < 1$ µA
- –40 °C to +85 °C temperature range
- TDFN (10-pin, 3 × 3 mm) package (MSL1, 260 ºC per JEDEC J-STD-020)

Description

The AAT1153 SwitchReg™ is a 1.2 MHz constant frequency current mode PWM step-down converter. It is ideal for portable equipment requiring very high current up to 2 A from single-cell Lithium-Ion batteries while still achieving over 90% efficiency during peak load conditions. The AAT1153 also can run at 100% duty cycle for low dropout operation, extending battery life in portable systems while light load operation provides very low output ripple for noise-sensitive applications.

The AAT1153 can supply up to 2 A output load current from a 2.5 V to 5.5 V input voltage and the output voltage can be regulated as low as 0.6 V. The high switching frequency minimizes the size of external components while keeping switching losses low. The internal slope compensation setting allows the device to operate with smaller inductor values to optimize size and provide efficient operation.

The AAT1153 is available with adjustable (0.6 V to V_{IN}) output voltage. The device is available in a Pb-free, 10-pin, 3 × 3 mm TDFN package and is rated over the –40 °C to +85 °C temperature range.

A typical application circuit is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

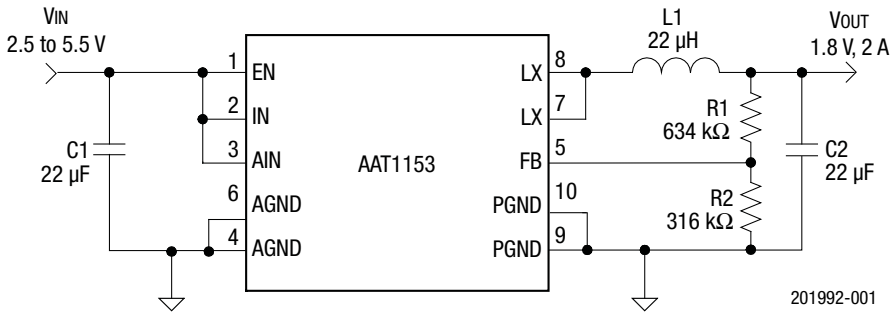


Figure 1. AAT1153 Typical Application Circuit

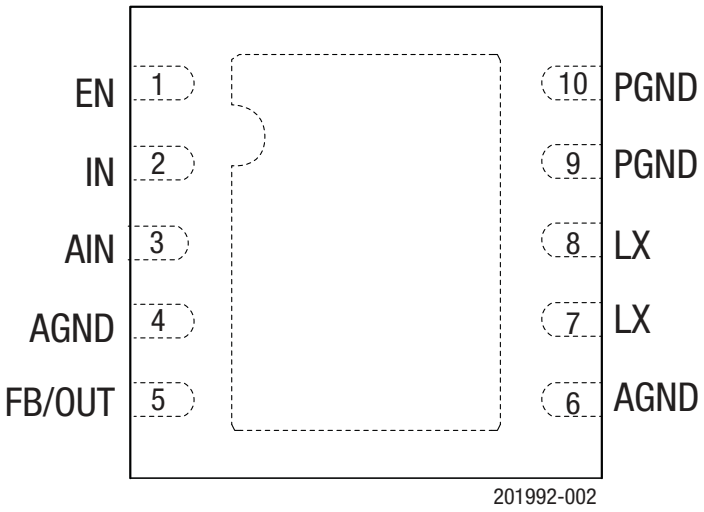


Figure 2. AAT1153 Pinout
(Top View)

Table 1. AAT1153 Signal Descriptions

Pin	Name	Description
1	EN	Enable pin. Active high. In shutdown, all functions are disabled drawing < 1 μA supply current. Do not leave EN floating.
2	IN	Power supply input pin. Must be closely decoupled to AGND with a 2.2 μF or greater ceramic capacitor.
3	AIN	Analog supply input pin. Provides bias for internal circuitry.
4, 6	AGND	Analog ground pin.
5	FB/OUT	Feedback input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6 V.
7, 8	LX	Switching node pin. Connect the output inductor to this pin.
9, 10	PGND	Power ground pin.
	EP	Power ground exposed pad. Must be connected to bare copper ground plane.

Electrical and Mechanical Specifications

The absolute maximum ratings of the AAT1153 are provided in Table 2, and electrical specifications are provided in Table 3.

Typical performance characteristics of the AAT1153 are illustrated in Figures 3 through 21.

Table 2. AAT1153 Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
Input supply voltages	V_{IN}, V_{AIN}	–0.3	+6.0	V
FB, LX voltages	V_{FB}, V_{LX}	–0.3	V_{IN} + 0.3	V
EN voltage	V_{EN}	–0.3	V_{IN} + 0.3	V
Ground voltages	PGND, AGND	–0.3	+6.0	V
Operating temperature range	T_A	–40	+85	°C
Storage temperature	T_{STG}	–65	+150	°C
Lead temperature (soldering, 10 s)	T_{LEAD}		300	°C
Thermal resistance[2,3]	θ_{JA}		45	°C/W
Thermal dissipation at T_A = 25 °C	P_D		2.2	W

[1] Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

[2] T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$.

[3] Thermal Resistance is specified with approximately 1 square inch of 1 oz. copper.

***ESD HANDLING**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. AAT1153 Electrical Specifications[1]
(V_{IN} = 3.6 V, T_A = –40 °C to +85°C, Typical Values are T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input voltage range[2]	V_{IN}		2.5		5.5	V
Output voltage range	V_{OUT}		0.6		V_{IN}	V
Input DC supply current	I_Q	Active mode: V_{FB} = 0.5 V		300	500	µA
		Shutdown mode: V_{EN} = 0 V, V_{AIN} = 5.5 V		0.1	1	µA
Feedback input bias current	I_{FB}	V_{FB} = 0.65 V			30	nA
Regulated feedback voltage[3]	V_{FB}	T_A = 25°C	0.5880	0.6000	0.6120	V
		0 °C ≤ T_A ≤ 85 °C	0.5865	0.6000	0.6135	V
		–40 °C ≤ T_A ≤ 85 °C	0.5850	0.6000	0.6150	V
Line regulation	$\Delta V_{LINEREG}/\Delta V_{IN}$	V_{IN} = 2.5 to 5.5 V, I_{OUT} = 10 mA		0.10	0.20	%/V
Load regulation	$\Delta V_{LOADREG}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 2 A		0.20		%/A
Output voltage accuracy	V_{FB}	V_{IN} = 2.5 to 5.5 V, I_{OUT} = 10 mA to 2 A	–3		+3	% V_{OUT}
Oscillator frequency	f_{OSC}	V_{FB} = 0.6 V	0.96	1.2	1.44	MHz
Startup time	t_{STUP}	From enable to output regulation		1.3		ms
Over-temperature shutdown threshold	T_{SD_THR}			170		°C
Over-temperature shutdown hysteresis	T_{SD_HYS}			10		°C
Peak switch current	I_{LIM}		2.5	3.5		A
P-CH MOSFET	$R_{DS(ON)\_P}$	V_{IN} = 3.6 V		135	200	mΩ
N-CH MOSFET	$R_{DS(ON)\_N}$	V_{IN} = 3.6 V		95	150	mΩ
Enable threshold low	V_{EN_L}				0.3	V
Enable threshold high	V_{EN_H}		1.5			V
Input low current	I_{IN_L}	V_{IN} = V_{EN} = 5.5 V	–1.0		1.0	µA

[1] The AAT1153 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

[2] V_{IN} should be not less than V_{OUT} + $V_{DROPOUT}$, where $V_{DROPOUT}$ = I_{OUT} x ($R_{DS(ON)\_P}$ + $ESR_{INDUCTOR}$, typically $V_{DROPOUT}$ = 0.3 V.

[3] The regulated feedback voltage is tested in an internal test mode that connects V_{FB} to the output of the error amplifier.

Typical Performance Characteristics

(V_{IN} = 3.6 V, T_A = –40 °C to +85°C, Typical Values are T_A = 25 °C, Unless Otherwise Noted)

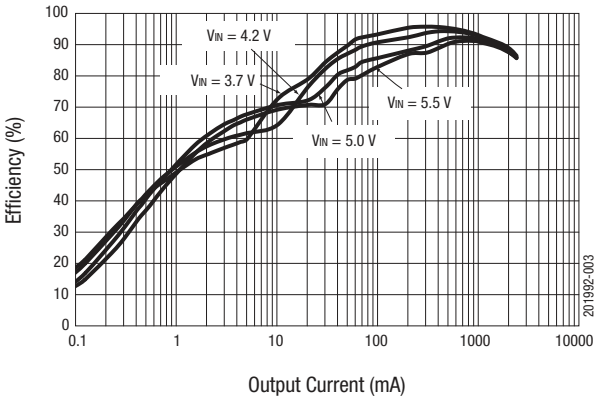


Figure 3. Efficiency vs Output Current
(V_{OUT} = 3.3 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

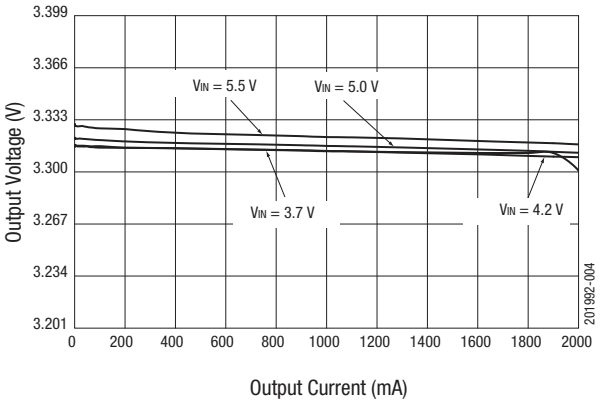


Figure 4. DC Regulation
(V_{OUT} = 3.3 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

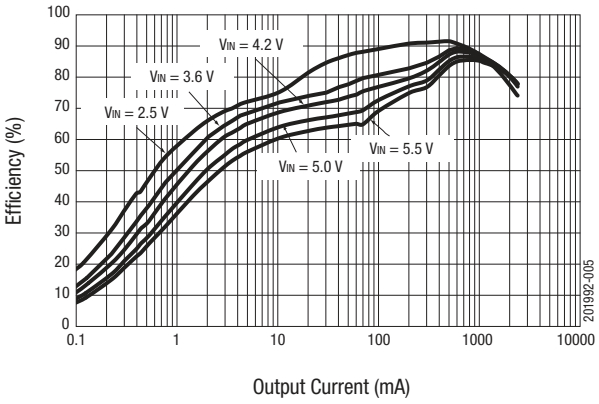


Figure 5. Efficiency vs Output Current
(V_{OUT} = 1.8 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

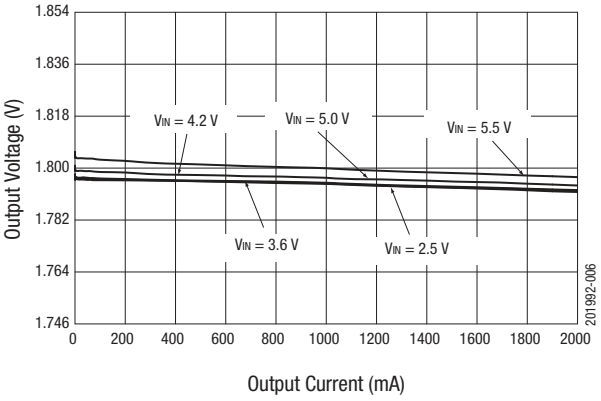


Figure 6. DC Regulation
(V_{OUT} = 1.8 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

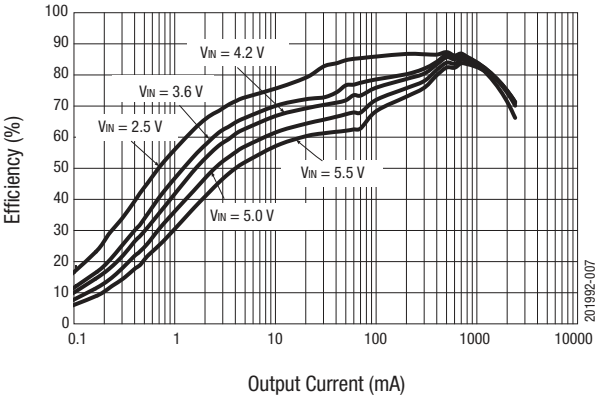


Figure 7. Efficiency vs Output Current
(V_{OUT} = 1.5 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

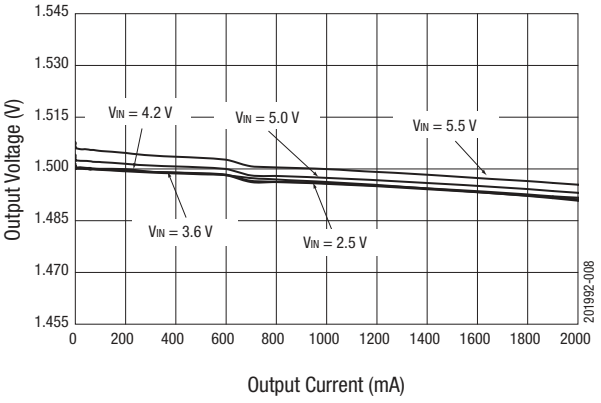


Figure 8. DC Regulation
(V_{OUT} = 1.5 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

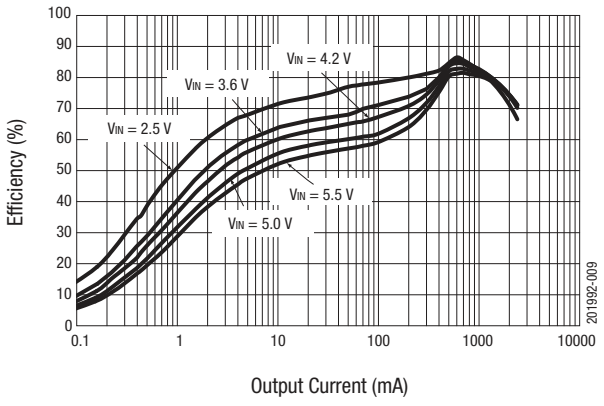


Figure 9. Efficiency vs Output Current
(V_{OUT} = 1.2 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

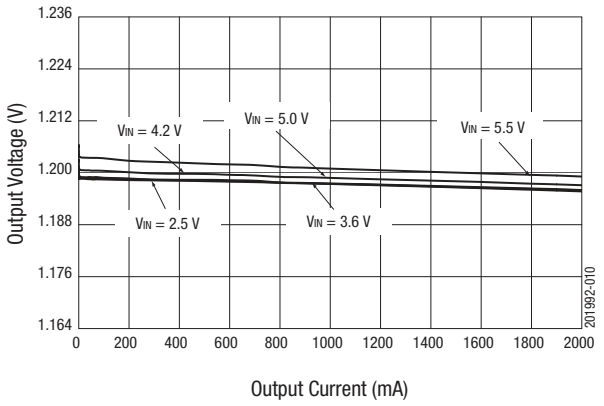


Figure 10. DC Regulation
(V_{OUT} = 1.2 V, T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

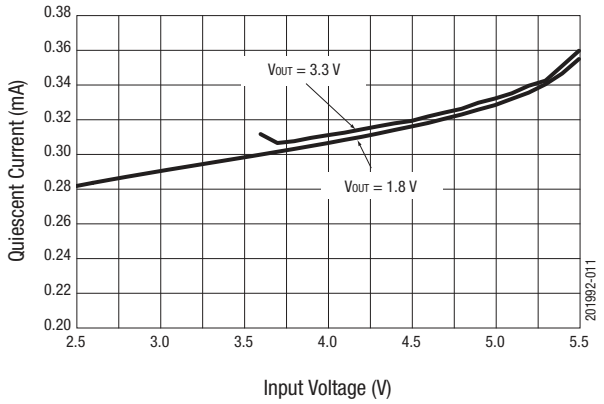


Figure 11. Quiescent Current vs Input Voltage
(T_A = 25 °C, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

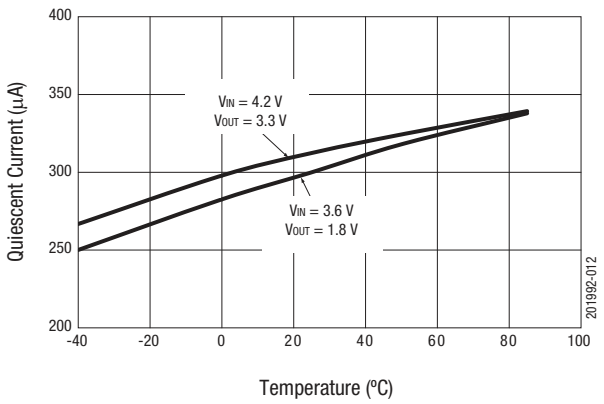


Figure 12. Quiescent Current vs Temperature
(L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

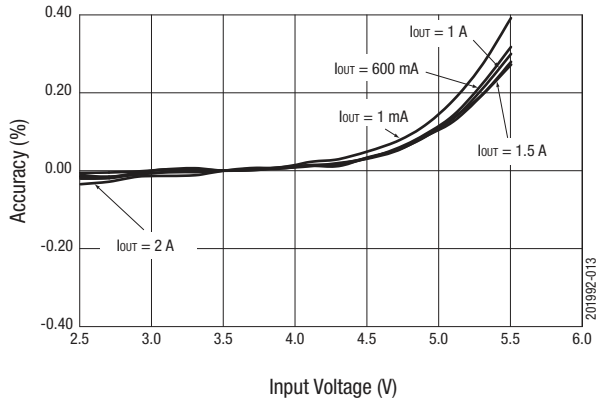


Figure 13. Line Regulation
(V_{OUT} = 1.8 V, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

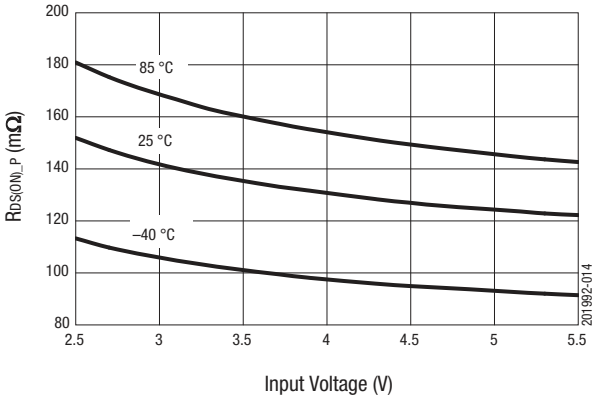


Figure 14. P-Channel $R_{DS(ON)}$ vs Input Voltage

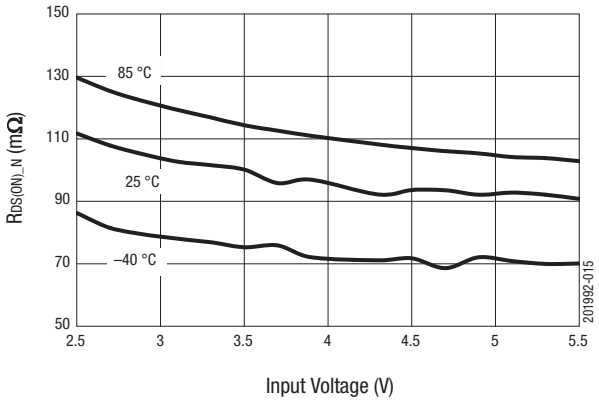


Figure 15. N-Channel $R_{DS(ON)}$ vs Input Voltage

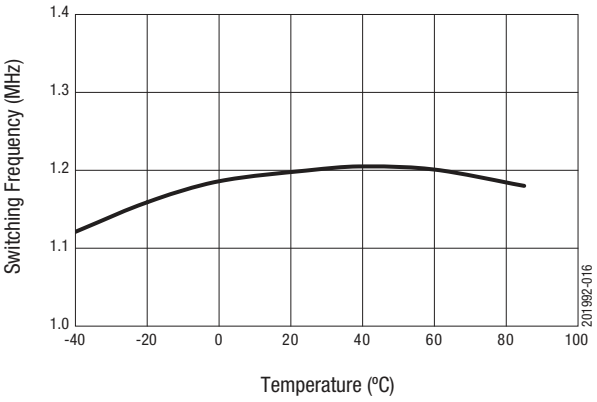


Figure 16. Switching Frequency vs Temperature (V_{IN} = 3.6 V, V_{OUT} = 1.8 V)

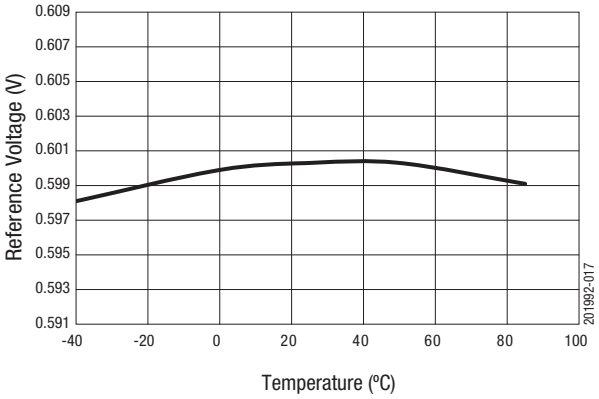


Figure 17. Reference Voltage vs Temperature (V_{IN} = 3.6 V)

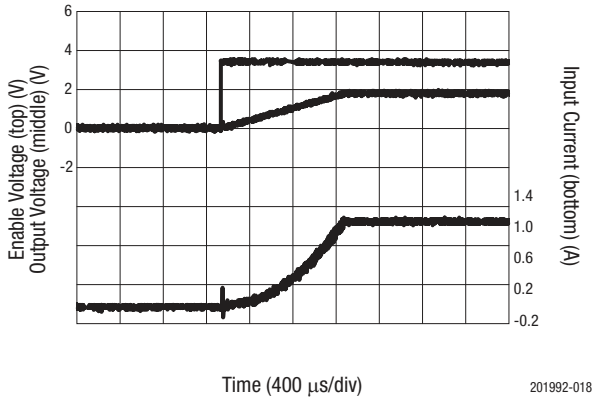


Figure 18. Soft Start (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 2 A, C_{FF} = 22 pF)

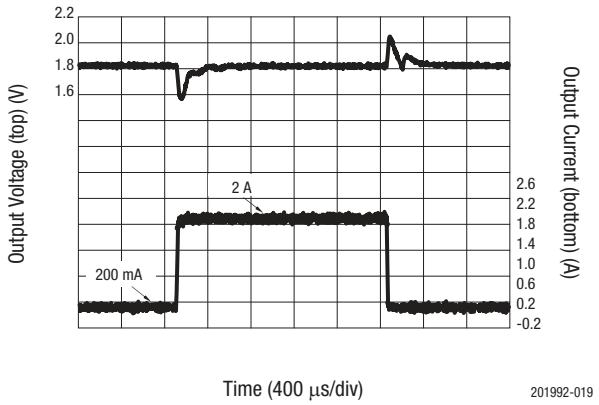


Figure 19. Load Transient Response (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, L = 2.2 µH, C_{IN} = C_{OUT} = 22 µF)

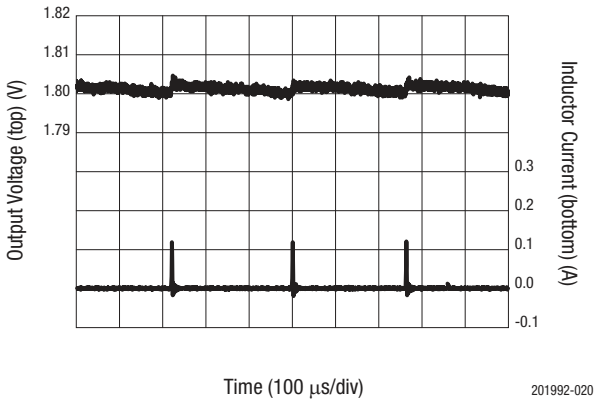


Figure 20. Output Ripple
(V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A, L = 2.2 μH)

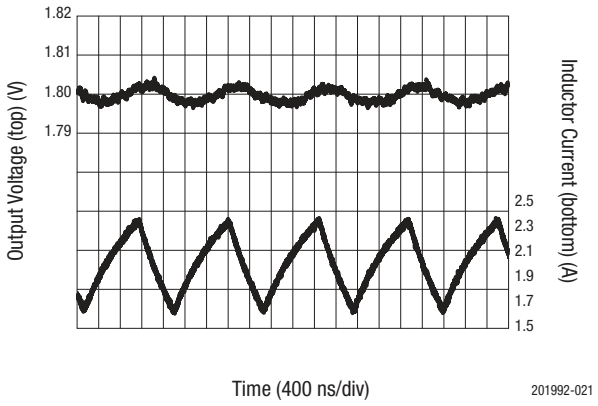
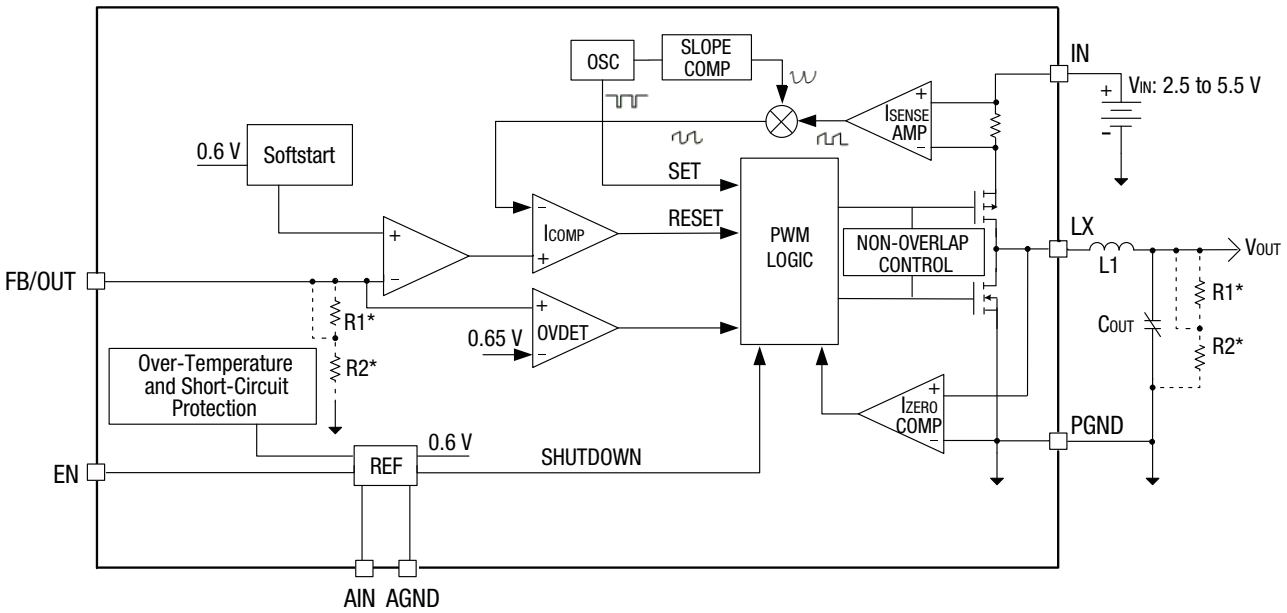


Figure 21. Output Ripple
(V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 2 A, L = 2.2 μH)



*The resistor divider R1 + R2 is internally set for the fixed output versions, and is externally set for the adjustable output versions.

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Figure 22. AAT1153 Functional Block Diagram

Functional Description

The AAT1153 is a high-output current monolithic switch-mode step-down DC-DC converter. The device operates at a fixed 1.2 MHz switching frequency, and uses a slope compensated current mode architecture. This step-down DC-DC converter can supply up to 2 A output current at V_{IN} = 3 V and has an input voltage range from 2.5 V to 5.5 V. It minimizes external component size and optimizes efficiency at the heavy load range. The slope compensation allows the device to remain stable over a wider range of inductor values so that smaller values (1 µH to 4.7 µH) with lower DCR can be used to achieve higher efficiency. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. The device can be programmed with external feedback to any voltage, ranging from 0.6 V to near the input voltage. It uses internal MOSFETs to achieve high efficiency and can generate very low output voltages by using an internal reference of 0.6 V. At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the low $R_{DS(ON)}$ drop of the P-channel high-side MOSFET and the inductor DCR. The internal error amplifier and compensation provides excellent transient response, load, and line regulation. Internal soft-start eliminates any output voltage overshoot when the enable or the input voltage is applied.

The functional block diagram is shown in Figure 22.

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for excellent load and line response with protection of the internal main switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET). During normal operation, the internal P-channel MOSFET is turned on for a specified time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. The current comparator, I_{COMP}, limits the peak inductor current. When the main switch is off, the synchronous rectifier turns on immediately and stays on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I_{ZERO}, or the beginning of the next clock cycle.

Control Loop

The AAT1153 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. A slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor. The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output

voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The error amplifier reference is fixed at 0.6 V.

Soft Start / Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. The enable pin is active high. When pulled low, the enable input (EN) forces the AAT1153 into a low-power, non-switching state. The total input current during shutdown is less than 1 μA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited to 3.5 A. To minimize power dissipation and stresses under current-limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. The termination lasts for seven consecutive clock cycles after a current limit has been sensed during a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 170 °C with 10 °C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Dropout Operation

When the battery input voltage decreases near the value of the output voltage, the AAT1153 allows the main switch to remain on for more than one switching cycle and increases the duty cycle until it reaches 100%. The duty cycle D of a step-down converter is defined as:

$$D = t_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where tON is the main switch on time and fOSC is the oscillator frequency. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor. At low input supply voltage, the RDS(ON) of the P-channel MOSFET increases, and the efficiency of the converter decreases. Caution must be exercised to ensure the heat dissipated does not exceed the maximum junction temperature of the IC.

Maximum Load Current

The AAT1153 operates with an input supply voltage as low as 2.5 V, however, the maximum load current decreases at lower input voltages due to a large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely, the current limit increases as the duty cycle decreases.

Applications Information

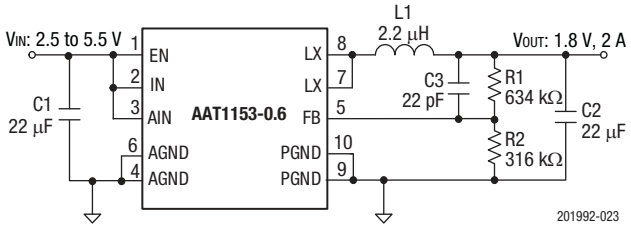


Figure 23. Basic Application Circuit

Setting the Output Voltage

Figure 23 shows the basic application circuit for the AAT1153. The AAT1153 can be externally programmed. Resistors R1 and R2 in Figure 23 program the output to regulate at a voltage higher than 0.6 V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59 kΩ. Although a larger value further reduces quiescent current, it also increases the impedance of the feedback node, making it more sensitive to external noise and interference. Table 4 summarizes the resistor values for various output voltages with R2 set to either 59 kΩ for good noise immunity or 316 kΩ for reduced no load input current.

The AAT1153, combined with an external feed forward capacitor (C3 in Figure 1), delivers enhanced transient response for extreme pulsed load applications. The addition of the feed forward capacitor typically requires a larger output capacitor C2 for stability. The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.6V \times \left(1 + \frac{R1}{R2}\right)$$

$$R1 = \left(\frac{V_{OUT}}{0.6V} - 1\right) \times R2$$

Table 4. Resistor Selections for Different Output Voltage Settings (Standard 1% Resistors Substituted for Calculated Values)

VOUT (V)	R1 (kΩ) (R2 = 59 kΩ)	R1 (kΩ) (R2 = 316 kΩ)
0.8	19.6	105
0.9	29.4	158
1.0	39.2	210
1.1	49.9	261
1.2	59.0	316
1.3	68.1	365
1.4	78.7	422
1.5	88.7	475
1.8	118	634
1.85	124	655
2.0	137	732
2.5	187	1000
3.3	267	1430

Inductor Selection

For most designs, the AAT1153 operates with inductor values of 1 µH to 4.7 µH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is inductor ripple current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 30% of the maximum load current 2 A, or

$$\Delta I_L = 600mA$$

For output voltages above 2.0 V, when light-load efficiency is important, the minimum recommended inductor is 2.2 µH.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR.

Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 20 mΩ to 100 mΩ range. For higher efficiency at heavy loads (above 200 mA), or minimal load regulation (but some transient overshoot), the resistance should be kept below 100 mΩ. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (2 A + 600 mA). Table 5 lists some typical surface-mount inductors that meet target applications for the AAT1153.

For example, the 2.2 µH CDRH5D16-2R2 inductor selected from Sumida has a 28.7 mΩ DCR and a 3.0 ADC current rating. At full load, the inductor DC loss is 57 mW which gives a 1.6% loss in efficiency for a 1200 mA, 1.8 V output.

Slope Compensation

The AAT1153 step-down converter uses peak current mode control with slope compensation for stability when duty cycles are greater than 50%. The slope compensation is set to maintain stability with lower value inductors which provide better overall efficiency. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. As an example, the value of the slope compensation is set to 1 A/µs which is large enough to guarantee stability when using a 2.2 µH inductor for all output voltage levels from 0.6V to 3.3 V.

The worst case external current slope (m) using the 2.2 µH inductor is when VOUT = 3.3 V and is:

$$m = \frac{V_{OUT}}{L} = \frac{3.3}{2.2} = 1.5A/\mu s$$

To keep the power supply stable when the duty cycle is above 50%, the internal slope compensation (mA) should be:

$$m_a \geq \frac{1}{2} \times m = 0.75A/\mu s$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. So the internal slope compensated value of 1 A/µs guarantees stability using a 2.2 µH inductor value for all output voltages from 0.6 V to 3.3 V.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current passing to the input. The calculated value varies with input voltage and is a maximum when VIN is double the output voltage.

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{OSC}}$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times 4 \times f_{OSC}}$$

A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22 µF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$I_{RMS(MAX)} = \frac{I_{OUT}}{2}$$

To minimize stray inductance, the capacitor is placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in Figures 24 and 25.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high-Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high-Q network and stabilizes the system.

Output Capacitor Selection

The function of output capacitance is to store energy to attempt to maintain a constant voltage. The energy is stored in the capacitor's electric field due to the voltage applied.

The value of output capacitance is generally selected to limit output voltage ripple to the level required by the specification.

Since the ripple current in the output inductor is usually determined by L, VOUT and VIN, the series impedance of the capacitor primarily determines the output voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C).

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_{OSC}}$$

In many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected.

For either continuous or discontinuous inductor current mode operation, the ESR of the COUT needed to limit the ripple to ΔVOUT, the peak-to-peak voltage is:

$$ESR \leq \frac{\Delta V_{OUT}}{\Delta I_L}$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. The output capacitor ripple current is the inductor current, IL, minus the output current, IOUT. The RMS value of the ripple current flowing in the output capacitance (continuous inductor current mode operation) is given by:

$$I_{RMS} = \Delta I_L \times \frac{\sqrt{3}}{6} = \Delta I_L \times 0.289$$

ESL can be a problem by causing ringing in the low megahertz region but can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

To meet the requirement of output voltage ripple small and regulation loop stability, ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple VOUT is determined by:

$$\Delta V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times f_{OSC} \times V_{IN}} \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

A 22 µF ceramic capacitor can satisfy most applications.

Thermal Calculations

There are three types of losses associated with the AAT1153 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_{OUT}^2 \times \left[R_{DS(ON)H} \times V_{OUT} + R_{DS(ON)L} \times \left(V_{IN} - V_{OUT}\right)\right]}{V_{IN}} + \left(t_{SW} \times f_{OSC} \times I_{OUT} + I_Q\right) \times V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{SW} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{OUT}^2 \times R_{DS(ON)H} + I_Q \times V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the DFN-10 package which is 45 °C/W.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA} + T_A$$

Layout Guidance

When laying out the PC board, the following layout guidelines should be followed to ensure proper operation of the AAT1153:

- The exposed pad (EP) must be reliably soldered to the GND plane. A PGND pad below EP is strongly recommended.
- The power traces, including the GND trace, the LX trace and the IN trace should be kept short, direct and wide to allow large current flow. The L1 connection to the LX pins should be as short as possible. Use several VIA pads when routing between layers.
- The input capacitor (C1) should connect as closely as possible to IN (Pin 2) and AGND (Pins 4 and 6) to get good power filtering.
- Keep the switching node, LX (Pins 7 and 8) away from the sensitive FB/OUT node.
- The feedback trace or OUT pin (Pin 2) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin (Pin 5) to minimize the length of the high impedance feedback trace.
- The output capacitor C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible and there should not be any signal lines under the inductor.
- The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Tables 5 and 6 lists the suggested component selection.

Table 5. Suggested Inductor Selection Information

Part Number	Inductance (µH)	Max DC Current (A)	DCR (mΩ)	Size L × W × H (mm)	Type	Manufacturer
CDRH5D16	2.2	3.0	28.7	5.8 × 5.8 × 1.8	Shielded	Sumida
CDRH5D16	3.3	2.6	35.6	5.8 × 5.8 × 1.8	Shielded	Sumida
CDRH8D28	4.7	3.4	19	8.3 × 8.3 × 3.0	Shielded	Sumida
SD53	2.0	3.3	23	5.2 × 5.2 × 3.0	Shielded	Coiltronics
SD53	3.3	2.6	29	5.2 × 5.2 × 3.0	Shielded	Coiltronics
SD53	4.7	2.1	39	5.2 × 5.2 × 3.0	Shielded	Coiltronics

Table 6 Suggested Capacitor Selection Information

Part Number	Value	Voltage (V)	Temp. Co.	Case	Manufacturer
GRM219R60J106KE19	10 µF	6.3	X5R	0805	Murata
GRM21BR60J226ME39	22 µF	6.3	X5R	0805	Murata
GRM1551X1E220JZ01B	22 pF	25	JIS	0402	Murata

Design Example

Specifications

V_{OUT} = 1.8 V @2 A

V_{IN} = 2.7 V to 4.2 V (3.6 V nominal)

f_{OSC} = 1.2 MHz

Transient droop = 200 mV

ΔV_{OUT} = 50 mV

1.8 V Output Inductor

$$\Delta I_L = 30\% \times I_{OUT} = 0.3 \times 2 = 600(mA)$$

$$L = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times \Delta I_L \times f_{OSC}} = \frac{1.8 \times (4.2 - 1.8)}{4.2 \times 0.6 \times 1.2 \times 10^6} = 1.4(\mu H)$$

For Sumida 2.2 µH inductor (CDRH2D14) with DCR 75 mΩ, the ΔI_L should be:

$$\Delta I_L = \frac{V_{OUT}}{L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times T = 395(mA)$$

$$I_{PKL} = I_{OUT} + \frac{\Delta I_L}{2} = 2 + \frac{0.395}{2} = 2.2(A)$$

$$P = I_{OUT}^2 \times DCR = (2)^2 \times 0.0287 = 114.8(mW)$$

1.8 V Output Capacitor

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_{OSC}} = \frac{3 \times 1.2}{0.2 \times 1.2 \times 10^6} = 25(\mu F); \quad use \quad 22\mu F$$

$$ESR \le \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{0.05}{0.395} = 0.13(\Omega)$$

Select a 22 µF, 10 mΩ ESR ceramic capacitor to meet the ripple 50 mV requirement.

$$\Delta V_{OUT} \le \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times f_{OSC} \times V_{IN}} \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right) = \frac{1.8 \times (4.2 - 1.8)}{2.2 \times 10^{-6} \times 1.2 \times 10^6 \times 4.2} \times \left(0.01 + \frac{1}{8 \times 1.2 \times 10^6 \times 22 \times 10^{-6}}\right) = 5.7(mV)$$

$$I_{RMS} = \Delta I_L \times 0.289 = 0.395 \times 0.289 = 114(mArms)$$

$$P_{COUT} = ESR \times I_{RMS}^2 = 0.01 \times 1^2 = 10(mW)$$

Input Capacitor

Input ripple V_{PP} = 25 mV

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times 4 \times f_{OSC}} = \frac{1}{\left(\frac{0.025}{2} - 0.01\right) \times 4 \times 1.2 \times 10^6} = 13.9(\mu F); \quad use \quad 22\mu F$$

$$I_{RMS} = \frac{I_{OUT}}{2} = \frac{2}{2} = 1(Arms)$$

$$P_{CIN} = ESR \times I_{RMS}^2 = 0.01 \times 1^2 = 10(mW)$$

AAT1153 Losses

$$P_{TOTAL} = I_{OUT}^2 \times R_{DS(ON)\_P} \times D + I_{OUT}^2 \times R_{DS(ON)\_N} \times (1 - D) + (t_{SW} \times f_{OSC} \times I_{OUT}) \times V_{IN}$$

$$= 2^2 \times 0.135 \times \frac{1.8}{4.2} + 2^2 \times 0.095 \times \left(1 - \frac{1.8}{4.2}\right) + \left(5 \times 10^{-9} \times 1.2 \times 10^6 \times 2\right) \times 4.2$$

$$= 498.9(mW)$$

Evaluation Board Description

The AAT1153 Evaluation Board is used to test the performance of the AAT1153. An Evaluation Board schematic diagram is provided in Figure 24. Layer details for the Evaluation Board are shown in Figure 25.

Package Information

Package dimensions for the 10-pin TDFN package are shown in Figure 26. Tape and reel dimensions are shown in Figure 27.

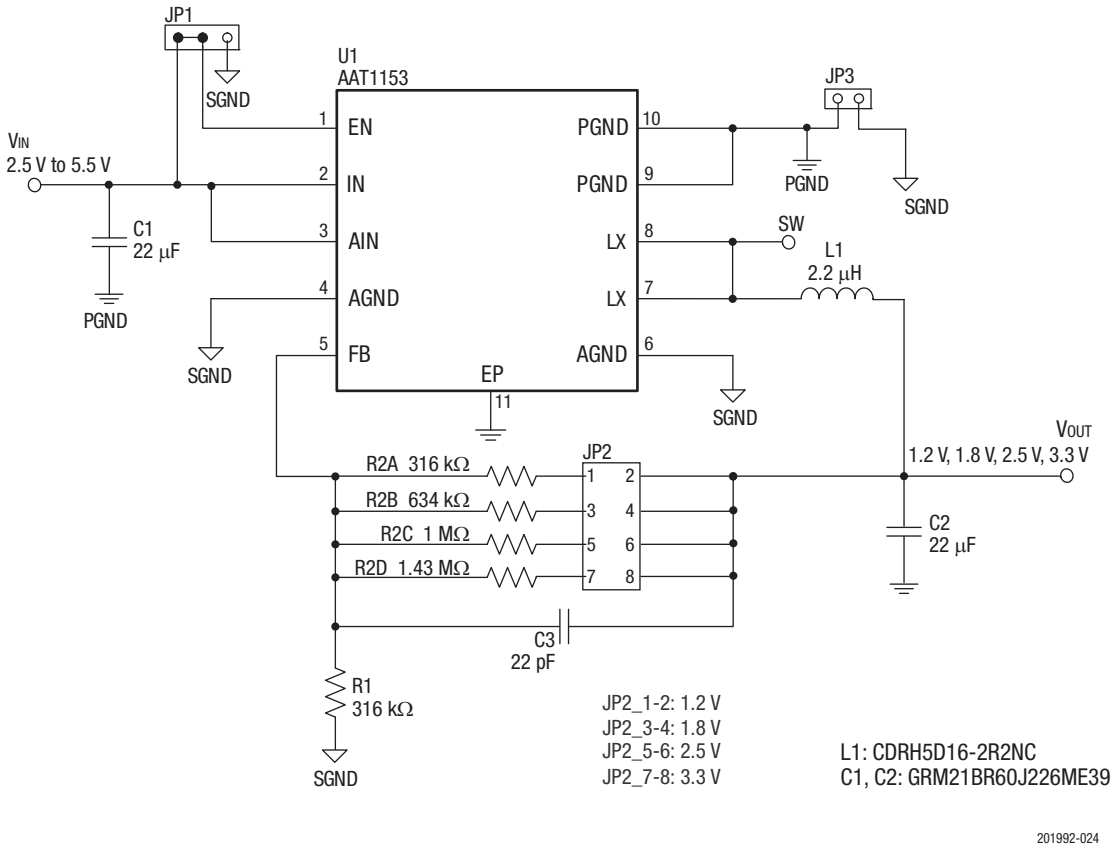
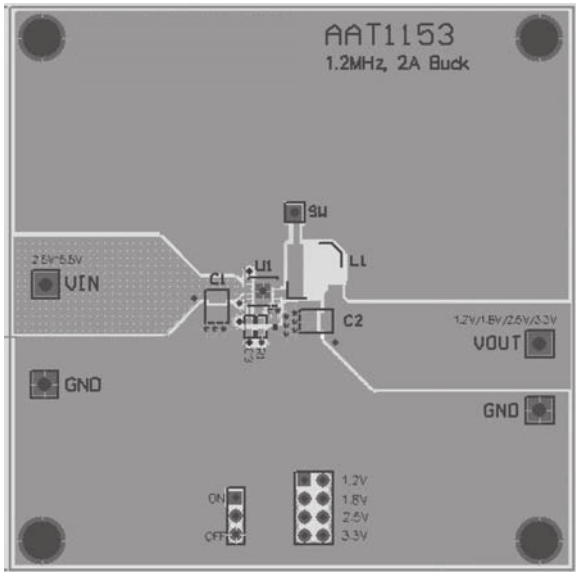
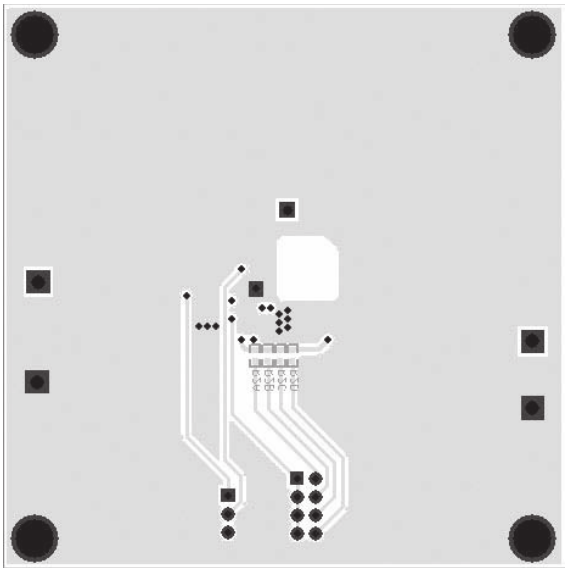


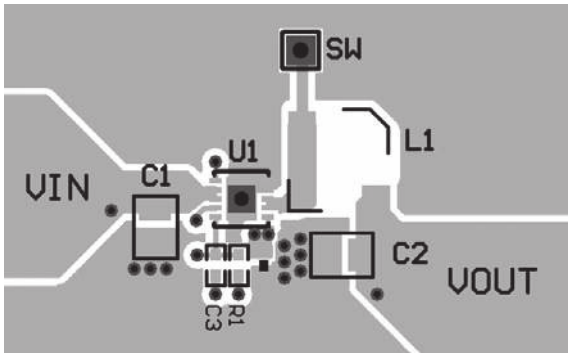
Figure 24. AAT1153 Evaluation Board Schematic



Component Side Layout



Solder Side Layout



Exploded View of Component Side Layout

201992-025

Figure 25. AAT1153 Evaluation Board Layer Details

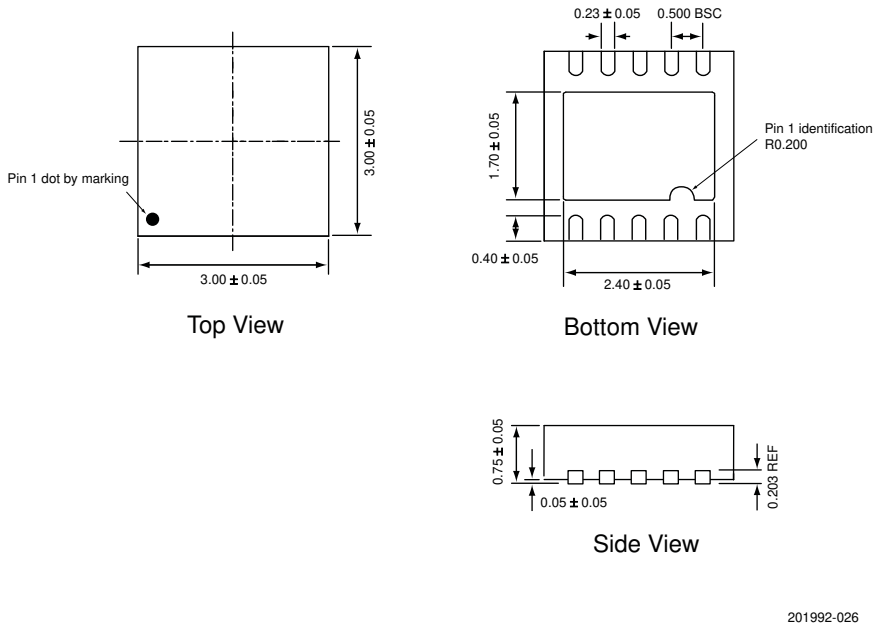


Figure 26. AAT1153 Package Dimensions

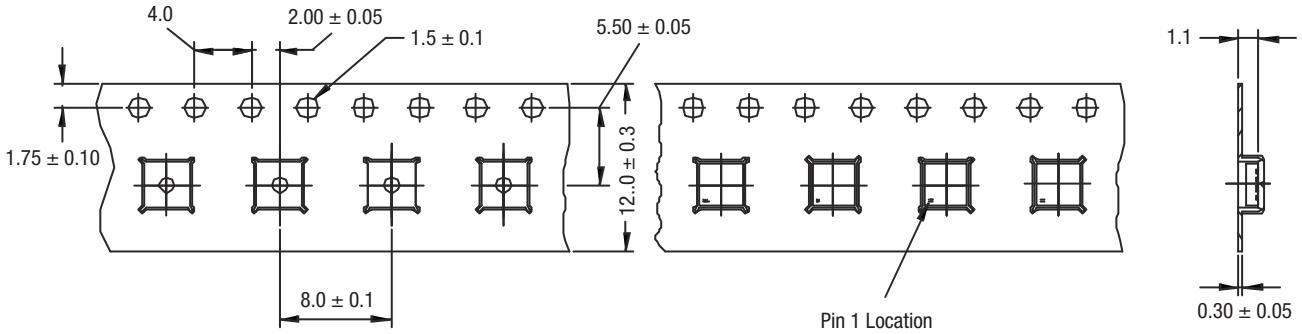


Figure 27. AAT1153 Tape and Reel Dimensions

Ordering Information

Model Name	Package	Marking	Manufacturing Part Number	Evaluation Board Part Number
AAT1153: 2 A Step-Down Converter	TDFN33-10[1]	ZSXYY[2]	**AAT1153IDE-0.6-T1**[3]	AAT1153IDE-0.6-EVB

[1] The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

[2] XYY = assembly and date code.

[3] Sample stock is generally held on all part numbers listed in **BOLD**.