



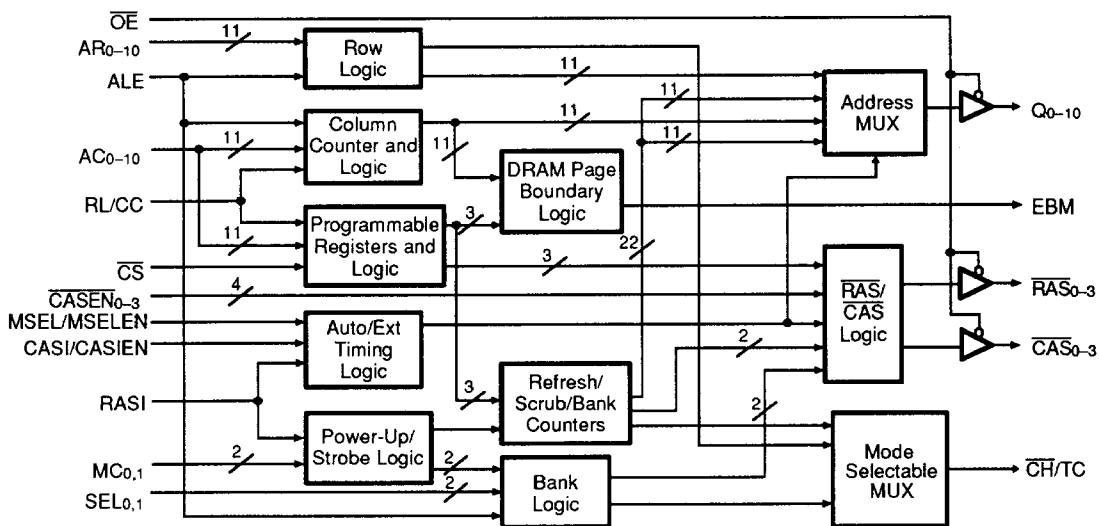
Am29C668

4M Configuration Dynamic Memory Controller/Driver

DISTINCTIVE CHARACTERISTICS

- Provides control for 4M, 1M, 256K, 64K dynamic RAMs
- Programmable Burst/Block Access support for Am29000, 68000 family, iAPX family
- Proprietary "Cache" Mode supports Page Mode accessing
- Nibble mode support (for Page Mode or Nibble Mode DRAMs)
- Selectable Address and Strobe autotiming or external timing
- Supports "Scrubbing" with refresh when used in an EDC system
- Supports CAS before RAS refresh
- Byte and Bank CAS Decoding
- Selectable 2 or 4 bank drive
- Outputs directly drive up to 88 DRAMs, with a guaranteed worst-case limit on the undershoot and overshoot
- Low-power advanced sub-micron CMOS process
- User configurable to replace Am2968A and Am29368 DMCs

BLOCK DIAGRAM



11068-001C

GENERAL DESCRIPTION

The Am29C668 4M Configurable Dynamic Memory Controller/Driver (CDMC) is designed for high performance memory systems. The CDMC acts as the address controller between the processor and the dynamic memory array. It uses its 11-bit row latch and 11-bit-column latch and counter to hold the row and column addresses, respectively, for multiplexing these to any DRAM size up to 4M. These latches and counter and the row/column refresh counter are used to directly drive the address lines of the DRAM array. The output of the 2-bit bank latch is decoded to select the bank to be accessed.

The Am29C668 has two basic modes of operation, read/write and refresh. In the read/write mode, the Am29C668 latches the row, column, and bank addresses and multiplexes them to the DRAM array. This

multiplexing occurs under the control of the internally-generated timing strobes in the Auto Timing Mode, or the externally-generated MSEL in External Timing Mode. The read/write mode of the Am29C668 may be optimized for the shortest memory access time, through burst/block access, "cache" mode access or nibble mode access.

In the refresh mode, the refresh address is generated by the Am29C668 refresh counter. This counter is automatically adjusted for different DRAM sizes. If memory scrubbing is not being implemented, only the row counter is used to generate the row address for refresh. When memory scrubbing is being performed in EDC systems, both the row and column address counters are used.

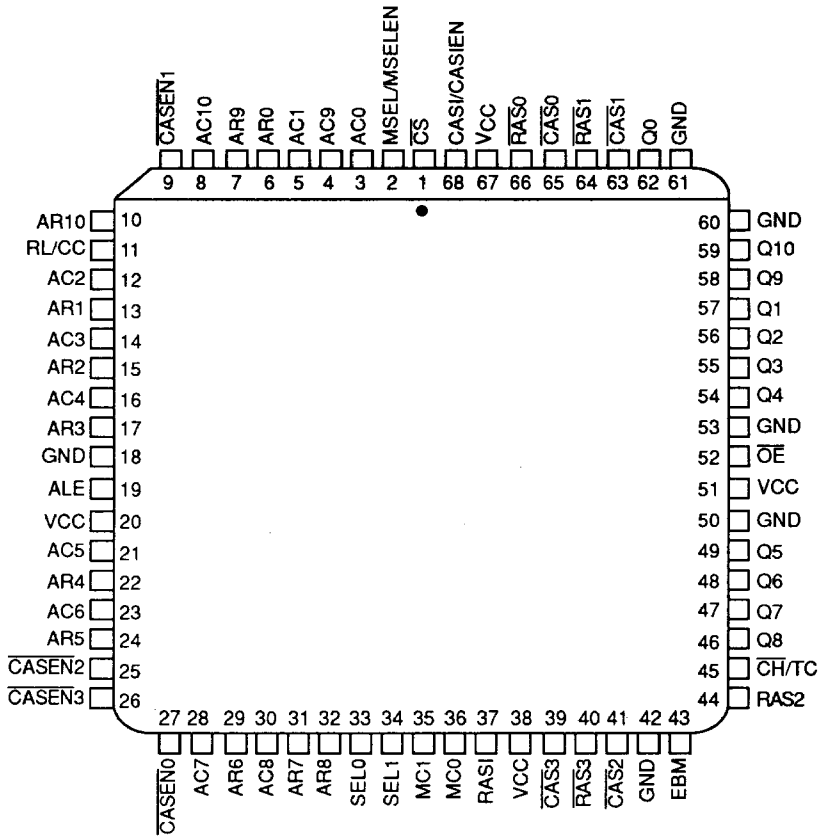
RELATED AMD PRODUCTS

Part No.	Description
Am29C60A	High Speed CMOS Cascadable 16-Bit EDC
Am29C660E	9 ns CMOS Cascadable 32-Bit EDC
Am29C676	11-Bit Driver for 4M x 1 and 4M x 4 DRAMs
Am29C983	9-Bit x 4-Port Multiple Bus Exchange
Am2965/6	8-Bit Dynamic RAM Driver Inverting/Non-Inverting
Am29C983A	9-Bit x 4-Port Multiple Bus Exchange, High Speed
Am29C985	9-Bit x 4-Port MBE with Parity
Am29C827A	10-Bit 48 mA Bus Buffer

CONNECTION DIAGRAM

Top View

PLCC



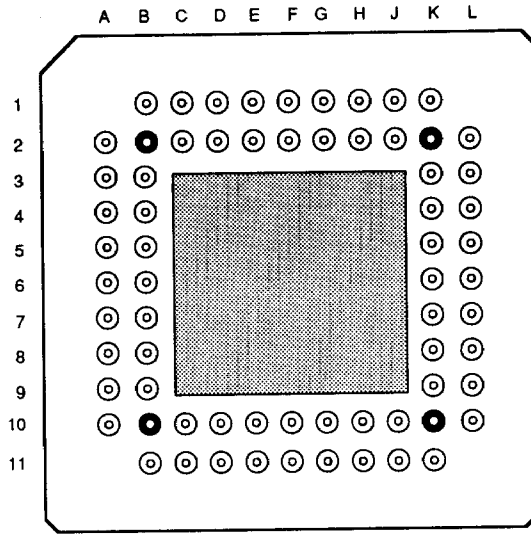
11068-002A

Note:

Pin 1 is marked for orientation (PLCC only).

CONNECTION DIAGRAM
Top View (Pins Pointing Down)

PGA*



11068-003A

*Pinout matches socketed PLCC pinout and footprint.

PGA PIN DESIGNATIONS

(Sorted by Pin Number)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
AR ₁₀	A-2	$\overline{\text{CASEN}}_2$	B-9	MC ₀	F-10	Q ₁	K-4
AC ₂	A-3	AC ₇	B-10	MC ₁	F-11	Q ₃	K-5
AC ₃	A-4	$\overline{\text{CASEN}}_0$	B-11	V _{CC}	G-1	GND	K-6
AC ₄	A-5	AR ₉	C-1	CASI/CASIEN	G-2	V _{CC}	K-7
GND	A-6	AC ₁₀	C-2	V _{CC}	G-10	Q ₅	K-8
V _{CC}	A-7	AC ₈	C-10	RASI	G-11	Q ₇	K-9
AR ₄	A-8	AR ₆	C-11	$\overline{\text{CAS}}_0$	H-1	$\overline{\text{CH/TC}}$	K-10
AR ₅	A-9	AC ₁	D-1	$\overline{\text{RAS}}_0$	H-2	EBM	K-11
$\overline{\text{CASEN}}_3$	A-10	AR ₀	D-2	$\overline{\text{RAS}}_3$	H-10	GND	L-2
$\overline{\text{CASEN}}_1$	B-1	AR ₈	D-10	$\overline{\text{CAS}}_3$	H-11	Q ₉	L-3
RL/CC	B-2	AR ₇	D-11	$\overline{\text{CAS}}_1$	J-1	Q ₂	L-4
AR ₁	B-3	AC ₀	E-1	$\overline{\text{RAS}}_1$	J-2	Q ₄	L-5
AR ₂	B-4	AC ₉	E-2	GND	J-10	$\overline{\text{OE}}$	L-6
AR ₃	B-5	SEL ₁	E-10	$\overline{\text{CAS}}_2$	J-11	GND	L-7
ALE	B-6	SEL ₀	E-11	GND	K-1	Q ₆	L-8
AC ₅	B-7	$\overline{\text{CS}}$	F-1	Q ₀	K-2	Q ₈	L-9
AC ₆	B-8	MSEL/MSELEN	F-2	Q ₁₀	K-3	$\overline{\text{RAS}}_2$	L-10

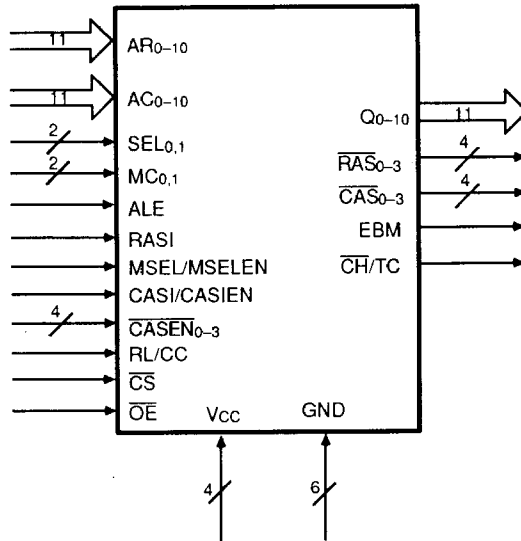
(Sorted by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
AC ₀	E-1	AR ₆	C-11	EBM	K-11	Q ₆	L-8
AC ₁	D-1	AR ₇	D-11	GND	A-6	Q ₇	K-9
AC ₂	A-3	AR ₈	D-10	GND	J-10	Q ₈	L-9
AC ₃	A-4	AR ₉	C-1	GND	K-1	Q ₉	L-3
AC ₄	A-5	AR ₁₀	A-2	GND	K-6	Q ₁₀	K-3
AC ₅	B-7	ALE	B-6	GND	L-2	$\overline{\text{RAS}}_0$	H-2
AC ₆	B-8	$\overline{\text{CH/TC}}$	K-10	GND	L-7	$\overline{\text{RAS}}_1$	J-2
AC ₇	B-10	$\overline{\text{CAS}}_0$	H-1	MC ₀	F-10	$\overline{\text{RAS}}_2$	L-10
AC ₈	C-10	$\overline{\text{CAS}}_1$	J-1	MC ₁	F-11	$\overline{\text{RAS}}_3$	H-10
AC ₉	E-2	$\overline{\text{CAS}}_2$	J-11	MSEL/MSELEN	F-2	RASI	G-11
AC ₁₀	C-2	$\overline{\text{CAS}}_3$	H-11	$\overline{\text{OE}}$	L-6	RL/CC	B-2
AR ₀	D-2	$\overline{\text{CASEN}}_0$	B-11	Q ₀	K-2	SEL ₀	E-11
AR ₁	B-3	$\overline{\text{CASEN}}_1$	B-1	Q ₁	K-4	SEL ₁	E-10
AR ₂	B-4	$\overline{\text{CASEN}}_2$	B-9	Q ₂	L-4	V _{CC}	A-7
AR ₃	B-5	$\overline{\text{CASEN}}_3$	A-10	Q ₃	K-5	V _{CC}	G-1
AR ₄	A-8	CASI/CASIEN	G-2	Q ₄	L-5	V _{CC}	G-10
AR ₅	A-9	$\overline{\text{CS}}$	F-1	Q ₅	K-8	V _{CC}	K-7

PGA to PLCC PIN CONVERSION

A2	10	B9	25	F10	36	K4	57
A3	12	B10	28	F11	35	K5	55
A4	14	B11	27	G1	67	K6	53
A5	16	C1	7	G2	68	K7	51
A6	18	C2	8	G10	38	K8	49
A7	20	C10	30	G11	37	K9	47
A8	22	C11	29	H1	65	K10	45
A9	24	D1	5	H2	66	K11	43
A10	26	D2	6	H10	40	L2	60
B1	9	D10	32	H11	39	L3	58
B2	11	D11	31	J1	63	L4	56
B3	13	E1	3	J2	64	L5	54
B4	15	E2	4	J10	42	L6	52
B5	17	E10	34	J11	41	L7	50
B6	19	E11	33	K1	61	L8	48
B7	21	F1	1	K2	62	L9	46
B8	23	F2	2	K3	59	L10	44

LOGIC SYMBOL



Die Size: 0.233" x 0.165"

Gate Count: 3600

11068-004B

Package Information

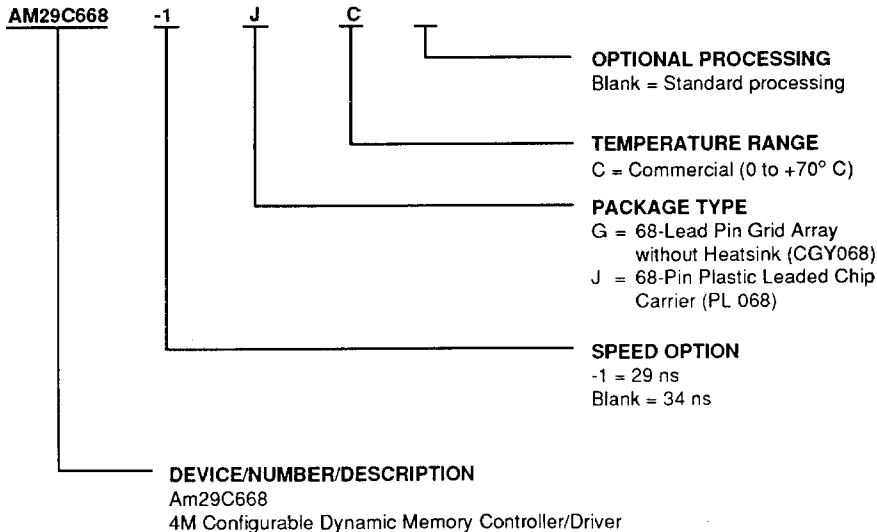
Parameter	PGA	PLCC	Units
θ_{JA}	34	35	°C/W

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of these elements:

- Device Number
- Speed Option (if applicable)
- Package Type
- Temperature Range
- Optional Processing



Valid Combinations	
AM29C668	JC, GC
AM29C668-1	

Valid Combinations

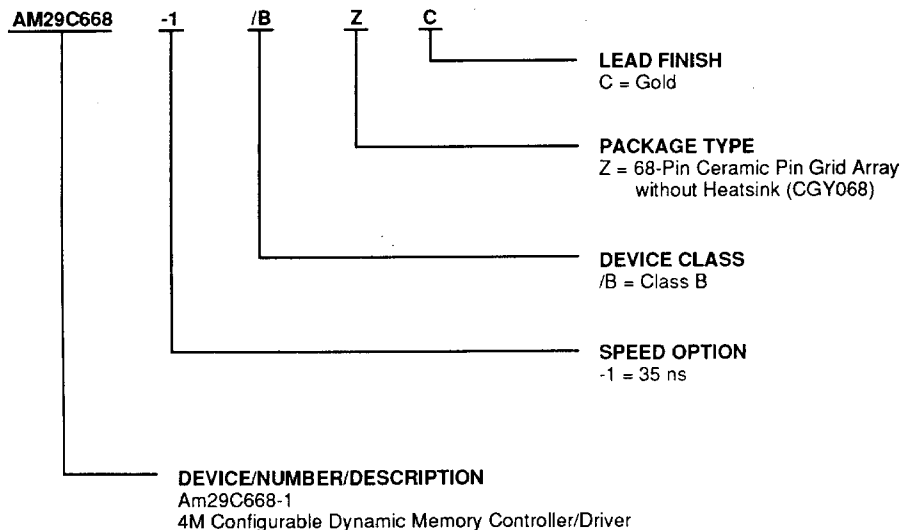
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of these elements:

- Device Number
- Speed Option (if applicable)
- Device Class
- Package Type
- Lead Finish



Valid Combinations	
AM29C668-1	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11

PIN DESCRIPTION

AC₀₋₁₀ and AR₀₋₁₀

Column and Row Address Inputs (Inputs(22))

The address on these lines is latched by the LOW going edge of the Address Latch Enable (ALE) signal. AC₀₋₁₀ are connected to the lower side of the system address bus and are driven on the output address lines Q₀₋₁₀ when the MSEL (Multiplexer Select) signal is HIGH. AR₀₋₁₀ are connected to the upper side of the system address bus and are driven on the output address lines Q₀₋₁₀ when the MSEL signal is LOW.

AC₀₋₇ and AR₀₋₇ are used for 64K DRAMs.
AC₀₋₈ and AR₀₋₈ are used for 256K DRAMs.
AC₀₋₉ and AR₀₋₉ are used for 1M DRAMs.
AC₀₋₁₀ and AR₀₋₁₀ are used for 4M DRAMs.

ALE

Address Latch Enable (Input; Active HIGH)

This input causes the Row Latch, Column Latch and Counter, and the Bank Latch to become transparent allowing the latches to accept new input data. A LOW input on ALE latches the input data, assuming it meets specified set-up and hold requirements.

$\overline{\text{CH}}/\text{TC}$

Cache Hit/Terminal Count (Outputs; Active LOW/HIGH)

This is a dual function output, dependent upon the Mode Control inputs in the Configuration Register. If the Mode Control inputs are 1,0 (MC_{0,1} = 10) the Am29C668 is in the Refresh-With-Scrubbing or Initialize mode and this output acts as the Terminal Count (TC).

Cache Hit ($\overline{\text{CH}}$) (if bit #6 in the configuration register is set to "1")

This output goes active (LOW) when the current memory access is to the same row and the same bank as the previous access. The $\overline{\text{CH}}$ signal is used to facilitate Fast Page Mode or Static Column accesses.

As **Terminal Count**, this output goes active (HIGH) when the Refresh Counter has gone through an entire count. The Refresh Counter is user configured for DRAM size (64K, 256K, 1M, 4M) and number of banks (2 or 4), which are programmable via the Memory Size Bits and the $\overline{\text{RAS}}/\overline{\text{CAS}}$ Configuration Bit, respectively, in the Configuration Register (Reference Figure 6). The TC signal is used to indicate the end of initialization in an Error Detection and Correction (EDC) system.

$\overline{\text{CAS}}_{0-3}$

Column Address Strobe (Outputs (4); Active LOW; Three State)

Each $\overline{\text{CAS}}_n$ output will go active when selected by SEL_{0,1} in a bank-wise $\overline{\text{CAS}}$ decoding method (CDM = 0, reference Figure 6) or when selected by $\overline{\text{CASEN}}_{0-3}$ in a byte-wise $\overline{\text{CAS}}$ decoding implementation. This will occur only when CASI goes active in the External Timing

Mode or when CASIEN and the internally generated $\overline{\text{CAS}}$ go active in the Auto Timing Mode.

Each output provides a $\overline{\text{CAS}}_n$ signal to one of four banks of the dynamic memory, if four banks are used. If two banks are used, each bank can use 2 $\overline{\text{CAS}}_n$ signals to reduce the capacitive load on each. The number of banks (2 or 4) is programmable via the $\overline{\text{RAS}}/\overline{\text{CAS}}$ Configuration Bit in the Configuration Register (reference Table 4).

The $\overline{\text{CAS}}_n$ outputs contain pull-up resistors which ensure a logical HIGH (inactive) when in the high impedance state.

$\overline{\text{CASEN}}_{0-3}$

Column Address Strobe Enable (Inputs (4); Active LOW)

When a byte-wise method is used for $\overline{\text{CAS}}$ decoding these four inputs are decoded externally to handle byte operations. The timing generation may be Auto or External. Only those $\overline{\text{CAS}}_n$ outputs will be activated whose corresponding $\overline{\text{CASEN}}_n$ inputs are selected by the external byte decode circuit.

When a bank-wise method is used for $\overline{\text{CAS}}$ decoding these inputs are not used.

CASI/CASIEN

Column Address Strobe Input/Column Address Strobe Input Enable (Input; Active HIGH)

This is a dual function input. In the External Timing mode this input is used as CASI. With a bank-wise $\overline{\text{CAS}}$ decoding method, the internally decoded $\overline{\text{CAS}}_n$ output is forced LOW after CASI goes active. When used as CASI with a byte-wise decoding method, the selected $\overline{\text{CAS}}_n$ output is forced LOW depending upon the externally decoded $\overline{\text{CASEN}}_n$ inputs after CASI goes active.

In Auto Timing Mode this input is used as CASIEN. With a bank-wise $\overline{\text{CAS}}$ decoding method, the decoded $\overline{\text{CAS}}_n$ output is forced LOW, if both the internally generated $\overline{\text{CAS}}$ and the CASIEN signals are active. This input is used to delay the $\overline{\text{CAS}}_{0-3}$ outputs from going active if desired, resulting in a longer auto timing access sequence. This input is generally not used as CASIEN with a byte-wise $\overline{\text{CAS}}$ decoding implementation.

$\overline{\text{CS}}$

Chip Select (Input; Active LOW)

This input is used to enable the Am29C668. When active, the Am29C668 operates normally in all four modes. When $\overline{\text{CS}}$ goes inactive (HIGH), the device will not enter the Read/Write mode.

EBM

End Burst/Block Mode (Output Active HIGH)

This output is only used in the burst/block mode of data transfer. It indicates to the processor that the Am29C668 cannot perform any more data transfers in

the burst/block mode for one of two reasons. Either the DRAM page boundary is reached (in which case a new row address is required from the processor), or a programmed allowable number of transfers has been completed.

GND (6) 0 V Power Supply

These pins are the 0 V power supply for the Am29C668. All grounds must be connected for proper device operation.

MC_{0,1} Mode Control (Inputs (2))

These inputs specify one of four modes of operation of the Am29C668. Operating modes are described in Table 1.

MSEL/MSELEN

Multiplexer Select/Multiplexer Select Enable (Input; Active HIGH)

This is a dual function input. In the External Timing mode this input is used as **MSEL**. When MSEL is HIGH the column address is selected. When MSEL is LOW the row address is selected.

In the Auto Timing Mode this input acts as **MSELEN**. When MSELEN is HIGH and the internally generated MSEL is active the column address is selected. When MSELEN is LOW or the internally generated MSEL is inactive the row address is selected. MSELEN is used to delay the address change from row to column, if desired, resulting in a longer auto timing access sequence.

The address may come from either the address latches and counter or the refresh address counter depending upon MC_{0,1}. The MSEL/MSELEN input is only applicable in the Read/Write or Refresh with Scrubbing Modes.

OE

Output Enable (Input; Active LOW)

This input enables/disables the output signals. When \overline{OE} is inactive (HIGH), all address outputs of the Am29C668 enter a high impedance state and the \overline{RAS}_n and \overline{CAS}_n outputs are pulled inactive (HIGH).

Q₀₋₁₀

Address Outputs (Outputs(11); Three State)

These edge rate controlled outputs drive the dynamic memory address inputs. The drivers on these lines are able to drive high capacitive loads, which are specified at 350pF. Greater capacitive loads may also be driven, however. See section labeled "Typical Change in Propagation Delay vs Loading Capacitance" following the AC Characteristics.

RAS₀₋₃

Row Address Strobe (Outputs (4); Active LOW; Three State)

Each Row Address Strobe output provides a \overline{RAS}_n signal to one of four memory banks. Each will go low when selected by SEL_{0,1} and only when RAS_I goes HIGH. All four go LOW in response to RAS_I in the refresh modes.

When a 2 bank $\overline{RAS}/\overline{CAS}$ configuration is selected (RCC = 1), RAS₀ and RAS₁ are tied together internally, as are RAS₂ and RAS₃. This reduces the capacitive loading on the \overline{RAS}_n outputs in a two bank system (reference Table 4).

In four bank mode, the \overline{RAS}_n outputs are decoded with SEL_{0,1}. In two bank mode these outputs are decoded with SEL₀. In this case SEL₁, should be tied LOW.

The RAS_n outputs contain pull-up resistors which ensure a logical HIGH (inactive) when in the high impedance state.

RAS_I

Row Address Strobe Input (Input; Active HIGH)

During normal memory cycles, the decoded \overline{RAS}_n outputs ($\overline{RAS}_0, \overline{RAS}_1, \overline{RAS}_2, \overline{RAS}_3$) as determined by SEL_{0,1} and the RCC bit in the Configuration Register are forced LOW after RAS_I goes active HIGH. During refresh, all four RAS_n outputs go LOW after RAS_I goes active HIGH. If auto timing is enabled, the HIGH going edge of RAS_I also initiates the internal timing cycle and its LOW going edge terminates the internal timing cycle.

RL/CC

Register Load/Column Clock (Input)

This is a dual function pin which depends upon the Mode Control inputs (MC_{0,1}). If MC_{0,1} = 11, the Am29C668 is in the Reset Mode and this pin acts as the Register Load signal. If MC_{0,1} = 01 the Am29C668 is in the Read/Write Mode and this input acts as the Column Clock signal.

When used as **Register Load**, the LOW-to-HIGH edge of the signal loads either the Burst Count Register, the Mask Register, or the Configuration Register via the AC₀₋₁₀ Address Inputs. (Reference Figure 5).

When used as **Column Clock**, the HIGH-to-LOW edge of the signal increments the Column Counter during burst and nibble mode accessing.

SEL_{0,1}

Bank Select (Inputs (2))

These two inputs are the highest-order address bits when the Am29C668 is used in the normal access mode or in the burst/block access mode. SEL_{0,1} is used in the Read/Write Mode to select which bank of memory will receive the \overline{RAS}_n and \overline{CAS}_n signals when RAS_I and CAS_I (or the internally generated CAS in the auto-timing mode) go active HIGH. The \overline{CAS}_n signals will not be decoded from SEL_{0,1} if a byte-wise \overline{CAS} decoding scheme is selected. In two bank mode, only SEL₀ is used. SEL₁ should be tied LOW.

V_{CC} (4) + 5 V

Positive Power Supply Voltage

These inputs provide the power necessary to operate the Am29C668. All power supply inputs must be connected for proper device operation.

Table 1. Mode Control Function

MC ₀	MC ₁	Operating Mode
0	0	<p>Refresh Without Scrubbing (a more detailed description can be found in the section entitled "Refresh Modes")</p> <p>a) $\overline{\text{RAS}}$-Only Refresh: Refresh cycles are performed with only the row refresh counter being used to increment addresses. In this mode, all four $\overline{\text{RAS}}_n$ outputs are active while the four $\overline{\text{CAS}}_n$ outputs are held inactive.</p> <p>b) $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh: Refresh addresses are generated internally by the DRAMs. In this mode, all four $\overline{\text{CAS}}_n$ outputs are active followed by all four $\overline{\text{RAS}}_n$ outputs going active. This new type of refresh is selected via the CBR-bit in the Configuration Register. In this mode, RASI controls the $\overline{\text{CAS}}_n$ outputs and CASI controls the $\overline{\text{RAS}}_n$ outputs.</p>
1	0	<p>Refresh With Scrubbing/Initialize (EDC Systems)</p> <p>This mode may be used only in systems with Error Detection and Correction (EDC) capability. In this mode, refresh cycles are performed with both the row and column refresh counters generating the addresses. MSEL is used to select between the row and column addresses. All four $\overline{\text{RAS}}_n$ signals go active in response to RASI and one $\overline{\text{CAS}}_n$ output goes active in response to CASI. The CAS_n output is decoded from the bank refresh counter. The remaining three $\overline{\text{CAS}}_n$ outputs are left inactive, while their respective banks undergo normal refresh. This mode is also used to initialize the memory array by writing a known data pattern and corresponding check bits.</p>
0	1	<p>Read/Write</p> <p>This mode is used to perform read/write operations. The row address is taken from the row latch and the column address is taken from the column latch and counter. $\text{SEL}_{0,1}$ are decoded to determine which $\overline{\text{RAS}}_n$ and $\overline{\text{CAS}}_n$ will be active.</p>
1	1	<p>Reset/Configuration</p> <p>This mode is used to clear the refresh counters and the Register Logic. These operations are performed on the HIGH-to-LOW transition of RASI. This mode is used to load the configuration, burst count, and mask registers.</p>

Table 2. Address Output Function

\overline{CS}	MC ₁	MC ₀	Internal MSEL	Mode	Address Multiplexer Output
0	0	0	X	Refresh W/O Scrubbing	Row Counter
	0	1	1	Refresh with Scrubbing	Column Counter
			0		Row Counter
	1	0	1	Read/Write	Column Latch
			0		Row Latch
	1	1	X	Reset/Configuration	All Zero
	1	0	0	X	Refresh W/O Scrubbing
0		1	1	Refresh with Scrubbing	Column Counter
			0		Row Counter
1		0	X	Read/Write	All Zero
1		1	X	Reset	All Zero

X = Don't care

Table 3. $\overline{\text{RAS}}$ Output Function

Inputs						Outputs			
Internal RAS _i	$\overline{\text{CS}}$	MC	SEL*	RCC**	MODE	$\overline{\text{RAS}}_n$			
		1 0	1 0			3	2	1	0
0	X	X X	X X	X	No operation	1	1	1	1
1	0	0 0	X X	X	Refresh W/O Scrubbing	0	0	0	0
		0 1	X X	X	Refresh with Scrubbing	0	0	0	0
		1 0	0 0	0	Read/Write	1	1	1	0
			X 0	1		1	1	0	0
			0 1	0		1	1	0	1
			X 1	1		0	0	1	1
			1 0	0		1	0	1	1
			X 0	1		1	1	0	0
			1 1	0		0	1	1	1
			X 1	1		0	0	1	1
	1 1	X X	X	Reset/Configuration		0	0	0	0
	1	0 0	X X	X		Refresh W/O Scrubbing	0	0	0
		0 1			Refresh with Scrubbing	0	0	0	0
		1 0			Read/Write	1	1	1	1
1 1		Reset			0	0	0	0	

* After Internal RAS_i is asserted, changing SEL_{0,1} will not effect the $\overline{\text{RAS}}_n$ decoding until Internal RAS_i is deasserted.

** Reference Figure 6.

Table 4. $\overline{\text{RAS}}/\overline{\text{CAS}}$ Configuration Decode*

RCC	Mode	$\overline{\text{RAS}}/\overline{\text{CAS}}$ CONFIGURATION		
0	4-Bank	RAS ₀	CAS ₀	BANK 0
		RAS ₁	CAS ₁	BANK 1
		RAS ₂	CAS ₂	BANK 2
		RAS ₃	CAS ₃	BANK 3
1	2-Bank	RAS ₀	CAS ₀	BANK 0
		RAS ₁	CAS ₁	
		RAS ₂	CAS ₂	BANK 1
		RAS ₃	CAS ₃	

*CDM = 0

Table 5. $\overline{\text{CAS}}$ Output Function

Inputs								Outputs							
CDM**	Internal CASI†	$\overline{\text{CS}}$	CBR**	MC	SEL*	Internal Counter	RCC**	$\overline{\text{CAS}}_n$							
				1 0	1 0	1 0		3	2	1	0				
0	1	0	1	0 0	X X	X X	X	0	0	0	0				
			0					1	1	1	1				
			1	0	0 1	X X	X X	X X	X	1	1	1	1		
			0							1	1	1	0		
			1							1	1	0	0		
			0							1	1	0	1		
			1							0	0	1	1		
			0							1	0	1	1		
			1							1	1	0	0		
			0							0	1	1	1		
			1	0	0	1	1								
			0	X	1 0	0 0	X X	X X	X	0	1	1	1	0	
			1							1	1	0	0		
			0							1	1	0	1		
			1							0	0	1	1		
			0	1	0	1	1								
		1	1	1	0	0									
		0	0	1	1	1									
		1	0	0	1	1									
		1	0	0	1	1									
		1	1	X X	X X	X X	X	1	1	1	1				
		1	0	1	1	0 0	X X	X X	X	0	0	0	0		
					0					1	1	1	1		
					1	0	0 1	X X	X X	X X	X	1	1	1	1
					0							1	1	1	0
					1							1	1	0	0
					0							1	1	0	1
					1							0	0	1	1
					0							1	0	1	1
				1	1							1	0	0	
				0	0							1	1	1	
				1	0	0	1	1							
X	1 0			X X	X X	X	1	1	1	1					
X	1 1			X X	X X	X	1	1	1	1					
0	X			X	X X	X X	X X	X	1	1	1	1			

† In the external timing mode, Internal CASI follows the CASI input. In Autotiming Mode, this signal is generated internally and is enabled by the CASIEN inputs.

* After Internal RASI is asserted, changing SEL_{0,1} will not effect the $\overline{\text{CAS}}_n$ decoding until Internal RASI is deasserted.

** Reference Figure 6. For CDM = 1, $\overline{\text{CASEN}} = 3$ will enable their respective $\overline{\text{CAS}}_0 = 3$ in read/write mode.

FUNCTIONAL DESCRIPTION (Note 1)

General Description

The Am29C668 4M Configurable Dynamic Memory Controller/Driver provides the controls required to operate dynamic RAMs up to 4Mbit x n. Manufactured in sub-micron CMOS technology, the Am29C668 performs the address control and generation function and strobe control and generation for 64K, 256K, 1M or 4M DRAMs. The Am29C668 controls the address to the DRAMs from the processor in the read/write mode and it generates and controls the address to the DRAMs in the refresh mode. The Am29C668 also generates the row and column address strobe signals in the read/write and refresh modes.

The Am29C668 has on-chip series damping resistors on its driver outputs to restrict the output signals to +0.8-V overshoot and -1.0V undershoot maximum (See Switching Waveforms).

Logic Overview

The functional blocks of the Am29C668 can be summarized as follows (reference block diagram):

- Row Logic
- Column Counter and Logic
- Bank Logic
- Programmable Registers and Logic
- Auto/External Timing Logic
- Power-Up/Strobe Logic
- DRAM Page Boundary Logic
- Refresh/Scrubbing/Bank Counters
- Address Multiplexer
- RAS/CAS Logic

Row Logic

This block (Figure 1) consists of a Row Latch, a Register, and a Comparator. The 11-bit Row Latch holds the DRAM row address. It is transparent when the Address Latch Enable signal is HIGH, and the address is latched on the LOW-going edge of ALE.

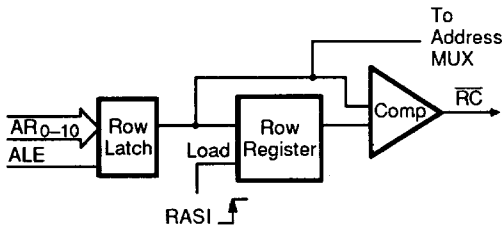


Figure 1. Row Logic

11068-005A

Note:

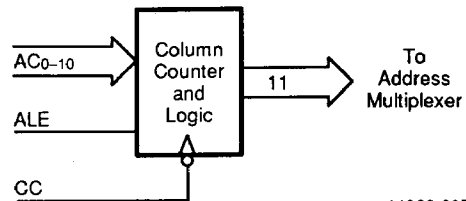
1. Modes of operation are described beginning on page 22.

The 11-bit Row Register holds the row address of the previous DRAM access. The register is clocked at the beginning of every access where $MC_{0,1} = 01$ by the HIGH-going edge of the RAS1 input.

The Row and Bank Comparator compares the row and bank addresses of the current access with the row address of the previous access and generates the Cache Hit (\overline{CH}) signal. \overline{CH} is LOW if the current row and bank addresses are the same as the previous row and bank addresses, respectively. \overline{CH} is high if they are not. This indicator is used by the external timing generator during Cache Mode accesses. The RAS1 input is held active (HIGH) if consecutive accesses are to the same row in the same bank, saving precharge time and access time on the current RAS_n . The RAS1 input is deactivated if consecutive accesses are to different rows or banks, thereby ending the "cache" access.

Column Counter and Logic

The block (Figure 3) consists of the Column Latch and Counter. The 11-bit loadable counter holds the DRAM column address. The counter is transparent when ALE is HIGH and the address is loaded on the LOW-going edge of ALE. The HIGH-to-LOW edge of the signal increments the Column Counter. ALE must be LOW in order to increment the counter.



11068-007A

Figure 3. Column Counter and Logic

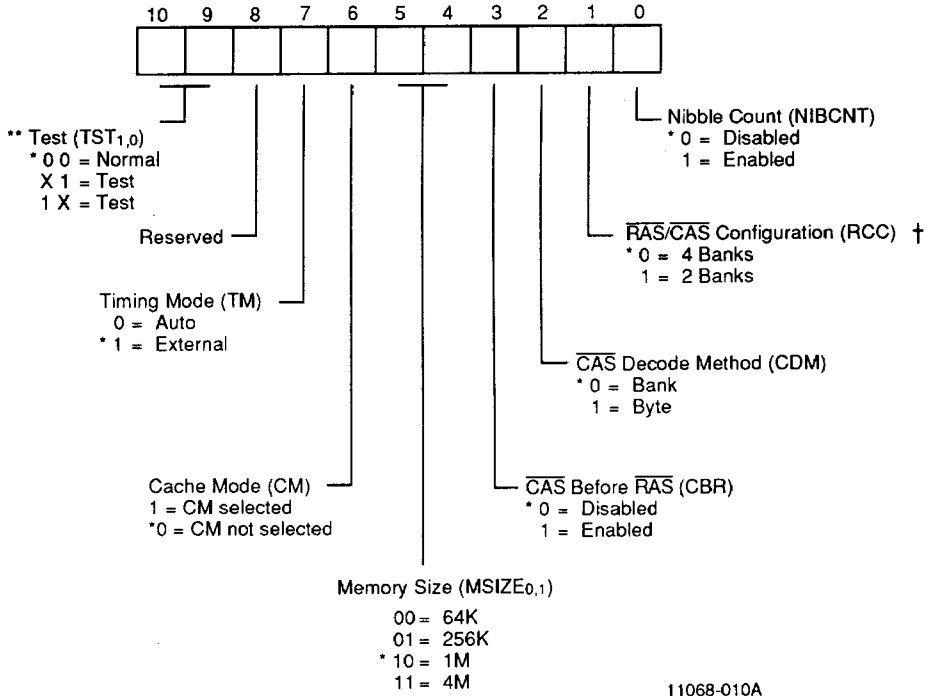
If the Nibble Count bit of the Configuration Register is enabled (NIBCNT = 1), then only the two LSBs of the Column Latch are clocked, generating a modulo four nibble count (Reference Nibble Mode section).

is used only in the Burst/Block mode of access. Reference Figure 6a.

The Register Load Logic loads the Burst Count, Mask and Configuration Registers via the address bus (AC₀₋₁₀) dependent upon the state of the Register Load-

ing diagram in Figure 7. RL/CC Decoder and Register Load Logic are shown in Figure 8.

The DRAM Size Decoder determines the DRAM size being used. The MSIZE_{1,0} bits in the Configuration Register are used to decode the size of the DRAMs being used as shown in Figure 6.

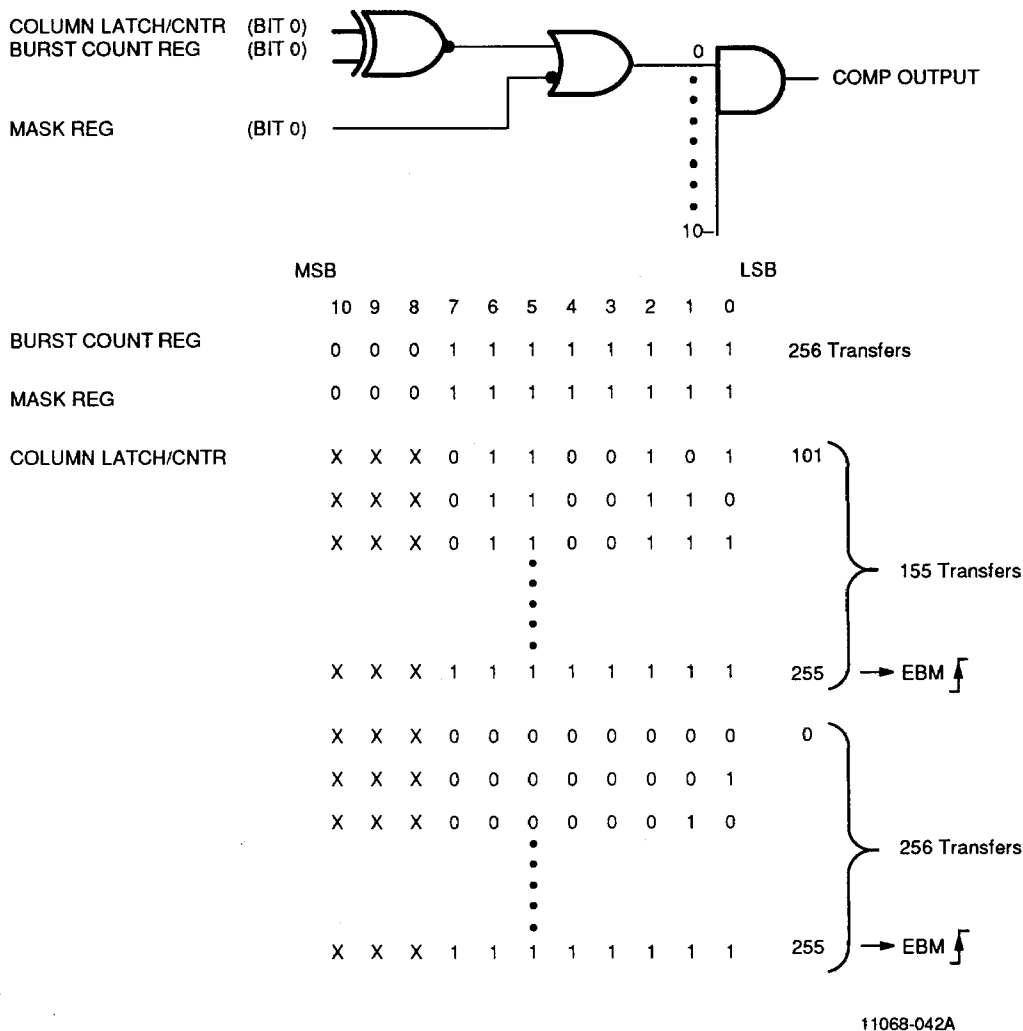


* Default. The Am29C668 will power up in Am29368 mode if the user does not reprogram the configuration register.

† Reference Table 4.

** These bits are used during factory testing only.

Figure 6. Configuration Register Options



11068-042A

Figure 6a. Programmable Burst Logic with 256-word Burst Length Example

In this example, the self alignment feature of the Am29C668 is shown. The first burst is terminated on the DRAM page boundary by the EBM output. All subsequent bursts are then set at 256 transfers, which has been programmed via the Burst Count and Mask registers.

Auto/External Timing Logic

When Auto Timing mode is selected via the Timing Mode (TM) bit in the Configuration Register (TM = 0), this circuit generates internal timing delays between RASI-MSEL and MSEL-CASI. These delays are optimized for use with 100ns DRAMs.

In the Auto Timing mode the CASI/CASIEN input acts as CASIEN. In this mode internal \overline{CAS} is generated from the active (HIGH) edge of RASI and is deactivated when RASI goes inactive by the Auto Timing Circuit. This internally generated \overline{CAS} is gated with the CASIEN input to generate the \overline{CAS}_n outputs. This gating circuit allows the Auto-Timing to be externally overridden (Figure 9). It is used for specialty DRAM accesses.

In the External Timing mode (TM = 1), the internal \overline{CAS} signal follows the externally generated CASI input.

In the Auto Timing Mode the MSEL/MSELEN input acts as MSELEN. In this mode, internal MSEL is generated from the active (HIGH) edge of RASI, and is deactivated when RASI goes inactive, by the Auto Timing Circuit. This internally generated MSEL is gated with the MSELEN input to generate the internal MSEL signal. This feature is used to extend row address hold time via external control (overriding the Auto Timing feature).

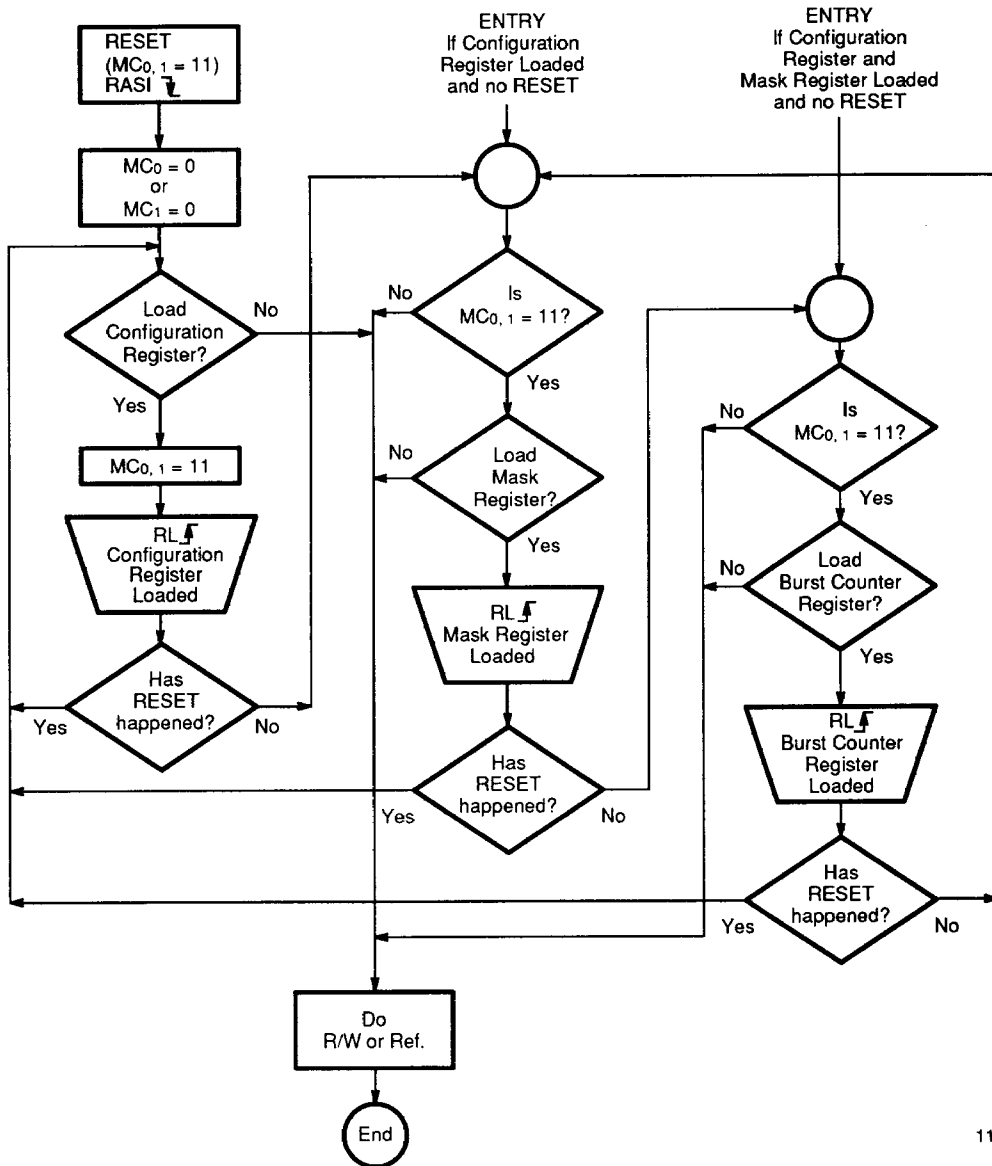
In the External Timing mode (TM = 1), the internal MSEL signal follows the externally generated MSEL input.

The Auto Timing mode allows 4 banks of 16-bit data plus 6 EDC check bits or 2 banks of 32-bit data plus 7 EDC

check bits comprised of 100ns DRAMs to be operated without external drivers.

Power-up/Strobe Logic

This block automatically presets the Am29C668 to the default condition upon power-up (Figure 6). This circuit also generates all the internal control signals for the Refresh Counter, Configuration, Burst Count, and Mask Registers, the Register Load Logic, and the Bank Register.



11068-013C

Figure 7. Register Loading (See paragraph on next page)

Figure 7. Register Loading. The Configuration Register must be loaded before the Mask and Burst Count Registers may be loaded. Once the Configuration Register is loaded, the Register Load Logic will toggle between loading the Mask Register and Burst Count Register. The Configuration Register may only be loaded

immediately after a reset. The Mask Register and Burst Count Register are only used in the Burst/Block access mode, in other modes only the Configuration Register need be loaded if the user wishes to alter its default mode indicated in Figure 6.

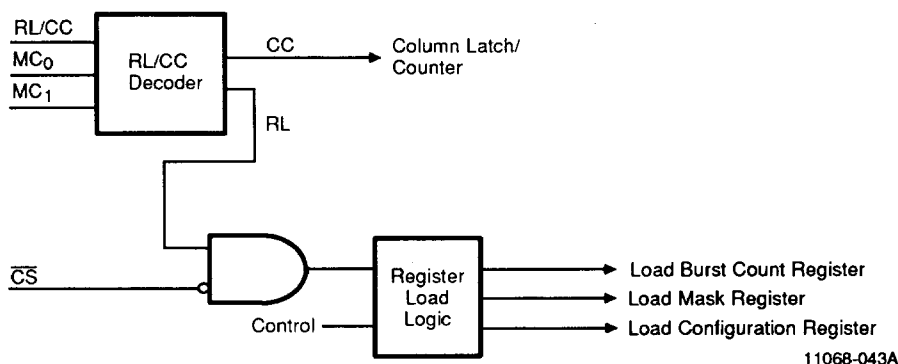


Figure 8. Register Load Logic and RL/CC Decoder (Register Logic)

DRAM Page Boundary Logic

This logic block indicates to the processor when a page boundary on the DRAM is reached. It monitors the contents of the Column Latch/Counter and, depending upon the outputs of the DRAM Size Decoder, signals an End of Burst/Block Mode (EBM) when a page boundary is reached. A page boundary condition is reached when the contents of the Column Latch/Counter equals the DRAM page boundary address.

This logic is used only in the Burst/Block mode of access.

Refresh/Scrubbing/Bank Counters

This block (Figure 10) contains the 11-bit Row Refresh Counter, 11-bit Column Refresh Counter, and 2-bit Bank Refresh Counter. All three counters are synchronous and are reset when $MC_{0,1} = 11$ and RAS \bar{I} transitions from HIGH to LOW. These counters are clocked when $MC_{0,1} = 00$ or 10 and RAS \bar{I} transitions from HIGH to LOW.

The size of the Row and Column Refresh Counters are automatically adjusted for the DRAM size being used. This is done by selecting the proper Row Counter output to go to the low order Column Counter input and similarly selecting the proper Column Counter output to go to the low order Bank Counter input. This selection is de-

termined by the outputs of the DRAM Size Decoder with the help of a multiplexer.

The $\overline{RAS}/\overline{CAS}$ Configuration Bit of the Configuration Register selects which bit of the Bank Counter is used for the Terminal Count (TC) output, depending upon whether 2 or 4 banks of DRAM are used.

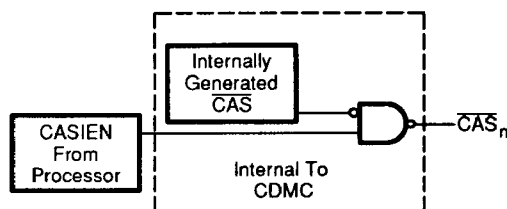
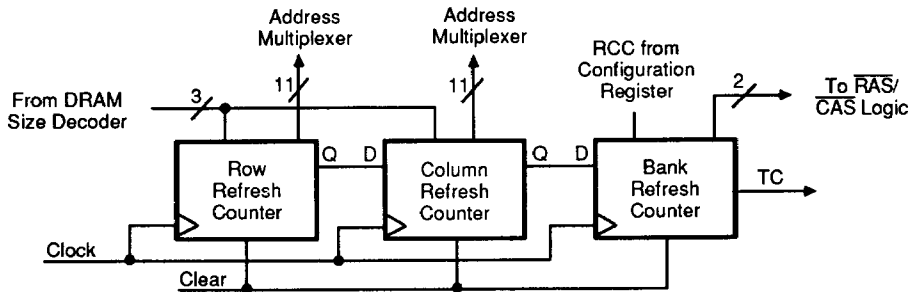


Figure 9. Auto Timing with External Override

Address Multiplexer

This block is an 11-bit, four input multiplexer which selects the address to the DRAMs. Its four address inputs are the row latch output, column latch/counter output, row refresh counter output, and column refresh counter output. The $MC_{0,1}$, internal MSEL, and \overline{CS} input signals are decoded to select one of the four addresses.



11068-012A

Figure 10. Refresh/Scrubbing/Bank Counters

RAS/CAS Logic

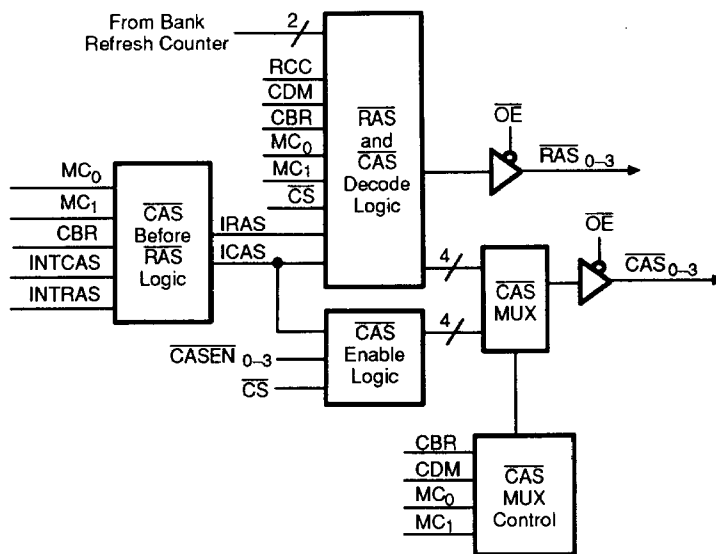
This block (Figure 11) contains the $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Logic, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Decode Logic, $\overline{\text{CAS}}$ Enable Logic, and $\overline{\text{CAS}}$ Multiplexer.

The $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Logic switches the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lines to the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Decode Logic if the CBR selection bit in the Configuration Register is set (1). This allows a $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ refresh to be accomplished without altering the order of the RASi and CASi input strobes. Refresh With Scrubbing ($\text{MC}_{0,1} = 10$) is not allowed when the CBR bit is set (1).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Decode Logic decodes the internal $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ timing signals to generate the four RAS_n and four $\overline{\text{CAS}}_n$ output signals.

The $\overline{\text{CAS}}$ Enable Logic is used if a byte-wise $\overline{\text{CAS}}$ decoding method is selected. Byte enables are decoded externally and are connected to the $\overline{\text{CASEN}}_{0-3}$ inputs. In the $\overline{\text{CAS}}$ Enable Logic all the $\overline{\text{CASEN}}_{0-3}$ signals are individually gated with the internal $\overline{\text{CAS}}$ signal to generate the $\overline{\text{CAS}}_n$ proper outputs.

The $\overline{\text{CAS}}$ Multiplexer is a 4-bit, two input multiplexer. It selects one set of $\overline{\text{CAS}}_n$ signals to the output depending upon the $\overline{\text{CAS}}$ decode method being used (selected by the CDM bit in the Configuration Register) and the operating mode (selected by $\text{MC}_{0,1}$).



11068-011A

Figure 11. $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ Logic

MODES OF OPERATION

The Am29C668 has two basic modes of operation, read/write and refresh.

Read/Write Modes

In the read/write mode the Am29C668 latches the row, column and bank addresses and multiplexes them to the DRAM array under the control of the internally generated timing strobes in the Auto Timing Mode or the externally generated MSEL in the External Timing Mode. The timing option is selected via the Timing Mode (TM) bit in the Configuration Register (Figure 6).

The row address is latched in the DRAMs by the active (LOW-going) edge of the \overline{RAS}_n output, which follows the active (HIGH-going) edge of the RASI input. The address lines are then switched to column address by either an internally generated signal in the Auto Timing Mode or by pulling MSEL active HIGH in the External Timing Mode. The column address is latched in the DRAMs on the active (LOW-going) edge of the \overline{CAS}_n output, which follows either an internally generated signal in the Auto Timing Mode or the active (HIGH-going) edge of the CASI input in the External Timing Mode.

The read/write mode of the Am29C668 may be optimized for the shortest memory cycle time, through burst/block accesses, nibble mode accesses, or "cache" mode accesses.

Burst/Block Mode

When a burst/block access is requested by the processor, the Am29C668 latches the initial row, column, and bank addresses. Subsequent column addresses are generated internally by the Am29C668, allowing consecutive memory locations to be accessed at high speed without the processor actually generating each memory location address. This type of transfer can be used by high performance processors to fill their on-chip or external cache when a cache miss is encountered.

During a burst access the CC input of the Am29C668 is toggled after the initial row, column, and bank addresses have been latched. While the RASI input is held high by the processor, each high-to-low transition of CC increments the column address for the next memory access.

The burst access will continue until a programmed number of accesses (which is stored in the Burst Count Register) has been completed or a page boundary is reached. Both conditions are indicated to the processor by the EBM output.

Nibble Mode

For Nibble mode accesses the Nibble Count bit (NIBCNT) in the Configuration Register is set to "1". This bit enables only the two least significant bits of the Column Latch and Counter to be clocked, allowing the Column Latch and Counter to perform a modulo four

count when making a nibble burst access (as in the case of the 68030 processor) using non-nibble DRAMs.

When "nibble" DRAMs are used nibble accesses are accomplished by toggling CASI (Reference Figure 25).

Cache Mode

This mode allows the efficient use of page mode and fast page mode DRAMs by comparing back-to-back row and bank addresses from the processor.

In the "cache" mode of access of the Am29C668 the \overline{RAS}_n output is held active (LOW) and any location in that row is accessed by only changing the column address. This makes the entire row look like a cache, since any access in that row can be made at high speed. To select the cache access mode, the Cache Mode (CM) bit in the Configuration Register is set to "1". The row and bank addresses of consecutive accesses are compared by the Am29C668. If the row and bank addresses of consecutive accesses match, \overline{CH} goes active (LOW) and signals the timing generator not to deactivate the RASI input but only to toggle the CASI/CASIEN input. If the row and bank addresses of consecutive accesses do not match, the \overline{CH} signal goes inactive (HIGH) and informs the timing generator to deactivate the RASI input and start a new RASI cycle after the current cycle has gone through a \overline{RAS} precharge cycle. When the RASI input is activated, its HIGH-going edge loads the row and bank registers with the contents of the row and bank latches, respectively, saving the current values for the next comparison.

Refresh Modes

Normal Refresh

In the normal refresh mode, the refresh address is generated by the Am29C668 refresh counter. The row refresh counter is used to generate the row address. All corresponding rows in all four banks are refreshed simultaneously by generating all four \overline{RAS}_n outputs in response to the RASI input. Hence, the entire memory may be refreshed by stepping through the row refresh counter once. The row refresh counter is incremented to the next refresh address by the inactive (LOW going) edge of the RASI input.

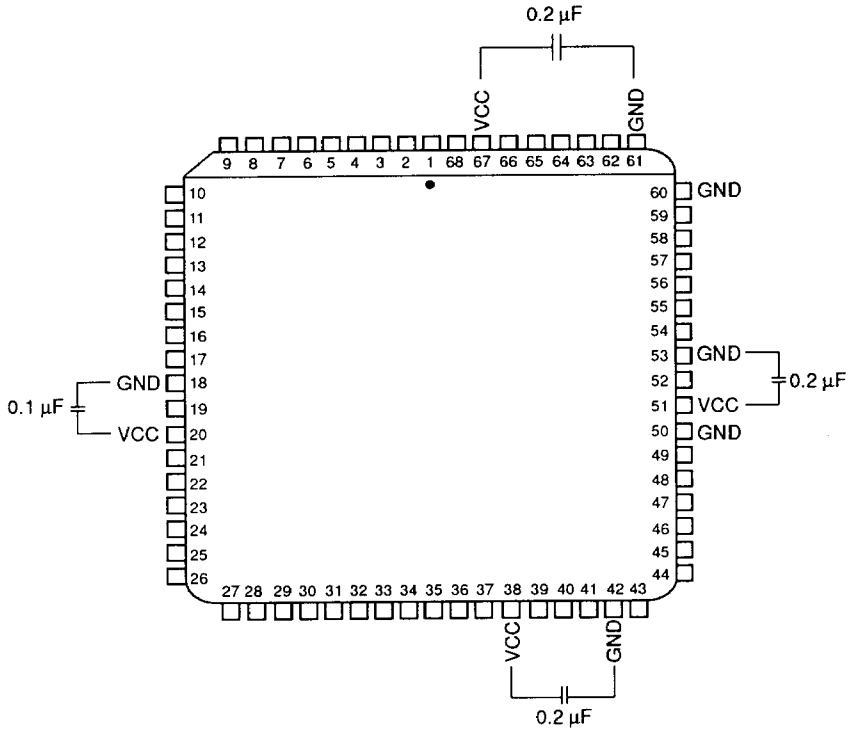
Refresh With Scrubbing

When memory scrubbing is performed in systems employing error detection and correction (EDC), the row, column, and bank refresh counters are used. In this case, all four corresponding rows are refreshed and one location of one row is "scrubbed", ie...a read/modify/write cycle is performed. An entire memory array can be scrubbed by stepping through the row, column, and bank address counters once. The Am29C668 has four independent \overline{CAS}_n outputs allowing a single bit to be accessed during refresh cycles.

CAS Before RAS Refresh

This is a feature of some dynamic RAMs. The DRAM on-chip refresh counter is updated and a refresh cycle performed by generating a $\overline{\text{CAS}}$ strobe before the $\overline{\text{RAS}}$ strobe. This refresh support is selected by enabling (setting to "1") the $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ bit in the Configuration Register. Refresh with scrubbing ($\text{MC}_{0,1} = 10$) is not allowed when the CBR bit is set (1).

In this mode, $\overline{\text{RAS}}$ controls the $\overline{\text{CAS}}_n$ outputs and CAS_i controls the $\overline{\text{RAS}}_n$ outputs. This allows a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh to be accomplished without altering the order of the $\overline{\text{RAS}}$ and CAS_i input strobes. When this mode is set, memory "scrubbing" ($\text{MC}_{0,1} = 10$) is prohibited.



11068-042A

Figure 12. Device Decoupling – Vcc and Ground Pin Connections

Notes:

Due to the high switching speeds and high drive capability of the Am29C668, it is necessary to decouple the device for proper operation. Multilayer ceramic capacitors are recommended. It is important to mount the capacitors as close as possible to the power pins (Vcc, GND) to minimize lead inductance and noise. A ground plane is strongly recommended. A wire wrapped board without power and ground planes is not recommended.

It is strongly recommended that this part be directly surface mounted whenever possible. Should a PLCC, or PGA socket be required, a one-time-insertion-only socket with minimal lead length is necessary for proper device function. The socket lead inductance should be 8nH maximum per pin.

The socket may be obtained from Methode Electronics (Part #213-068-101) at (800) 323-6858 or AMP (Part #821574-1, 821574-3, 641749-2) at (800) 522-6752.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Operating Temperature	-55 to +125°C
Maximum V _{cc}	-0.5 to +7.0 V
DC Voltage Applied to Any Pin	-0.5 to (V _{cc} +0.3) V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Ambient Temperature (T _A)	0 to +70°C
Supply Voltage (V _{cc})	+4.50 to +5.50 V

Military (M)

Case Temperature (T _c)	-55 to +125°C
Supply Voltage (V _{cc})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1,2,3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)		0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}		5.0	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND		-5.0	μA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. I _{OH} = -10 mA	2.7		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 10 mA		0.5	V
V _{ON}	Output Undershoot Voltage (Note 4)	C _L = 50 pF		-1.0	V
V _{OP}	Output Overshoot Voltage (Note 4)	C _L = 50 pF		0.8	V
V _{OP}	Output Overshoot Voltage (Note 4)	C _L = 50 pF		0.8	V
I _{OZ}	Off-State (High Impedence) Output Current; Q Outputs	V _{CC} = Max. V _O = 0V V _O = V _{CC} (Max)		-10 10	μA
I _{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V _{CC} = Max. 4.3V ≤ V _{IN} , V _{IN} ≤ 0.2V f _{OP} = 0		5.0	mA
I _{CC1}	Quiescent Input Power Supply Current (@ TTL HIGH)	V _{CC} = Max. V _{IN} = 2.4 f _{OP} = 0		25	mA
I _{CCD}	Dynamic Power Supply Current (Note 5)	V _{CC} = Max. 4.3 V ≤ V _{IN} , V _{IN} ≤ 0.2V C _L = 150pF OE = LOW	MIL COM'L	7 7	mA/ MHz
I _{CC}	Total Power Supply Current (Notes 3 and 5)	V _{CC} = Max., f _{OP} = 10 MHz OE = LOW 50% Duty cycle, C _L = 150pF 4.3 V ≤ V _{IN} , V _{IN} ≤ 0.2V V _{CC} = Max., f _{OP} = 10 MHz OE = LOW 50% Duty cycle, C _L = 150pF V _{IN} = 3.4, V _{IL} = 0.4 V	MIL COM'L MIL COM'L	100 100 100 100	mA

Notes:

- For conditions shown as Min. or Max., use appropriate value specified under Operating Range for the applicable device type.
- Tested with limited test pattern.
- Total Power Supply Current is the sum of the Quiescent Current and the dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Power Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCD}(f_{OP}) \text{ (CMOS Inputs), } I_{CC} = I_{CC1} + I_{CCD}(f_{OP}) \text{ (TTL Inputs), } f_{OP} = \text{Operating Frequency in Megahertz}$$
 During device characterization, two addresses, one \overline{RAS}_n and one \overline{CAS}_n output were toggled at f_{OP} = 10 MHz during I_{CC} measurement
- V_{ON} and V_{OP} are not production tested but are guaranteed by characterization data for surface mounted devices with proper capacitive decoupling. Limits specified are for all outputs switching simultaneously with minimum specified loading. As loading increases, V_{ON} and V_{OP} will approach zero. Reference Switching Waveforms.
- Not tested in production. Guaranteed by characterization data.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
 Capacitive Loading = 350 pF for all Q_n, $\overline{\text{RAS}}_n$, and $\overline{\text{CAS}}_n$; 150 pF for all other outputs (minimum tester load). See Note 1.

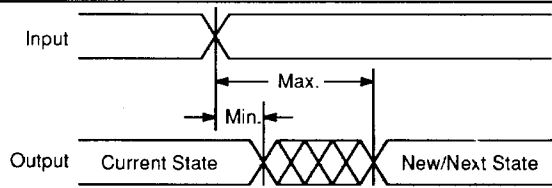
No.	Parameter Symbol	Parameter Description	Test Conditions	Commercial				Military		Unit
				Am29C668		Am29C668-1		Am29C668-1		
				Min.	Max.	Min.	Max.	Min.	Max.	
COMMON PARAMETERS										
1	t _{PD}	ACn/ARn to Qn (Note 4)	ALE = 1	2	34	3	29	0	35	ns
2	t _{PD}	MCn to Qn (Note 4)		6	35	7	30	4	37	ns
3	t _{PD}	ALE to Qn (Note 4)		4	34	5	29	3	37	ns
4	t _{PD}	$\overline{\text{CS}}$ to Qn (Note 4)		6	36	7	32	6	39	ns
5	t _s	ACn/ARn to ALE \downarrow Set up time		4		4		3		ns
6	t _H	ACn/ARn to ALE \downarrow Hold time		5		5		4		ns
7	t _s	SELn to ALE \downarrow Set up time		4		4		3		ns
8	t _H	SELn to ALE \downarrow Hold time		4		4		3		ns
9	t _s	MCn to RAS \uparrow Set up time		5		5		3		ns
10	t _H	MCn to RAS \uparrow Hold time		5		5		3		ns
10A	t _s	MCn to RAS \downarrow Set up time	MCn = 11	4		4		3		ns
11	t _s	$\overline{\text{CS}}\downarrow$ to RAS \uparrow	(Note 3)	4		4		3		ns
12	t _H	$\overline{\text{CS}}\uparrow$ to RAS \downarrow	(Note 3)	4		4		3		ns
13	t _s	SELn to RAS \uparrow Set up time	ALE = 1	4		4		3		ns
14	t _H	SELn to RAS \downarrow Hold time	ALE = 1	4		4		3		ns
15	t _{PWL}	RAS \uparrow Pulse Width LOW		10		10		10		ns
16	t _{PWH}	RAS \uparrow Pulse Width HIGH		10		10		10		ns
EXTERNAL TIMING MODE										
17	t _{PD}	RAS \uparrow to $\overline{\text{RAS}}_n\downarrow$ (active edges) (Note 4)		9	30	9	26	8	32	ns
17A	t _{PD}	RAS \downarrow to $\overline{\text{RAS}}_n\uparrow$ (inactive edges) (Note 4)		4	23	4	21	3	23	ns
18	t _{PD}	CAS \uparrow to $\overline{\text{CAS}}_n\downarrow$ (active edges) (Note 4)		7	31	8	27	9	32	ns
18A	t _{PD}	CAS \downarrow to $\overline{\text{CAS}}_n\uparrow$ (inactive edges) (Note 4)		4	23	5	21	4	23	ns
19	t _{PD}	MSEL to Qn		4	34	8	30	3	37	ns
AUTO TIMING MODE										
20	t _{PD}	RAS \uparrow to $\overline{\text{RAS}}_n\downarrow$ (active edges) (Note 4)		9	30	9	26	8	32	ns
20A	t _{PD}	RAS \downarrow to $\overline{\text{RAS}}_n\uparrow$ (inactive edges) (Note 4)		4	23	4	20	3	23	ns
21	t _{SKEW}	$\overline{\text{RAS}}_n$ to Qn (row address) (Note 4)	MSELEN = 1	12		13		9		ns
21A	t _{PD}	RAS \uparrow to Qn (column address)	MSELEN = 1	20	70	20	65	20	75	ns
22	t _{PD}	RAS \uparrow to $\overline{\text{CAS}}_n\downarrow$	CASIEN = 1 (Note 2)		98		88		102	ns
23	t _{SKEW}	$\overline{\text{RAS}}_n\downarrow$ to $\overline{\text{CAS}}_n\downarrow$	CASIEN = 1	22	78	25	72	20	82	ns
24	t _{SKEW}	Qn (column address) to $\overline{\text{CAS}}_n$	MSELEN = 1 CASIEN = 1	4		4		4		ns

SWITCHING CHARACTERISTICS (Continued)

No.	Parameter Symbol	Parameter Description	Test Conditions	Commercial				Military		Unit
				Am29C668		Am29C668-1		Am29C668-1		
				Min.	Max.	Min.	Max.	Min.	Max.	
AUTO TIMING MODE										
25	t_{PD}	MSELEN to Qn (column address) (Note 4)		6	34	7	30	6	37	ns
26	t_{PD}	CASIE \overline{L} to \overline{CASn} \overline{L} (active edges) (Note 4)		6	31	7	27	8	32	ns
26A	t_{PD}	CASIE \overline{L} to \overline{CASn} \overline{L} (inactive edges) (Note 4)		3	23	4	21	4	23	ns
SPECIALTY MODES										
27	t_{PD}	CC \overline{L} to Qn (Note 4)		5	32	6	29	6	34	ns
28	t_{PD}	CC \overline{L} to EBM		4	23	5	20	4	25	ns
29	t_{PW}	CC Pulse Width LOW or HIGH		10		10		12		ns
32	t_{PD}	ARn to \overline{CH}	ALE = 1		19		17		21	ns
33	t_{PD}	ALE to EBM \overline{L}		4	20	4	18	4	22	ns
34	t_{PD}	ALE to \overline{CH}			17		15		18	ns
35	t_{PD}	RAS \overline{L} to TC			30		24		35	ns
36	t_s	ACn to RL \overline{L} Set up time		3		2		0		ns
37	t_H	ACn to RL \overline{L} Hold time		12		11		12		ns
38	t_s	MCn, \overline{CS} to RL \overline{L} Set up time		7		6		7		ns
39	t_H	MCn, \overline{CS} to RL \overline{L} Hold time		7		6		7		ns
40	t_{PW}	RL Pulse Width LOW or HIGH		10		10		10		ns
41	t_{PD}	\overline{CASENn} to \overline{CASn} (Note 4)		2	27	3	23	3	30	ns
OUTPUT SKEWS (worst case for any given device)										
42	t_{SKEW}	{ $t_{PD}(ACn/ARn$ to Qn)– $t_{PD}(RAS\overline{L} to \overline{RASn})}$	MCn = 01		20		18		21	ns
42A	t_{SKEW}	{ $t_{PD}(ACn/ARn$ to Qn)– $t_{PD}(CAS\overline{L} to \overline{CASn})}$	MCn = 01		18		16		18	ns
43	t_{SKEW}	{ $t_{PD}(MCn$ to Qn)– $t_{PD}(RAS\overline{L} to \overline{RASn})}$	MCn = 00, 01		22		19		23	ns
44	t_{SKEW}	{ $t_{PD}(MSEL$ to Qn)– $t_{PD}(RAS\overline{L} to \overline{RASn})}$	MCn = 01		21		18		23	ns
45	t_{SKEW}	{ $t_{PD}(MSEL$ to Qn)– $t_{PD}(CAS\overline{L} to \overline{CASn})}$	MCn = 01		19		17		20	ns
THREE-STATE OUTPUTS										
46	t_{PLZ}	Output Disable Time from LOW	CL = 350 pF		24		24		25	ns
47	t_{PHZ}	Output Disable Time from HIGH			28		26		30	ns
48	t_{PZL}	Output Enable Time from LOW			18		16		18	ns
49	t_{PZH}	Output Enable Time from HIGH			18		16		18	ns

Notes:

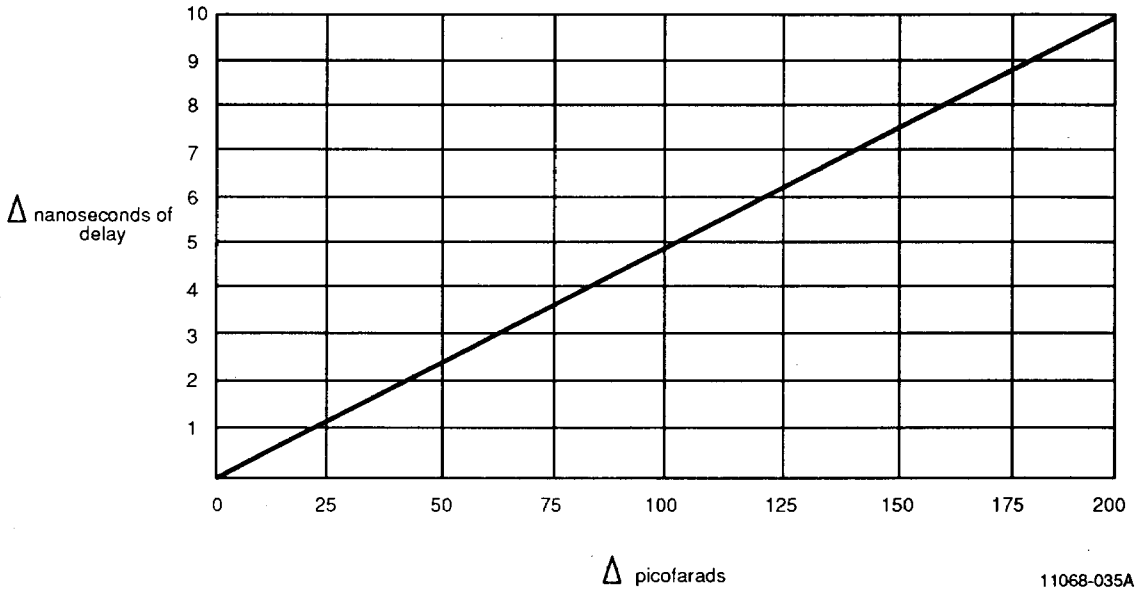
1. To calculate propagation delays at loads other than those specified, see section labeled "TYPICAL Change in Propagation Delay vs. Loading Capacitance" on the following page.
2. For deassertion, removal of RAS \overline{L} will deassert \overline{CASn} with tPD indicated by external timing parameter 18A.
3. Not included in Group A testing. Not production tested. These parameters are included to ease system design—for reference only.
4. Refer to Figure 13 for information on how the min. and max. parameters are specified.



11068-066A

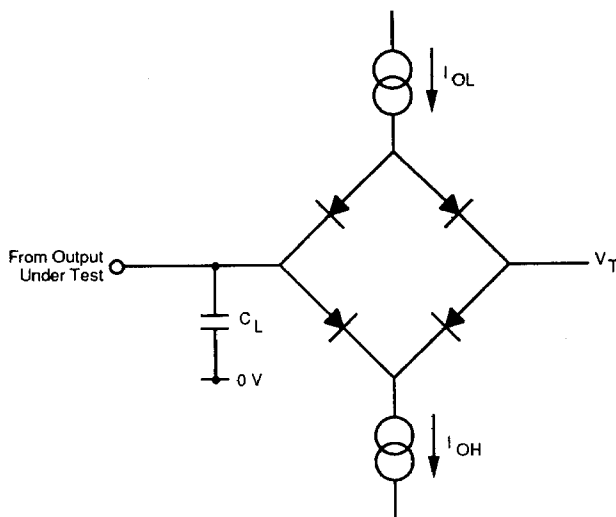
Figure 13. Minimum and Maximum Timings Specification

TYPICAL Change in Propagation Delay vs Loading Capacitance



11068-035A

SWITCHING TEST CIRCUIT

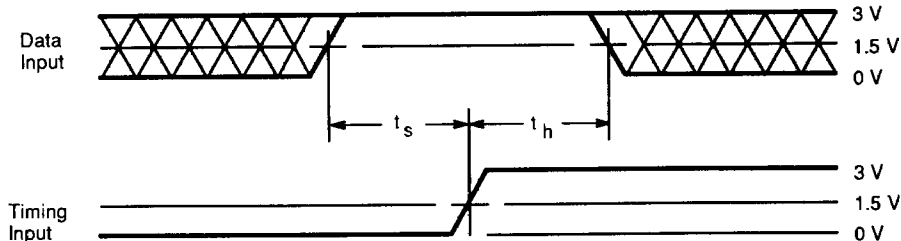


11068-036A

Notes:

1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

SWITCHING TEST WAVEFORMS

**Notes:**

1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

11068-037A

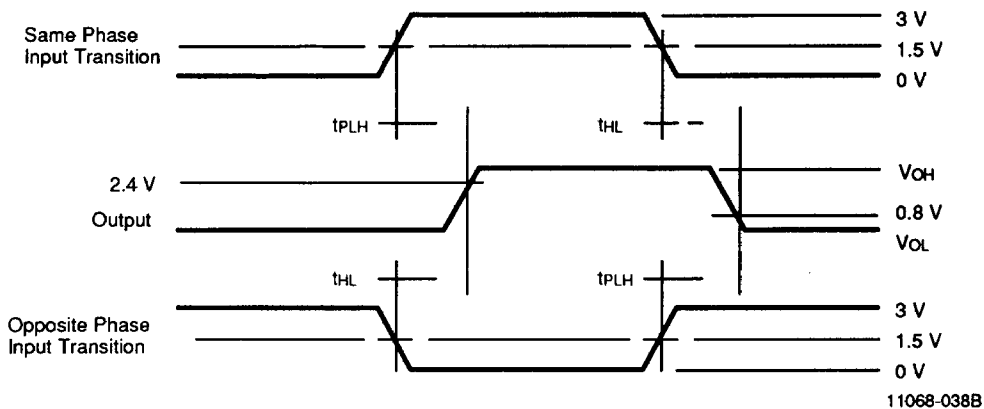
Setup and Hold Times

Notes on Testing

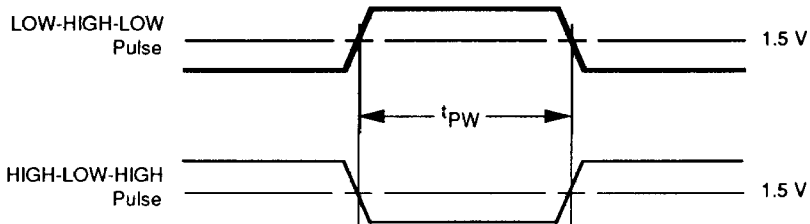
Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0\text{ V}$ and $V_{IH} \geq 3\text{ V}$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Proper device grounding is critical when device testing. Multi-layer performance boards with radial decoupling between power and ground planes is recommended. Wiring unused interconnect pins to the ground plane is recommended. The ground plane must be sustained from the performance board to the device under test interface board. To minimize inductance, heavy-gauge stranded wire with twisted pairs should be used for power wiring.

SWITCHING WAVEFORMS

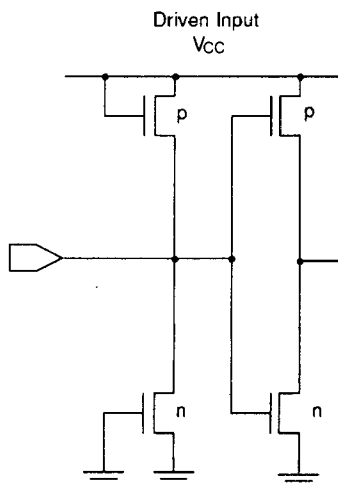


Propagation Delay



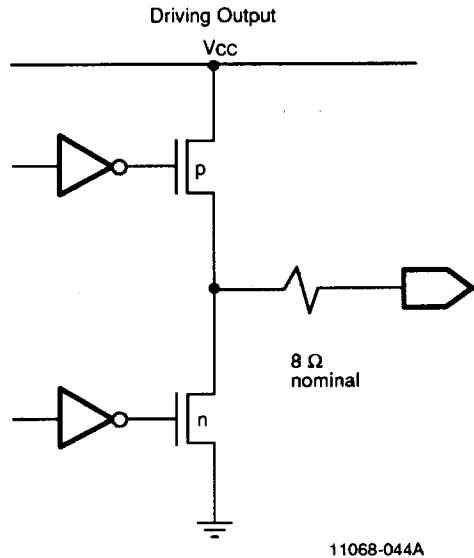
11068-039A

Input Pulse Width

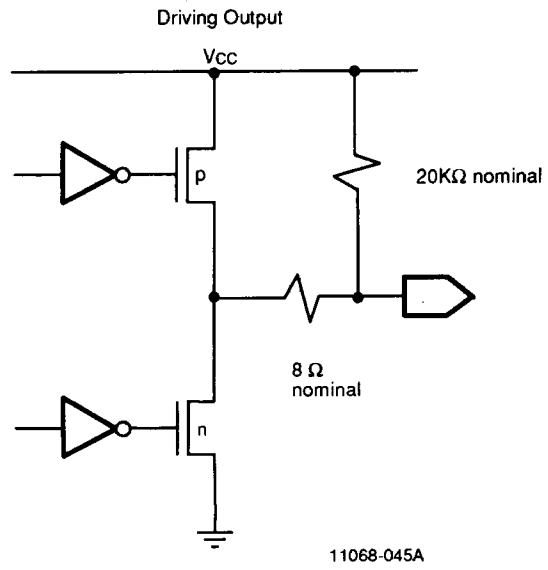


11068-040A

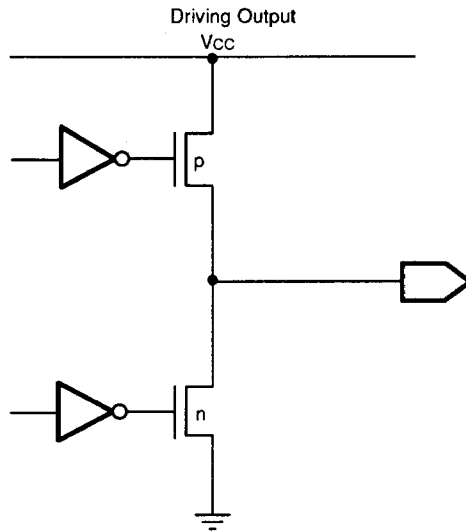
Equivalent Input Circuit



**Equivalent Output Circuit
(Q_n Outputs)**

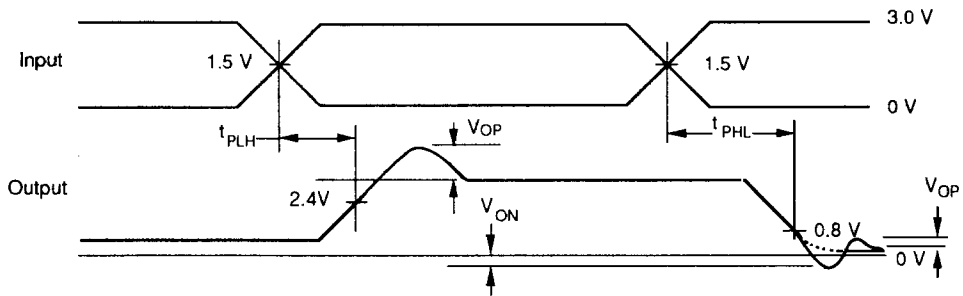


**Equivalent Output Circuit
(RAS_n, CAS_n Outputs)**



11068-046A

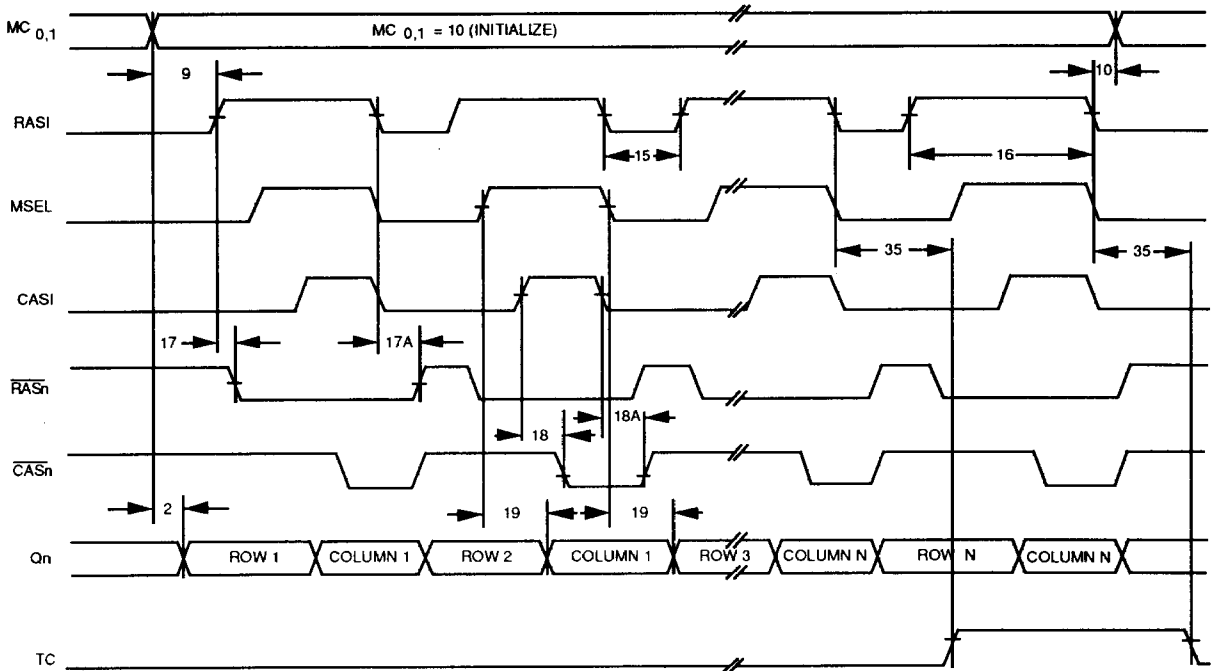
Equivalent Output Circuit
(All outputs except Q_n , \overline{RAS}_n , \overline{CAS}_n)



11068-041B

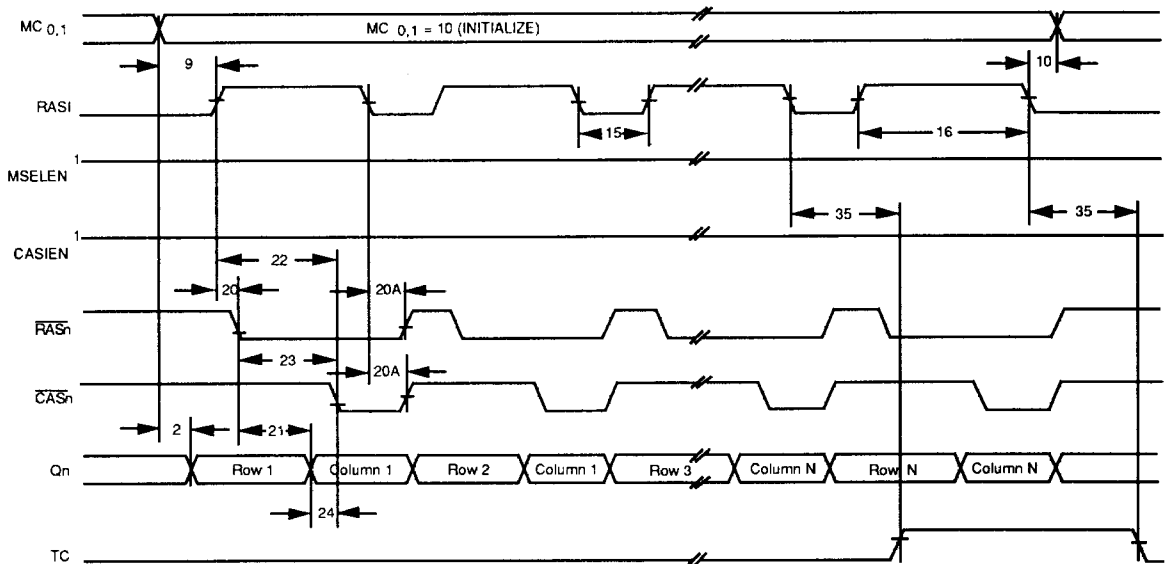
Output Drivers Level

SWITCHING WAVEFORMS



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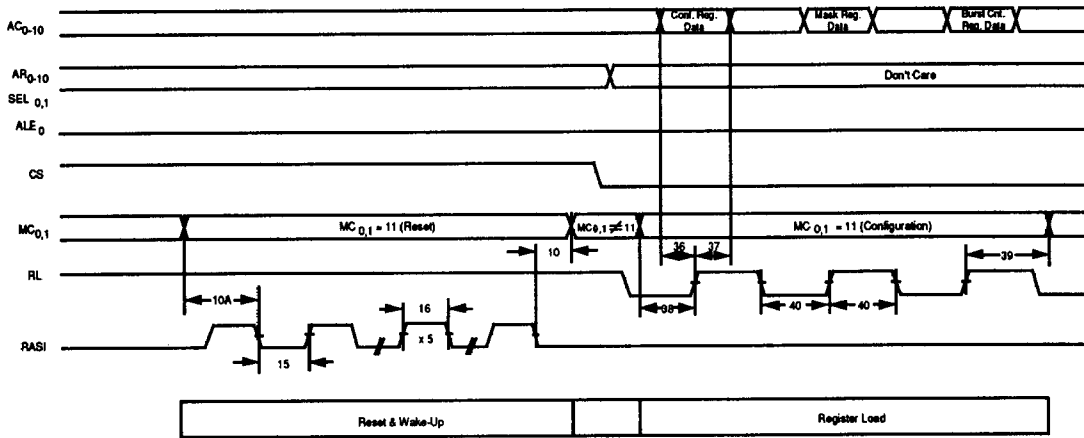
Figure 13. EDC Initialization with External Timing



11068C-048A

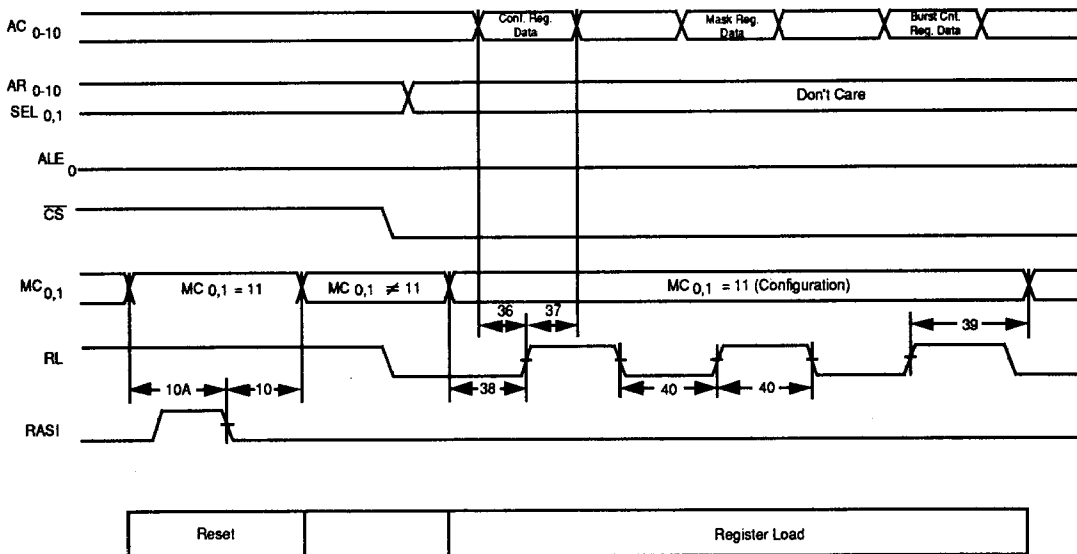
Figure 14. EDC Initialization with Auto-Timing

SWITCHING WAVEFORMS



11068C-049A

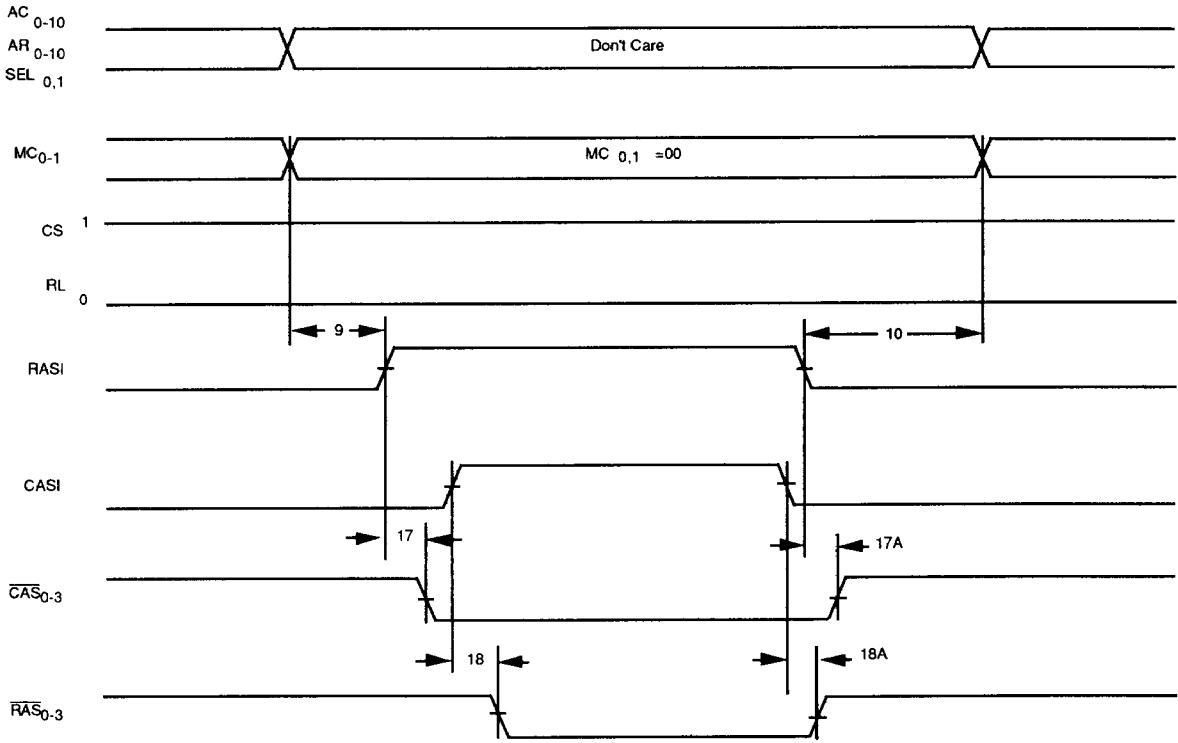
Figure 15. Reset, Wake Up, and Register Load Operation



11068C-050A

Figure 15a. Reset and Register Load Operation

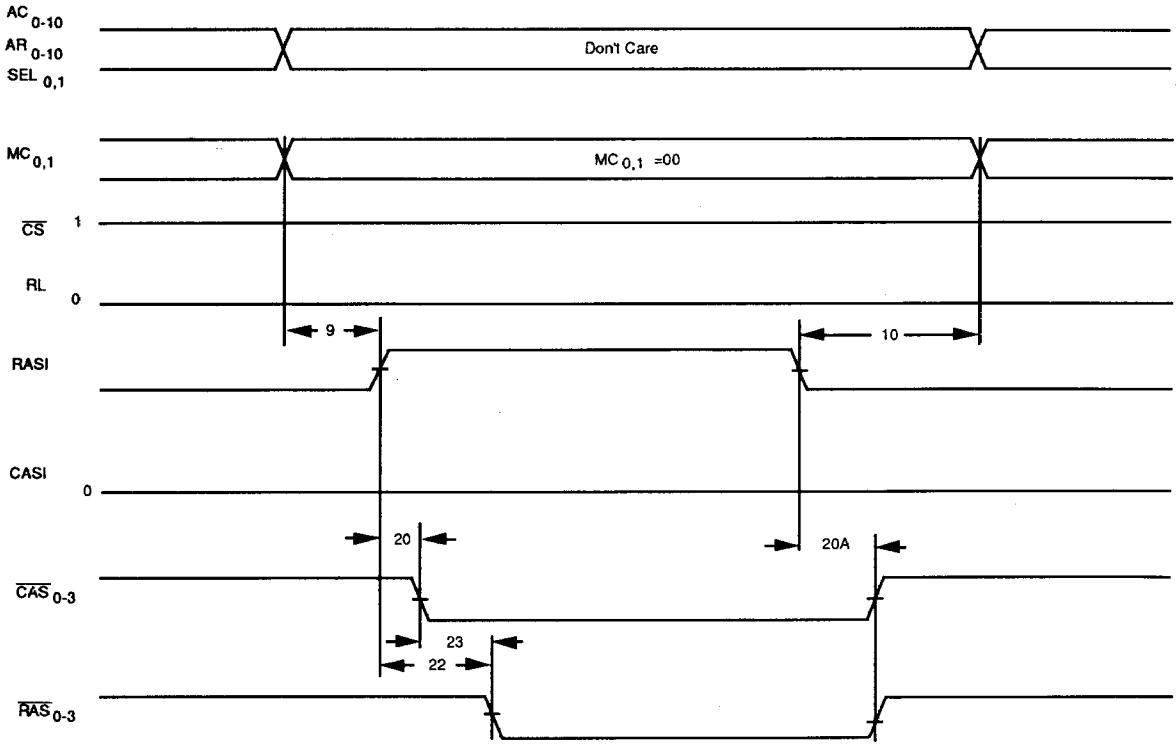
SWITCHING WAVEFORMS



11068C-051A

Figure 15b. CAS Before RAS Refresh with External Timing

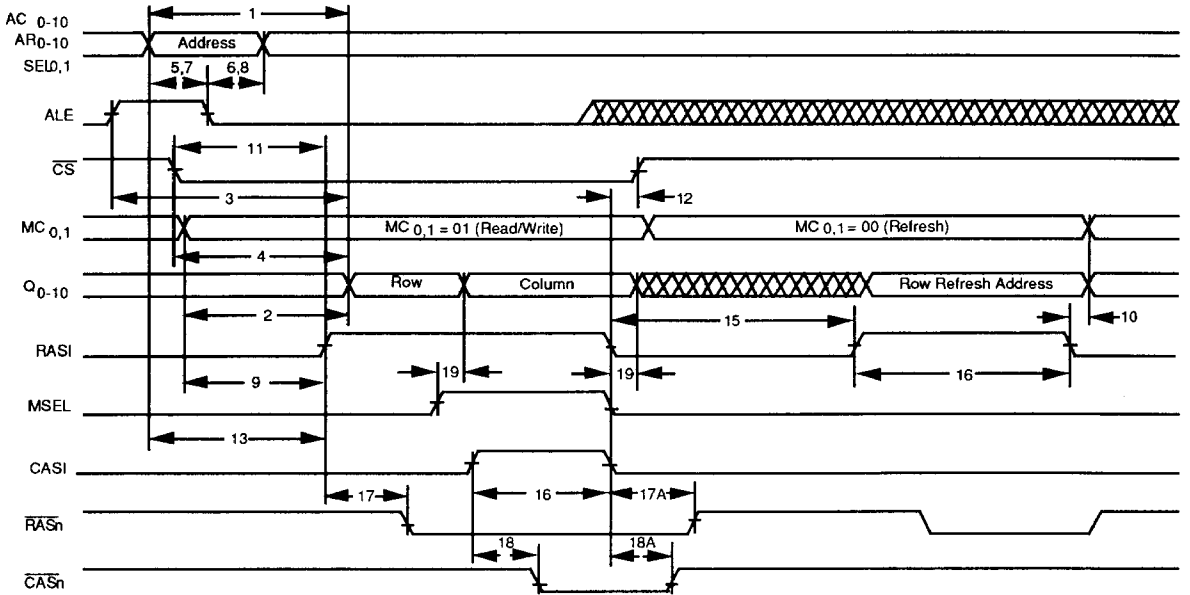
SWITCHING WAVEFORMS



11068C-052A

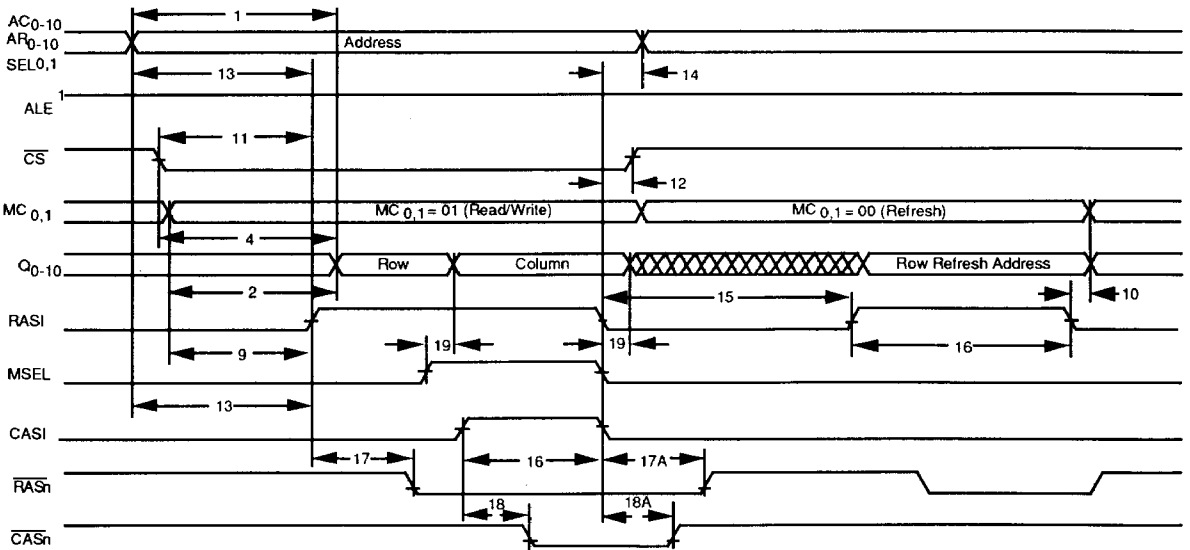
Figure 15c. CAS Before RAS Refresh with Auto Timing

SWITCHING WAVEFORMS



11068C-053A

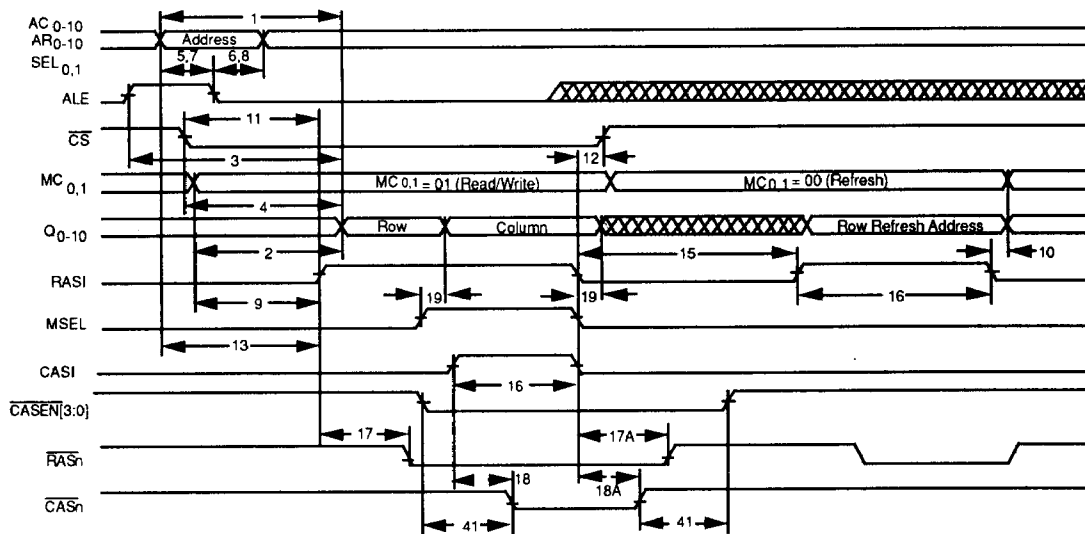
Figure 16. Standard Read/Write, Refresh Accesses with External Timing



11068C-054A

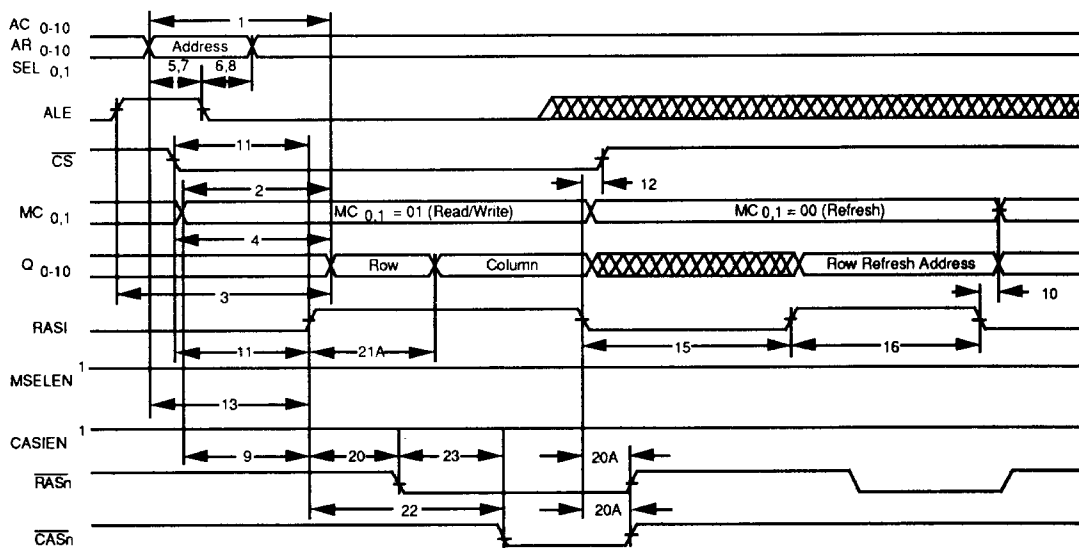
Figure 17. Standard Read/Write, Refresh Accesses with ALE = 1

SWITCHING WAVEFORMS



11068C-055A

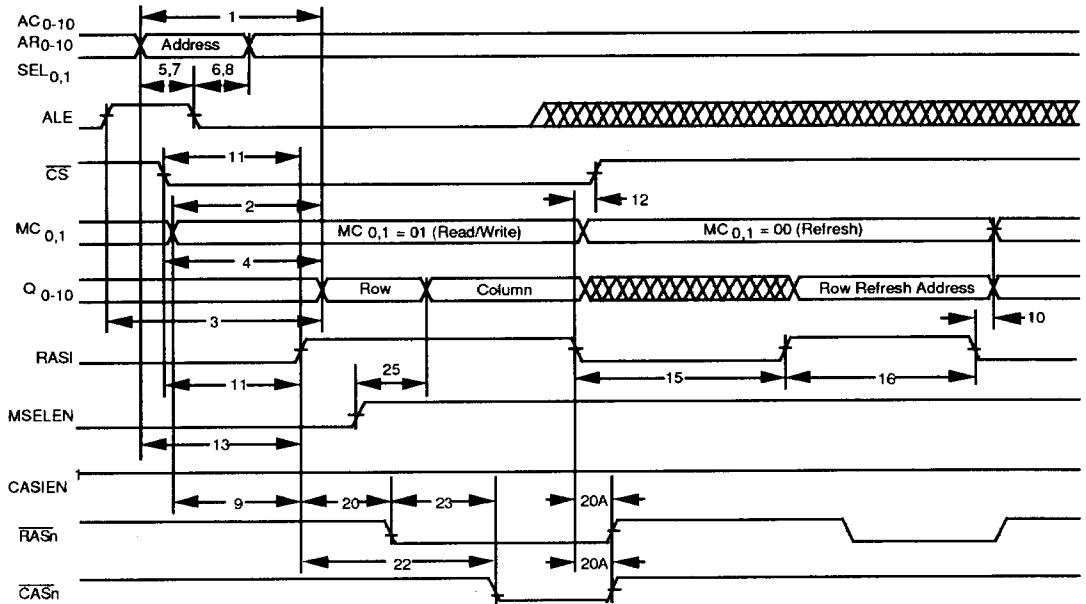
Figure 18. Standard Read/Write, Byte Access; Refresh (External Timing)



11068C-056A

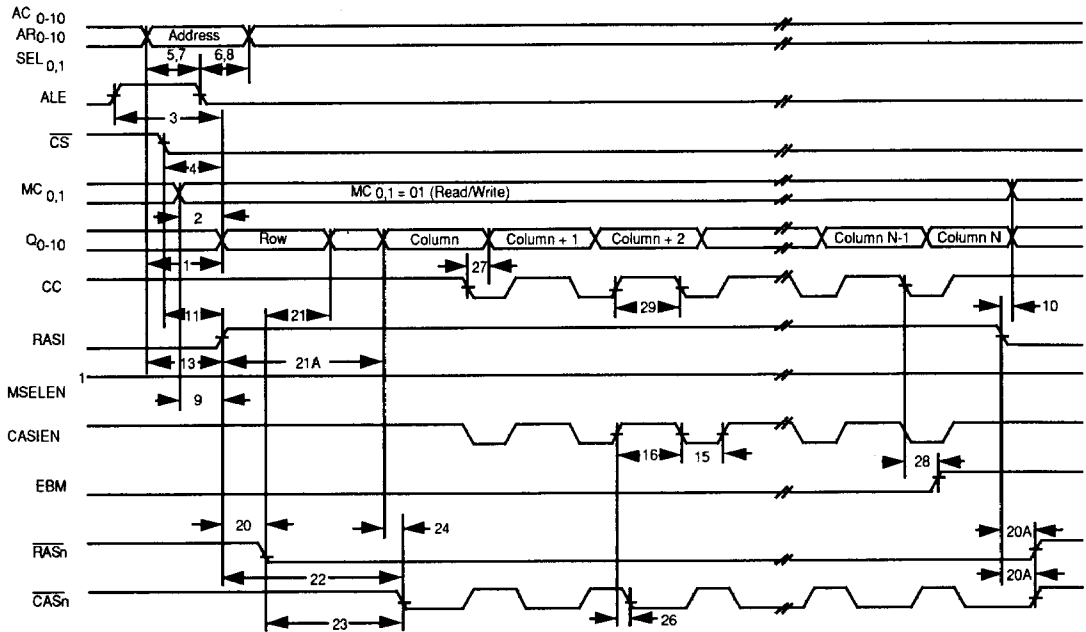
Figure 19. Standard Read/Write, Refresh Accesses with Auto-Timing

SWITCHING WAVEFORMS



11068C-057A

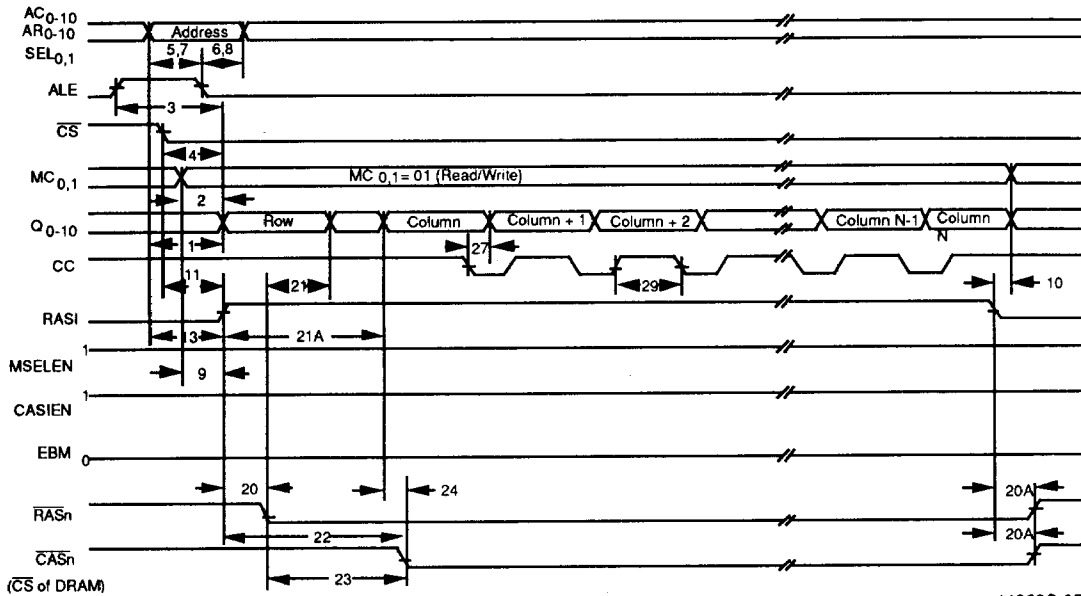
Figure 20. Read/Write, with Auto-Timing with External Override on MSELN



11068C-058A

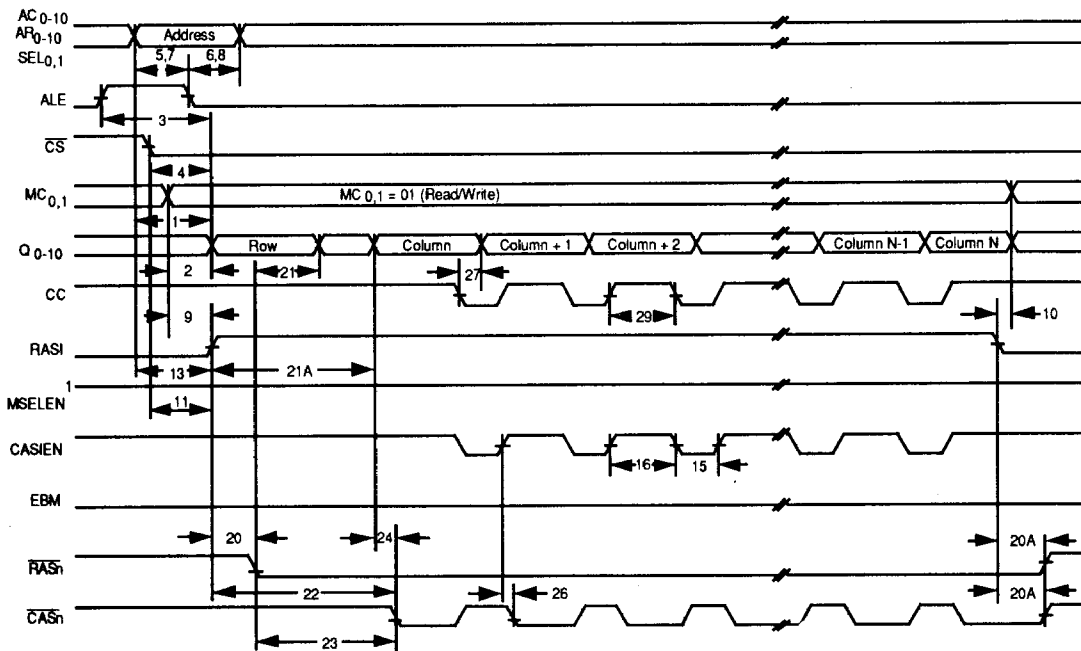
Figure 21. Burst Mode Access Ended by the Am29C668 (Auto-Timing with External Override on CAS_iEN)

SWITCHING WAVEFORMS



11068C-059A

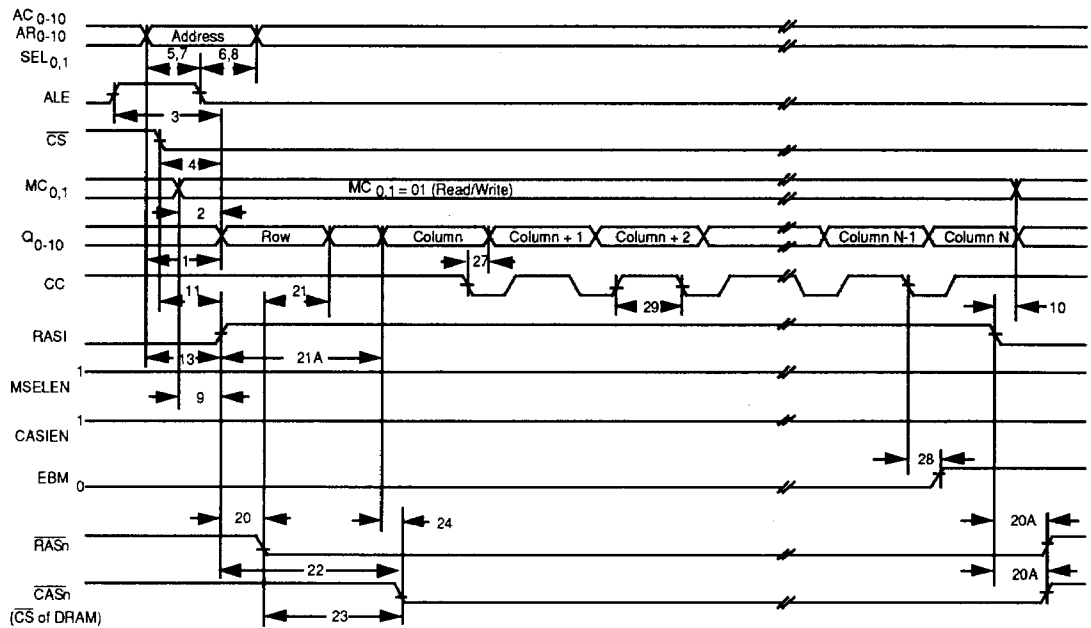
Figure 22. Burst Mode Access with Static Column DRAMs Ended by the Microprocessor (Auto-Timing)



11068C-060A

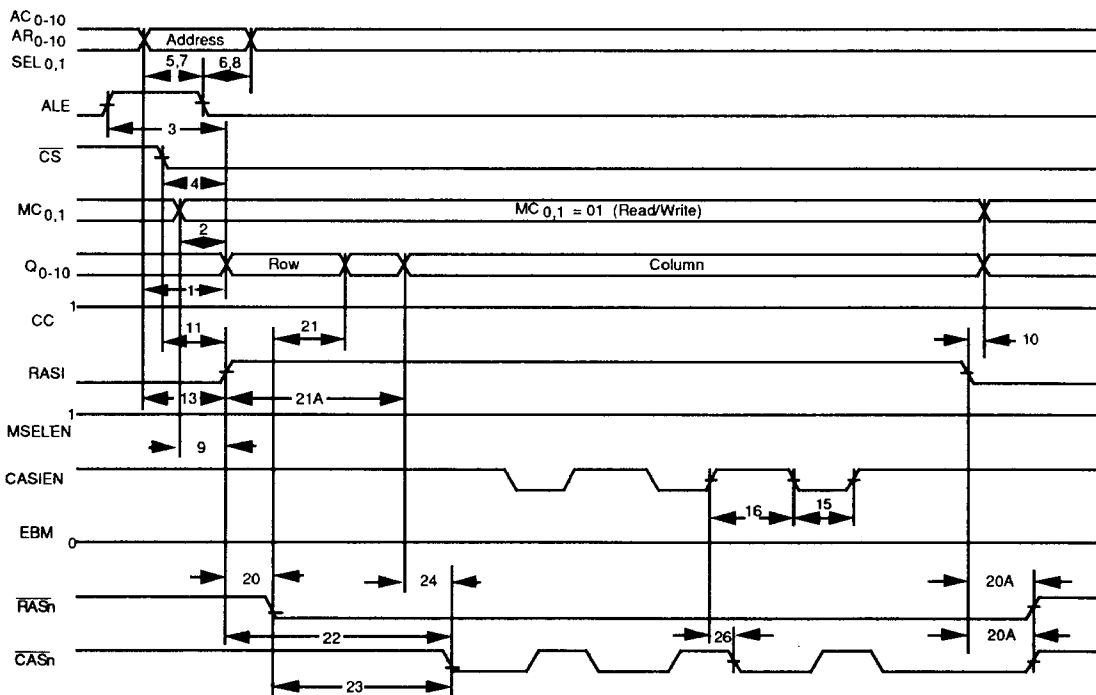
Figure 23. Burst Mode Access Ended by the Microprocessor (Auto-Timing with External Override)

SWITCHING WAVEFORMS



11068C-061A

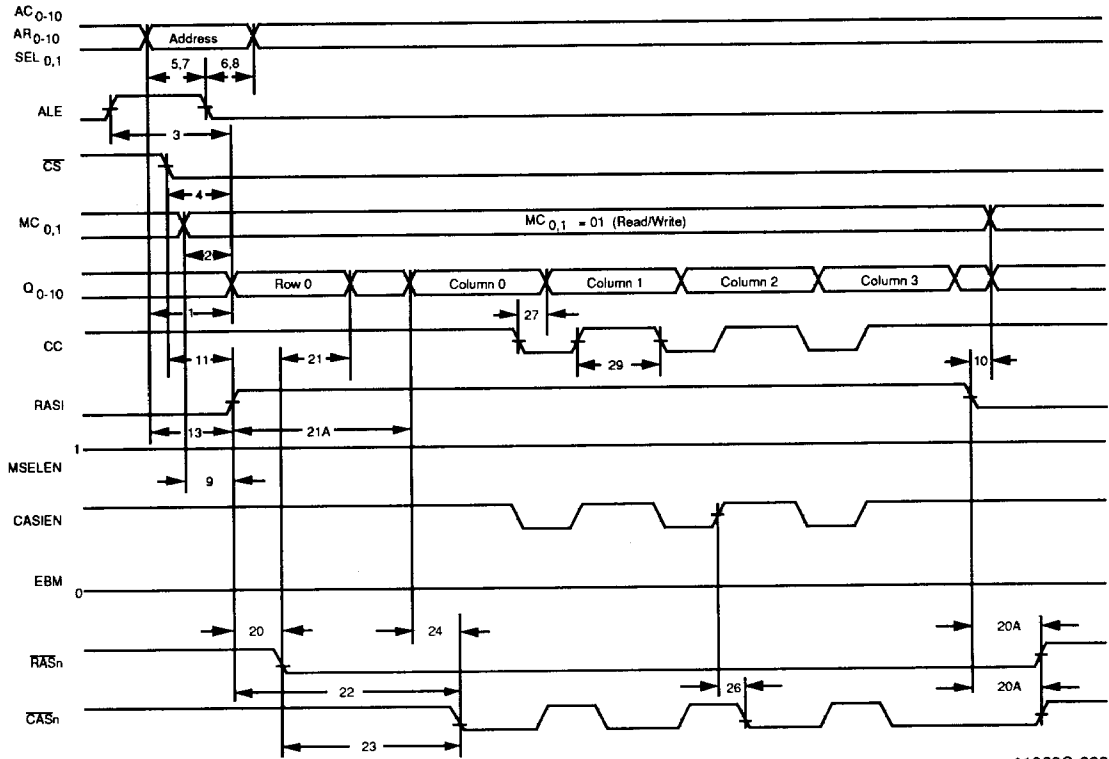
Figure 24. Burst Mode Access with Static Column DRAMs Ended by the Am29C668 (Auto-Timing)



11068C-062A

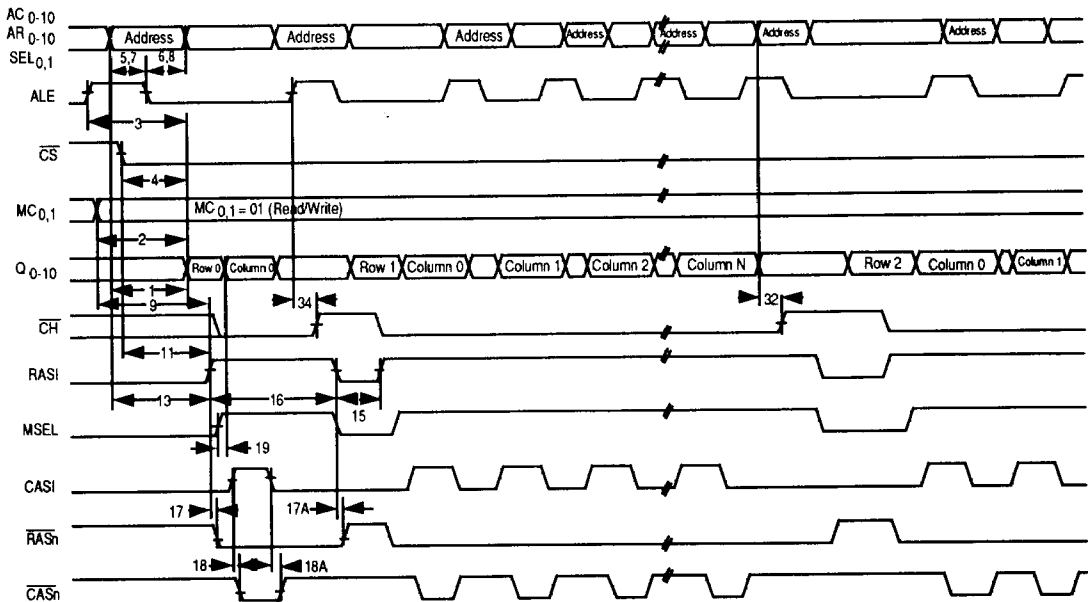
Figure 25. Burst Mode Access with Nibble Mode DRAMs (Auto-Timing with External Override)

SWITCHING WAVEFORMS



11068C-063A

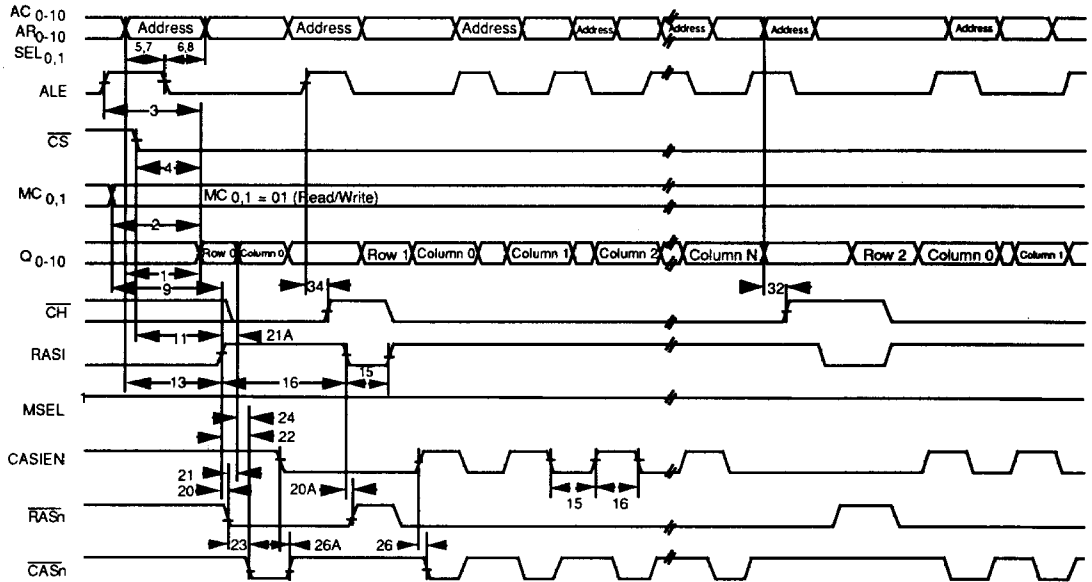
Figure 26. Nibble Mode Access with Page Mode DRAMs (Auto-Timing with External Override on CASIEN)



11068C-064A

Figure 27. "Cache" Mode Access with Page Mode DRAMs (External Timing)

SWITCHING WAVEFORMS



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Figure 28. "Cache" Mode Access with Page Mode DRAMs (Auto-Timing with External Override)