

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 4.5A, 500V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

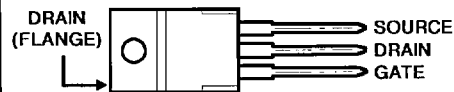
Description

The BUZ41A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ41A is supplied in the JEDEC TO-220AB plastic package.

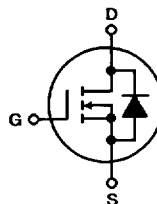
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	BUZ41A	UNITS
Drain-Source Voltage	500	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	500	V
Continuous Drain Current $T_C = +35^\circ\text{C}$	4.5	A
Pulsed Drain Current $T_C = +25^\circ\text{C}$	18	A
Gate-Source Voltage	± 20	V
Maximum Power Dissipation $T_C = +25^\circ\text{C}$	75	W
Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
DIN Humidity Category - DIN 40040	E	
IEC Climatic Category - DIN IEC 68-1	55/150/56	

Specifications BUZ41A

ELECTRICAL CHARACTERISTICS At Case Temperature (T_c) = 25° C Unless Otherwise Specified

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}$ $I_D = 0.25\text{ mA}$	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_J = 25\text{ }^{\circ}\text{C}$ $T_J = 125\text{ }^{\circ}\text{C}$ $V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20\text{ V}$ $V_{DS} = 0\text{ V}$	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 2.5\text{ A}$	—	1.4	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}$ $I_D = 2.5\text{ A}$	1.5	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$	—	1500	2000	pF
Output Capacitance	C_{oss}		—	110	170	
Reverse Transfer Capacitance	C_{rss}		—	40	70	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30\text{ V}$ $I_D = 2.6\text{ A}$ $V_{GS} = 10\text{ V}$ $R_{GS} = 50\text{ }\Omega$	—	30	45	ns
			—	40	60	
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		—	110	140	
			—	50	65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR} $T_c = 25^\circ\text{ C}$	—	—	4.5	A
Pulsed Reverse Drain Current	I_{DRM}	—	—	18	A
Diode Forward Voltage	V_{SD} $I_F = 2 \times I_{DR}$ $V_{GS} = 0\text{ V}, T_j = 25^\circ\text{ C}$	—	1.1	1.5	V
Reverse Recovery Time	t_{rr} $T_j = 25^\circ\text{ C}, I_F = I_{DR}$	—	1200	—	ns
Reverse Recovered Charge	Q_{RR} $di_F/dt = 100\text{ A}/\mu\text{s}, V_R = 100\text{ V}$	—	6	—	μC

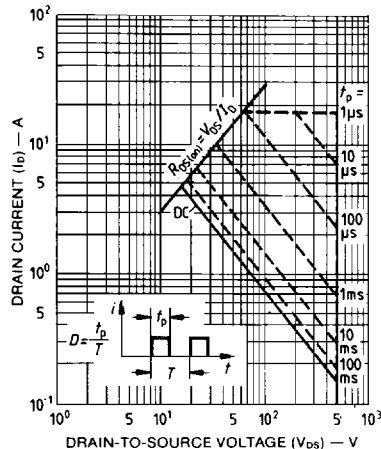


Fig. 1 - Maximum safe operating areas for all types.

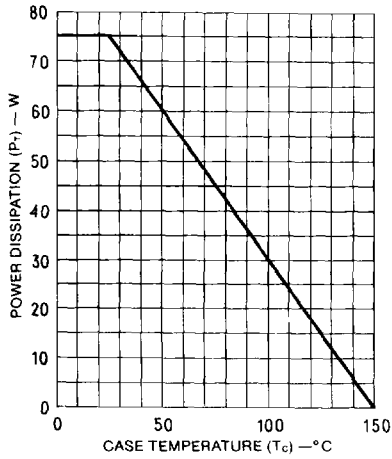


Fig. 2 - Power vs. temperature derating curve for all types.

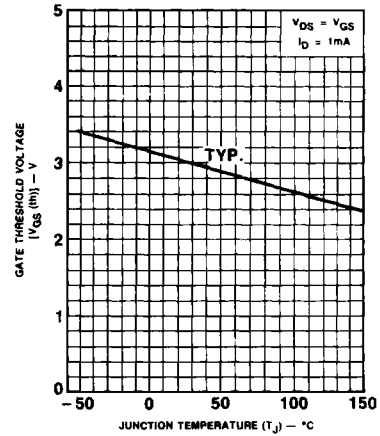


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

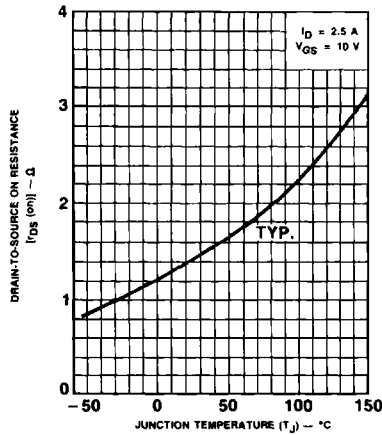


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

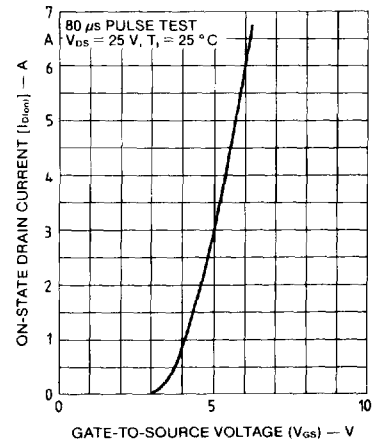


Fig. 5 - Typical transfer characteristics for all types.

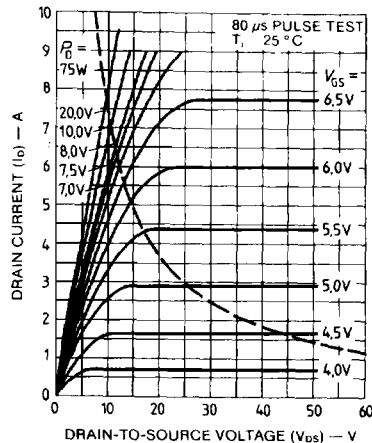


Fig. 6 - Typical output characteristics.

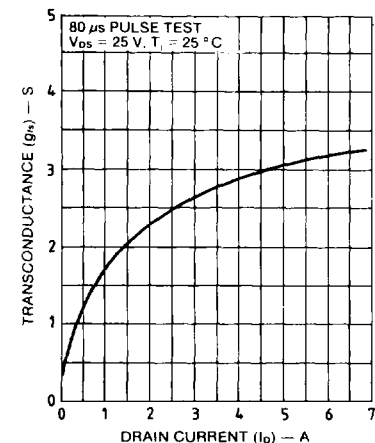


Fig. 7 - Typical transconductance vs. drain current.

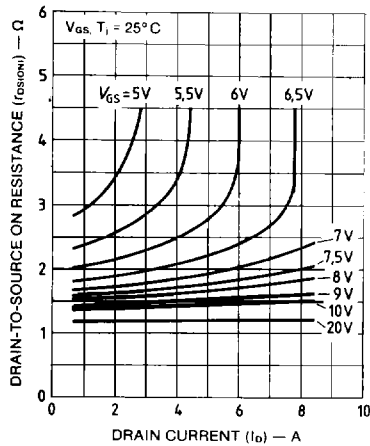


Fig. 8 - Typical on-resistance vs. drain current.

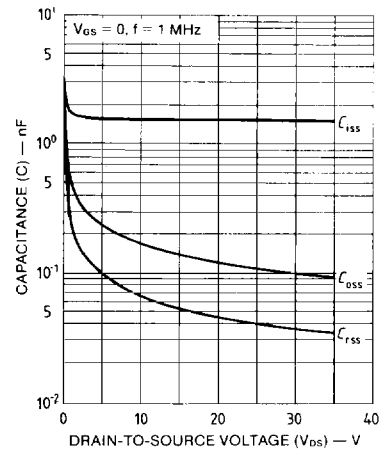


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

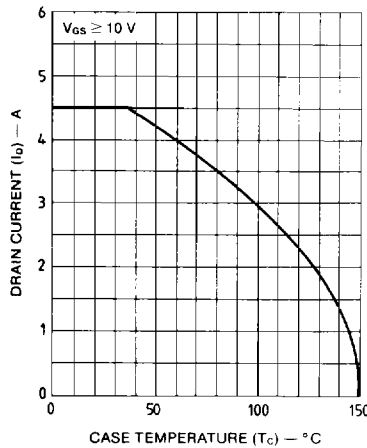


Fig. 10 - Maximum drain current vs. case temperature.

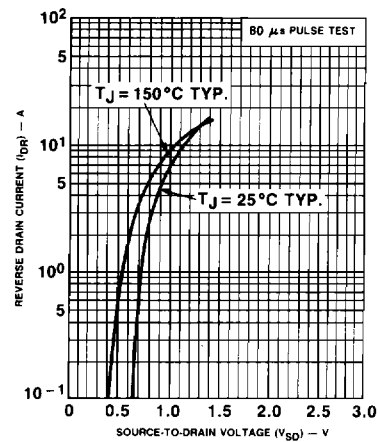


Fig. 11 - Typical source-drain diode forward voltage.

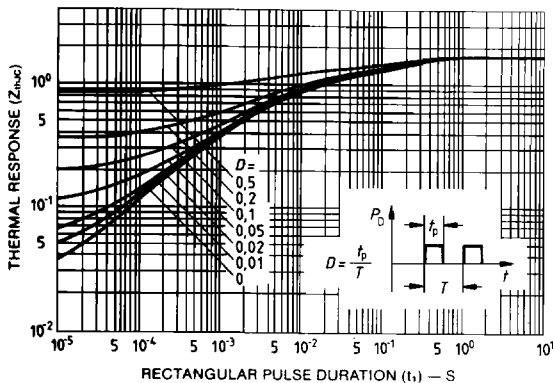


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

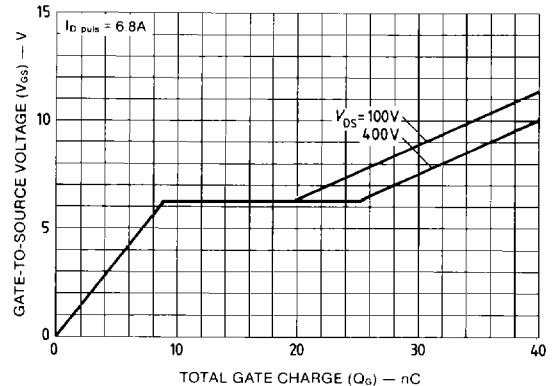


Fig. 13 - Typical gate charge vs. gate-to-source voltage.