Intel386™ EX Embedded Microprocessor

Datasheet

Product Features

- Static Intel386™ CPU Core
  - —Low Power Consumption
  - —Operating Power Supply
    EXTB: 2.7 V to 3.6 V
    EXTC: 4.5 V to 5.5 V
  - —Operating Frequency
    20 MHz EXTB at 2.7 V to 3.6 V
    25 MHz EXTB at 3.0 V to 3.6 V;
    25/33 MHz EXTC at 4.5 V to 5.5 V
- Transparent Power-management System Architecture
  - —Intel System Management Mode Architecture Extension for Truly Compatible Systems
  - —Power Management Transparent to Operating Systems and Application Programs
  - —Programmable Power-management Modes
- Powerdown Mode
  - —Clock Stopping at Any Time
  - —Only 10–20 µA Typical CPU Sink Current
- Full 32-bit Internal Architecture
  - —8-, 16-, 32-bit Data Types
  - —8 General Purpose 32-bit Registers
- Runs Intel386 Architecture Software in a Cost-effective 16-bit Hardware Environment
  - —Runs Same Applications and Operating Systems as the Intel386 SX and Intel386 DX Processors
  - —Object Code Compatible with 8086, 80186, 80286, and Intel386 Processors
- High-performance 16-bit Data Bus
  - —Two-clock Bus Cycles
  - —Address Pipelining Allows Use of Slower, Inexpensive Memories
- Extended Temperature Range
- Integrated Memory Management Unit
  - —Virtual Memory Support
  - —Optional On-chip Paging
  - —4 Levels of Hardware-enforced Protection
  - —MMU Fully Compatible with MMUs of the 80286 and Intel386 DX Processors
- Virtual 8086 Mode Allows Execution of 8086 Software in a Protected and Paged System
- Large Uniform Address Space
  - —64 Megabyte Physical
  - —64 Terabyte Virtual
  - —4 Gigabyte Maximum Segment Size
- On-chip Debugging Support Including Breakpoint Registers
- Complete System Development Support
- High Speed CHMOS Technology
- Two Package Types
  - —132-pin Plastic Quad Flatpack
  - —144-pin Thin Quad Flatpack
- Integrated Peripheral Functions
  - —Clock and Power Management Unit
  - —Chip-select Unit
  - —Interrupt Control Unit
  - —Timer/Counter Unit
  - —Watchdog Timer Unit
  - —Asynchronous Serial I/O Unit
  - —Synchronous Serial I/O Unit
  - —Parallel I/O Unit
  - —DMA and Bus Arbiter Unit
  - —Refresh Control Unit
  - —JTAG-compliant Test-logic Unit

This datasheet applies to devices marked EXTB and EXTC. If you require information about devices marked EXSA or EXTA, refer to a previous revision of this datasheet, order number 272420-004.

Order Number: 272420-007
October 1998

Datasheet

Contents

Figures

Tables

Revision History

This datasheet applies to devices marked EXTB and EXTC. If you require information about devices marked EXSA or EXTA, refer to a previous revision of this datasheet, order number 272420-004.

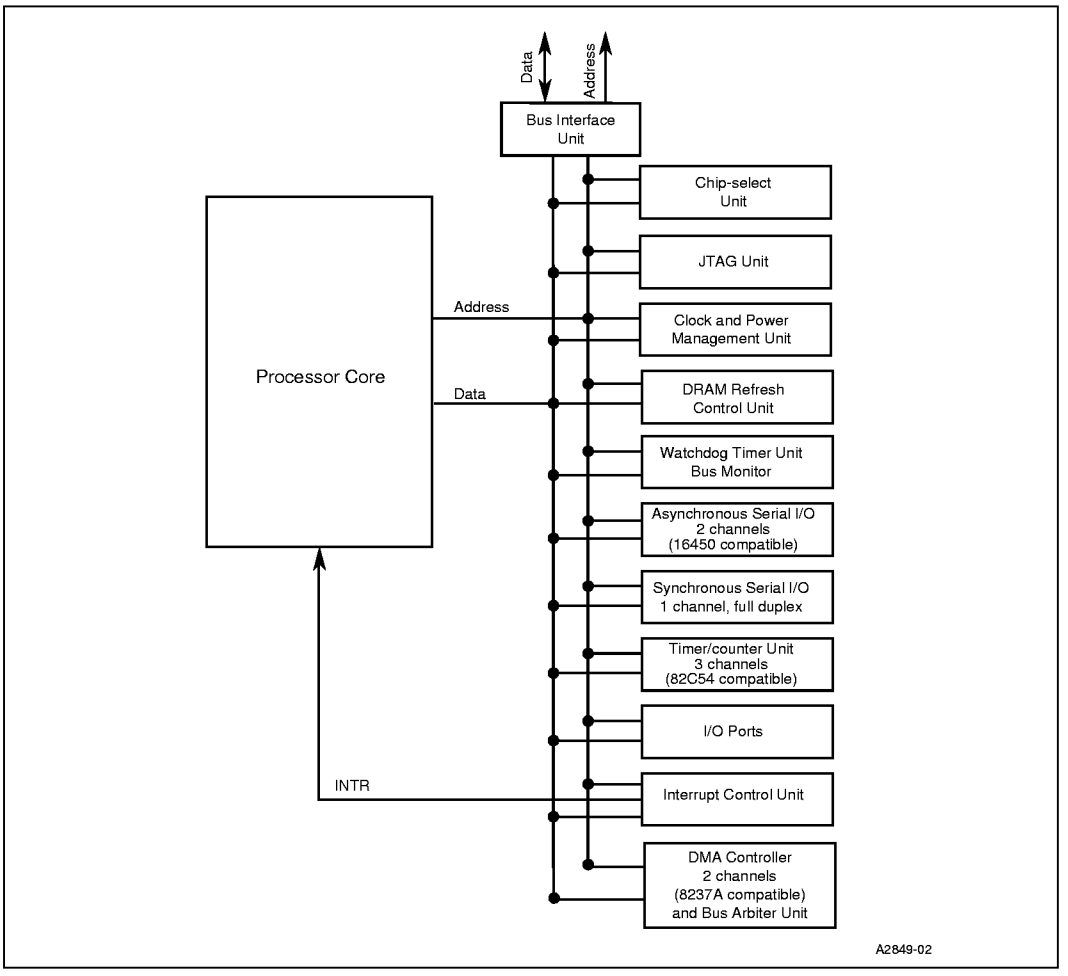
Revision	Date	Description
007	10/98	The document was updated to the larger page size. All known device errata for the datasheet have been incorporated into this new revision.
006	5/96	Corrections added.
005	12/95	This datasheet applied to the new EXTB and EXTC devices.
004	9/94	This datasheet applied to devices marked EXSA or EXTA.

1.0 Introduction

The Intel386™ EXTB embedded processor operates at 20 or 25 MHz at 3 Volts nominal. The Intel386 EXTC embedded processor operates at 25 or 33 MHz at 5 Volts. In this datasheet, "Intel386 EX processor" refers to both the Intel386 EXTB and EXTC processors.

The Intel386 EX embedded processor is a highly integrated, 32-bit, fully static processor optimized for embedded control applications. With a 16-bit external data bus, a 26-bit external address bus, and Intel's System Management Mode (SMM), the Intel386 EX microprocessor brings the vast software library of Intel386 architecture to embedded systems. It provides the performance benefits of 32-bit programming with the cost savings associated with 16-bit hardware systems.

Figure 1. Intel386™ EX Embedded Processor Block Diagram



2.0 Pin Assignment

Figure 2. Intel386™ EX Embedded Processor 132-Pin PQFP Pin Assignment

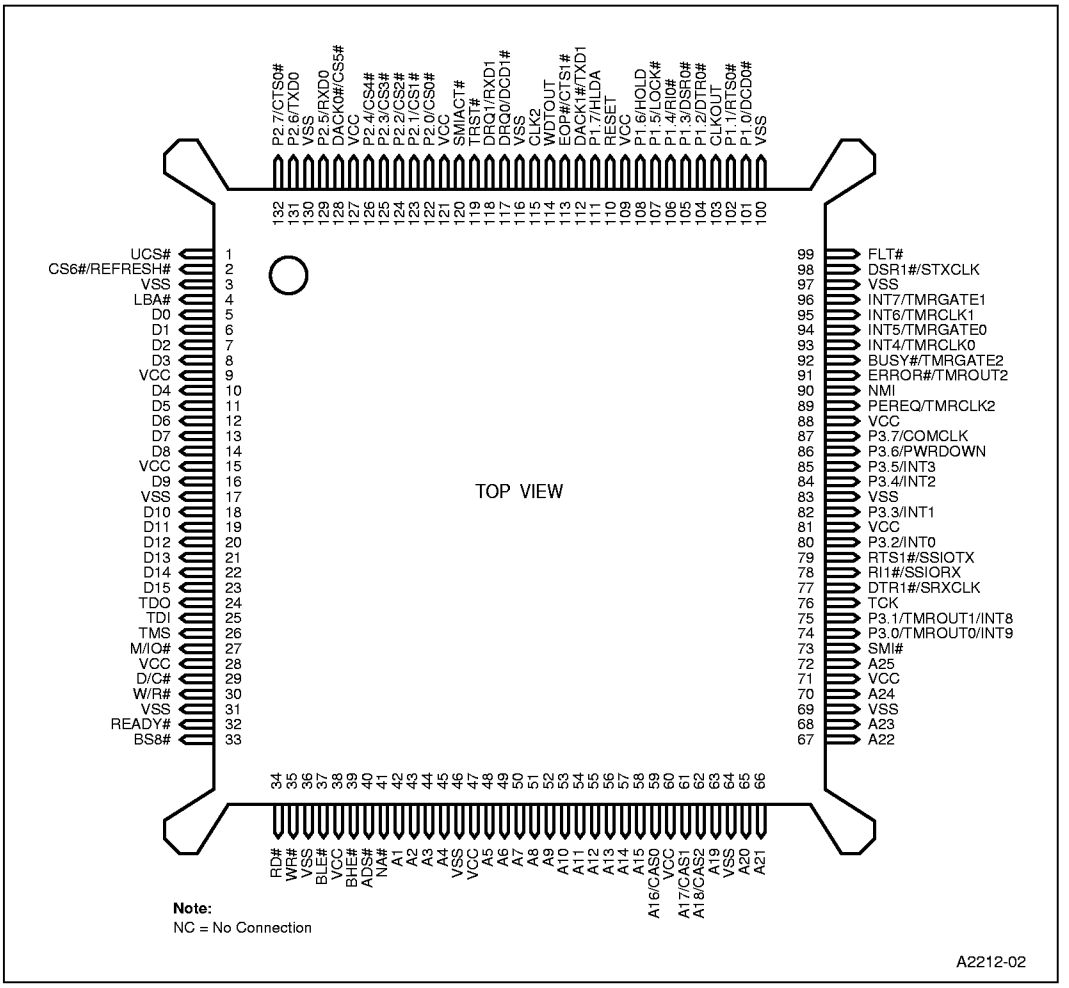


Table 1. 132-Pin PQFP Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	UCS#	34	RD#	67	A22	100	V_{SS}
2	CS6#/REFRESH#	35	WR#	68	A23	101	P1.0/DCD0#
3	V_{SS}	36	V_{SS}	69	V_{SS}	102	P1.1/RTS0#
4	LBA#	37	BLE#	70	A24	103	CLKOUT
5	D0	38	V_{CC}	71	V_{CC}	104	P1.2/DTR0#
6	D1	39	BHE#	72	A25	105	P1.3/DSR0#
7	D2	40	ADS#	73	SMI#	106	P1.4/RI0#
8	D3	41	NA#	74	P3.0/TMROUT0/INT9	107	P1.5/LOCK#
9	V_{CC}	42	A1	75	P3.1/TMROUT1/INT8	108	P1.6/HOLD
10	D4	43	A2	76	TCK	109	V_{CC}
11	D5	44	A3	77	DTR1#/SRXCLK	110	RESET
12	D6	45	A4	78	RI1#/SSIORX	111	P1.7/HLDA
13	D7	46	V_{SS}	79	RTS1#/SSIOTX	112	DACK1#/TXD1
14	D8	47	V_{CC}	80	P3.2/INT0	113	EOP#/CTS1#
15	V_{cc}	48	A5	81	V_{CC}	114	WDTOUT
16	D9	49	A6	82	P3.3/INT1	115	CLK2
17	V_{ss}	50	A7	83	V_{SS}	116	V_{SS}
18	D10	51	A8	84	P3.4/INT2	117	DRQ0/DCD1#
19	D11	52	A9	85	P3.5/INT3	118	DRQ1/RXD1
20	D12	53	A10	86	P3.6/PWRDOWN	119	TRST#
21	D13	54	A11	87	P3.7/COMCLK	120	SMIACT#
22	D14	55	A12	88	V_{CC}	121	V_{CC}
23	D15	56	A13	89	PEREQ/TMRCLK2	122	P2.0/CS0#
24	TDO	57	A14	90	NMI	123	P2.1/CS1#
25	TDI	58	A15	91	ERROR#/TMROUT2	124	P2.2/CS2#
26	TMS	59	A16/CAS0	92	BUSY#/TMRGATE2	125	P2.3/CS3#
27	M/IO#	60	V_{CC}	93	INT4/TMRCLK0	126	P2.4/CS4#
28	V_{CC}	61	A17/CAS1	94	INT5/TMRGATE0	127	V_{CC}
29	D/C#	62	A18/CAS2	95	INT6/TMRCLK1	128	DACK0#/CS5#
30	W/R#	63	A19	96	INT7/TMRGATE1	129	P2.5/RXD0
31	V_{SS}	64	V_{SS}	97	V_{SS}	130	V_{SS}
32	READY#	65	A20	98	DSR1#/STXCLK	131	P2.6/TXD0
33	BS8#	66	A21	99	FLT#	132	P2.7/CTS0#

Figure 3. Intel386™ EX Embedded Processor 144-Pin TQFP Pin Assignment

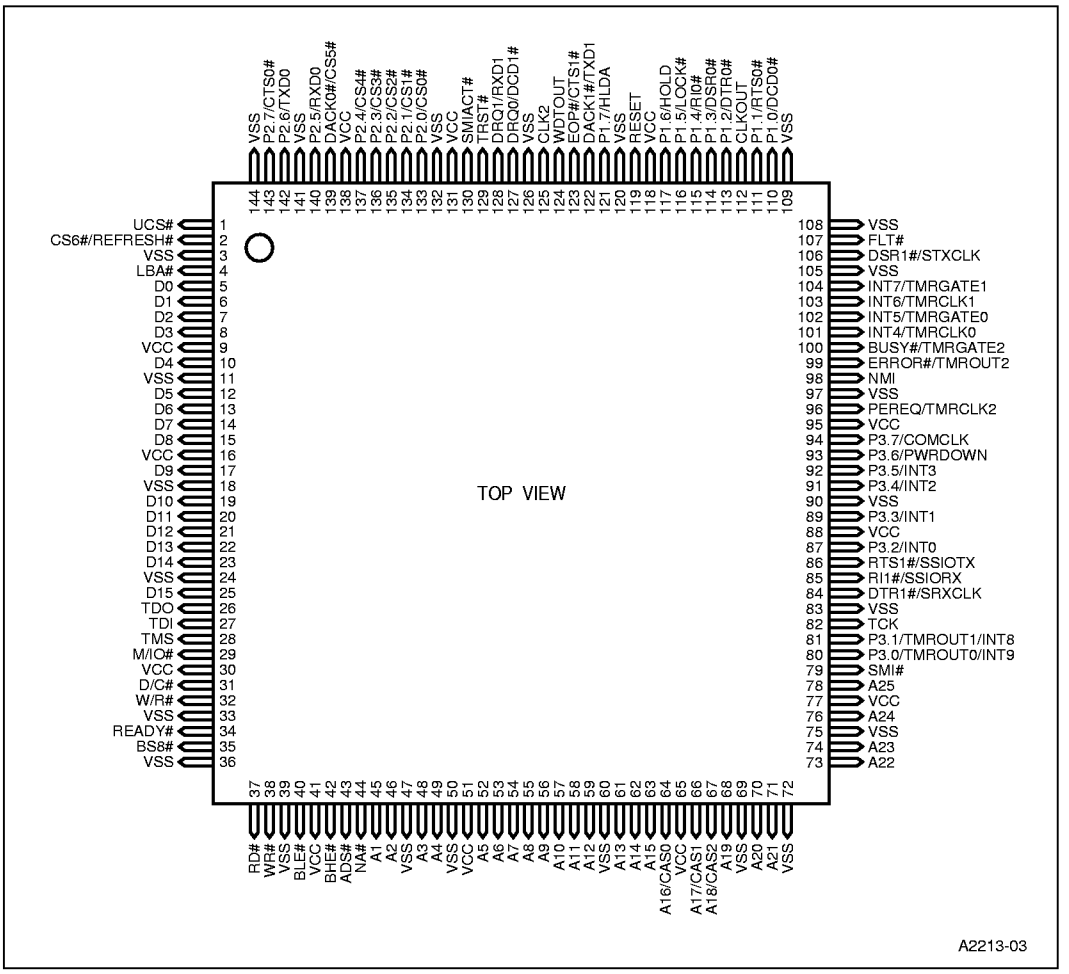


Table 2. 144-Pin TQFP Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	UCS#	37	RD#	73	A22	109	V_{SS}
2	CS6#/REFRESH#	38	WR#	74	A23	110	P1.0/DCD0#
3	V_{SS}	39	V_{SS}	75	V_{SS}	111	P1.1/RTS0#
4	LBA#	40	BLE#	76	A24	112	CLKOUT
5	D0	41	V_{CC}	77	V_{CC}	113	P1.2/DTR0#
6	D1	42	BHE#	78	A25	114	P1.3/DSR0#
7	D2	43	ADS#	79	SMI#	115	P1.4/RI0#
8	D3	44	NA#	80	P3.0/TMROUT0/INT9	116	P1.5/LOCK#
9	V_{CC}	45	A1	81	P3.1/TMROUT1/INT8	117	P1.6/HOLD
10	D4	46	A2	82	TCK	118	V_{CC}
11	V_{SS}	47	V_{SS}	83	V_{SS}	119	RESET
12	D5	48	A3	84	DTR1#/SRXCLK	120	V_{SS}
13	D6	49	A4	85	RI1#/SSIORX	121	P1.7/HLDA
14	D7	50	V_{SS}	86	RTS1#/SSIOTX	122	DACK1#/TXD1
15	D8	51	V_{CC}	87	P3.2/INT0	123	EOP#/CTS1#
16	V_{CC}	52	A5	88	V_{CC}	124	WDTOUT
17	D9	53	A6	89	P3.3/INT1	125	CLK2
18	V_{SS}	54	A7	90	V_{SS}	126	V_{SS}
19	D10	55	A8	91	P3.4/INT2	127	DRQ0/DCD1#
20	D11	56	A9	92	P3.5/INT3	128	DRQ1/RXD1
21	D12	57	A10	93	P3.6/PWRDOWN	129	TRST#
22	D13	58	A11	94	P3.7/COMCLK	130	SMIACT#
23	D14	59	A12	95	V_{CC}	131	V_{CC}
24	V_{SS}	60	V_{SS}	96	PEREQ/TMRCLK2	132	V_{SS}
25	D15	61	A13	97	V_{SS}	133	P2.0/CS0#
26	TDO	62	A14	98	NMI	134	P2.1/CS1#
27	TDI	63	A15	99	ERROR#/TMROUT2	135	P2.2/CS2#
28	TMS	64	A16/CAS0	100	BUSY#/TMRGATE2	136	P2.3/CS3#
29	M/IO#	65	V_{CC}	101	INT4/TMRCLK0	137	P2.4/CS4#
30	V_{CC}	66	A17/CAS1	102	INT5/TMRGATE0	138	V_{CC}
31	D/C#	67	A18/CAS2	103	INT6/TMRCLK1	139	DACK0#/CS5#
32	W/R#	68	A19	104	INT7/TMRGATE1	140	P2.5/RXD0
33	V_{SS}	69	V_{SS}	105	V_{SS}	141	V_{SS}
34	READY#	70	A20	106	DSR1#/STXCLK	142	P2.6/TXD0
35	BS8#	71	A21	107	FLT#	143	P2.7/CTS0#
36	V_{SS}	72	V_{SS}	108	V_{SS}	144	V_{SS}

3.0 Pin Description

Table 4 lists the Intel386 EX embedded processor pin descriptions. Table 3 defines the abbreviations used in the Type and Output States columns of Table 4.

Table 3. Pin Type and Output State Nomenclature

Symbol	Description
Pin Type	
#	The named signal is active low.
I	Standard TTL input signal.
O	Standard CMOS output signal.
I/O	Input and output signal.
I/OD	Input and open-drain output signal.
ST	Schmitt-triggered input signal.
P	Power pin.
G	Ground pin.
Output State	
H(1)	Output driven to V_{CC} during Bus Hold
H(0)	Output driven to V_{SS} during Bus Hold
H(Z)	Output floats during Bus Hold
H(Q)	Output remains active during Bus Hold
H(X)	Output retains current state during Bus Hold
R(WH)	Output Weakly Held at V_{CC} during Reset
R(WL)	Output Weakly Held at V_{SS} during Reset
R(1)	Output driven to V_{CC} during Reset
R(0)	Output driven to V_{SS} during Reset
R(Z)	Output floats during Reset
R(Q)	Output remains active during Reset
R(X)	Output retains current state during Reset
I(1)†	Output driven to V_{CC} during Idle Mode
I(0)	Output driven to V_{SS} during Idle Mode
I(Z)	Output floats during Idle Mode
I(Q)	Output remains active during Idle Mode
I(X)	Output retains current state during Idle Mode
P(1)	Output driven to V_{CC} during Powerdown Mode
P(0)	Output driven to V_{SS} during Powerdown Mode
P(Z)	Output floats during Powerdown Mode
P(Q)	Output remains active during Powerdown Mode
P(X)	Output retains current state during Powerdown Mode

† The idle mode output states assume that no internal bus master (DMA or RCU) has control of the bus during idle mode

Table 4. Intel386™ EX Microprocessor Pin Descriptions (Sheet 1 of 6)

Symbol	Type	Output States	Name and Function
A25:1	O	H(Z) R(1) I(1) P(1)	**Address Bus** outputs physical memory or port I/O addresses. These signals are valid when ADS# is active and remain valid until the next T1, T2P, or Ti. During HOLD cycles they are driven to a high-impedance state. A18:16 are multiplexed with CAS2:0.
ADS#	O	H(Z) R(1) I(1) P(1)	**Address Status** indicates that the processor is driving a valid bus-cycle definition and address (W/R#, D/C#, M/IO#, A25:1, BHE#, BLE#) onto its pins.
BHE#	O	H(Z) R(0) I(X) P(0)	**Byte High Enable** indicates that the processor is transferring a high data byte.
BLE#	O	H(Z) R(0) I(X) P(1)	**Byte Low Enable** indicates that the processor is transferring a low data byte.
BS8#	I		**Bus Size** indicates that an 8-bit device is currently being addressed.
BUSY#	I		**Busy** indicates that the math coprocessor is busy. If BUSY# is sampled LOW at the falling edge of RESET, the processor performs an internal self test. BUSY# is multiplexed with TMRGATE2 and has a temporary weak pull-up resistor.
CAS2:0	O	H(Z) R(1) I(1) P(1)	**Cascade Address** carries the slave address information from the 8259A master interrupt module during interrupt acknowledge bus cycles. CAS2:0 are multiplexed with A18:16.
CLK2	ST		**Clock Input** is connected to an external clock that provides the fundamental timing for the device.
CLKOUT	O	H(Q) R(Q) I(Q) P(0)	**CLKOUT** is a PH1P clock output.
COMCLK	I		**Serial Communications Baud Clock** is an alternate clock source for the asynchronous serial ports. COMCLK is multiplexed with P3.7 and has a temporary weak pull-down resistor.
CS4:0#	O	H(1) R(WH) I(Q) P(X)	**Chip-selects** are activated when the address of a memory or I/O bus cycle is within the address region programmed by the user. They are multiplexed as follows: CS6# with REFRESH#, CS5# with DACK0#, and CS4:0# with P2.4:0.
CS6:5#	O	H(1) R(1) I(Q) P(X)	**Chip-selects** are activated when the address of a memory or I/O bus cycle is within the address region programmed by the user. They are multiplexed as follows: CS6# with REFRESH#, CS5# with DACK0#, and CS4:0# with P2.4:0.
CTS1:0#	I		**Clear to Send SIO1 and SIO0** prevent the transmission of data to the asynchronous serial port's RXD1 and RXD0 pins, respectively. CTS1# is multiplexed with EOP#, and CTS0# is multiplexed with P2.7. CTS1# requires an external pull-up resistor. Both have temporary weak pull-up resistors.

NOTES:
1. X if clock source is internal; Q if clock source is external
2. Q if JTAG unit is shifting out data, Z if it is not

Table 4. Intel386™ EX Microprocessor Pin Descriptions (Sheet 2 of 6)

Symbol	Type	Output States	Name and Function
D15:0	I/O	H(Z) R(Z) P(Z)	**Data Bus** inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles. During writes, this bus is driven during phase 2 of T1 and remains active until phase 2 of the next T1, T1P, or Ti. During reads, data is latched on the falling edge of phase 2.
DACK1:0#	O	H(1) R(1) I(Q) P(X)	**DMA Acknowledge 1 and 0** signal to an external device that the processor has acknowledged the corresponding DMA request and is relinquishing the bus. DACK1# is multiplexed with TXD1, and DACK0# is multiplexed with CS5#.
D/C#	O	H(Z) R(1) I(0) P(0)	**Data/Control** indicates whether the current bus cycle is a data cycle (memory or I/O read or write) or a control cycle (interrupt acknowledge, halt, or code fetch).
DCD1:0	I		**Data Carrier Detect SIO1 and SIO0** indicate that the modem or data set has detected the corresponding asynchronous serial channel's data carrier. DCD1# is multiplexed with DRQ0, and DCD0# is multiplexed with P1.0 and has a temporary weak pull-up resistor.
DRQ1:0	I		**DMA External Request 1 and 0** indicate that a peripheral requires DMA service. DRQ1 is multiplexed with RXD1, and DRQ0 is multiplexed with DCD1#.
DSR1:0#	I		**Data Set Ready SIO1 and SIO0** indicate that the modem or data set is ready to establish a communication link with the corresponding asynchronous serial channel. DSR1# is multiplexed with STXCLK and has a permanent weak pull-up resistor, and DSR0# is multiplexed with P1.3 and has a temporary weak pull-up resistor.
DTR1:0#	O	H(X) R(WH) I(X) P(X)	**Data Terminal Ready SIO1 and SIO0** indicate that the corresponding asynchronous serial channel is ready to establish a communication link with the modem or data set. DTR1# is multiplexed with SRXCLK, and DTR0# is multiplexed with P1.2.
EOP#	I/OD	H(Z) R(WH) I(Z) P(Z)	**End of Process** indicates that the processor has reached terminal count during a DMA transfer. An external device can also pull this pin LOW. EOP# is multiplexed with CTS1#.
ERROR#	I		**Error** indicates that the math coprocessor has an error condition. ERROR# is multiplexed with TMROUT2 and has a temporary weak pull-up resistor.
FLT#	I		**Float** forces all bidirectional and output signals except TDO to a high-impedance state. It has a permanent weak pull-up resistor. This pin should be tied to V_{CC} through a 3 to 7 KOhm pull-up resistor.
HLDA	O	H(1) R(WL) I(Q) P(X)	**Bus Hold Acknowledge** indicates that the processor has surrendered control of its local bus to another bus master. HLDA is multiplexed with P1.7.
HOLD	I		**Bus Hold Request** allows another bus master to request control of the local bus. HLDA active indicates that bus control has been granted. HOLD is multiplexed with P1.6. It has a temporary weak pull-down resistor.

NOTES:
1. X if clock source is internal; Q if clock source is external
2. Q if JTAG unit is shifting out data, Z if it is not

Table 4. Intel386™ EX Microprocessor Pin Descriptions (Sheet 3 of 6)

Symbol	Type	Output States	Name and Function
INT9:0	I		**Interrupt Requests** are maskable inputs that cause the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle. They are multiplexed as follows: INT9 with TMROUT0 and P3.0, INT8 with TMROUT1 and P3.1, INT7 with TMRGATE1, INT6 with TMRCLK1, INT5 with TMRGATE0, INT4 with TMRCLK0, and INT3:0 with P3.5:2. INT9, INT8, and INT3:0 have temporary weak pull-down resistors.
LBA#	O	H(1) R(1) I(Q) P(X)	**Local Bus Access** is asserted whenever the processor provides the READY# signal to terminate a bus transaction. This occurs when an internal peripheral address is accessed or when the chip-select unit provides the READY# signal.
LOCK#	O	H(Z) R(WH) I(X) P(X)	**Bus Lock** prevents other bus masters from gaining control of the system bus. LOCK# is multiplexed with P1.5.
M/IO#	O	H(Z) R(0) I(1) P(1)	**Memory/IO** Indicates whether the current bus cycle is a memory cycle or an I/O cycle. When M/IO# is HIGH, the bus cycle is a memory cycle; when M/IO# is LOW, the bus cycle is an I/O cycle.
NA#	I		**Next Address** requests address pipelining.
NMI	ST		**Nonmaskable Interrupt Request** is a non-maskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge cycle.
PEREQ	I		**Processor Extension Request** indicates that the math coprocessor has data to transfer to the processor. PEREQ is multiplexed with TMRCLK2 and has a temporary weak pull-down resistor.
P1.5:0	I/O	H(X) R(WH) I(X) P(X)	**Port 1, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P1.7 with HLDA, P1.6 with HOLD, P1.5 with LOCK#, P1.4 with RI0#, P1.3 with DSR0#, P1.2 with DTR0#, P1.1 with RTS0#, and P1.0 with DCD0#.
P1.7:6	I/O	H(X) R(WL) I(X) P(X)	**Port 1, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P1.7 with HLDA, P1.6 with HOLD, P1.5 with LOCK#, P1.4 with RI0#, P1.3 with DSR0#, P1.2 with DTR0#, P1.1 with RTS0#, and P1.0 with DCD0#.
P2.7,4:0	I/O	H(X) R(WH) I(X) P(X)	**Port 2, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P2.7 with CTS0#, P2.6 with TXD0, P2.5 with RXD0, and P2.4:0 with CS4:0#.
P2.6:5	I/O	H(X) R(WL) I(X) P(X)	**Port 2, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P2.7 with CTS0#, P2.6 with TXD0, P2.5 with RXD0, and P2.4:0 with CS4:0#.
P3.7:0	I/O	H(X) R(WL) I(X) P(X)	**Port 3, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P3.7 with COMCLK, P3.6 with PWRDOWN, P3.5:2 with INT3:0, and P3.1:0 with TMROUT1:0 and INT8:9.

NOTES:
1. X if clock source is internal; Q if clock source is external
2. Q if JTAG unit is shifting out data, Z if it is not

Table 4. Intel386™ EX Microprocessor Pin Descriptions (Sheet 4 of 6)

Symbol	Type	Output States	Name and Function
PWRDOWN	O	H(Q) R(WL) I(X) P(1)	**Powerdown** indicates that the processor is in powerdown mode. PWRDOWN is multiplexed with P3.6.
RD#	O	H(1) R(1) I(1) P(1)	**Read Enable** indicates that the current bus cycle is a read cycle.
READY#	I/O	H(Z) R(Z) I(Z) P(Z)	**Ready** indicates that the current bus transaction has completed. An external device or an internal signal can drive READY#. Internally, the chip-select wait-state logic can generate the ready signal and drive the READY# pin active.
RESET	ST		**Reset** suspends any operation in progress and places the processor into a known reset state.
REFRESH#	O	H(1) R(1) I(Q) P(X)	**Refresh** indicates that the current bus cycle is a refresh cycle. REFRESH# is multiplexed with CS6#.
RI1:0#	I		**Ring Indicator SIO1 and SIO0** indicate that the modem or data set has received a telephone ringing signal. RI1# is multiplexed with SSIORX, and RI0# is multiplexed with P1.4 and has a temporary weak pull-up resistor.
RTS1#	O	H(X) R(WL) I(X) P(X)	**Request-to-send SIO1 and SIO0** indicate that corresponding asynchronous serial channel is ready to exchange data with the modem or data set. RTS1# is multiplexed with SSIOTX, and RTS0# is multiplexed with P1.1.
RTS0#	O	H(X) R(WH) I(X) P(X)	**Request-to-send SIO1 and SIO0** indicate that corresponding asynchronous serial channel is ready to exchange data with the modem or data set. RTS1# is multiplexed with SSIOTX, and RTS0# is multiplexed with P1.1.
RXD1:0	I		**Receive Data SIO1 and SIO0** accept serial data from the modem or data set to the corresponding asynchronous serial channel. RXD1 is multiplexed with DRQ1, and RXD0 is multiplexed with P2.5 and has a temporary weak pull-down resistor.
SMI#	ST		**System Management Interrupt** invokes System Management Mode (SMM). SMI# is the highest priority external interrupt. It is latched on its falling edge and forces the CPU into SMM upon completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# cannot interrupt LOCKed bus cycles or a currently executing SMM. When the processor receives a second SMI# while in SMM, it latches the second SMI# on the SMI# falling edge. However, the processor must exit SMM by executing a resume instruction (RSM) before it can service the second SMI#. SMI# has a permanent weak pull-up resistor.
SMIACT#	O	H(1) R(1) I(X) P(X)	**System Management Interrupt Active** indicates that the processor is operating in System Management Mode (SMM). It is asserted when the processor initiates an SMM sequence and remains asserted (LOW) until the processor executes the resume instruction (RSM).

NOTES:
1. X if clock source is internal; Q if clock source is external
2. Q if JTAG unit is shifting out data, Z if it is not

Table 4. Intel386™ EX Microprocessor Pin Descriptions (Sheet 5 of 6)

Symbol	Type	Output States	Name and Function
SRXCLK	I/O	H(Q) R(WH) I(Q) P(X)/P(Q)[Note 1]	**SSIO Receive Clock** synchronizes data being accepted by the synchronous serial port. SRXCLK is multiplexed with DTR1#.
SSIORX	I		**SSIO Receive Serial Data** accepts serial data (most-significant bit first) being sent to the synchronous serial port. SSIORX is multiplexed with RI1#.
SSIOTX	O	H(Q) R(WL) I(Q) P(X)/P(Q)[Note 1]	**SSIO Transmit Serial Data** sends serial data (most-significant bit first) from the synchronous serial port. SSIOTX is multiplexed with RTS1#. Intel does not specify a data hold time for SSIOTX. Slower external devices may require additional hardware to properly interface the SSIO unit.
STXCLK	I/O	H(Q) R(WH) I(Q) P(X)/P(Q)[Note 1]	**SSIO Transmit Clock** synchronizes data being sent by the synchronous serial port. STXCLK is multiplexed with DSR1.
TCK	I		**TAP (Test Access Port) Controller Clock** provides the clock input for the JTAG logic. It has a permanent weak pull-up resistor.
TDI	I		**TAP (Test Access Port) Controller Data Input** is the serial input for test instructions and data. It has a permanent weak pull-up resistor.
TDO	O	H(Z)/H(Q)[Note 2] R(Z)/R(Q)[Note 2] I(Z)/I(Q)[Note 2] P(Z)/ P(Q)[Note 2]	**TAP (Test Access Port) Controller Data Output** is the serial output for test instructions and data.
TMRCLK2:0	I		**Timer/Counter Clock Inputs** can serve as external clock inputs for the corresponding timer/counters. (The timer/counters can also be clocked internally.) They are multiplexed as follows: TMRCLK2 with PEREQ, TMRCLK1 with INT6, and TMRCLK0 with INT4. TMRCLK2 has a temporary weak pull-down resistor.
TMRGATE2:0	I		**Timer/Counter Gate Inputs** can control the corresponding timer/counter's counting (enable, disable, or trigger, depending on the programmed mode). They are multiplexed as follows: TMRGATE2 with BUSY#, TMRGATE1 with INT7, and TMRGATE0 with INT5. TMRGATE2 has a temporary weak pull-up resistor.
TMROUT2	O	H(Q) R(WH) I(Q) P(X)/P(Q)[Note 1]	**Timer/Counter Outputs** provide the output of the corresponding timer/counter. The form of the output depends on the programmed mode. They are multiplexed as follows: TMROUT2 with ERROR#, TMROUT1 with P3.1 and INT8, and TMROUT0 with P3.0 and INT9.
TMROUT1:0	O	H(Q) R(WL) I(Q) P(X)/P(Q)[Note 1]	**Timer/Counter Outputs** provide the output of the corresponding timer/counter. The form of the output depends on the programmed mode. They are multiplexed as follows: TMROUT2 with ERROR#, TMROUT1 with P3.1 and INT8, and TMROUT0 with P3.0 and INT9.
TMS	I		**TAP (Test Access Port) Controller Mode Select** controls the sequence of the TAP controller's states. It has a permanent weak pull-up resistor.

NOTES:
1. X if clock source is internal; Q if clock source is external
2. Q if JTAG unit is shifting out data, Z if it is not

Table 4. Intel386™ EX Microprocessor Pin Descriptions (Sheet 6 of 6)

Symbol	Type	Output States	Name and Function
TRST#	ST		**TAP (Test Access Port) Controller Reset** resets the TAP controller at power-up and each time it is activated. It has a permanent weak pull-up resistor.
TXD1	O	H(Q) R(1) I(Q) P(X)/P(Q)[Note 1]	**Transmit Data SIO1 and SIO0** transmit serial data from the individual serial channels. TXD1 is multiplexed with DACK1#, and TXD0 is multiplexed with P2.6.
TXD0	O	H(Q) R(WL) I(Q) P(X)/P(Q)[Note 1]	**Transmit Data SIO1 and SIO0** transmit serial data from the individual serial channels. TXD1 is multiplexed with DACK1#, and TXD0 is multiplexed with P2.6.
UCS#	O	H(1) R(0) I(Q) P(X)	**Upper Chip-select** is activated when the address of a memory or I/O bus cycle is within the address region programmed by the user.
V_{CC}	P		**System Power** provides the nominal DC supply input. This pin is connected externally to a V_{CC} board plane.
V_{SS}	G		**System Ground** provides the 0 V connection from which all inputs and outputs are measured. This pin is connected externally to a ground board plane.
WDTOUT	O	H(Q) R(0) I(Q) P(X)	**Watchdog Timer Output** indicates that the watchdog timer has expired.
W/R#	O	H(Z) R(0) I(1) P(1)	**Write/Read** indicates whether the current bus cycle is a write cycle or a read cycle. When W/R# is HIGH, the bus cycle is a write cycle; when W/R# is LOW, the bus cycle is a read cycle.
WR#	O	H(1) R(1) I(1) P(1)	**Write Enable** indicates that the current bus cycle is a write cycle.

NOTES:
1. X if clock source is internal; Q if clock source is external
2. Q if JTAG unit is shifting out data, Z if it is not

4.0 Functional Description

The Intel386 EX microprocessor is a fully static, 32-bit processor optimized for embedded applications. It features low power and low voltage capabilities, integration of many commonly used DOS-type peripherals, and a 32-bit programming architecture compatible with the large software base of Intel386 processors. The following sections provide an overview of the integrated peripherals.

4.1 Clock Generation and Power Management Unit

The clock generation circuit includes a divide-by-two counter, a programmable divider for generating a prescaled clock (PSCLK), a divide-by-two counter for generating baud-rate clock inputs, and Reset circuitry. The CLK2 input provides the fundamental timing for the chip. It is divided by two internally to generate a 50% duty cycle Phase1 (PH1) and Phase 2 (PH2) for the core and integrated peripherals. For power management, separate clocks are routed to the core (PH1C/PH2C) and the peripheral modules (PH1P/PH2P). To help synchronize with external devices, the PH1P clock is provided on the CLKOUT output pin.

Two Power Management modes are provided for flexible power-saving options. During Idle mode, the clocks to the CPU core are frozen in a known state (PH1C low and PH2C high), while the clocks to the peripherals continue to toggle. In Powerdown mode, the clocks to both core and peripherals are frozen in a known state (PH1C low and PH2C high). The Bus Interface Unit will not honor any DMA, DRAM refresh, or HOLD requests in Powerdown mode because the clocks to the entire device are frozen.

4.2 Chip-select Unit

The Chip-Select Unit (CSU) decodes bus cycle address and status information and enables the appropriate chip-selects. The individual chip-selects become valid in the same bus state as the address and become inactive when either a new address is selected or the current bus cycle is complete.

The CSU is divided into eight separate chip-select regions, each of which can enable one of the eight chip-select pins. Each chip-select region can be mapped into memory or I/O space. A memory-mapped chip-select region can start on any $2^{(n+1)}$ Kbyte address location (where n = 0–15, depending upon the mask register). An I/O-mapped chip-select region can start on any $2^{(n+1)}$ byte address location (where n = 0–15, depending upon the mask register). The size of the region is also dependent upon the mask used.

4.3 Interrupt Control Unit

The Intel386 EX processor's Interrupt Control Unit (ICU) contains two 8259A modules connected in a cascade mode. These modules are similar to the industry-standard 8259A architecture.

The Interrupt Control Unit directly supports up to ten external (INT9:0) and up to eight internal interrupt request signals. Pending interrupt requests are posted in the Interrupt Request Registers, which contain one bit for each interrupt request signal. When an interrupt request is asserted, the corresponding Interrupt Request Register bit is set. The 8259A modules can be programmed to

recognize either an active-high level or a positive transition on the interrupt request lines. An internal Priority Resolver decides which pending interrupt request (if more than one exists) is the highest priority, based on the programmed operating mode. The Priority Resolver controls the single interrupt request line to the CPU. The Priority Resolver's default priority scheme places the master interrupt controller's IR0 as the highest priority and the master's IR7 as the lowest. The priority can be modified through software.

Besides the ten interrupt request inputs available to the Intel386 EX microprocessor, additional interrupts can be supported by cascaded external 8259A modules. Up to four external 8259A units can be cascaded to the master through connections to the INT3:0 pins. In this configuration, the interrupt acknowledge (INTA#) signal can be decoded externally using the ADS#, D/C#, W/R#, and M/IO# signals.

4.4 Timer/Counter Unit

The Timer/Counter Unit (TCU) on the Intel386 EX microprocessor has the same basic functionality as the industry-standard 82C54 counter/timer. The TCU provides three independent 16-bit counters, each capable of handling clock inputs up to 8 MHz. This maximum frequency must be considered when programming the input clocks for the counters. Six programmable timer modes allow the counters to be used as event counters, elapsed-time indicators, programmable one-shots, and in many other applications. All modes are software programmable.

4.5 Watchdog Timer Unit

The Watchdog Timer (WDT) unit consists of a 32-bit down-counter that decrements every PH1P cycle, allowing up to 4.3 billion count intervals. The WDTOUT pin is driven high for sixteen CLK2 cycles when the down-counter reaches zero (the WDT times out). The WDTOUT signal can be used to reset the chip, to request an interrupt, or to indicate to the user that a ready-hang situation has occurred. The down-counter can also be updated with a user-defined 32-bit reload value under certain conditions. Alternatively, the WDT unit can be used as a bus monitor or as a general-purpose timer.

4.6 Asynchronous Serial I/O Unit

The Intel386 EX microprocessor's asynchronous Serial I/O (SIO) unit is a Universal Asynchronous Receiver/ Transmitter (UART). Functionally, it is equivalent to the National Semiconductor NS16450 and INS8250. The Intel386 EX embedded processor contains two full-duplex, asynchronous serial channels.

The SIO unit converts serial data characters received from a peripheral device or modem to parallel data and converts parallel data characters received from the CPU to serial data. The CPU can read the status of the serial port at any time during its operation. The status information includes the type and condition of the transfer operations being performed and any errors (parity, framing, overrun, or break interrupt).

Each asynchronous serial channel includes full modem control support (CTS#, RTS#, DSR#, DTR#, RI#, and DCD#) and is completely programmable. The programmable options include character length (5, 6, 7, or 8 bits), stop bits (1, 1.5, or 2), and parity (even, odd, forced, or none). In addition, it contains a programmable baud-rate generator capable of clock rates from 0 to 512 Kbaud.

4.7 Synchronous Serial I/O Unit

The Synchronous Serial I/O (SSIO) unit provides for simultaneous, bidirectional communications. It consists of a transmit channel, a receive channel, and a dedicated baud-rate generator. The transmit and receive channels can be operated independently (with different clocks) to provide non-lockstep, full-duplex communications; either channel can originate the clocking signal (Master Mode) or receive an externally generated clocking signal (Slave Mode).

The SSIO provides numerous features for ease and flexibility of operation. With a maximum clock input of CLK2/4 to the baud-rate generator, the SSIO can deliver a baud rate of up to 8.25 Mbits per second with a processor clock of 33 MHz. Each channel is double buffered. The two channels share the baud-rate generator and a multiply-by-two transmit and receive clock. The SSIO supports 16-bit serial communications with independently enabled transmit and receive functions and gated interrupt outputs to the interrupt controller.

4.8 Parallel I/O Unit

The Intel386 EX microprocessor has three 8-bit, general-purpose I/O ports. All port pins are bidirectional, with TTL-level inputs and CMOS-level outputs. All pins have both a standard operating mode and a peripheral mode (a multiplexed function), and all have similar sets of control registers located in I/O address space.

4.9 DMA and Bus Arbiter Unit

The Intel386 EX microprocessor's DMA controller is a two-channel DMA; each channel operates independently of the other. Within the operation of the individual channels, several different data transfer modes are available. These modes can be combined in various configurations to provide a very versatile DMA controller. Its feature set has enhancements beyond the 8237 DMA family; however, it can be configured such that it can be used in an 8237-like mode. Each channel can transfer data between any combination of memory and I/O with any combination (8 or 16 bits) of data path widths. An internal temporary register that can disassemble or assemble data to or from either an aligned or a nonaligned destination or source optimizes bus bandwidth.

The bus arbiter, a part of the DMA controller, works much like the priority resolving circuitry of a DMA. It receives service requests from the two DMA channels, the external bus master, and the DRAM Refresh Control Unit. The bus arbiter requests bus ownership from the core and resolves priority issues among all active requests when bus mastership is granted.

Each DMA channel consists of three major components: the Requestor, the Target, and the Byte Count. These components are identified by the contents of programmable registers that define the memory or I/O device being serviced by the DMA. The Requestor is the device that requires and requests service from the DMA controller. Only the Requestor is considered capable of initializing

or terminating a DMA process. The Target is the device with which the Requestor wishes to communicate. The DMA process considers the Target a slave that is incapable of controlling the process. The Byte Count dictates the amount of data that must be transferred.

4.10 Refresh Control Unit

The Refresh Control Unit (RCU) simplifies dynamic memory controller design with its integrated address and clock counters. Integrating the RCU into the processor allows an external DRAM controller to use chip-selects, wait state logic, and status lines.

The Refresh Control Unit:

- Provides a programmable-interval timer
- Provides the bus arbitration logic to gain control of the bus to run refresh cycles
- Contains the logic to generate row addresses to refresh DRAM rows individually
- Contains the logic to signal the start of a refresh cycle

The RCU contains a 13-bit address counter that forms the refresh address, supporting DRAMs with up to 13 rows of memory cells (13 refresh address bits). This includes all practical DRAM sizes for the Intel386 EX microprocessor's 64 Mbyte address space.

4.11 JTAG Test-logic Unit

The JTAG Test-logic Unit provides access to the device pins and to a number of other testable areas on the device. It is fully compliant with the IEEE 1149.1 standard and thus interfaces with five dedicated pins: TRST#, TCK, TMS, TDI, and TDO. It contains the Test Access Port (TAP) finite-state machine, a 4-bit instruction register, a 32-bit identification register, and a single-bit bypass register. The test-logic unit also contains the necessary logic to generate clock and control signals for the Boundary Scan chain.

Since the test-logic unit has its own clock and reset signals, it can operate autonomously. While the rest of the microprocessor is in Reset or Powerdown, the JTAG unit can read or write various register chains.

5.0 Design Considerations

This section describes the Intel386 EX microprocessor's instruction set and its component and revision identifiers.

5.1 Instruction Set

The Intel386 EX microprocessor uses the same instruction set as the Intel386 SX microprocessor with the following exceptions.

The Intel386 EX microprocessor has one new instruction (RSM). This Resume instruction causes the processor to exit System Management Mode (SMM). RSM requires 338 clocks per instruction (CPI).

The Intel386 EX microprocessor requires more clock cycles than the Intel386 SX microprocessor to execute some instructions. Table 5 lists these instructions and the Intel386 EX microprocessor clock count. For the equivalent Intel386 SX microprocessor clock count, refer to the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* datasheet (order number 240187).

Table 5. Microprocessor Clocks Per Instruction

Instruction	Clock Count (1)		
	Virtual 8086 Mode(2)	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode(3)
POPA		29	35
IN: Fixed Port Variable Port	 27 28	 14 15	 8/29 9/29
OUT: Fixed Port Variable Port	 27 28	 14 15	 8/29 9/29
INS	30	17	10/32
OUTS	31	18	11/33
REP INS	31+6*n* (Note 4)	17+7*n* (Note 4)	11+7*n*/32+6*n* (Note 4)
REP OUTS	30+8*n* (Note 4)	16+8*n* (Note 4)	10+8*n*/31+8*n* (Note 4)
HLT		7	7
MOV CR0, reg		10	10

NOTES:
1. For IN, OUT, INS, OUTS, REP INS, and REP OUTS instructions, add one clock count for each wait state generated by the peripheral being accessed (the values in the table are for zero wait state).
2. The clock count values in this column apply if I/O permission allows I/O to the port in virtual 8086 mode. If the I/O bit map denies permission, exception fault 13 occurs; see clock counts for the INT 3 instruction in the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* datasheet (order number 240187).
3. When two clock counts are listed, the smaller value refers to the case where CPL ≤ IOPL and the larger value refers to the case where CPL>IOPL. CPL is the current privilege level, and IOPL is the I/O privilege level.
4. *n* = the number of times repeated.

5.2 Component and Revision Identifiers

To assist users, the microprocessor holds a component identifier and revision identifier in its DX register after reset. The upper 8 bits of DX hold the component identifier, 23H. (The lower nibble, 3H, identifies the Intel386 architecture, while the upper nibble, 2H, identifies the second member of the Intel386 microprocessor family.)

The lower 8 bits of DX hold the revision level identifier. The revision identifier will, in general, chronologically track those component steppings that are intended to have certain improvements or distinction from previous steppings. The revision identifier will track that of the Intel386 CPU whenever possible. However, the revision identifier value is not guaranteed to change with every stepping revision or to follow a completely uniform numerical sequence, depending on the type or intent of the revision or the manufacturing materials required to be changed. Intel has sole discretion over these characteristics of the component. The initial revision identifier for the Intel386 EX microprocessor is 09H.

5.3 Package Thermal Specifications

The Intel386 EX microprocessor is specified for operation with a minimum case temperature ($T_{CASE(MIN)}$) of -40° C and a maximum case temperature ($T_{CASE(MAX)}$) dependent on power dissipation (see Figures 4 through 7). The case temperature can be measured in any environment to determine whether the microprocessor is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

An increase in the ambient temperature (T_A) causes a proportional increase in the case temperature (T_{CASE}) and the junction temperature (T_J), which is the junction temperature on the die itself. A packaged device produces thermal resistance between junction and case temperatures (θ_{JC}) and between junction and ambient temperatures (θ_{JA}). The relationships between the temperature and thermal resistance parameters are expressed by these equations:

$T_J = T_{CASE} + P \times \theta_{JC}$

$T_A = T_J - P \times \theta_{JA}$

$T_{CASE} = T_A + P \times [\theta_{JA} - \theta_{JC}]$

P = power dissipated as heat = $V_{CC} \times I_{CC}$

A safe operating temperature can be calculated from the above equations by using the maximum safe T_J of 120° C, the power drawn by the chip in the specific design, and the θ_{JC} value from Table 6. The θ_{JA} value depends on the airflow (measured at the top of the chip) provided by the system ventilation, board layout, board thickness, and potentially other factors in the design of the application. The θ_{JA} values are given for reference only and are not guaranteed.

Table 6. Thermal Resistances (0 °C/W) θ_{JA}, θ_{JC}

Package	θ_{JC}	θ_{JA} vs. Airflow (ft/min)		
		0	100	200
132 PQFP	7	28	24	22
144 TQFP	4	36	31	27

Figures 4 through 7 provide maximum case temperature as a function of frequency.

Figure 4. Maximum Case Temperature vs. Frequency for Typical Power Values (132-lead PQFP, V_{CC} = 5.5 V)

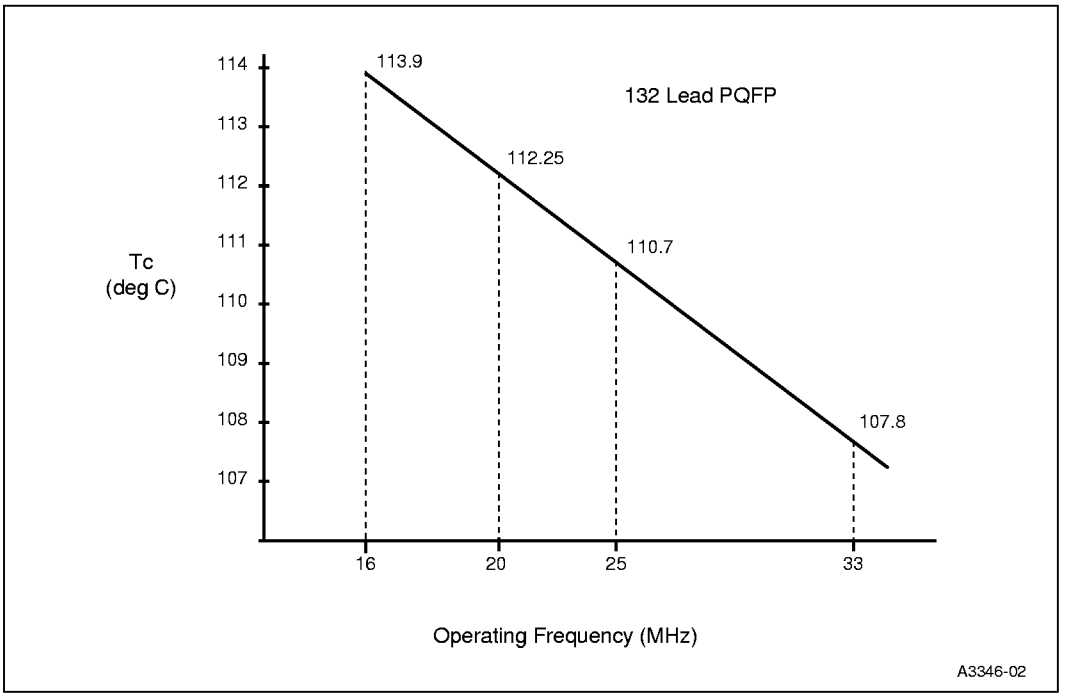


Figure 5. Maximum Case Temperature vs. Frequency for Typical Power Values (144-lead TQFP, V_{CC} = 5.5 V nominal)

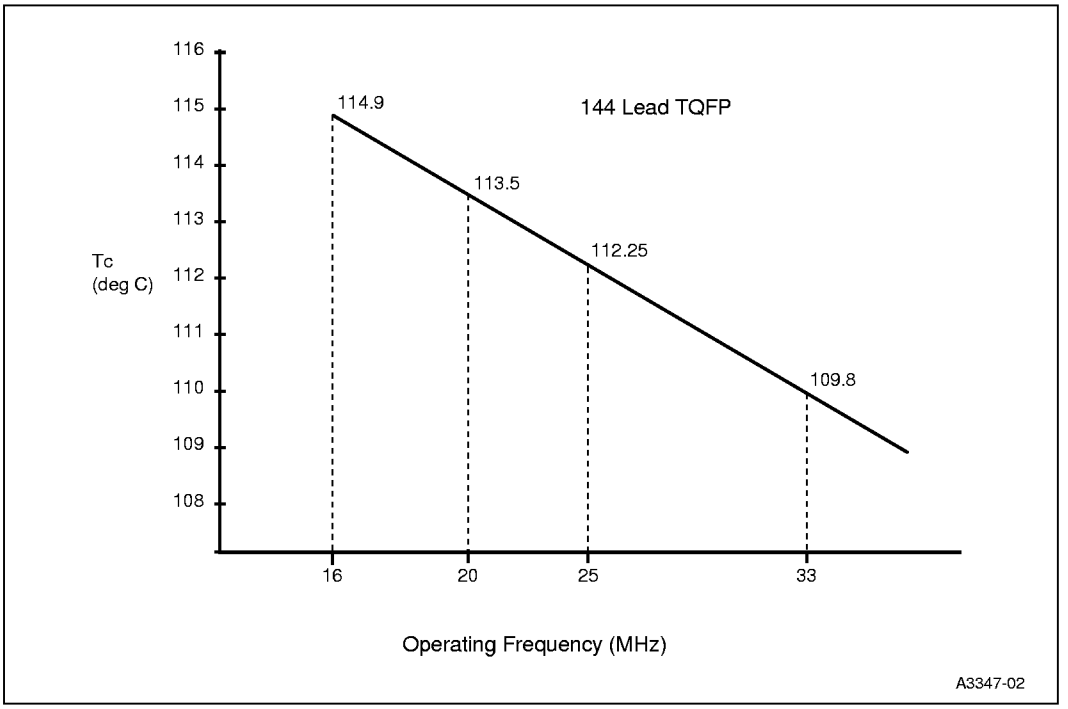


Figure 6. Maximum Case Temperature vs. Frequency for Typical Power Values (132-lead PQFP, V_{CC} = 3.6 V)

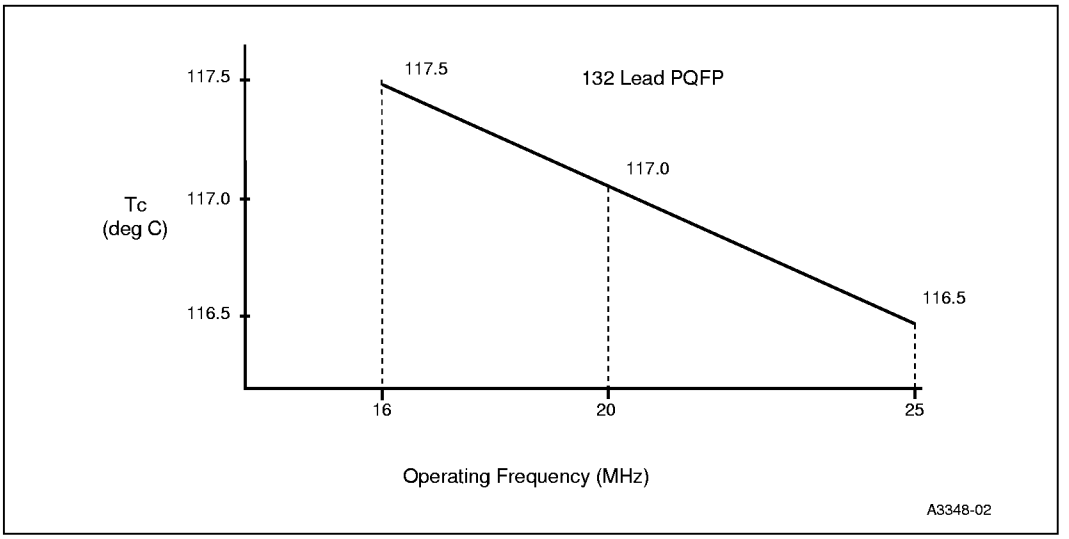
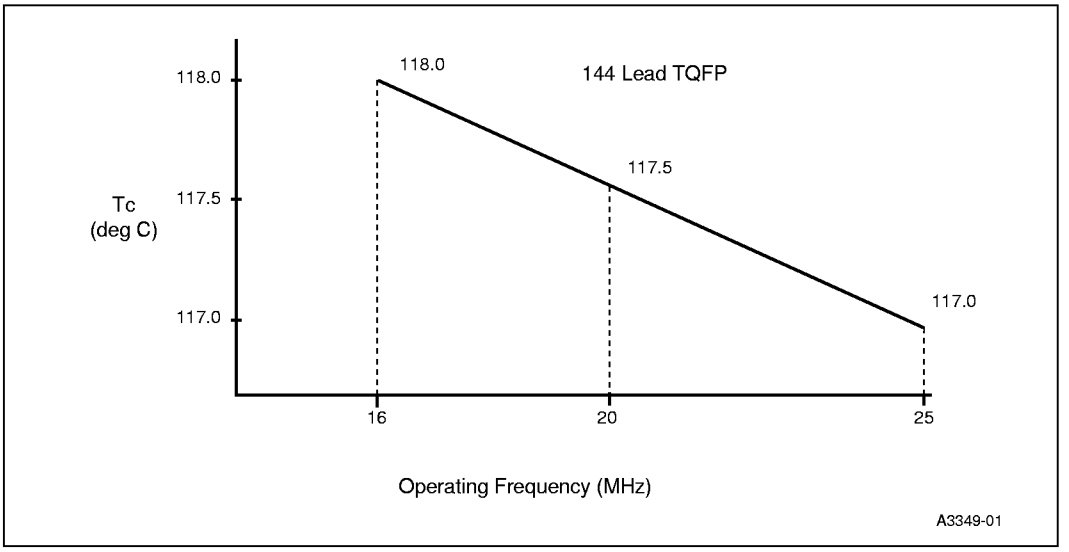


Figure 7. Maximum Case Temperature vs. Frequency for Typical Power Values (144-lead TQFP, V_{CC} = 3.6 V)



6.0 Electrical Specifications

6.1 Maximum Ratings

Warning: Stressing the device beyond the "Maximum Ratings" may cause permanent damage. These are stress ratings only.

Table 7. 5 V Intel386 EXTC Processor Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Supply Voltage with Respect to V_{SS}	–0.5 V to 6.5 V
Voltage on Other Pins	–0.5 V to V_{CC} + 0.5 V
V_{CC} (Digital Supply Voltage)	4.5 V to 5.5 V
T_{CASE} (Case Temperature Under Bias) $T_{CASE(MIN)}$ $T_{CASE(MAX)}$	 -40°C (see Figures 4 and 5)
F_{OSC} (Operating Frequency)	0 MHz to 33 MHz

Table 8. 3 V Intel386 EXTB Processor Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Supply Voltage with Respect to V_{SS}	–0.5 V to 4.6 V
Voltage on Other Pins	–0.5 V to V_{CC} + 0.5 V
V_{CC} (Digital Supply Voltage)	20 MHz — 2.7 V to 3.6 V 25 MHz — 3.0 V to 3.6 V
T_{CASE} (Case Temperature Under Bias) $T_{CASE(MIN)}$ $T_{CASE(MAX)}$	 -40°C (see Figures 6 and 7)
F_{OSC} (Operating Frequency)	0 MHz to 25 MHz

6.2 DC Specifications

Table 9. 5-Volt DC Characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{IL}	Input Low Voltage for all input pins except CLK2, TRST#, RESET, SMI#, and NMI	–0.3	0.8	V	
V_{IH}	Input High Voltage for all input pins except CLK2, TRST#, RESET, SMI#, and NMI	2.0	V_{CC} + 0.3	V	
V_{ILC}	Input Low Voltage for CLK2, TRST#, RESET, SMI#, and NMI	-0.3	0.8	V	
V_{IHC}	Input High Voltage for CLK2, TRST#, RESET, SMI#, and NMI	V_{CC}-0.8	V_{CC}+0.3	V	
V_{OL}	Output Low Voltage All pins except Port 3 Port 3		 0.45 0.45	 V V	 I_{OL} = 8 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage All output pins All pins except Port 3 Port 3 pins (2 max)	 V_{CC}-0.5 2.45 2.45		 V V V	 I_{OH} = –0.2 mA I_{OH} = –8 mA I_{OH} = –16 mA
V_{OLC}	CLKOUT		0.45	V	I_{OL} = 2 mA
V_{OHC}	CLKOUT	V_{CC}-0.5 2.45		V	I_{OH} = –0.2 mA I_{OH} = –2 mA
I_{LI}	Input Leakage Current		±15	µA	$0 \le V_{IN} \le V_{CC}$ FLT# is not tested for I_{LI}
I_{LO}	Output Leakage Current		±15	µA	$0.45V \le V_{OUT} \le V_{CC}$
I_{CC}	Supply Current		320 250	mA mA	F_{OSC} =33 MHz F_{OSC} =25 MHz (tested with device held in reset, inputs held in their inactive state)
I_{IDLE}	Idle Mode Current		110 85	mA mA	F_{OSC} =33 MHz F_{OSC} =25 MHz
I_{PD}	Powerdown Current		100	µA	
C_S	Pin Capacitance (any pin to V_{SS})		10	pF	Not tested

Table 10. 3-Volt DC Characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{IL}	Input Low Voltage for all input pins except CLK2, TRST#, RESET, SMI#, and NMI	–0.3	0.8	V	
V_{IH}	Input High Voltage for all input pins except CLK2, TRST#, RESET, SMI#, and NMI	2.0	V_{CC} + 0.3	V	
V_{ILC}	Input Low Voltage for CLK2, TRST#, RESET, SMI#, and NMI	-0.3	0.8	V	
V_{IHC}	Input High Voltage for CLK2, TRST#, RESET, SMI#, and NMI	V_{CC}-0.6	V_{CC}+0.3	V	
V_{OL}	Output Low Voltage All pins except Port 3 Port 3 pins (2 max)		0.20 0.45 0.45	V V V	I_{OL} = 100 µA, 2.7 V ≤ V_{CC} ≤ 3.6 V (LVCMOS) I_{OL} = 4mA, 3.0 V≤V_{CC}≤3.6 V (LVTTL) I_{OL} = 8mA, 3.0 V≤V_{CC}≤3.6 V (LVTTL)
V_{OH}	Output High Voltage All pins except Port 3 Port 3	V_{CC}-0.2 V_{CC}-0.65 V_{CC}-0.65		V V V	I_{OH}= -100 µA, 2.7 V≤V_{CC}≤3.6 V (LVCMOS) I_{OH}= -4mA, 3.0 V≤V_{CC}≤3.6V (LVTTL) I_{OH}= -8mA, 3.0 V≤V_{CC}≤3.6V (LVTTL)
V_{OLC}	CLKOUT		0.2 0.45	V	I_{OL} = 100 µA, 2.7 V ≤ V_{CC} ≤ 3.6 V I_{OL} = 1 mA, 3.0 V ≤ V_{CC} ≤ 3.6 V (LVTTL)
V_{OHC}	CLKOUT	V_{CC}-0.2 V_{CC}-0.65		V	I_{OH} = -100 µA, 2.7 V ≤ V_{CC} ≤ 3.6 V I_{OH} = -1 mA, 3.0 V ≤ V_{CC} ≤ 3.6 V (LVTTL)
I_{LI}	Input Leakage Current		±5	µA	0 ≤ V_{IN} ≤ V_{CC} FLT# is not tested for I_{LI}
I_{LO}	Output Leakage Current		±15	µA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	Supply Current		140 110	mA mA	F_{OSC} = 25 MHz, V_{CC}=3.6 V F_{OSC} = 20 MHz, V_{CC}=3.6 V (tested with device held in reset, inputs held in their inactive state)
I_{IDLE}	Idle Mode Current		50 40	mA mA	F_{OSC} = 25 MHz, V_{CC}=3.6 V F_{OSC} = 20 MHz, V_{CC}=3.6 V
I_{PD}	Powerdown Current		100	µA	
C_S	Pin Capacitance (any pin to V_{SS})		10	pF	Not tested

6.3 AC Specifications

Table 11 lists output delays, input setup requirements, and input hold requirements for the 5 V EXTC processor; Table 12 is for the EXTB processor. All AC specifications are relative to the CLK2 rising edge crossing the $V_{CC}/2$ level for the EXTB, or 2.0 Volts for the EXTC.

Figures 8 and 9 show the measurement points for AC specifications for the EXTB and EXTC processors. Inputs must be driven to the indicated voltage levels when AC specifications are measured. Output delays are specified with minimum and maximum limits measured as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs ADS#, W/R#, CS5:0#, UCS#, D/C#, M/IO#, LOCK#, BHE#, BLE#, REFRESH#/CS6#, READY#, LBA#, A25:1, HLDA and SMIACT# change only at the beginning of phase one. D15:0 (write cycles) and PWRDOWN change only at the beginning of phase two. RD# and WR# change to their active states at the beginning of phase two. RD# changes to its inactive state (end of cycle) at the beginning of phase one. See the *Intel386™ EX Embedded Microprocessor User's Manual* for a detailed explanation of early READY# vs. late READY#.

The READY#, HOLD, BUSY#, ERROR#, PEREQ, BS8#, and D15:0 (read cycles) inputs are sampled at the beginning of phase one. The NA#, SMI#, and NMI inputs are sampled at the beginning of phase two.

Figure 8. Drive Levels and Measurement Points for AC Specifications (EXTC)

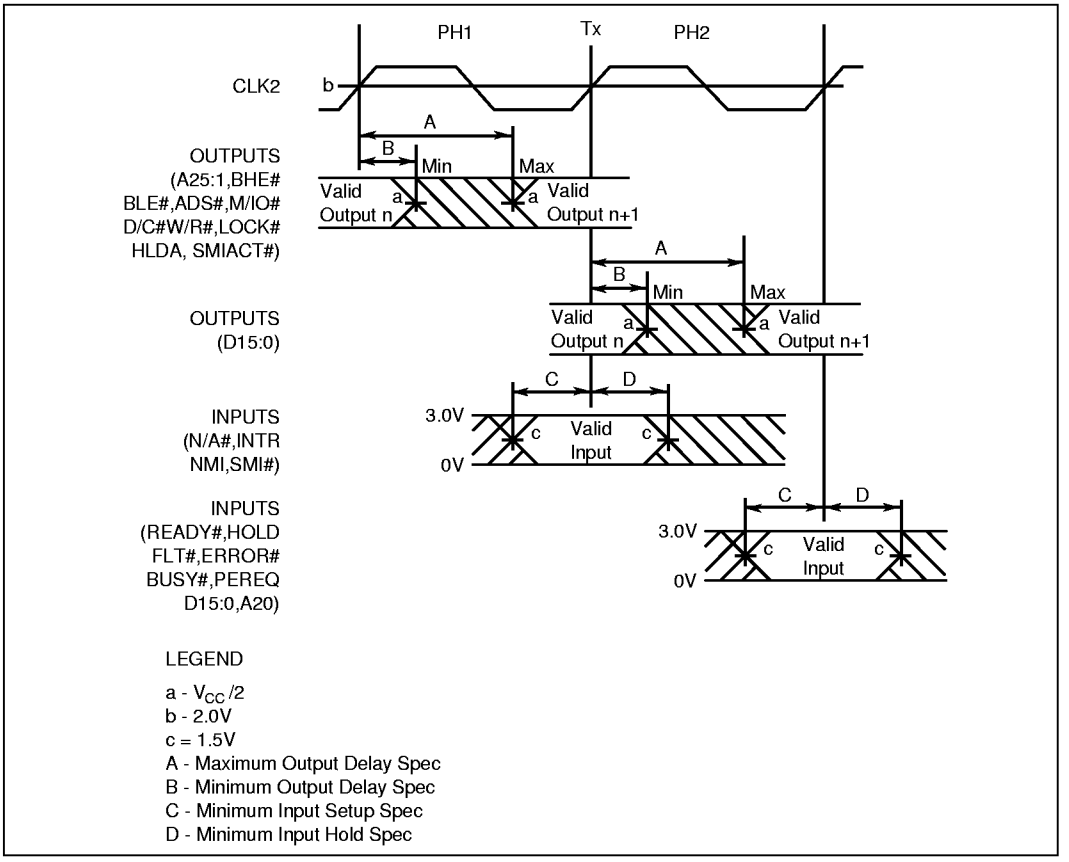


Figure 9. Drive Levels and Measurement Points for AC Specifications (EXTB)

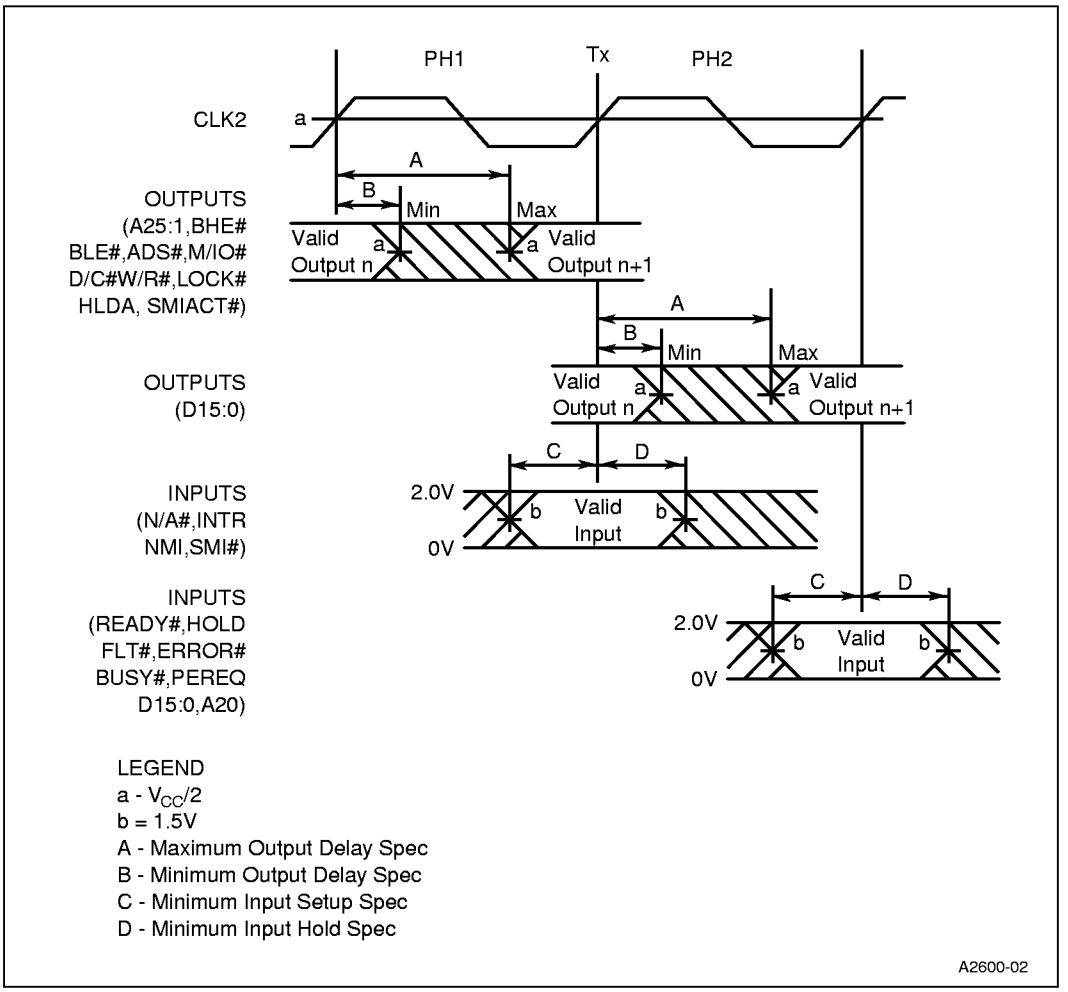


Table 11. 5-Volt AC Characteristics (Sheet 1 of 5)

Symbol	Parameter	33 MHz		25 MHz		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
	Operating Frequency	0	33	0	25	one-half CLK2 frequency in MHz (1)
t_1	CLK2 Period	15		20		
t_{2a}	CLK2 High Time	6.25		7		(2)
t_{2b}	CLK2 High Time	4		4		(2)
t_{3a}	CLK2 Low Time	6.25		7		(2)
t_{3b}	CLK2 Low Time	4.5		5		(2)
t_4	CLK2 Fall Time		4		7	(2)
t_5	CLK2 Rise Time		4		7	(2)
t_6	A25:1 Valid Delay	4	21	4	24	C_L = 50 pF
t_7	A25:1 Float Delay	4	28	4	28	(3)
t_8	BHE#, BLE#, LOCK# Valid Delay	4	21	4	24	C_L = 50 pF
t_{8a}	SMIACT# Valid Delay	4	21	4	24	C_L = 50 pF
t_9	BHE#, BLE#, LOCK# Float Delay	4	28	4	28	(3)
t_{10}	M/IO#, D/C#, W/R#, ADS#, REFRESH# Valid Delay	4	21	4	24	C_L = 50 pF
t_{10a}	RD#, WR# Valid Delay	4	18	4	22	
t_{10b}	WR# Valid Delay for the rising edge with respect to phase two (external late READY#)	4	28	4	28	(6)
t_{11}	M/IO#, D/C#, W/R#, REFRESH#, ADS# Float Delay	4	28	4	28	(3)
t_{12}	D15:0 Write Data Valid Delay	4	23	4	23	C_L = 50 pF
t_{13}	D15:0 Write Data Float delay	4	22	4	22	(3)
t_{14}	HLDA Valid Delay	4	18	4	22	C_L = 50 pF
t_{15}	NA# Setup Time	5		5		
t_{16}	NA# Hold Time	3		3		
t_{19}	READY# Setup Time	8		9		
t_{19a}	BS8# Setup Time	11		11		

NOTE:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 11. 5-Volt AC Characteristics (Sheet 2 of 5)

Symbol	Parameter	33 MHz		25 MHz		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t_{20}	READY#, BS8# Hold Time	4		4		
t_{21}	D15:0 Read Setup Time	7		7		
t_{22}	D15:0 Read Hold Time	4		4		
t_{23}	HOLD Setup Time	8		8		
t_{24}	HOLD Hold Time	3		3		
t_{25}	RESET Setup Time	5		5		
t_{26}	RESET Hold Time	2		3		
t_{27}	NMI Setup Time	6		6		(4)
t_{27a}	SMI# Setup Time	6		6		(4)
t_{28}	NMI Hold Time	6		6		(4)
t_{28a}	SMI# Hold Time	6		6		(4)
t_{29}	PEREQ, ERROR#, BUSY# Setup Time	6		6		(4)
t_{30}	PEREQ, ERROR#, BUSY# Hold Time	5		5		(4)
t_{31}	READY# Valid Delay	4	24	4	26	C_L = 30 pF
t_{32}	READY# Float Delay	4	34	4	34	
t_{33}	LBA# Valid Delay	4	20	4	22	
t_{34}	CS6:0#, UCS# Valid Delay	4	24 (25 in SMM)	4	30	C_L = 30 pF
t_{35}	CLKOUT Valid Delay	2	9	2	14	C_L = 30 pF
t_{36}	PWRDOWN Valid Delay	4	15	4	18	
t_{41}	A25:1, BHE#, BLE# Valid to WR# Low	0		0		
t_{41a}	UCS#, CS6:0# Valid to WR# Low	0		0		
t_{42}	A25:1, BHE#, BLE# Hold After WR# High	0		0		(6)
t_{42a}	UCS#, CS6:0# Hold after WR# High	0		0		
t_{42b}	A25:1. BHE#, BLE# Hold After WR# High	10		10		(7, 8)

NOTE:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 11. 5-Volt AC Characteristics (Sheet 3 of 5)

Symbol	Parameter	33 MHz		25 MHz		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t_{43}	D15:0 Output Valid to WR# High	2CLK2 –10		2CLK2 – 10		(5)
t_{44}	D15:0 Output Hold After WR# High	CLK2 –10		CLK2 –10		
t_{45}	WR# High to D15:0 Float		CLK2 + 10		CLK2 + 10	(3)
t_{46}	WR# Pulse Width	2CLK2 –10		2CLK2 –10		(7)
t_{47}	A25:1, BHE#, BLE# Valid to D15:0 Valid		4CLK2 - 28		4CLK2- 31	(5)
t_{47a}	UCS#, CS6:0# Valid to D15-D0 Valid		4CLK2 - 31		4CLK2 - 35	(5)
t_{48}	RD# Low to D15:0 Input Valid		3CLK2 – 25		3CLK2 – 29	(5)
t_{49}	D15:0 Hold After RD# High	0		0		
t_{50}	RD# High to D15:0 Float		CLK2		CLK2	(3)
t_{51}	A25:1, BHE#, BLE# Hold After RD# High	0		0		
t_{51a}	UCS#, CS6:0# Hold after RD# High	0		0		
t_{52}	RD# Pulse Width	3CLK2 –10		3CLK2 –10		
Synchronous Serial I/O (SSIO) Unit						
t_{100}	STXCLK, SRXCLK Frequency (Master Mode)		CLK2/8		CLK2/8	(Unit is MHz)
t_{101}	STXCLK, SRXCLK Frequency (Slave Mode)		CLK2/8		CLK2/8	(Unit is MHz)
t_{102}	STXCLK, SRXCLK Low Time	7CLK2/2		7CLK2/2		(2)
t_{103}	STXCLK, SRXCLK High Time	7CLK2/2		7CLK2/2		(2)
t_{104}	STXCLK Low to SSIOTX Delay		3CLK2		3CLK2	
t_{105}	SSIORX to SRXCLK High Setup Time	0		0		(2)
t_{106}	SSIORX from SRXCLK Hold Time	3CLK2		3CLK2		

NOTE:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 11. 5-Volt AC Characteristics (Sheet 4 of 5)

Symbol	Parameter	33 MHz		25 MHz		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
Timer Control Unit (TCU) Inputs						
t_{107}	TMRCLK*n* Frequency		8		8	(Unit is MHz)
t_{108}	TMRCLK*n* Low	60		60		
t_{109}	TMRCLK*n* High	60		60		
t_{110}	TMRGATE*n* High Width	50		50		
t_{111}	TMRGATE*n* Low Width	50		50		
t_{112}	TMRGATE*n* to TMRCLK Setup Time (external TMRCLK only)	10		10		
t_{112a}	TMRGATE*n* to TMRCLK Hold Time (external TMRCLK only)	11		11		
Timer Control Unit (TCU) Outputs						
t_{113}	TMRGATE*n* Low to TMROUT Valid		29		32	
t_{114}	TMRCLK*n* Low to TMROUT Valid		29		32	
Interrupt Control Unit (ICU) Inputs						
t_{115}	D7:0 Setup Time (INTA# Cycle 2)	7		7		
t_{116}	D7:0 Hold Time (INTA# Cycle 2)	4		4		
Interrupt Control Unit (ICU) Outputs						
t_{117}	CLK2 High to CAS2:0 Valid		25		28	
DMA Unit Inputs						
t_{118}	DREQ Setup Time (Sync Mode)	15		15		
t_{119}	DREQ Hold Time (Sync Mode)	4		4		(2)
t_{120}	DREQ Setup Time (Async Mode)	9		9		
t_{121}	DREQ Hold Time (Async Mode)	9		9		(2)

NOTE:
1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 11. 5-Volt AC Characteristics (Sheet 5 of 5)

Symbol	Parameter	33 MHz		25 MHz		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t_{122}	EOP# Setup Time (Sync Mode)	15		15		
t_{123}	EOP# Hold Time (Sync Mode)	4		4		
t_{124}	EOP# Setup Time (Async Mode)	9		9		
t_{125}	EOP# Hold Time (Async Mode)	9		9		
DMA Unit Outputs						
t_{126}	DACK# Output Valid Delay	4	21	4	25	
t_{127}	EOP# Active Delay	4	25	4	25	
t_{128}	EOP# Float Delay	4	25	4	25	(3)
JTAG Test-logic Unit						
t_{129}	TCK Frequency		10		10	(Unit is MHz)

NOTE:
1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 12. 3-Volt AC Characteristics (Sheet 1 of 5)

Symbol	Parameter	25 MHz 3.0 V to 3.6 V		20 MHz 2.7 V to 3.6 V		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
	Operating Frequency	0	25	0	20	one-half CLK2 frequency in MHz(1)
t_1	CLK2 Period	20		25		
t_{2a}	CLK2 High Time	7		8		(2)
t_{2b}	CLK2 High Time	4		5		(2)
t_{3a}	CLK2 Low Time	7		8		(2)
t_{3b}	CLK2 Low Time	5		6		(2)
t_4	CLK2 Fall Time		7		8	(2)
t_5	CLK2 Rise Time		7		8	(2)
t_6	A25:1 Valid Delay	4	32	4	36	C_L = 50 pF
t_7	A25:1 Float Delay	4	29	4	36	(3)
t_8	BHE#, BLE#, LOCK# Valid Delay	4	32	4	34	C_L = 50 pF
t_{8a}	SMIACT# Valid Delay	4	32	4	34	C_L = 50 pF
t_9	BHE#, BLE#, LOCK# Float Delay	4	23	4	32	(3)
t_{10}	M/IO#, D/C#, W/R#, ADS#, REFRESH# Valid Delay	4	32	4	34	C_L = 50 pF
t_{10a}	RD#, WR# Valid Delay	4	30	4	32	
t_{10b}	WR# Valid Delay for the rising edge with respect to phase two (external late READY#)	4	37	4	37	(6)
t_{11}	M/IO#, D/C#, W/R#, REFRESH#, ADS# Float Delay	4	30	4	34	(3)
t_{12}	D15:0 Write Data Valid Delay	4	31	4	34	C_L = 50 pF
t_{13}	D15:0 Write Data Float delay	4	20	4	28	(3)
t_{14}	HLDA Valid Delay	4	30	4	32	C_L = 50 pF
t_{15}	NA# Setup Time	9		9		
t_{16}	NA# Hold Time	12		15		

NOTE:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 12. 3-Volt AC Characteristics (Sheet 2 of 5)

Symbol	Parameter	25 MHz 3.0 V to 3.6 V		20 MHz 2.7 V to 3.6 V		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t_{19}	READY# Setup Time	15		17		
t_{19a}	BS8# Setup Time	17		19		
t_{20}	READY#, BS8# Hold Time	4		4		
t_{21}	D15:0 Read Setup Time	9		11		
t_{22}	D15:0 Read Hold Time	6		6		
t_{23}	HOLD Setup Time	17		22		
t_{24}	HOLD Hold Time	5		5		
t_{25}	RESET Setup Time	12		13		
t_{26}	RESET Hold Time	4		4		
t_{27}	NMI Setup Time	16		16		(4)
t_{27a}	SMI# Setup Time	16		16		(4)
t_{28}	NMI Hold Time	16		16		(4)
t_{28a}	SMI# Hold Time	16		16		(4)
t_{29}	PEREQ, ERROR#, BUSY# Setup Time	14		16		(4)
t_{30}	PEREQ, ERROR#, BUSY# Hold Time	5		5		(4)
t_{31}	READY# Valid Delay	4	33	4	42	C_L = 30 pF
t_{32}	READY# Float Delay	4	33	4	42	
t_{33}	LBA# Valid Delay	4	31	4	40	
t_{34}	CS6:0#, UCS# Valid Delay	4	33 (34 in SMM)	4	42	C_L = 30 pF
t_{35}	CLKOUT Valid Delay	4	14	4	18	C_L = 30 pF
t_{36}	PWRDOWN Valid Delay	4	26	4	29	
t_{41}	A25:1, BHE#, BLE# Valid to WR# Low	0		0		
t_{41a}	UCS#, CS6:0# Valid to WR# Low	0		0		
t_{42}	A25:1, BHE#, BLE# Hold After WR# High	0		0		(6)

NOTE:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 12. 3-Volt AC Characteristics (Sheet 3 of 5)

Symbol	Parameter	25 MHz 3.0 V to 3.6 V		20 MHz 2.7 V to 3.6 V		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t_{42a}	UCS#, CS6:0# Hold after WR# High	0		0		
t_{42b}	A25:1. BHE#, BLE# Hold After WR# High	10		10		(7, 8)
t_{43}	D15:0 Output Valid to WR# High	2CLK2 – 10		2CLK2 – 10		(5)
t_{44}	D15:0 Output Hold After WR# High	CLK2 –10		CLK2 –10		
t_{45}	WR# High to D15:0 Float		CLK2 + 10		CLK2 +10	(3)
t_{46}	WR# Pulse Width	2CLK2 –10		2CLK2 –10		(7)
t_{47}	A25:1, BHE#, BLE# Valid to D15:0 Valid		4CLK2-41		4CLK2 - 45	(5)
t_{47a}	UCS#, CS6:0# Valid to D15-D0 Valid		4CLK2 - 42		4CLK2 - 53	(5)
t_{48}	RD# Low to D15:0 Input Valid		3CLK2 – 39		3CLK2 – 43	(5)
t_{49}	D15:0 Hold After RD# High	0		0		
t_{50}	RD# High to D15:0 Float		CLK2		CLK2	(3)
t_{51}	A25:1, BHE#, BLE# Hold After RD# High	0		0		
t_{51a}	UCS#, CS6:0# Hold after RD# High	0		0		
t_{52}	RD# Pulse Width	3CLK2 –13		3CLK2 –15		
Synchronous Serial I/O (SSIO) Unit						
t_{100}	STXCLK, SRXCLK Frequency (Master Mode)		CLK2/8		CLK2/8	(Unit is MHz)
t_{101}	STXCLK, SRXCLK Frequency (Slave Mode)		CLK2/8		CLK2/8	(Unit is MHz)
t_{102}	STXCLK, SRXCLK Low Time	7CLK2/2		7CLK2/2		(2)

NOTE:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 12. 3-Volt AC Characteristics (Sheet 4 of 5)

Symbol	Parameter	25 MHz 3.0 V to 3.6 V		20 MHz 2.7 V to 3.6 V		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t_{103}	STXCLK, SRXCLK High Time	7CLK2/ 2		7CLK2/ 2		(2)
t_{104}	STXCLK Low to SSIOTX Delay		3CLK2		3CLK2	
t_{105}	SSIORX to SRXCLK High Setup Time	0		0		(2)
t_{106}	SSIORX from SRXCLK Hold Time	3CLK2		3CLK2		
Timer Control Unit (TCU) Inputs						
t_{107}	TMRCLK*n* Frequency		8		8	(Unit is MHz)
t_{108}	TMRCLK*n* Low	60		60		
t_{109}	TMRCLK*n* High	60		60		
t_{110}	TMRGATE*n* High Width	50		50		
t_{111}	TMRGATE*n* Low Width	50		50		
t_{112}	TMRGATE*n* to TMRCLK Setup Time (external TMRCLK only)	10		15		
t_{112a}	TMRGATE*n* to TMRCLK Hold Time (external TMRCLK only)	19		19		
Timer Control Unit (TCU) Outputs						
t_{113}	TMRGATE*n* Low to TMROUT Valid		44		52	
t_{114}	TMRCLK*n* Low to TMROUT Valid		48		52	

NOTE:
1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Table 12. 3-Volt AC Characteristics (Sheet 5 of 5)

Symbol	Parameter	25 MHz 3.0 V to 3.6 V		20 MHz 2.7 V to 3.6 V		Test Condition
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
Interrupt Control Unit (ICU) Inputs						
t_{115}	D7:0 Setup Time (INTA# Cycle 2)	9		11		
t_{116}	D7:0 Hold Time (INTA# Cycle 2)	6		6		
Interrupt Control Unit (ICU) Outputs						
t_{117}	CLK2 High to CAS2:0 Valid		36		46	
DMA Unit Inputs						
t_{118}	DREQ Setup Time (Sync Mode)	19		21		
t_{119}	DREQ Hold Time (Sync Mode)	4		4		(2)
t_{120}	DREQ Setup Time (Async Mode)	11		11		
t_{121}	DREQ Hold Time (Async Mode)	11		11		(2)
t_{122}	EOP# Setup Time (Sync Mode)	17		21		
t_{123}	EOP# Hold Time (Sync Mode)	4		4		
t_{124}	EOP# Setup Time (Async Mode)	11		11		
t_{125}	EOP# Hold Time (Async Mode)	11		11		
DMA Unit Outputs						
t_{126}	DACK# Output Valid Delay	4	31	4	33	
t_{127}	EOP# Active Delay	4	27	4	33	
t_{128}	EOP# Float Delay	4	27	4	33	(3)
JTAG Test-logic Unit						
t_{129}	TCK Frequency		10		10	(Unit is MHz)

NOTE:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
4. These inputs may be asynchronous to CLK2. The setup and hold specifications are given to ensure recognition within a specific CLK2 period.
5. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.
6. This specification assumes that READY# goes active after the rising edge of phase 2, so that WR# goes inactive as a result of READY# falling.
7. This specification assumes that READY# goes active before the rising edge of phase 2, so that WR# goes inactive as a result of phase 2 rising.
8. This specification applies if READY# is generated internally.

Figure 10. AC Test Loads

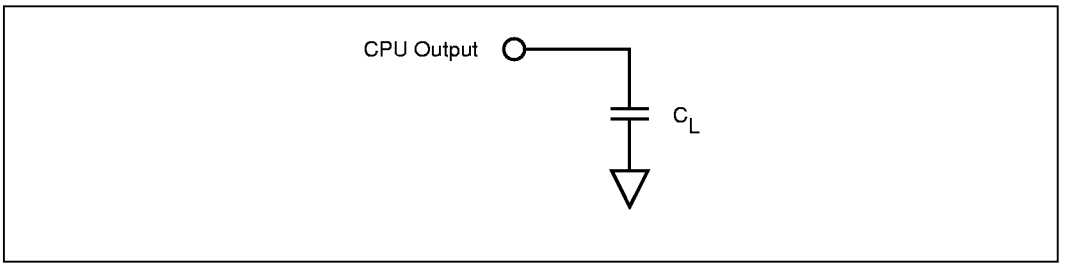


Figure 11. CLK2 Waveform

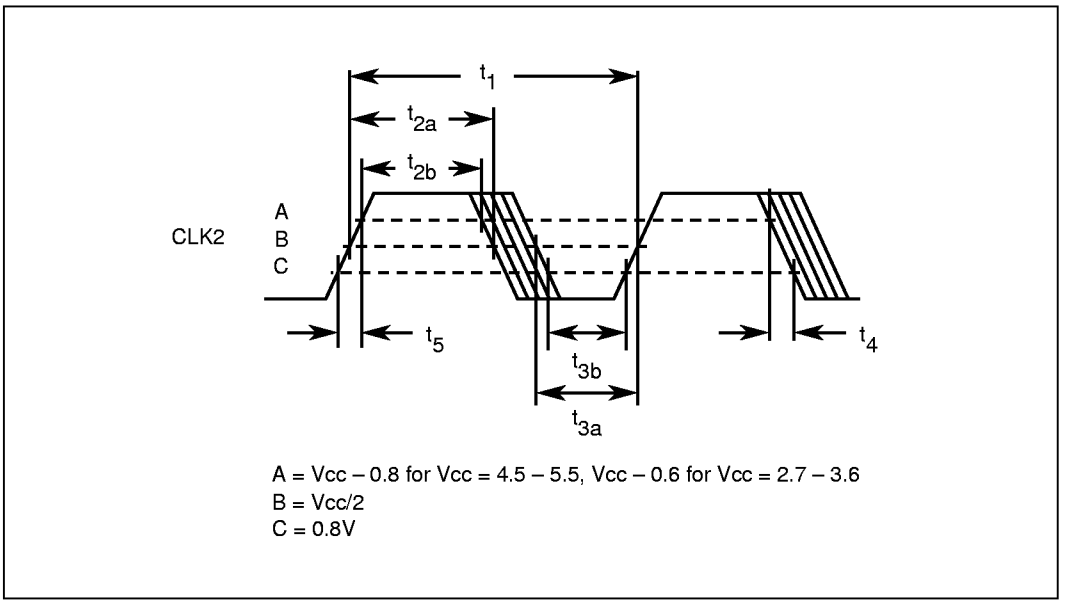


Figure 12. AC Timing Waveforms — Input Setup and Hold Timing

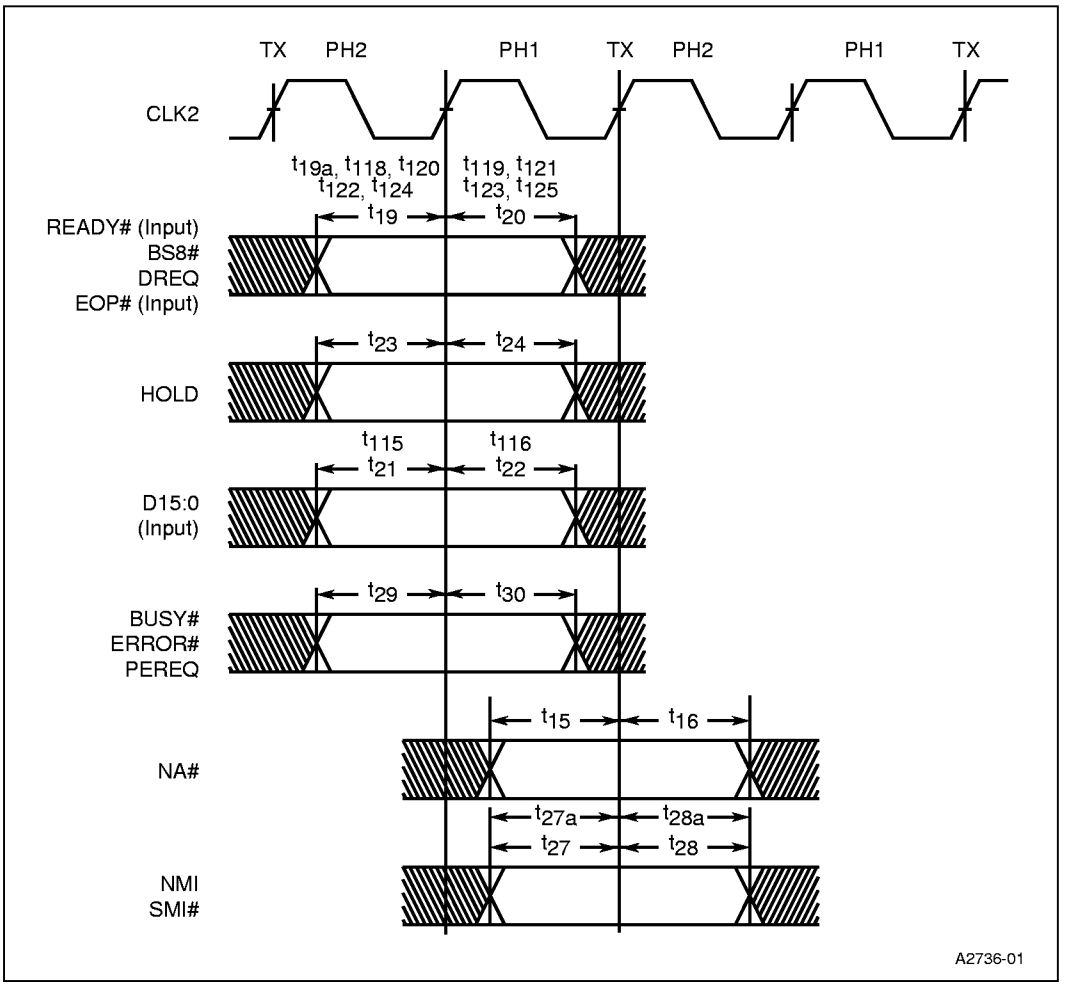


Figure 13. AC Timing Waveforms — Output Valid Delay Timing

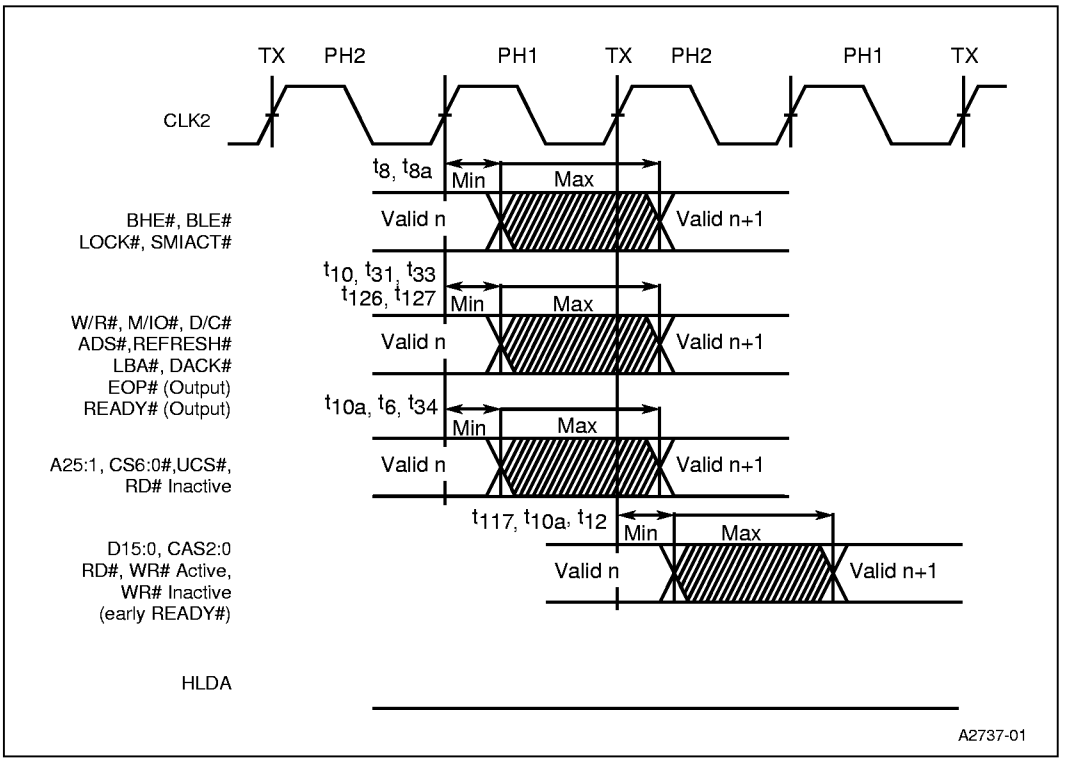


Figure 14. AC Timing Waveforms — Output Valid Delay Timing for External Late READY#

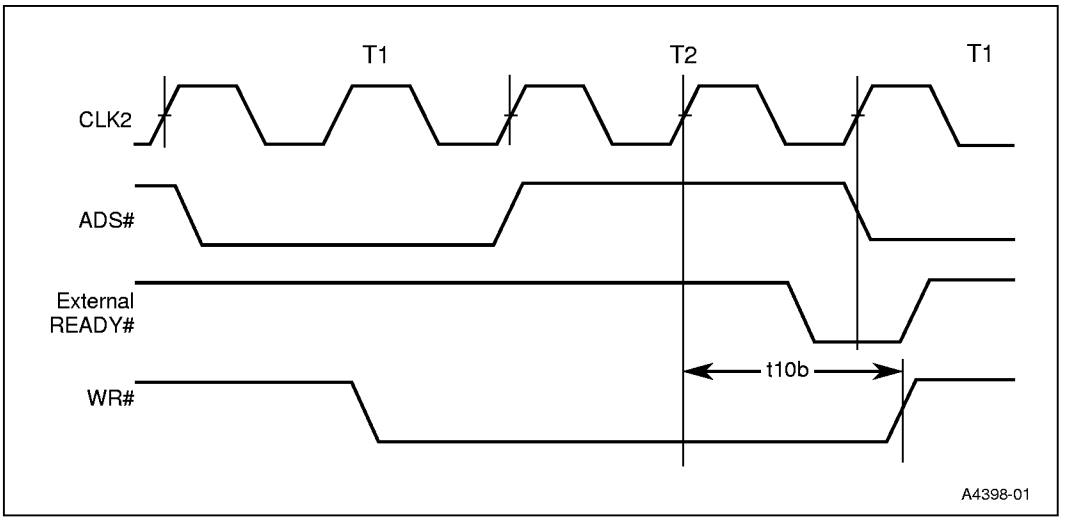


Figure 15. AC Timing Waveforms — Output Float Delay and HLDA Valid Delay Timing

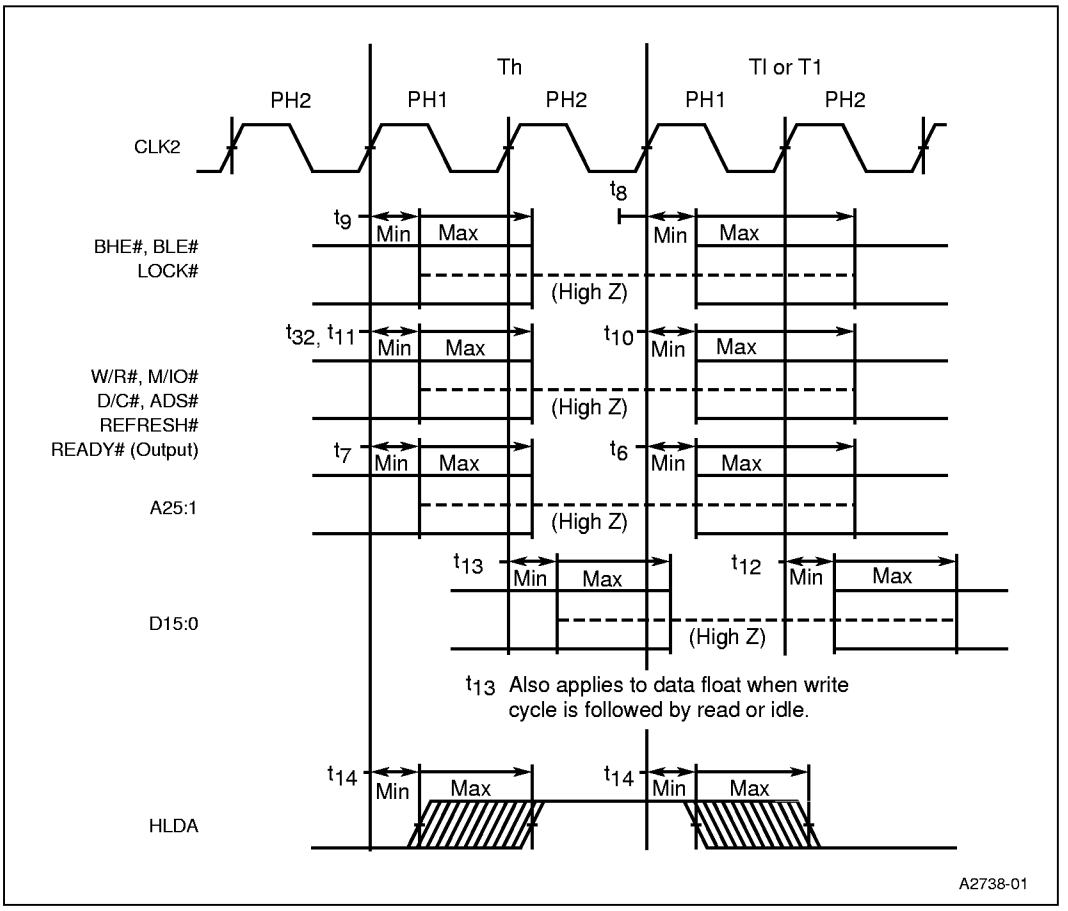


Figure 16. AC Timing Waveforms — RESET Setup and Hold Timing and Internal Phase

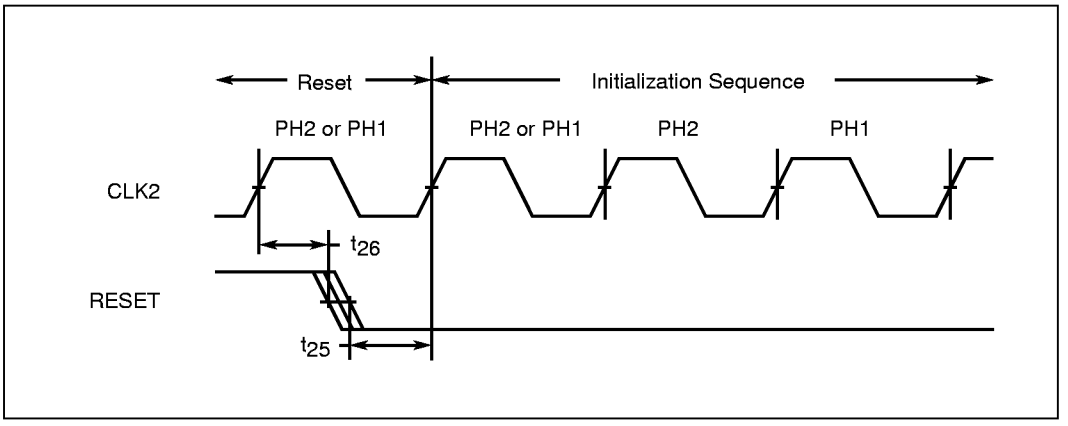


Figure 17. AC Timing Waveforms — Relative Signal Timing

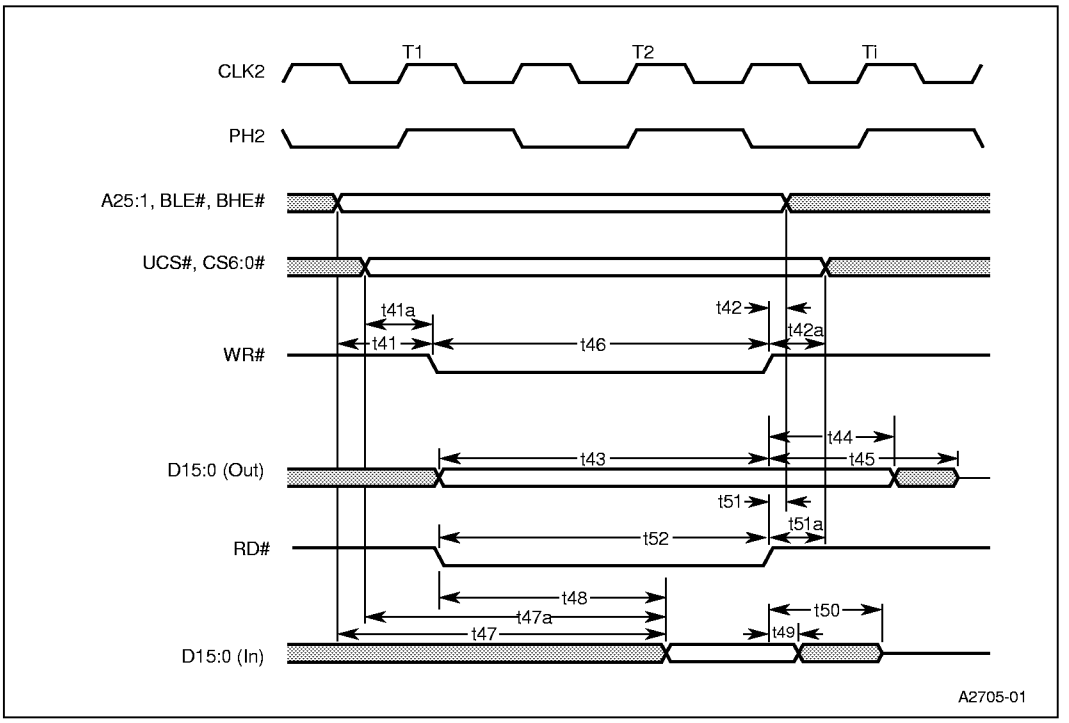


Figure 18. AC Timing Waveforms — SSIO Timing

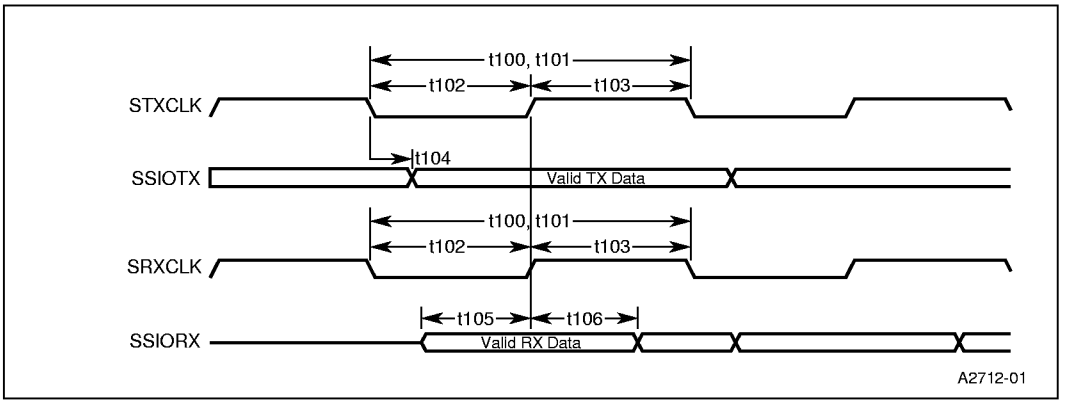
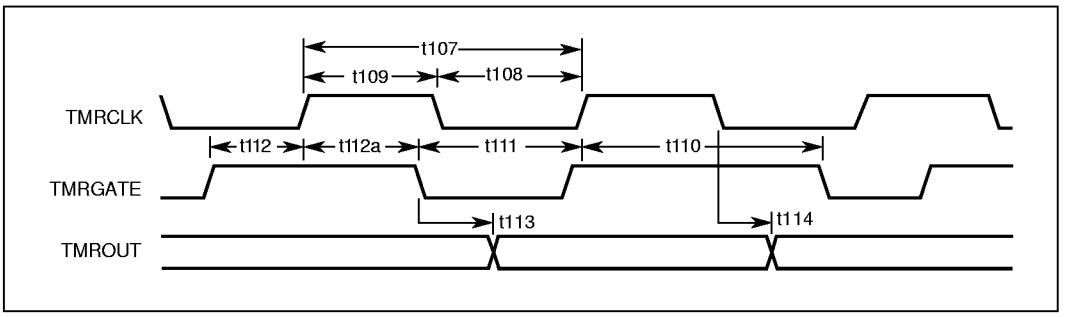


Figure 19. AC Timing Waveforms — Timer/Counter Timing



7.0 Bus Cycle Waveforms

Figures 20 through 30 present various bus cycles that are generated by the processor. What is shown in the figure is the relationship of the various bus signals to CLK2. These figures along with the information present in AC Specifications allow the user to determine critical timing analysis for a given application.

Figure 20. Basic Internal and External Bus Cycles

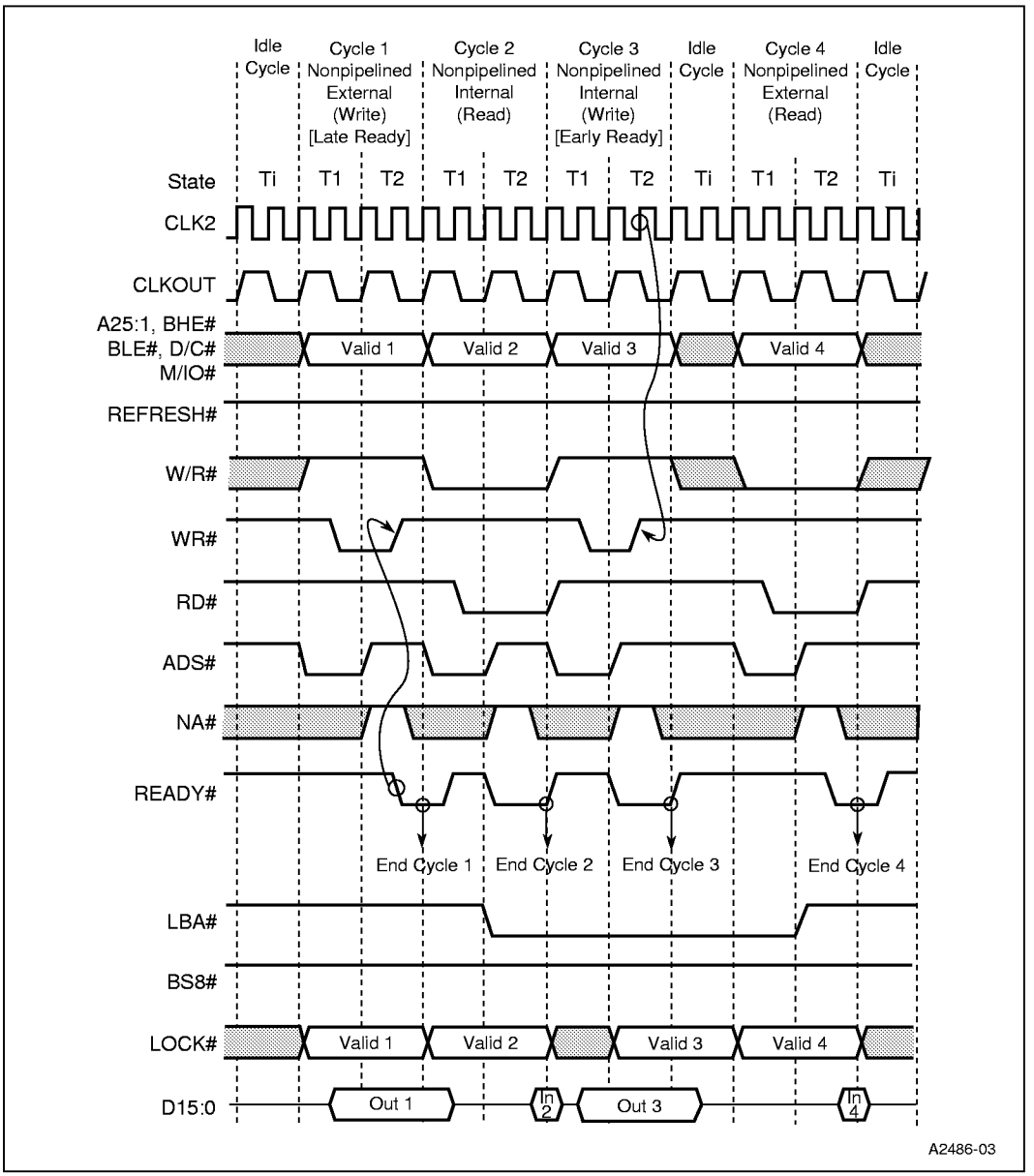


Figure 21. Nonpipelined Address Read Cycles

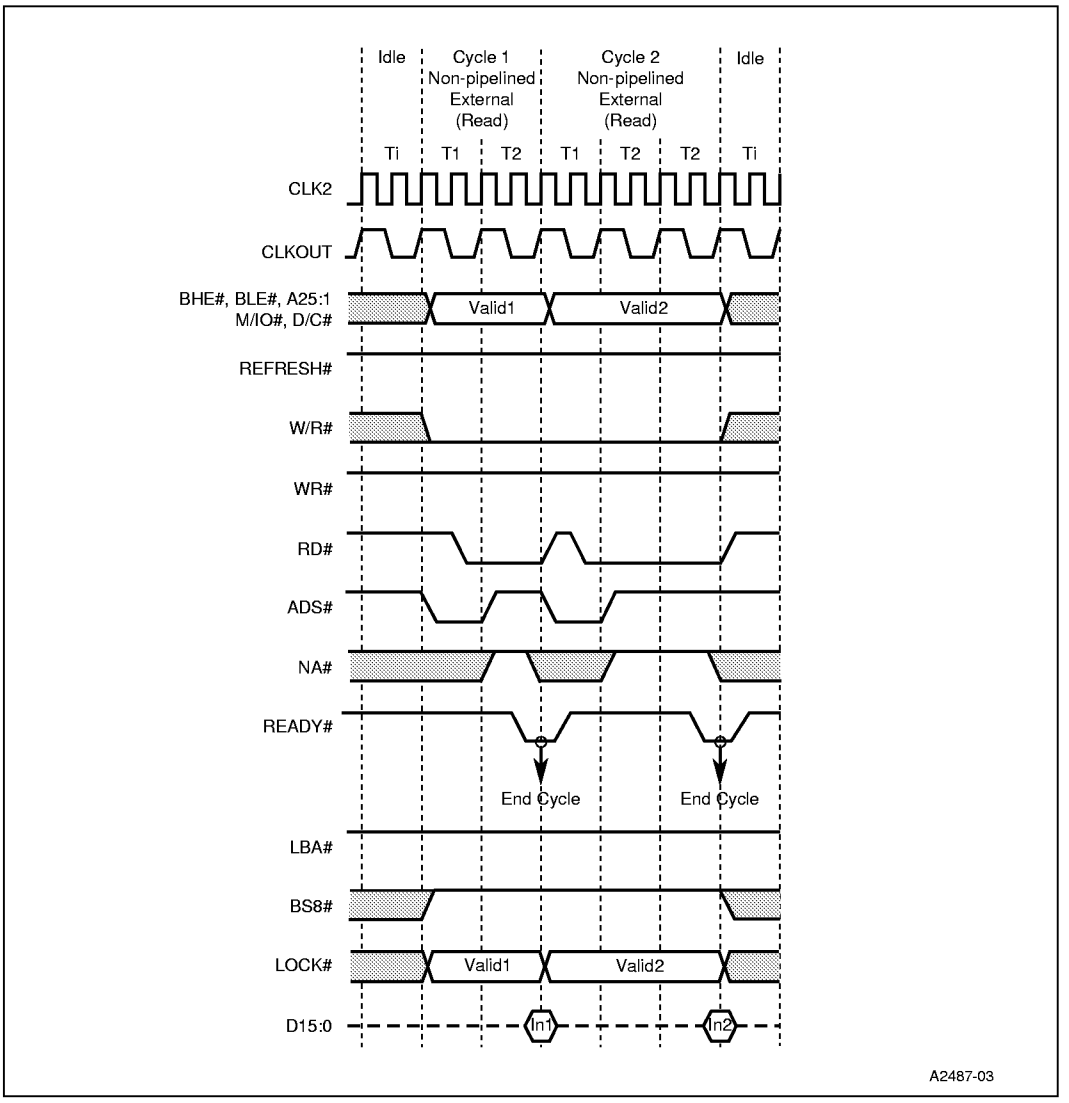


Figure 22. Pipelined Address Cycle

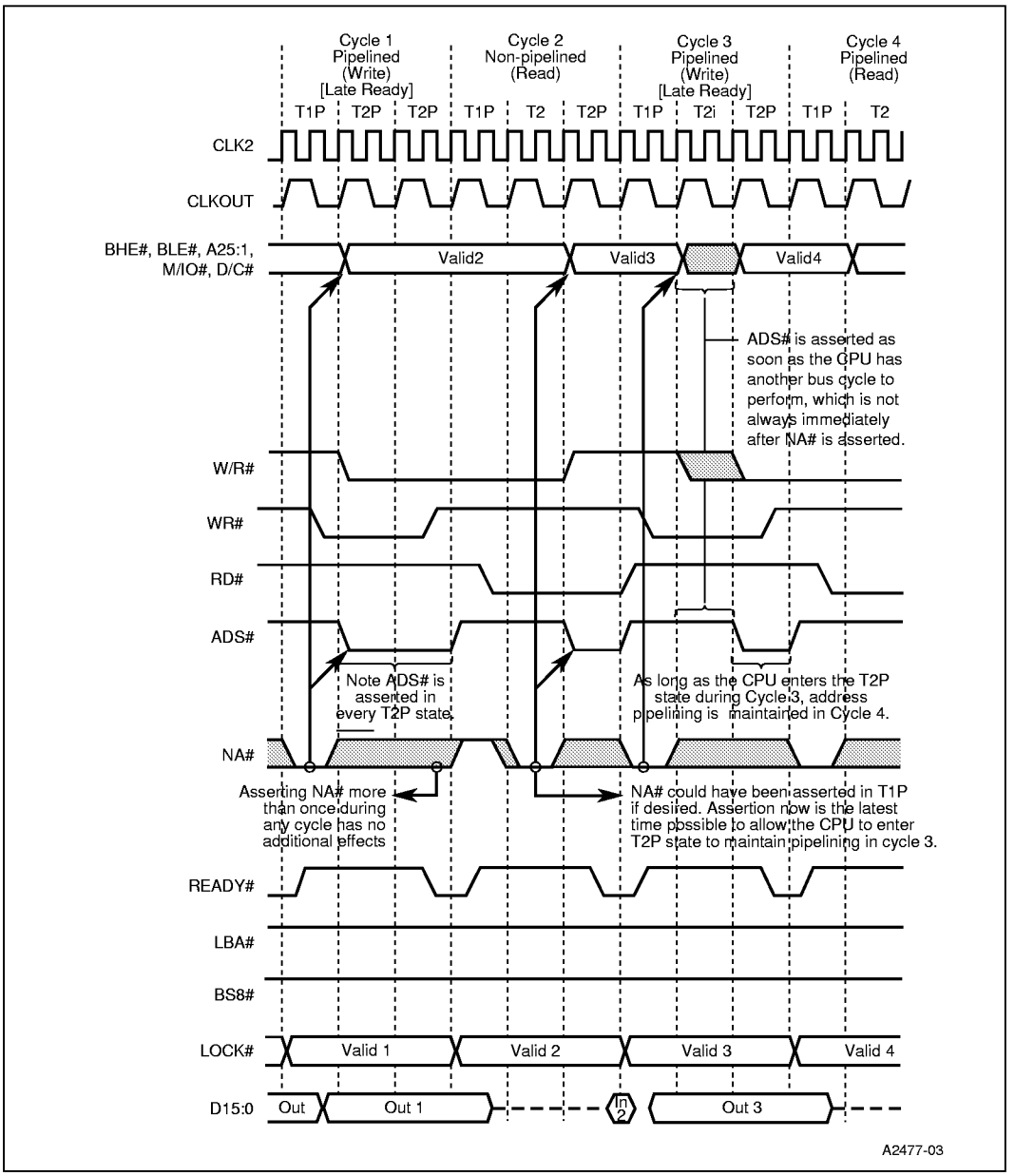


Figure 23. 16-bit Cycles to 8-bit Devices (using BS8#)

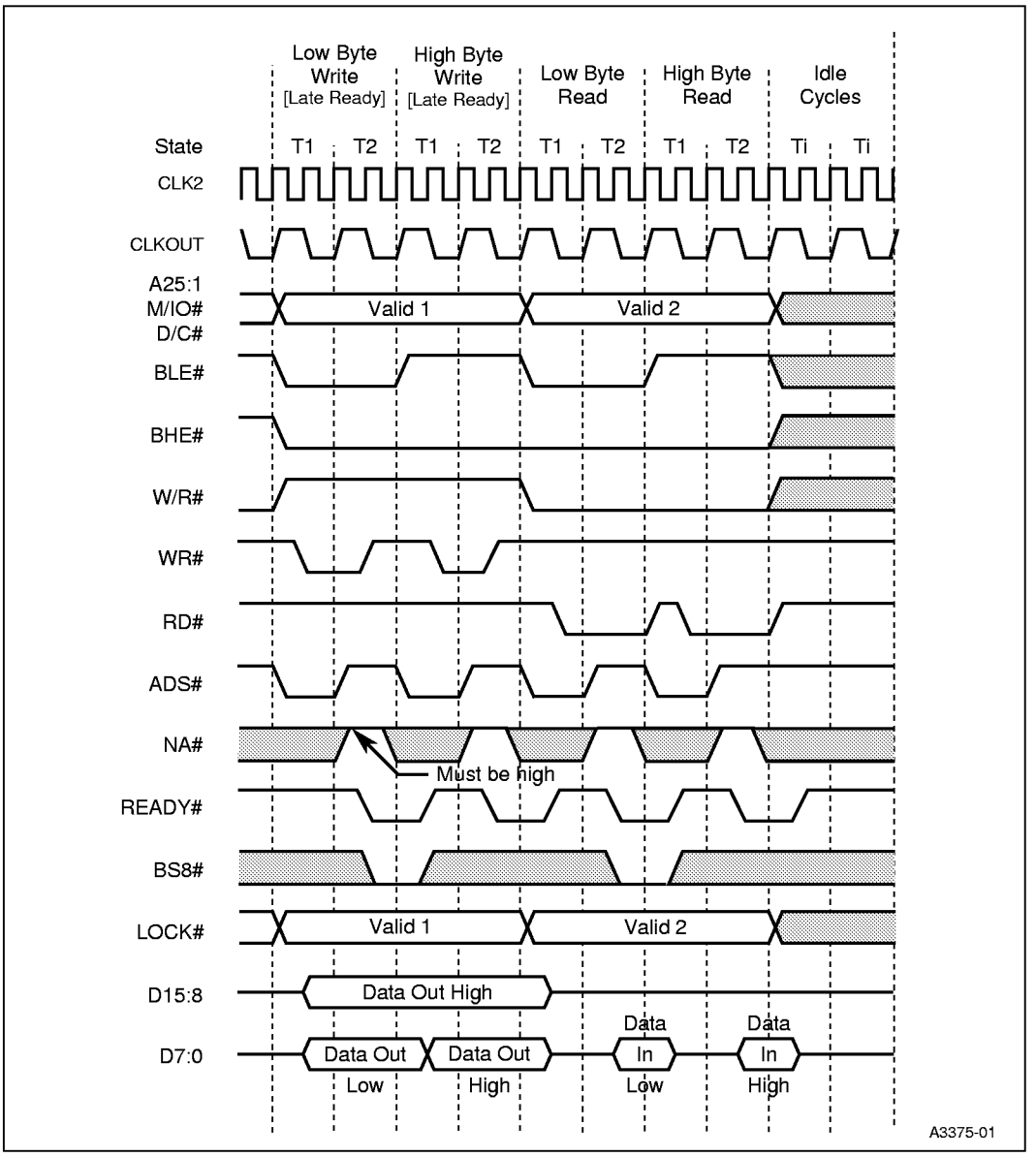


Figure 24. Basic External Bus Cycles

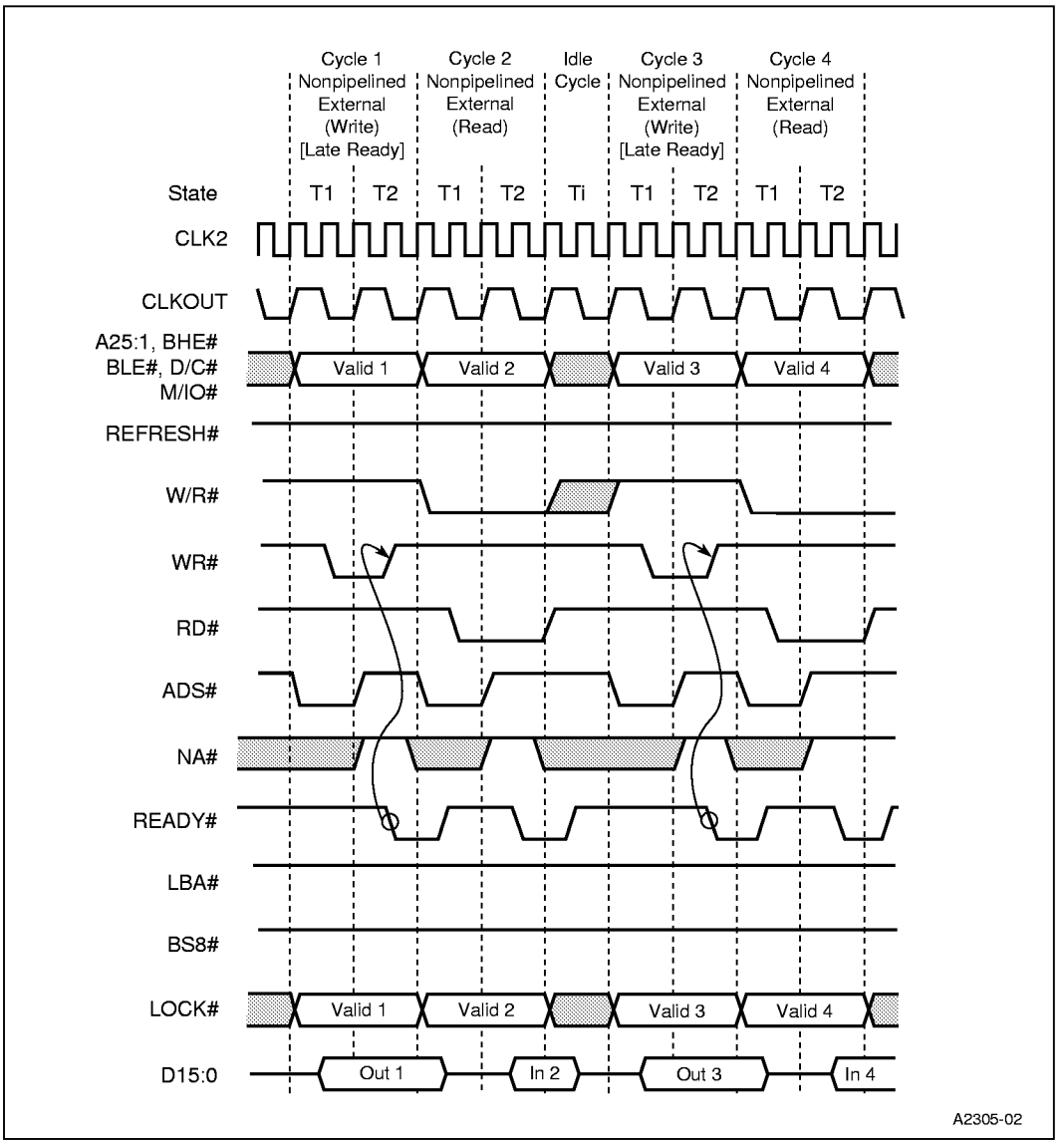


Figure 25. Nonpipelined Address Write Cycles

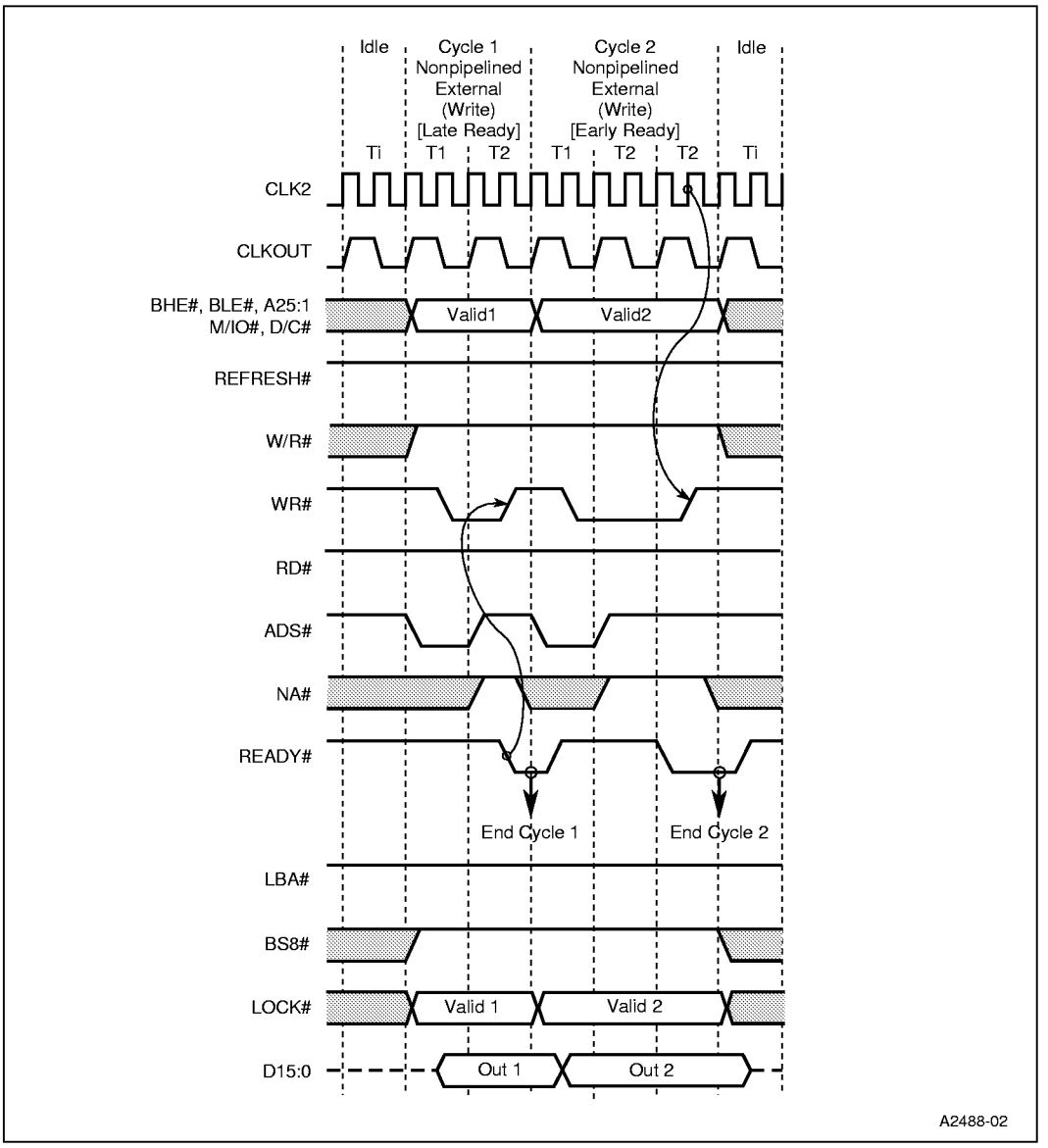
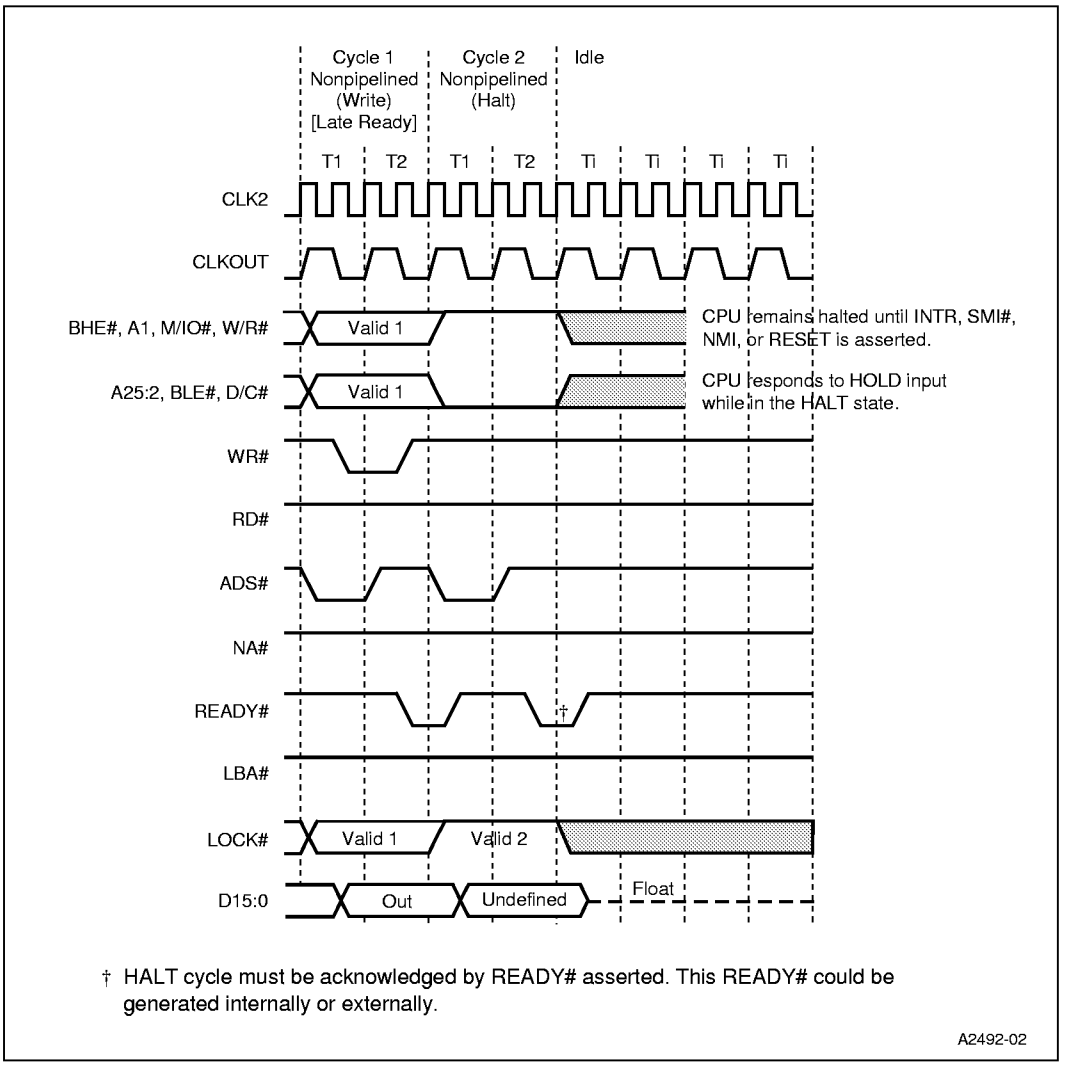


Figure 26. Halt Cycle



† HALT cycle must be acknowledged by READY# asserted. This READY# could be generated internally or externally.

A2492-02

Figure 27. Basic Refresh Cycle

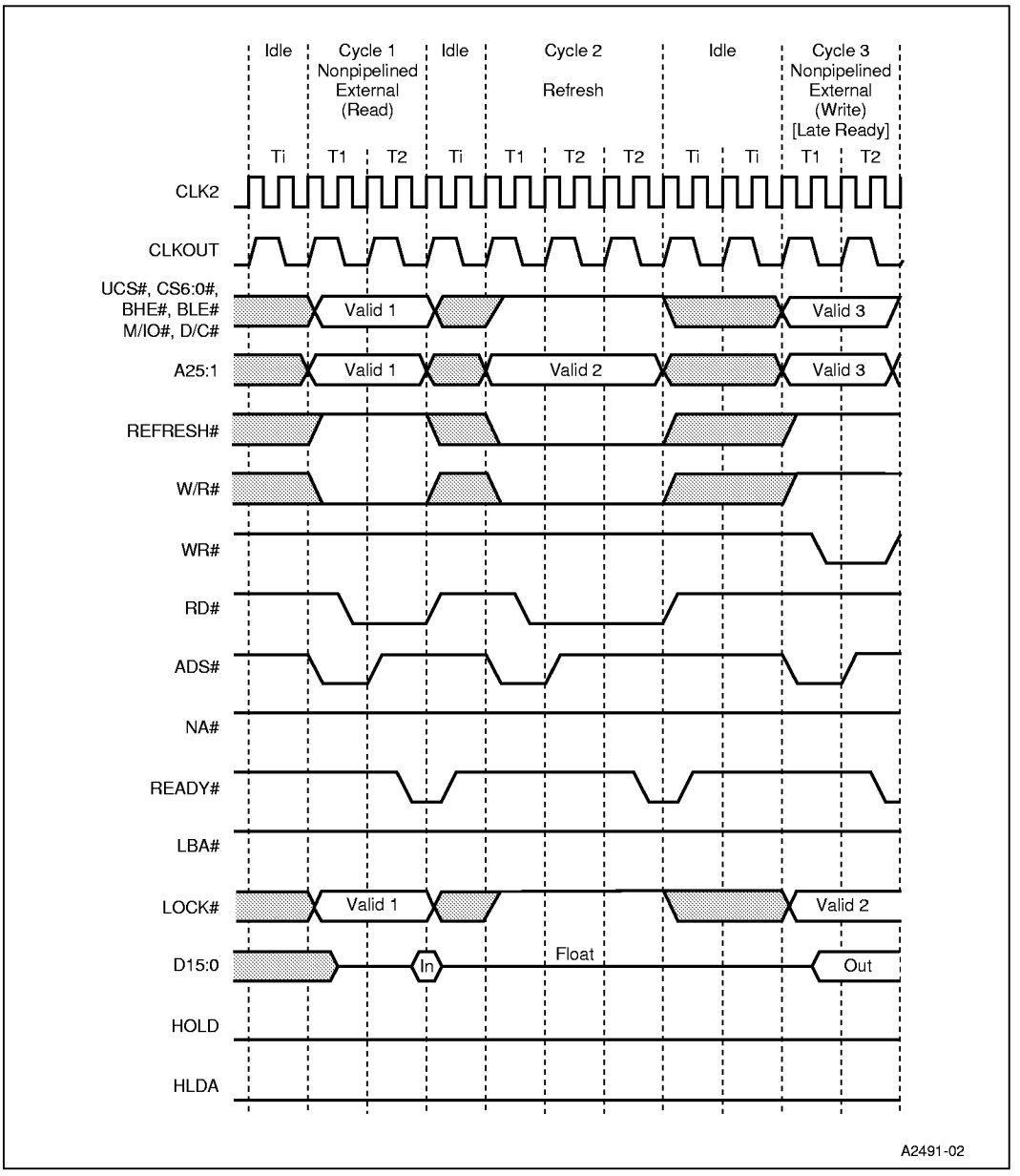


Figure 28. Refresh Cycle During HOLD/HLDA

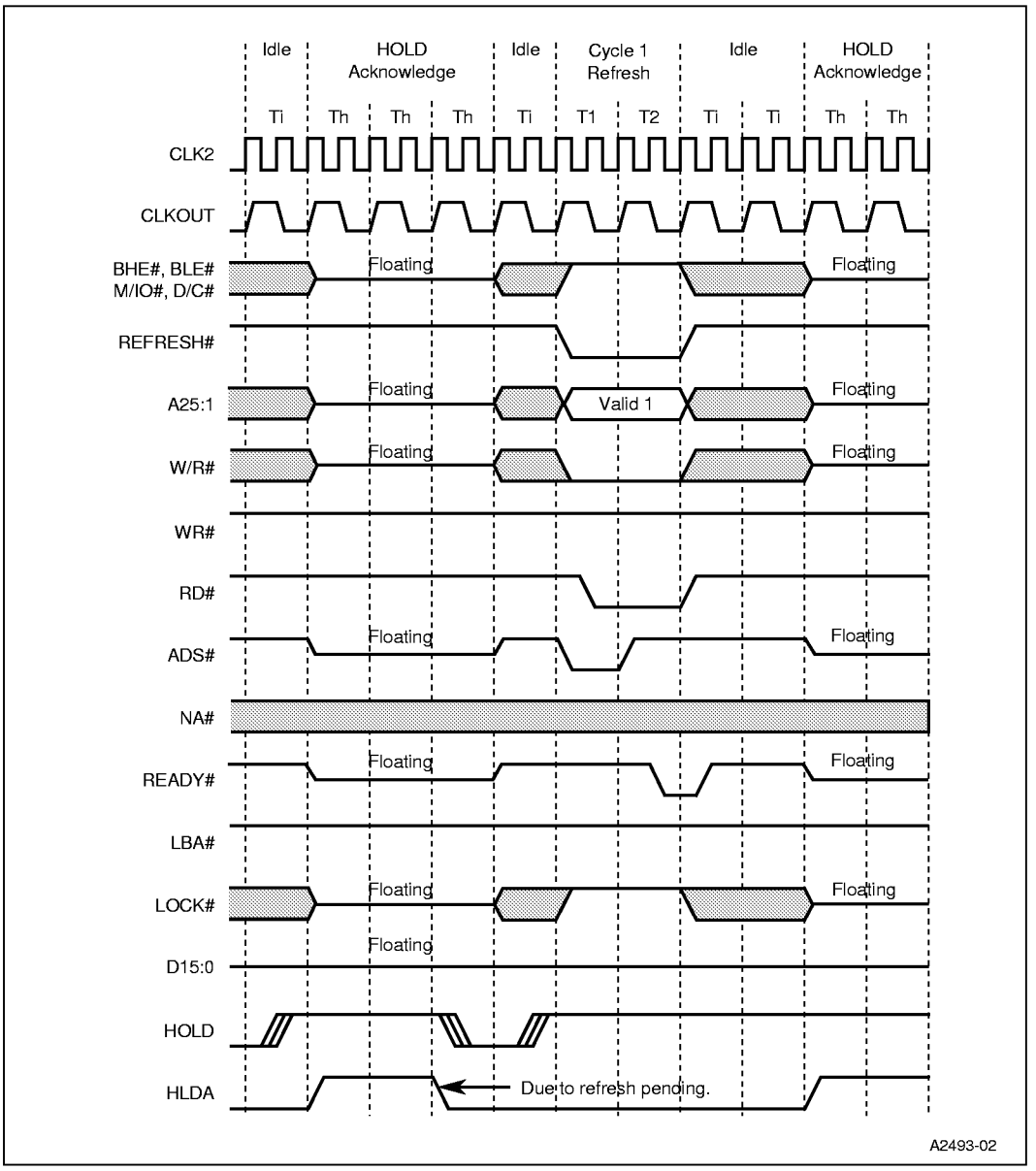


Figure 29. LOCK# Signal During Address Pipelining

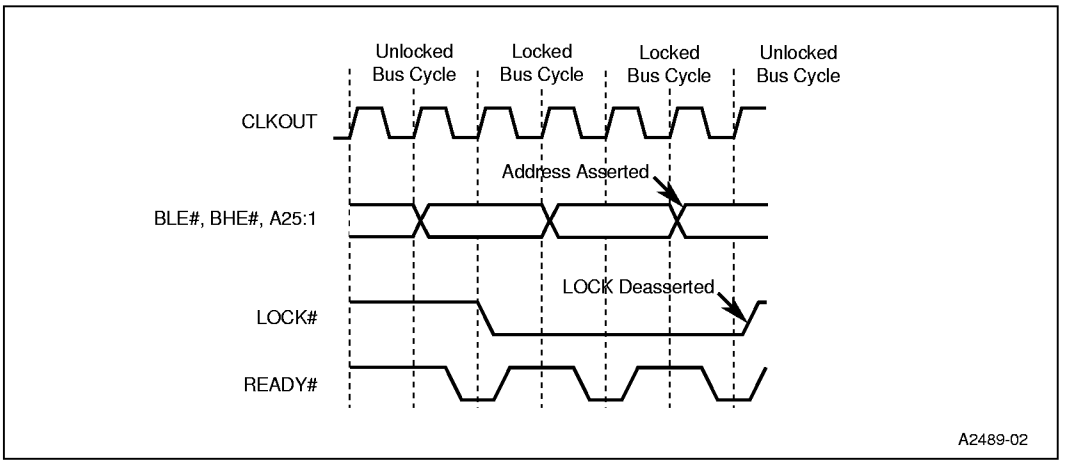


Figure 30. Interrupt Acknowledge Cycles